

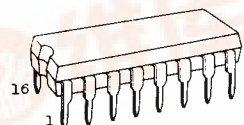
# TC5066BP, TC5067BP

C<sup>2</sup>MOS DIGITAL INTEGRATED CIRCUIT  
SILICON MONOLITHIC

TC5066BP 7-HIGH VOLTAGE BUFFER/NON INVERTING TYPE  
TC5067BP 7-HIGH VOLTAGE BUFFER/INVERTING TYPE

TC5066BP and TC5067BP contain seven independent circuits of buffers. TC5066BP in non-inverting type and TC5067BP is inverting type.

As both have the output of open drain structure with high breakdown voltage P-channel MOS FET (-50 volts.. ....Maximum Rating), these are suitable for driving fluorescent display tubes and for interfacing with high voltage MOS LSI's.



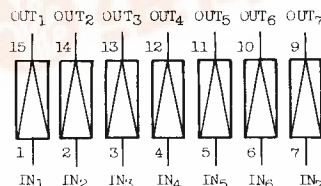
DIP 16 (3D16A-P)

## ABSOLUTE MAXIMUM RATINGS

CHARACTERISTIC	SYMBOL	RATING	UNIT
DC Supply Voltage	$V_{DD}$	$V_{SS}-0.5 \sim V_{SS}+20$	V
Input Voltage	$V_{IN}$	$V_{SS}-0.5 \sim V_{DD}+0.5$	V
Output Voltage	$V_{OUT}$	$V_{DD}-50 \sim V_{DD}+0.5$	V
Power Dissipation	$P_D$	300	mW
DC Input Current	$I_{IN}$	$\pm 10$	mA
Storage Temperature Range	$T_{stg}$	$-65 \sim 150$	$^{\circ}\text{C}$
Lead Temp./Time	$T_{sol}$	$260^{\circ}\text{C} \cdot 10\text{sec}$	

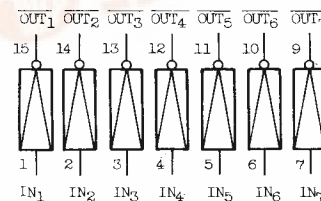
## PIN ASSIGNMENT

TC5066BP



$V_{DD} : 16, V_{SS} : 8$

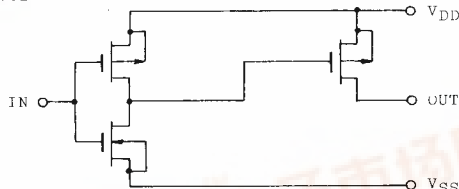
TC5067BP



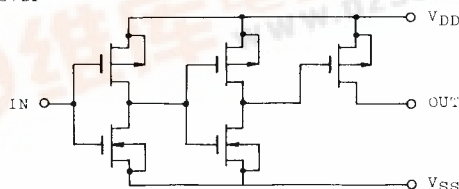
$V_{DD} : 16, V_{SS} : 8$

## LOGIC DIAGRAM

1/7 TC5066BP



1/7 TC5067BP



# TC5066BP, TC5067BP

## RECOMMENDED OPERATING CONDITIONS (VSS=0V)

CHARACTERISTIC	SYMBOL		MIN.	TYP.	MAX.	UNIT
Supply Voltage	V <sub>DD</sub>		3		18	V
Input Voltage	V <sub>IN</sub>		0		V <sub>DD</sub>	V
Operating Temp.	T <sub>opr</sub>		-40		85	°C

## ELECTRICAL CHARACTERISTICS (VSS=0V)

CHARACTERISTIC		SYMBOL	TEST CONDITIONS	VDD (V)	-40°C		25°C			85°C		UNIT	
					MIN.	MAX.	MIN.	TYP.	MAX.	MIN.	MAX.		
High Level Output Voltage		VOH	IOUT  < 1μA VIN=VSS or VDD	5 10 15	4.95 9.95 14.95	- - -	4.95 9.95 14.95	5.00 10.00 15.00	- - -	4.95 9.95 14.95	- - -	V	
High Level Output Current		IOH	VOH=3V (VDD-2V)	5	- 6	-	- 5	-10	-	- 4	-	mA	
			VOH=2V (VDD-3V)	5	- 9	-	- 8	-13	-	- 6	-		
			VOH=7V (VDD-3V)	10	-12	-	-10	-25	-	- 8	-		
			VOH=12V (VDD-3V)	15	-17	-	-15	-35	-	-12	-		
			VIN=VSS or VDD										
High Level Input Voltage (TC5066BP)		VIH	VOUT=4.5V VOUT=9.0V VOUT=13.5V	5 10 15	4.0 8.0 12.5	- - -	4.0 8.0 12.5		- - -	4.0 8.0 12.5	- - -	V	
			*										
Low Level Input Voltage (TC5066BP)		VIL	VOUT=0.5V VOUT=1.0V VOUT=1.5V	5 10 15	- - -	1.0 2.0 2.5	- - -		1.0 2.0 2.5	- - -	1.0 2.0 2.5		
			*										
High Level Input Voltage (TC5067BP)		VIH	VOUT=0.5V VOUT=1.0V VOUT=1.5V	5 10 15	3.5 7.0 11.0	- - -	3.5 7.0 11.0	2.75 5.5 8.25	- - -	3.5 7.0 11.0	- - -	V	
			*										
Low Level Input Voltage (TC5067BP)		VIL	VOUT=4.5V VOUT=9.0V VOUT=13.5V	5 10 15	- - -	1.5 3.0 4.0	- - -	2.25 4.5 6.75	1.5 3.0 4.0	- - -	1.5 3.0 4.0		
			*										
Output OFF Leak Current		IOFF	VOUT = 0V VOUT = -30V	15 15	- -	3 10	- -	0.01 1	3 10	- -	10 20	μA	
Input Current	H Level		IIH	VIH = 18V	18	-	0.3	-	10 <sup>5</sup>	0.3	-	1.0	μA
	L Level	IIL	VIL = 0V	18	-	-0.3	-	10 <sup>-5</sup>	-0.3	-	-1.0		
Quiescent Supply Current		IDD	VIN = VDD,VSS Outputs Open	5	-	4.0	-	0.005	4.0	-	30	μA	
				10	-	8.0	-	0.010	8.0	-	60		
				15	-	16.0	-	0.015	16.0	-	120		

\* R<sub>L</sub> = 20 kΩ

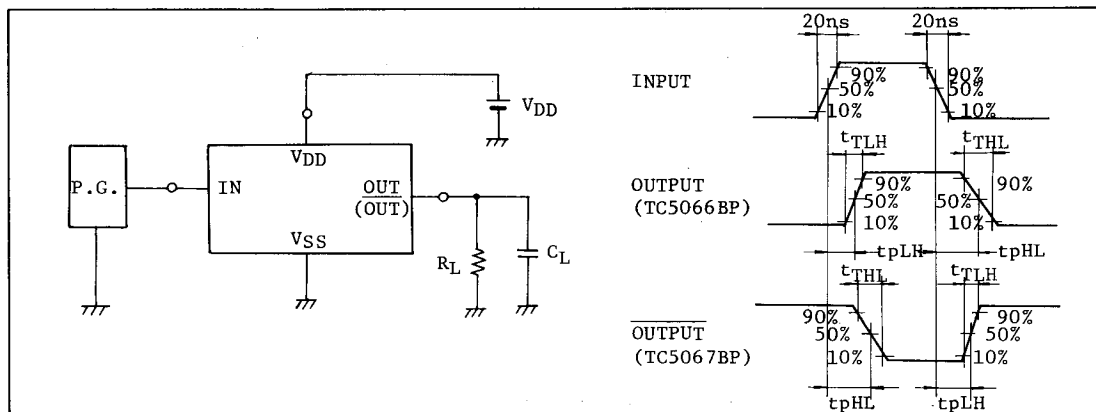


# TC5066BP, TC5067BP

SWITCHING CHARACTERISTICS (Ta=25°C, VSS=0V, CL=50pF)

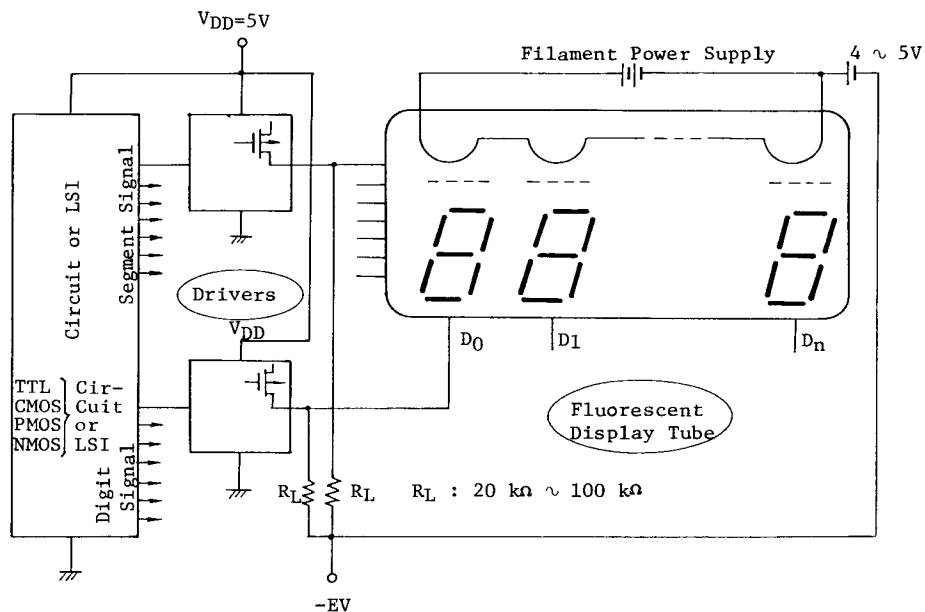
CHARACTERISTIC	SYMBOL	TEST CONDITIONS	VDD(V)	MIN.	TYP.	MAX.	UNIT
Output Rise Time	$t_{TLH}$	$R_L = 20\text{ k}\Omega$	5	-	100	200	ns
			10	-	50	100	
			15	-	40	80	
Output Fall Time	$t_{THL}$	$R_L = 20\text{ k}\Omega$	5	-	5.0	8.0	$\mu\text{s}$
			10	-	5.0	8.0	
			15	-	5.0	8.0	
(LOW-HIGH) Propagation Delay Time	$t_{pLH}$	$R_L = 20\text{ k}\Omega$	5	-	200	500	ns
			10	-	100	250	
			15	-	80	200	
(HIGH-LOW) Propagation Delay Time	$t_{pHL}$	$R_L = 20\text{ k}\Omega$	5	-	2.0	4.0	$\mu\text{s}$
			10	-	2.0	4.0	
			15	-	2.0	4.0	
Input Capacity	$C_{IN}$			-	5	7.5	pF

SWITCHING TIME TEST CIRCUIT AND WAVEFORM



EXAMPLES OF APPLICABLE CIRCUITS

(1) Fluorescent Display Tube Driving Circuit



(2) Interface between CMOS and PMOS

