

# VN0300 SERIES

## N-Channel Enhancement-Mode MOS Transistors

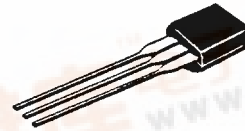
352-088

### PRODUCT SUMMARY

PART NUMBER	$V_{(BR)DSS}$ (V)	$r_{DS(ON)}$ ( $\Omega$ )	$I_D$ (A)	PACKAGE
VN0300L	30	1.2	0.64	TO-92
VN0300M	30	1.2	0.67	TO-237

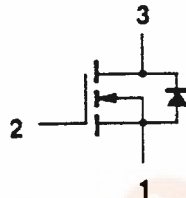
TO-92 (TO-226AA)

BOTTOM VIEW



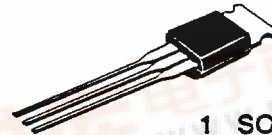
- 1 SOURCE
- 2 GATE
- 3 DRAIN

Performance Curves: VNDQ03



TO-237

BOTTOM VIEW



- 1 SOURCE
- 2 GATE
- 3 & TAB-DRAIN

### ABSOLUTE MAXIMUM RATINGS ( $T_A = 25^\circ\text{C}$ Unless Otherwise Noted)

PARAMETERS/TEST CONDITIONS	SYMBOL	LIMITS		UNITS	
		VN0300L	VN0300M		
Drain-Source Voltage	$V_{DS}$	30	30	V	
Gate-Source Voltage	$V_{GS}$	$\pm 30$	$\pm 30$		
Continuous Drain Current	$I_D$	$T_A = 25^\circ\text{C}$	0.64	0.67	A
		$T_A = 100^\circ\text{C}$	0.38	0.43	
Pulsed Drain Current <sup>1</sup>	$I_{DM}$	3	3		
Power Dissipation	$P_D$	$T_A = 25^\circ\text{C}$	0.8	1	W
		$T_A = 100^\circ\text{C}$	0.32	0.4	
Operating Junction & Storage Temperature Range	$T_J, T_{stg}$	-55 to 150		$^\circ\text{C}$	
Lead Temperature ( $1/16"$ from case for 10 sec.)	$T_L$	300			

### THERMAL RESISTANCE RATINGS

THERMAL RESISTANCE	SYMBOL	LIMITS		UNITS
		VN0300L	VN0300M	
Junction-to-Ambient	$R_{\theta JA}$	156	125	K/W

<sup>1</sup>Pulse width limited by maximum junction temperature



SPECIFICATIONS <sup>a</sup>			LIMITS			
PARAMETER	SYMBOL	TEST CONDITIONS	TYP <sup>b</sup>	MIN	MAX	UNIT
<b>STATIC</b>						
Drain-Source Breakdown Voltage	$V_{(BR)DSS}$	$I_D = 10 \mu A, V_{GS} = 0 V$	65	30		V
Gate-Threshold Voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}, I_D = 1 mA$	1.5	0.8	2.5	
Gate-Body Leakage	$I_{GSS}$	$V_{GS} = \pm 30 V, V_{DS} = 0 V$			$\pm 100$	nA
Zero Gate Voltage Drain Current	$I_{DSS}$	$V_{DS} = 30 V, V_{GS} = 0 V$			10	$\mu A$
		$T_J = 125^\circ C$			500	
On-State Drain Current <sup>c</sup>	$I_{D(ON)}$	$V_{DS} = 10 V, V_{GS} = 10 V$	3	1		A
Drain-Source On-Resistance <sup>c</sup>	$r_{DS(ON)}$	$V_{GS} = 5 V, I_D = 0.3 A$	1.4		3.3	$\Omega$
		$V_{GS} = 5 V, I_D = 1 A$	0.85		1.2	
		$T_J = 125^\circ C$	1.8		2.40	
Forward Transconductance <sup>c</sup>	$g_{FS}$	$V_{DS} = 10 V, I_D = 0.5 A$	500	200		mS
Common Source Output Conductance <sup>c</sup>	$g_{CS}$	$V_{DS} = 10 V, I_D = 0.1 A$	1500			$\mu S$
<b>DYNAMIC</b>						
Input Capacitance	$C_{iss}$	$V_{DS} = 15 V, V_{GS} = 0 V$ $f = 1 MHz$	38		100	pF
Output Capacitance	$C_{oss}$		28		95	
Reverse Transfer Capacitance	$C_{rss}$		8		25	
<b>SWITCHING</b>						
Turn-On Time	$t_{ON}$	$V_{DD} = 25 V, R_L = 24 \Omega, I_D = 1 A$ $V_{GEN} = 10 V, R_G = 25 \Omega$	9		30	ns
Turn-Off Time	$t_{OFF}$	(Switching time is essentially independent of operating temperature)	13		30	

- NOTES.
- a.  $T_A = 25^\circ C$  unless otherwise noted.
  - b. For design aid only, not subject to production testing.
  - c. Pulse test;  $PW = \leq 300 \mu S$ , duty cycle  $\leq 2\%$ .

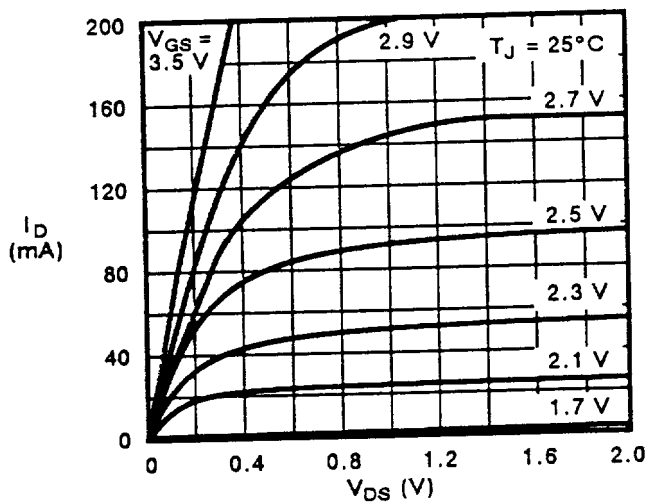
# VNDQ03

## N-Channel Enhancement-Mode MOSFETs

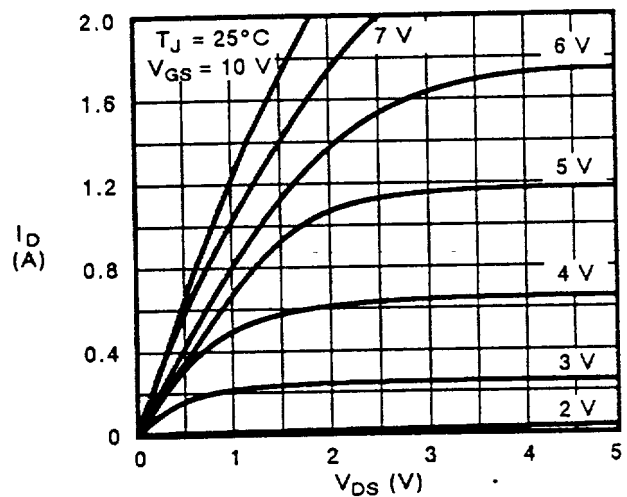
TYPE	PACKAGE	DEVICE
Single	TO-92 (TO-226AA)	• VN0300L, TN0201L, TN0401L
Single	TO-237	• VN0300M
Single	14-Pin Plastic	• VQ1001J
Quad	14-Pin Dual-In-Line	• VQ1001P
Quad	Chip	• Available as VNDQ1CHP

### TYPICAL CHARACTERISTICS

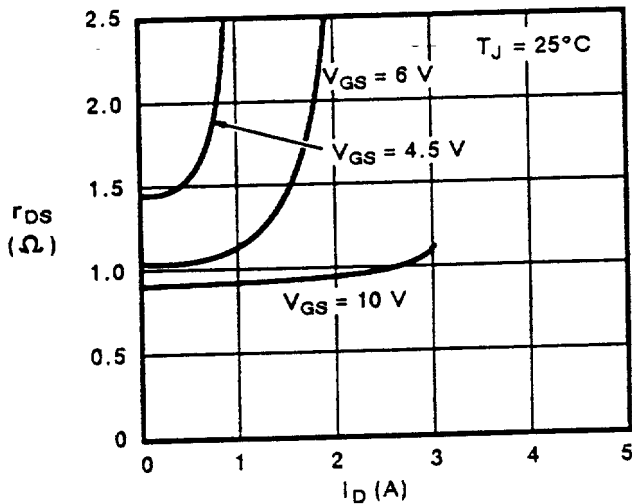
Output Characteristics for Low Gate Drive



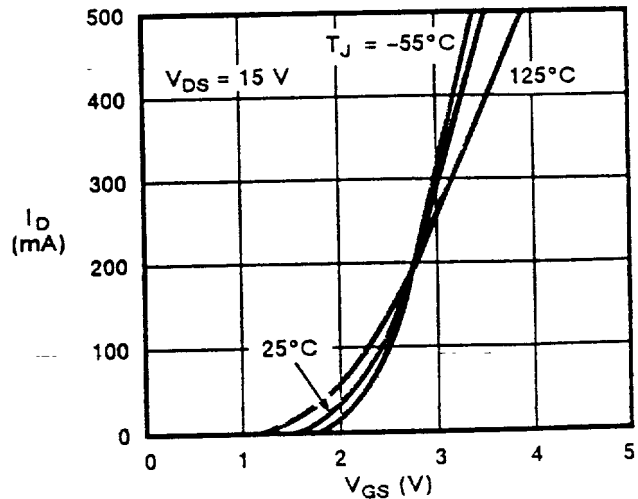
Ohmic Region Characteristics



On-Resistance



Transfer Characteristics

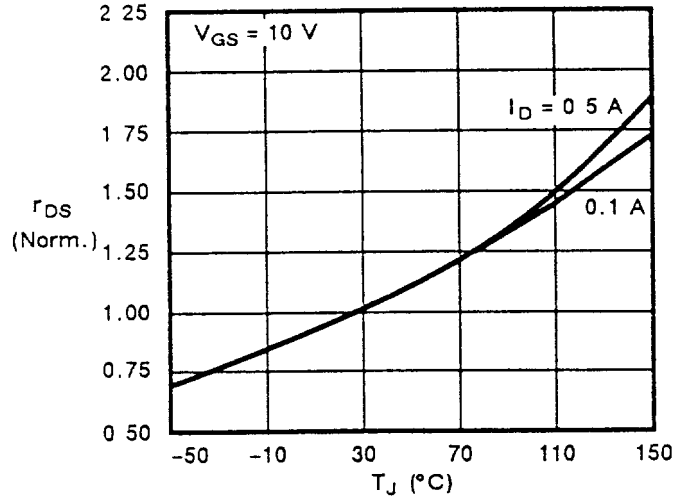


# VNDQ03

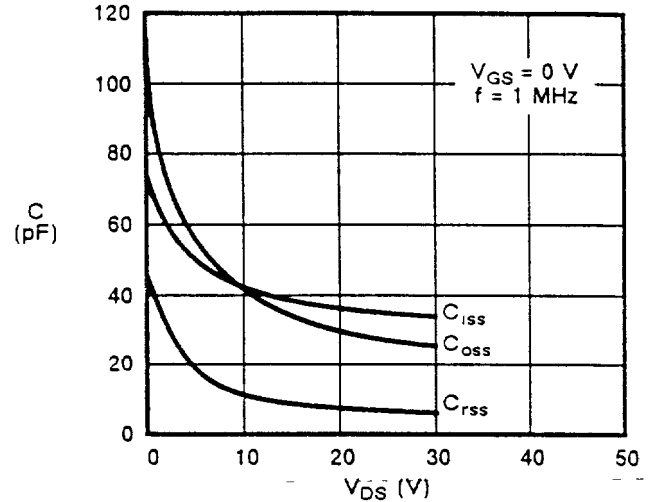


## TYPICAL CHARACTERISTICS (Cont'd)

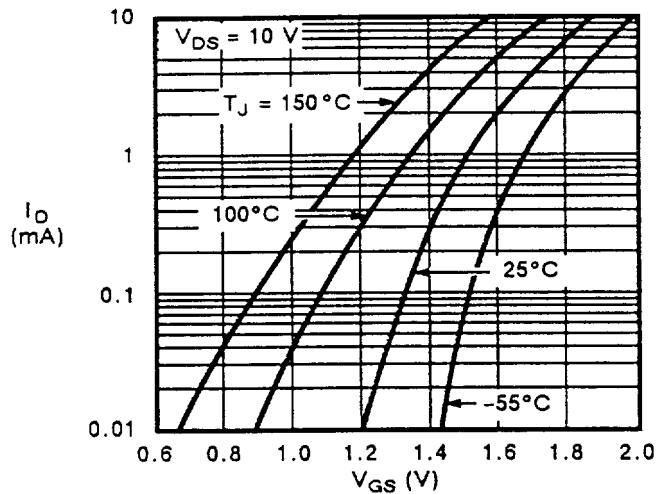
Normalized On-Resistance vs. Junction Temperature



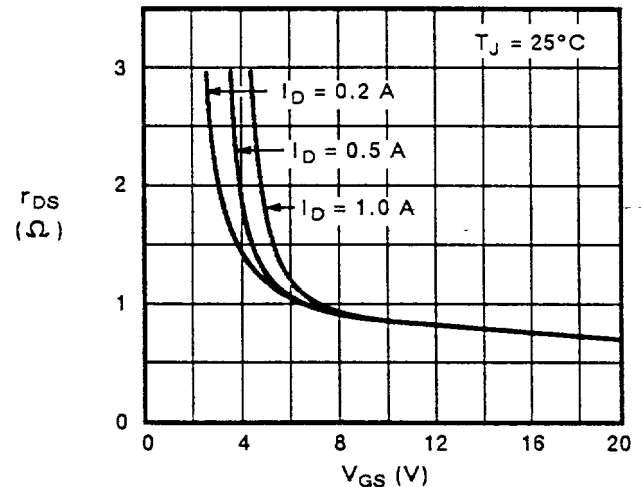
Capacitance



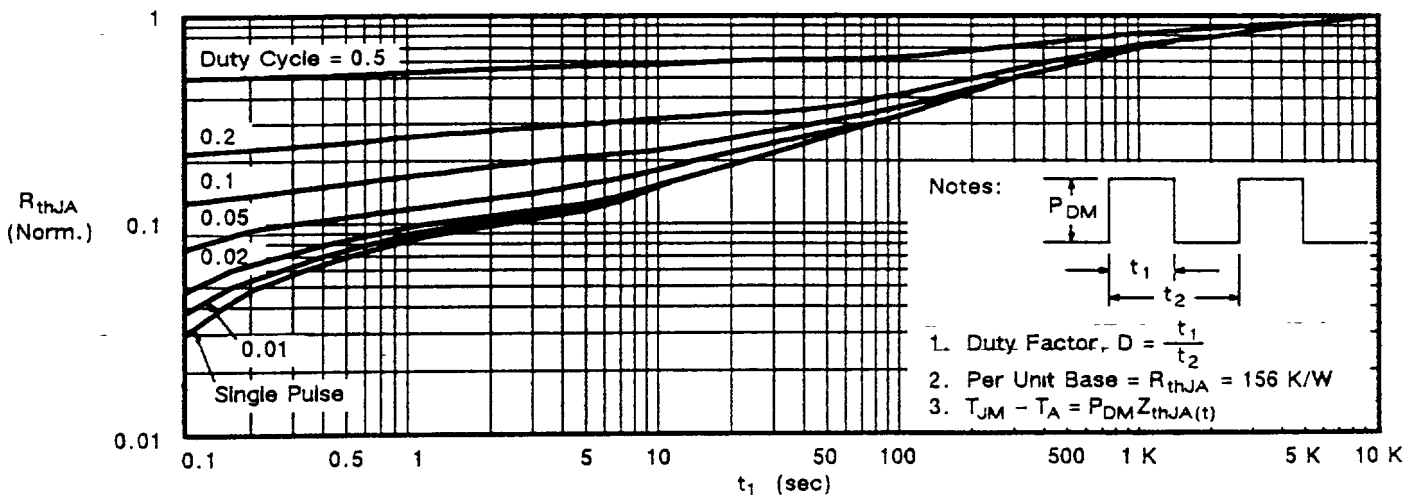
Threshold Region



On-Resistance vs. Gate to Source Voltage

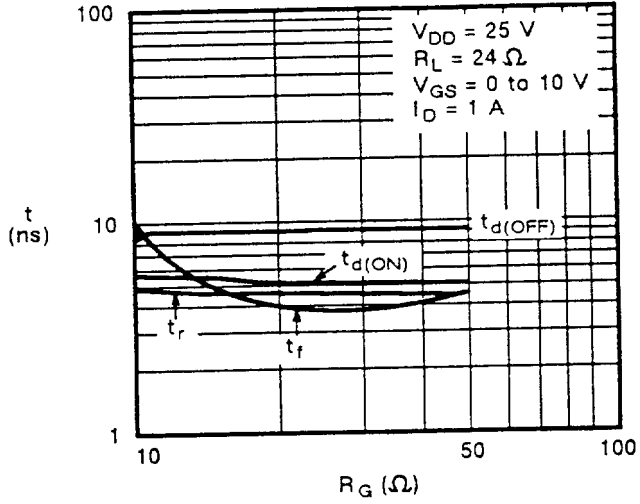


Normalized Effective Transient Thermal Impedance, Junction-to-Ambient (TO-92)

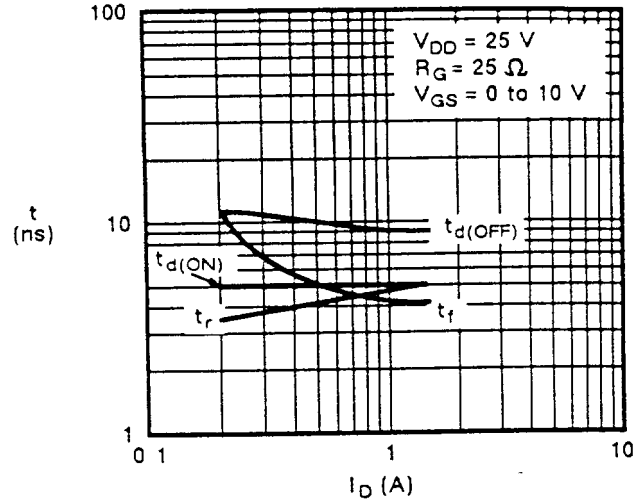


## TYPICAL CHARACTERISTICS (Cont'd)

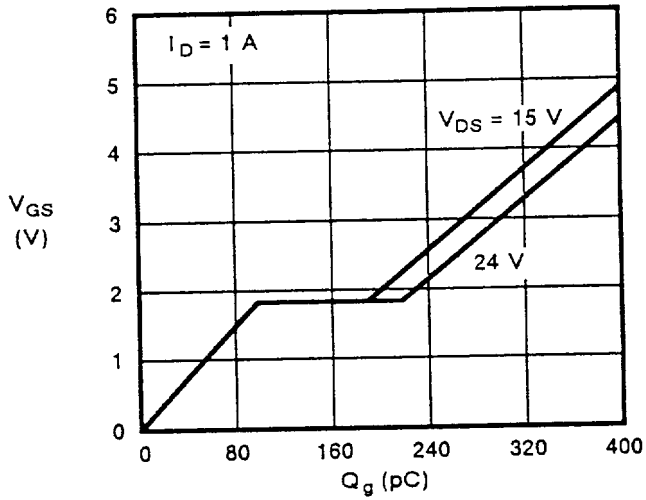
Drive Resistance Effects on Switching



Load Condition Effects on Switching



Gate Charge



Transconductance

