

## Section 18 Electrical Specifications

### 18.1 Absolute Maximum Ratings

Table 18-1 lists the absolute maximum ratings.

**Table 18-1 Absolute Maximum Ratings**

Item	Symbol	Rating	Unit
Supply voltage	V <sub>CC</sub>	-0.3 to +0.7	V
Programming voltage	V <sub>PP</sub>	-0.3 to +13.5	V
Input voltage (except port 6)	V <sub>in</sub>	-0.3 to V <sub>CC</sub> + 0.3	V
Input voltage (port 6)	V <sub>in</sub>	-0.3 to AV <sub>CC</sub> + 0.3	V
Analog supply voltage	AV <sub>CC</sub>	-0.3 to +7.0	V
Analog input voltage	VA <sub>N</sub>	-0.3 to AV <sub>CC</sub> + 0.3	V
Operating temperature	T <sub>opr</sub>	Regular specifications: -20 to +75	°C
		Wide-range specifications: -40 to +85	°C
Storage temperature	T <sub>stg</sub>	-55 to +125	°C

Note: Permanent damage to the chip may result if the absolute maximum ratings shown in table 18-1 are exceeded.

### 18.2 Electrical Characteristics

#### 18.2.1 DC Characteristics

Table 18-2 lists the DC characteristics.



**Table 18-2 DC Characteristics**
**Conditions:**  $V_{CC} = AV_{CC} = 5.0\text{ V} \pm 10\%^{*1}$ ,  $V_{SS} = AV_{SS} = 0\text{ V}$ ,

 $T_a = -20\text{ to }75^\circ\text{C}$  (Regular specifications)

 $T_a = -40\text{ to }85^\circ\text{C}$  (Wide-range specifications)

Item		Symbol	min	typ	max	Unit	Test
							Conditions
Input high voltage	$\overline{\text{RES}}$ , MD <sub>2</sub> , MD <sub>1</sub> , MD <sub>0</sub>	V <sub>IH</sub>	$V_{CC} - 0.7$	—	$V_{CC} + 0.3$	V	
	EXTAL		$V_{CC} \times 0.7$	—	$V_{CC} + 0.3$	V	
	Port 6		2.2	—	$AV_{CC} + 0.3$	V	
	Other input pins (except port 5)		2.2	—	$V_{CC} + 0.3$	V	
Input low voltage	$\overline{\text{RES}}$ , MD <sub>2</sub> , MD <sub>1</sub> , MD <sub>0</sub>	V <sub>IL</sub>	-0.3	—	0.5	V	
	Other input pins (except port 5)		-0.3	—	0.8		
Schmitt trigger input voltage	Port 5	VT <sup>-</sup>	1.0	—	2.5	V	
		VT <sup>+</sup>	2.0	—	3.5	V	
		VT <sup>+</sup> - VT <sup>-</sup>	0.4	—	—	V	
Input leakage current	$\overline{\text{RES}}$	I <sub>in</sub>	—	—	10.0	μA	V <sub>in</sub> = 0.5 to
	NMI, MD <sub>2</sub> , MD <sub>1</sub> , MD <sub>0</sub> ,		—	—	1.0	μA	V <sub>CC</sub> - 0.5 V
	Port 6		—	—	1.0	μA	V <sub>in</sub> = 0.5 to AV <sub>CC</sub> - 0.5 V
Leakage current in 3-state (off state)	Port 7, ports 5 to 1	I <sub>rsi</sub>	—	—	1.0	μA	V <sub>in</sub> = 0.5 to V <sub>CC</sub> - 0.5 V
Input pull-up MOS current	Ports 3 and 4	-I <sub>P</sub>	50	—	200	μA	V <sub>in</sub> = 0 V
Output high voltage	All output pins	V <sub>OH</sub>	$V_{CC} - 0.5$	—	—	V	I <sub>OH</sub> = -200 μA
			3.5	—	—	V	I <sub>OH</sub> = -1 mA
Output low voltage	All output pins (except $\overline{\text{RES}}$ )	V <sub>OL</sub>	—	—	0.4	V	I <sub>OL</sub> = 1.6 mA
			Port 3	—	—	1.0	V
		—	—	1.2	V	I <sub>OL</sub> = 10 mA	
	$\overline{\text{RES}}$	—	—	0.4	V	I <sub>OL</sub> = 2.6 mA	
Input capacitance	$\overline{\text{RES}}$	C <sub>in</sub>	—	—	60	pF	V <sub>in</sub> = 0 V
	NMI		—	—	30	pF	f = 1 MHz
	All input pins except $\overline{\text{RES}}$		—	—	15	pF	T <sub>a</sub> = 25°C



**Table 18-2 DC Characteristics (cont)**

Item		Symbol	Test				
			min	typ	max	Unit Conditions	
Current dissipation*	Normal operation	I <sub>CC</sub>	—	20	30	mA	f = 6 MHz
			—	25	40	mA	f = 8 MHz
			—	30	50	mA	f = 10 MHz
			—	12	20	mA	f = 6 MHz
	Sleep mode	—	16	25	mA	f = 8 MHz	
		—	20	30	mA	f = 10 MHz	
	Standby	—	0.01	5.0	μA		
Analog supply current	During A/D conversion	I <sub>ACC</sub>	—	0.6	2.0	mA	
	While waiting		—	0.01	5.0	μA	
RAM standby voltage		V <sub>RAM</sub>	2.0	—	—	V	

Note: AV<sub>CC</sub> must be connected to a power supply even when the A/D converter is not used.

\* Current dissipation values assume that V<sub>IH</sub> min = V<sub>CC</sub> - 0.5 V, V<sub>IL</sub> max = 0.5 V, all output pins are in the no-load state, and all MOS input pull-ups are off.

**Table 18-3 Allowable Output Current Sink Values**

Conditions: V<sub>CC</sub> = AV<sub>CC</sub> = 5.0 V ± 10%, V<sub>SS</sub> = AV<sub>SS</sub> = 0 V,

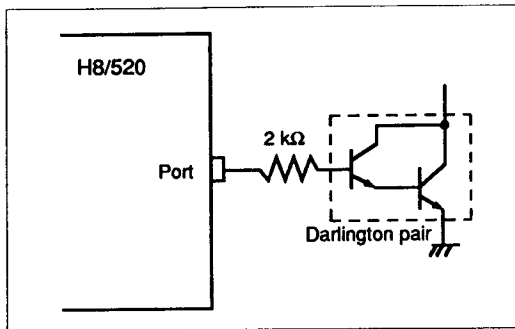
T<sub>a</sub> = -20 to 75°C (Regular specifications)

T<sub>a</sub> = -40 to 85°C (Wide-range specifications)

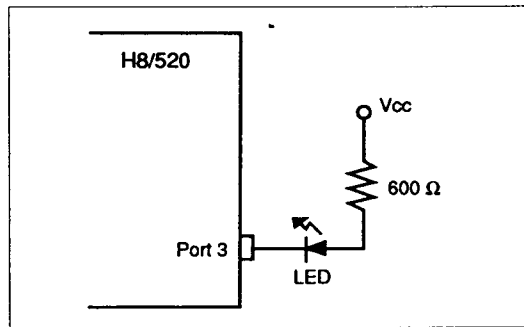
Item		Symbol	min	typ	max	Unit
Allowable output low current sink (per pin)	Port 3	I <sub>OL</sub>	—	—	10	mA
	RES		—	—	2.6	mA
	Other output pins		—	—	2.0	mA
Allowable output low current sink (total)	Port 3, total of 8 pins	Σ I <sub>OL</sub>	—	—	40	mA
	Total of all other output pins		—	—	80	mA
Allowable output high current sink (per pin)	All output pins	-I <sub>OH</sub>	—	—	2.0	mA
Allowable output high current sink (total)	Total of all output pins	Σ -I <sub>OH</sub>	—	—	40	mA

Note: To avoid degrading the reliability of the chip, be careful not to exceed the output current sink values in table 18-3. In particular, when driving a Darlington transistor pair or LED directly, be sure to insert a current-limiting resistor in the output path. See figures 18-1 and 18-2.





**Figure 18-1 Example of Circuit for Driving a Darlington Transistor Pair**



**Figure 18-2 Example of Circuit for Driving an LED**

### 18.2.2 AC Characteristics

The AC characteristics of the H8/520 chip are listed in three tables. Bus timing parameters are given in table 18-4, control signal timing parameters in table 18-5, and timing parameters of the on-chip supporting modules in table 18-6. See figure 18-3 for the output load circuit.

**Table 18-4 Bus Timing**

Conditions:  $V_{CC} = 5.0 \text{ V} \pm 10\%$ ,  $\phi = 0.5$  to 10 MHz,  $V_{SS} = 0 \text{ V}$   
 $T_a = -20$  to  $75^\circ\text{C}$  (Regular specifications)  
 $T_a = -40$  to  $85^\circ\text{C}$  (Wide-range specifications)

Item	Symbol	6 MHz		8 MHz		10 MHz		Unit	Test Conditions
		min	max	min	max	min	max		
Clock cycle time	$t_{cy}$	166.7	2000	125	2000	100	2000	ns	See figure 18-4
Clock pulse width low	$t_{CL}$	65	—	45	—	35	—	ns	
Clock pulse width high	$t_{CH}$	65	—	45	—	35	—	ns	
Clock rise time	$t_{Cr}$	—	15	—	15	—	15	ns	
Clock fall time	$t_{Cf}$	—	15	—	15	—	15	ns	
Address delay time	$t_{AD}$	—	70	—	60	—	55	ns	
Address hold time	$t_{AH}$	30	—	25	—	20	—	ns	
RD delay time 1	$t_{RDD1}$	—	70	—	60	—	40	ns	
RD delay time 2	$t_{RDD2}$	—	70	—	60	—	50	ns	
WR delay time 1	$t_{WRD1}$	—	70	—	60	—	50	ns	
WR delay time 2	$t_{WRD2}$	—	70	—	60	—	50	ns	
Write data strobe pulse width	$t_{DSWW}$	200	—	150	—	120	—	ns	
Address setup time 1	$t_{AS1}$	25	—	20	—	15	—	ns	
Address setup time 2	$t_{AS2}$	105	—	80	—	65	—	ns	See figure 18-4
Read data setup time	$t_{RDS}$	60	—	50	—	40	—	ns	

**Table 18-4 Bus Timing (cont)**

Item	Symbol	6 MHz		8 MHz		10 MHz		Unit	Test Conditions
		min	max	min	max	min	max		
Read data hold time	tRDH	0	—	0	—	0	—	ns	See figure 18-4
Read data access time	tACC	—	280	—	190	—	160	ns	
Write data delay time	tWDD	—	70	—	60	—	60	ns	
Write data setup time	tWDS	30	—	15	—	10	—	ns	
Write data hold time	tWDH	30	—	25	—	20	—	ns	
Wait setup time	tWTS	40	—	40	—	40	—	ns	See figure 18-5
Wait hold time	tWTH	10	—	10	—	10	—	ns	

**Table 18-5 Control Signal Timing**

Conditions:  $V_{CC} = 5.0\text{ V} \pm 10\%$ ,  $\phi = 0.5$  to 10 MHz,  $V_{SS} = 0\text{ V}$

$T_a = -20$  to  $75^\circ\text{C}$  (Regular specifications)

$T_a = -40$  to  $85^\circ\text{C}$  (Wide-range specifications)

Item	Symbol	6 MHz		8 MHz		10 MHz		Unit	Test Conditions
		min	max	min	max	min	max		
RES setup time	tRESS	200	—	200	—	200	—	ns	See figure 18-6
RES pulse width 1*	tRESW1	6.0	—	6.0	—	6.0	—	t <sub>cy</sub>	
RES pulse width 2*	tRESW2	520	—	520	—	520	—	t <sub>cy</sub>	
RES output delay time	tRESO	—	100	—	100	—	100	ns	See figure 18-7
RES output pulse width	tRESOW	132	—	132	—	132	—	t <sub>cy</sub>	
Mode programming setup time	tMDS	4.0	—	4.0	—	4.0	—	t <sub>cy</sub>	See figure 18-6
NMI setup time	tNMIS	150	—	150	—	150	—	ns	See figure 18-8
NMI hold time	tNMIH	10	—	10	—	10	—	ns	
IRQ <sub>0</sub> setup time	tIRQ0S	50	—	50	—	50	—	ns	
IRQ <sub>1</sub> to IRQ <sub>7</sub> setup time	tIRQ1S	50	—	50	—	50	—	ns	
IRQ <sub>1</sub> to IRQ <sub>7</sub> hold time	tIRQ1H	10	—	10	—	10	—	ns	
NMI pulse width (for recovery from software standby mode)	tNMIW	200	—	200	—	200	—	ns	
A/D trigger setup time	tTRGS	50	—	50	—	50	—	ns	See figure 18-18
A/D trigger hold time	tTRGH	10	—	10	—	10	—	ns	
Crystal oscillator settling time (reset)	tOSC1	20	—	20	—	20	—	ms	See figure 18-9
Crystal oscillator settling time (software standby)	tOSC2	10	—	10	—	10	—	ms	See figure 17-1

Note: \* tRESW2 applies when the RSTOE bit in the reset control/status register (RSTCR) is set to 1. tRESW1 applies when RSTOE is cleared to 0. tRESW1 also applies at power-up.

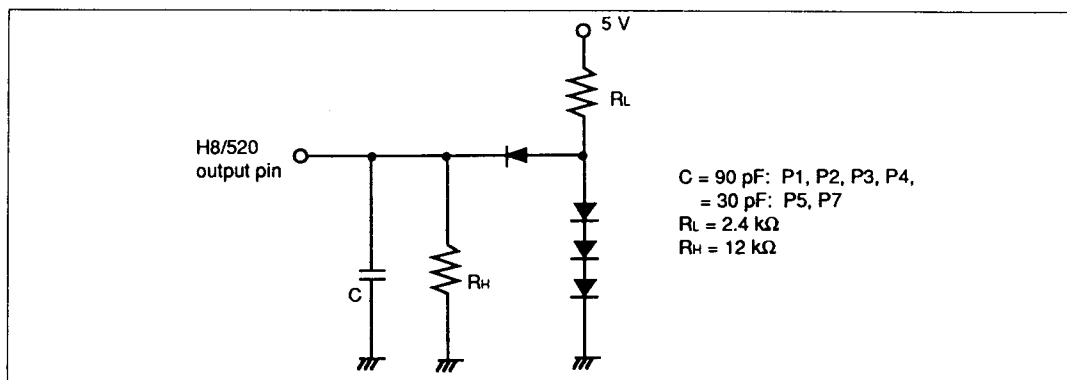


**Table 18-6 Timing Conditions of On-Chip Supporting Modules**

Conditions:  $V_{CC} = 5.0 \text{ V} \pm 10\%$ ,  $\phi = 0.5$  to 10 MHz,  $V_{SS} = 0 \text{ V}$   
 $T_a = -20$  to  $75^\circ\text{C}$  (Regular specifications)  
 $T_a = -40$  to  $85^\circ\text{C}$  (Wide-range specifications)

Item	Symbol	6 MHz		8 MHz		10 MHz		Unit	Test Conditions	
		min	max	min	max	min	max			
FRT	Timer output delay time	tFTOD	—	100	—	100	—	100	ns	See figure 18-11
	Timer input setup time	tFTIS	50	—	50	—	50	—	ns	
	Timer clock input setup time	tFTCS	50	—	50	—	50	—	ns	See figure 18-12
	Timer clock pulse width	tFTCW	1.5	—	1.5	—	1.5	—	t <sub>cy</sub>	
TMR	Timer output delay time	tTMOD	—	100	—	100	—	100	ns	See figure 18-13
	Timer clock input setup time	tTMCS	50	—	50	—	50	—	ns	See figure 18-14
	Timer clock pulse width	tTMCW	1.5	—	1.5	—	1.5	—	t <sub>cy</sub>	
	Timer reset input setup time	tTMRS	50	—	50	—	50	—	ns	See figure 18-15
SCI	Input clock cycle	(Async) t <sub>S<sub>cy</sub></sub>	2	—	2	—	2	—	t <sub>cy</sub>	See figure 18-16
		(Sync)	4	—	4	—	4	—	t <sub>cy</sub>	
	Input clock pulse width	t <sub>S<sub>CKW</sub></sub>	0.4	0.6	0.4	0.6	0.4	0.6	t <sub>S<sub>cy</sub></sub>	
	Transmit data delay time	(Sync) t <sub>R<sub>XD</sub></sub>	—	100	—	100	—	100	ns	See figure 18-17
	Receive data setup time	(Sync) t <sub>R<sub>XS</sub></sub>	100	—	100	—	100	—	ns	
Receive data hold time	(Sync) t <sub>R<sub>XH</sub></sub>	—	100	—	100	—	100	ns		
Ports	Output data delay time	t <sub>P<sub>WD</sub></sub>	—	100	—	100	—	100	ns	See figure 18-10
	Input data setup time	t <sub>P<sub>RS</sub></sub>	50	—	50	—	50	—	ns	
	Input data hold time	t <sub>P<sub>RH</sub></sub>	50	—	50	—	50	—	ns	

• Measurement Conditions for AC Characteristics



**Figure 18-3 Output Load Circuit**



### 18.2.3 A/D Converter Characteristics

Table 18-7 lists the characteristics of the on-chip A/D converter.

**Table 18-7 (1) A/D Converter Characteristics**

Conditions:  $V_{CC} = AV_{CC} = 5.0 \text{ V} \pm 10\%$ ,  $V_{SS} = AV_{SS} = 0 \text{ V}$ ,  
 $T_a = -40 \text{ to } 85^\circ\text{C}$  (Wide-range specifications)

Item	6 MHz			8 MHz			10 MHz			Unit
	min	typ	max	min	typ	max	min	typ	max	
Resolution	10	10	10	10	10	10	10	10	10	Bits
Conversion time	—	—	23.0	—	—	17.25	—	—	13.8	$\mu\text{s}$
Analog input capacitance	—	—	20	—	—	20	—	—	20	pF
Allowable signal-source impedance	—	—	10	—	—	10	—	—	10	k $\Omega$
Nonlinearity error	—	—	$\pm 2.0$	—	—	$\pm 2.0$	—	—	$\pm 2.0$	LSB
Offset error	—	—	$\pm 2.0$	—	—	$\pm 2.0$	—	—	$\pm 2.0$	LSB
Full-scale error	—	—	$\pm 2.0$	—	—	$\pm 2.0$	—	—	$\pm 2.0$	LSB
Quantizing error	—	—	$\pm 0.5$	—	—	$\pm 0.5$	—	—	$\pm 0.5$	LSB
Absolute accuracy	—	—	$\pm 2.5$	—	—	$\pm 2.5$	—	—	$\pm 2.5$	LSB

**Table 18-7 (2) A/D Converter Characteristics**

Conditions:  $V_{CC} = AV_{CC} = 5.0 \text{ V} \pm 10\%$ ,  $V_{SS} = AV_{SS} = 0 \text{ V}$ ,  
 $T_a = -20 \text{ to } 75^\circ\text{C}$  (Regular specifications)

Item	6 MHz			8 MHz			10 MHz			Unit
	min	typ	max	min	typ	max	min	typ	max	
Resolution	10	10	10	10	10	10	10	10	10	Bits
Conversion time	—	—	23.0	—	—	17.25	—	—	13.8	$\mu\text{s}$
Analog input capacitance	—	—	20	—	—	20	—	—	20	pF
Allowable signal-source impedance	—	—	10	—	—	10	—	—	10	k $\Omega$
Nonlinearity error	—	—	$\pm 3.5$	—	—	$\pm 3.5$	—	—	$\pm 3.5$	LSB
Offset error	—	—	$\pm 3.5$	—	—	$\pm 3.5$	—	—	$\pm 3.5$	LSB
Full-scale error	—	—	$\pm 3.5$	—	—	$\pm 3.5$	—	—	$\pm 3.5$	LSB
Quantizing error	—	—	$\pm 0.5$	—	—	$\pm 0.5$	—	—	$\pm 0.5$	LSB
Absolute accuracy	—	—	$\pm 4.0$	—	—	$\pm 4.0$	—	—	$\pm 4.0$	LSB



## 18.3 MCU Operational Timing

This section provides the following timing charts:

18.3.1 Bus timing	Figures 18-4 and 18-5
18.3.2 Control Signal Timing	Figures 18-6 to 18-8
18.3.3 Clock Timing	Figure 18-9
18.3.4 I/O Port Timing	Figure 18-10
18.3.5 16-Bit Free-Running Timer Timing	Figures 18-11 and 18-12
18.3.6 8-Bit Timer Timing	Figures 18-13 to 18-15
18.3.7 SCI Timing	Figures 18-16 and 18-17

### 18.3.1 Bus Timing

#### 1. Basic Bus Cycle (without Wait States) in Expanded Modes

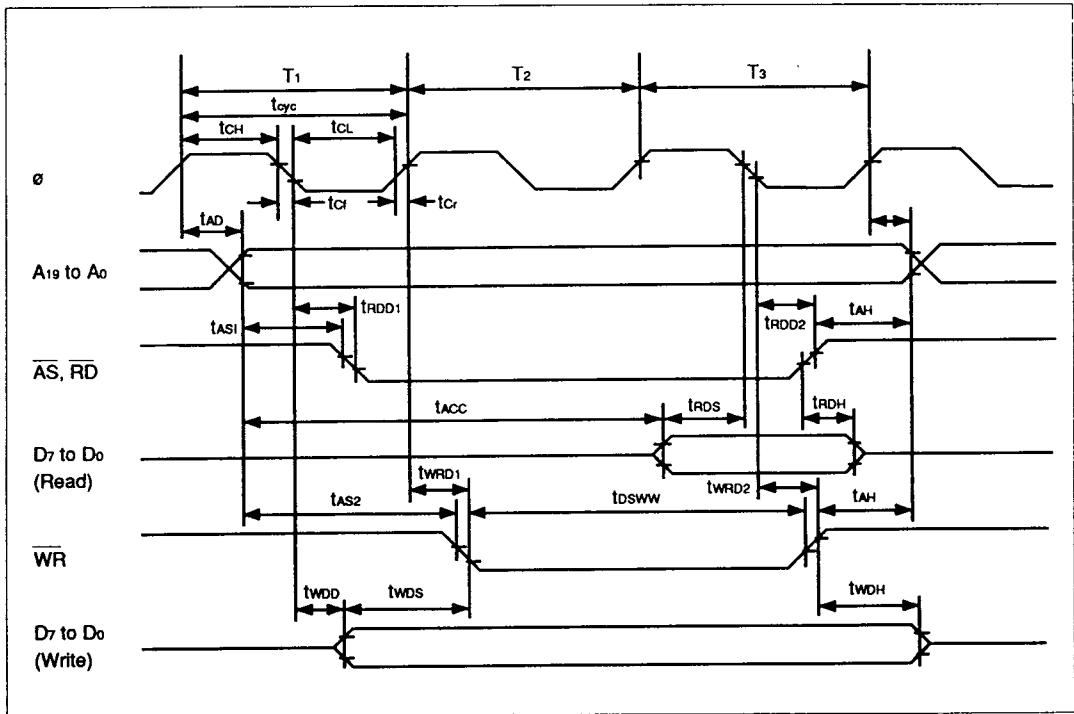
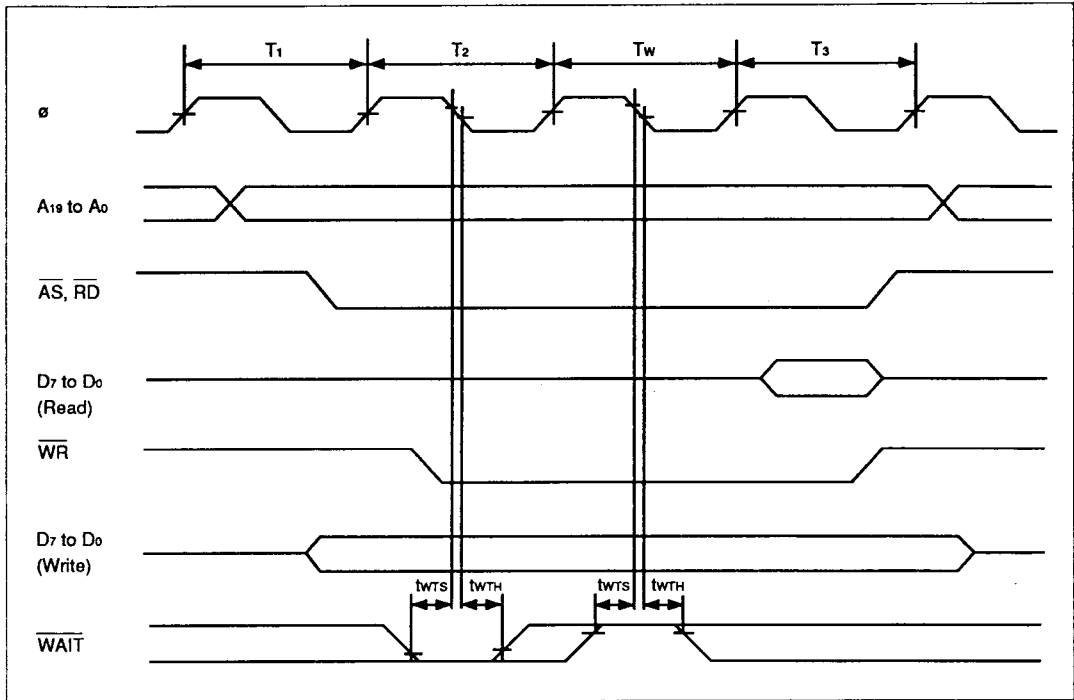


Figure 18-4 Basic Bus Cycle (without Wait States) in Expanded Modes



## 2. Basic Bus Cycle (with 1 Wait State) in Expanded Modes



**Figure 18-5 Basic Bus Cycle (with 1 Wait State) in Expanded Modes**



## 18.3.2 Control Signal Timing

### 1. Reset Input Timing

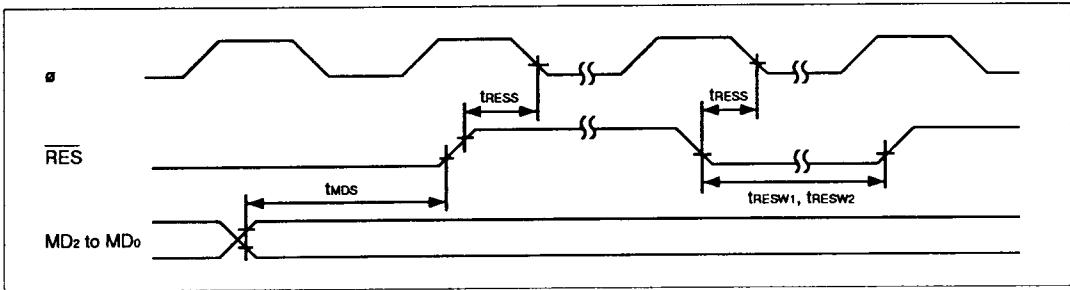


Figure 18-6 Reset Input Timing

### 2. Reset Output Timing

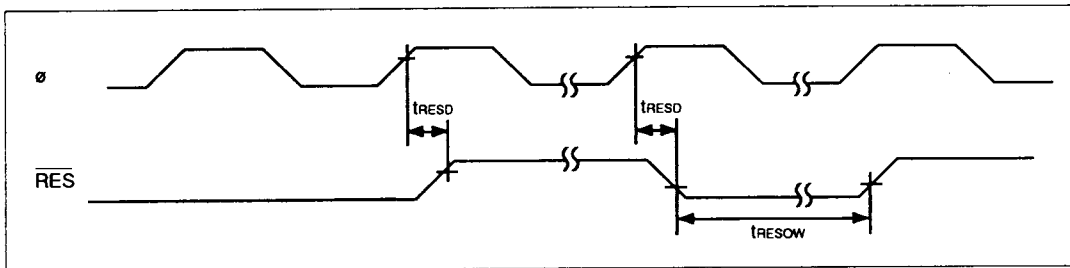


Figure 18-7 Reset Output Timing

### 3. Interrupt Input Timing

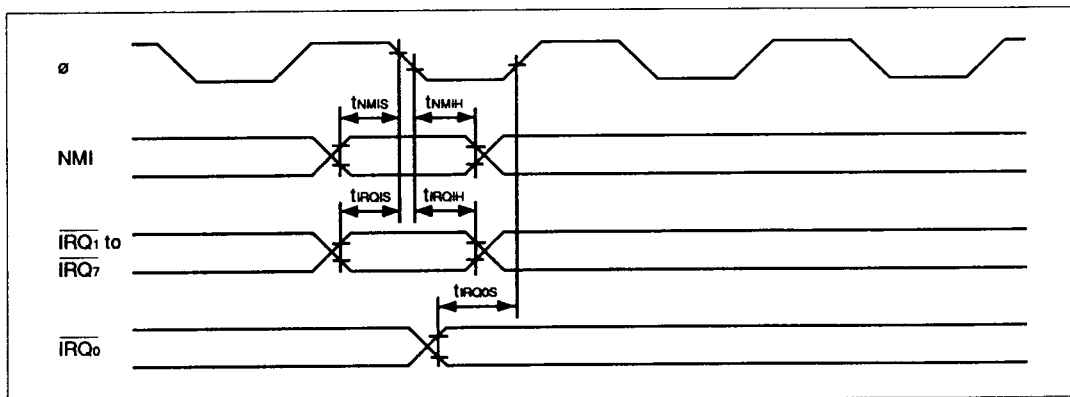
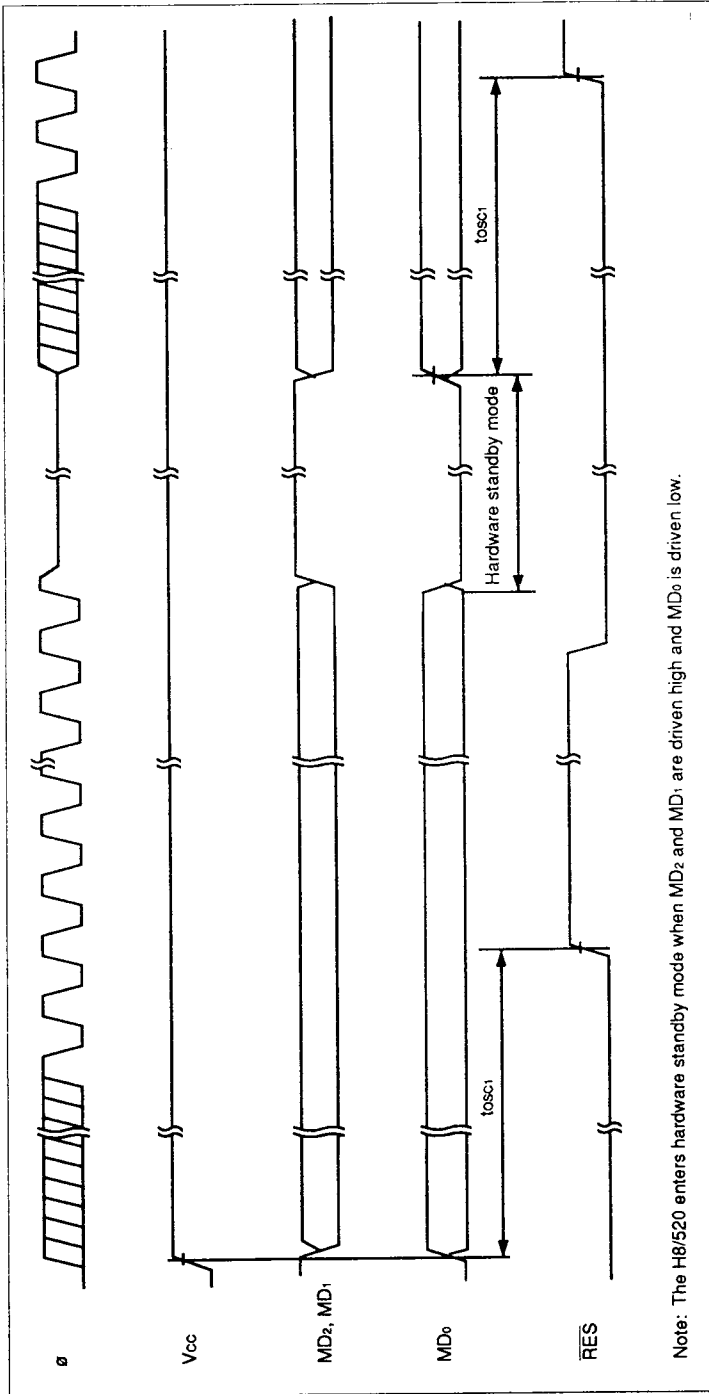


Figure 18-8 Interrupt Input Timing

### 18.3.3 Clock Oscillator Stabilization Timing



Note: The H8/520 enters hardware standby mode when MD<sub>2</sub> and MD<sub>1</sub> are driven high and MD<sub>0</sub> is driven low.

Figure 18-9 Clock Oscillator Stabilization

### 18.3.4 I/O Port Timing

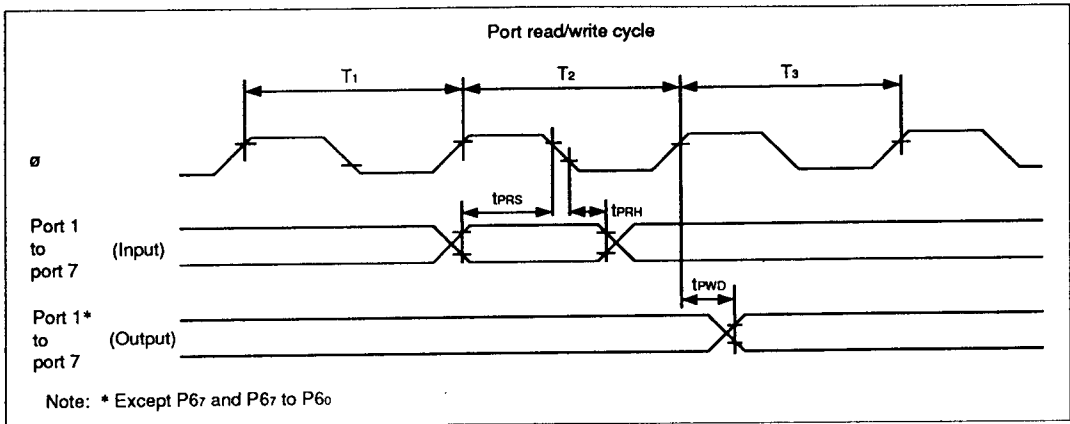


Figure 18-10 I/O Port Input/Output Timing



### 18.3.5 16-Bit Free-Running Timer Timing

#### 1. Free-Running Timer Input/Output Timing

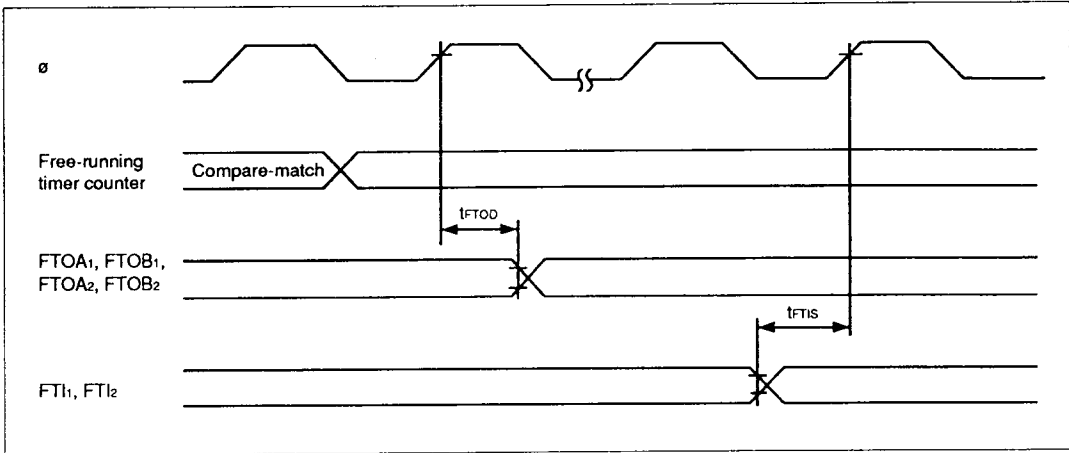


Figure 18-11 Free-Running Timer Input/Output Timing

#### 2. External Clock Input Timing for Free-Running Timers

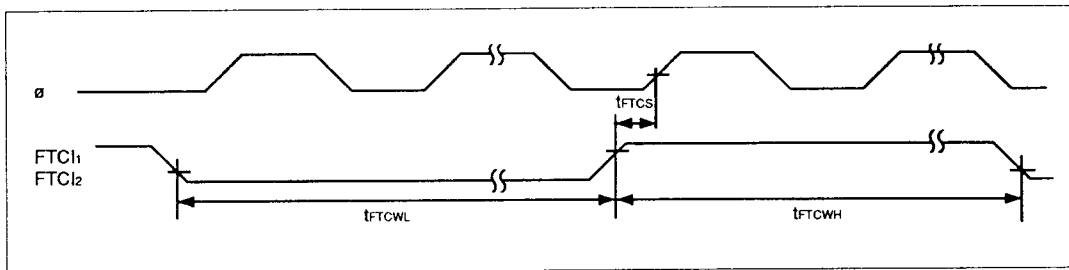


Figure 18-12 External Clock Input Timing for Free-Running Timers



### 18.3.6 8-Bit Timer Timing

#### 1. 8-Bit Timer Output Timing

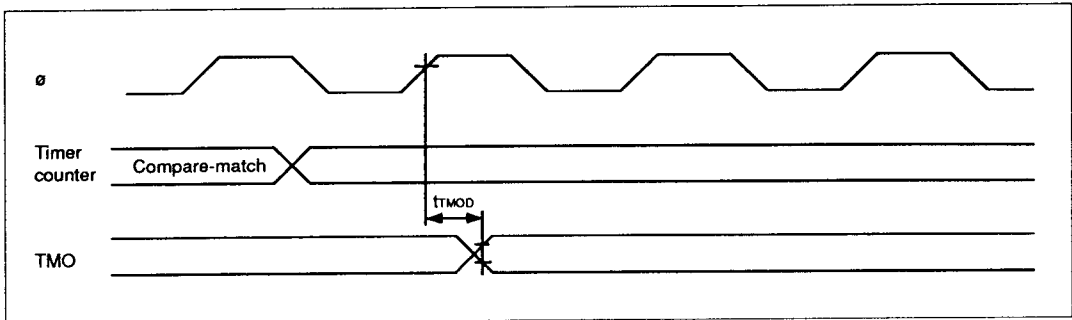


Figure 18-13 8-Bit Timer Output Timing

#### 2. 8-Bit Timer Clock Input Timing

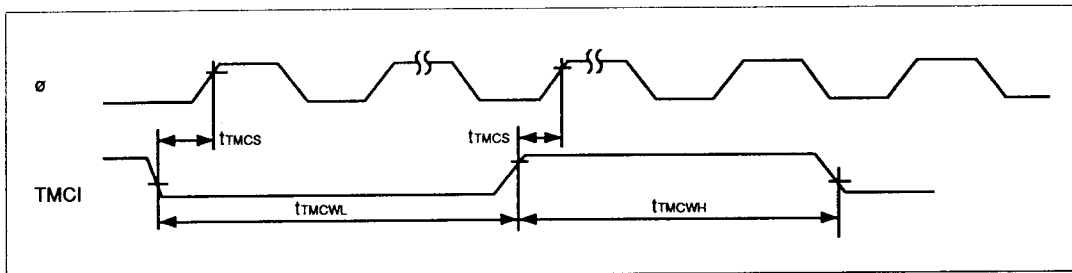


Figure 18-14 8-Bit Timer Clock Input Timing

#### 3. 8-Bit Timer Reset Input Timing

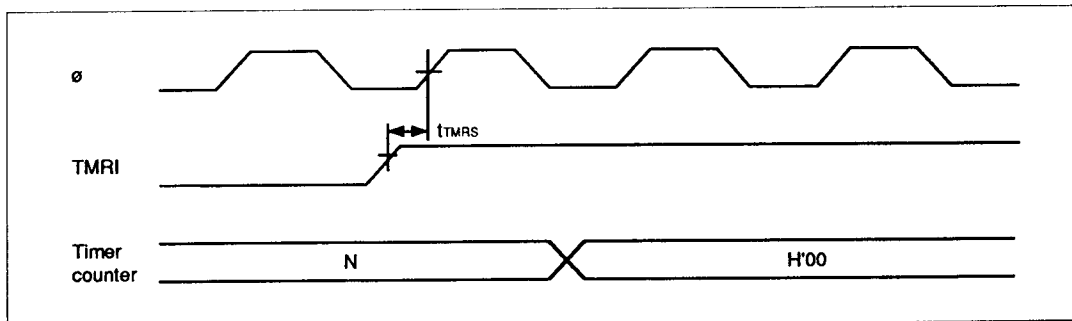


Figure 18-15 8-Bit Timer Reset Input Timing



### 18.3.7 Serial Communication Interface Timing

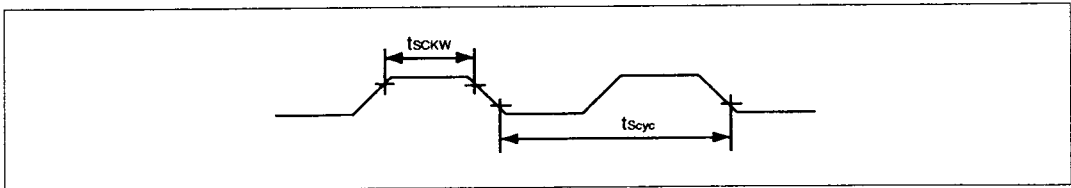


Figure 18-16 SCI Input Clock Timing

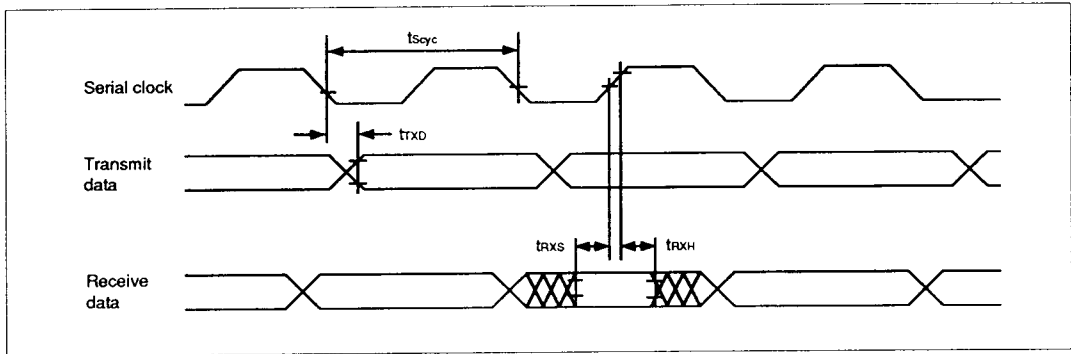


Figure 18-17 SCI Input/Output Timing (Synchronous Mode)

### 18.3.8 A/D External Trigger Input Timing

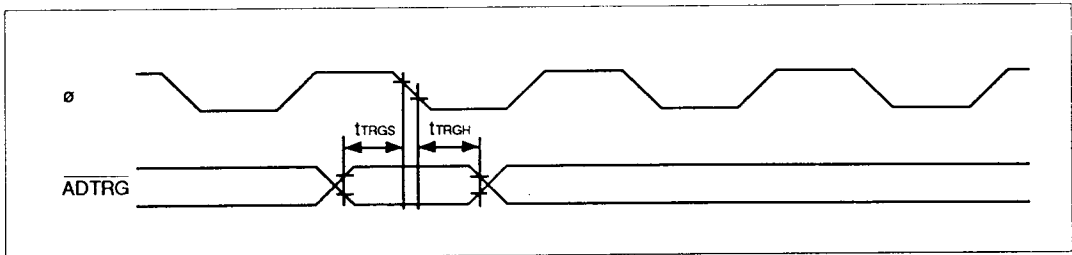


Figure 18-18 A/D External Trigger Input Timing



T-90-20

## Appendix F Package Dimensions

Figure F-1 shows the dimensions of the DC-64S package. Figure F-2 shows the dimensions of the DP-64S package. Figure F-3 shows the dimensions of the FP-64A package. Figure F-4 shows the dimensions of the CP-68 package.

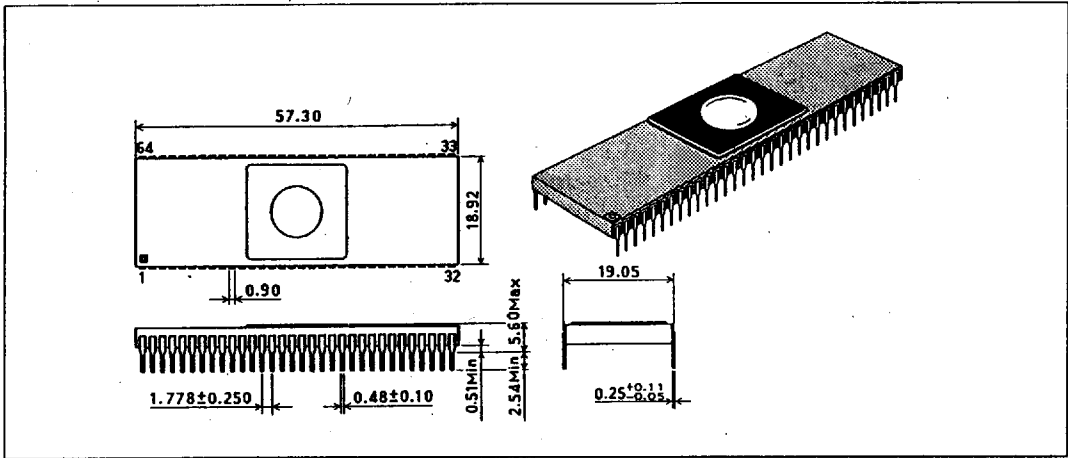


Figure F-1 Package Dimensions (DC-64S)

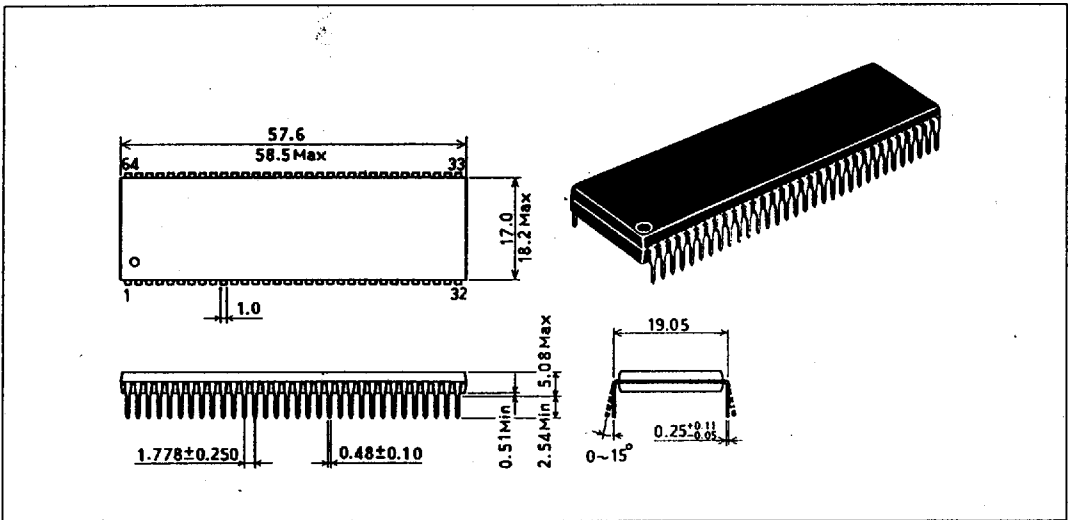


Figure F-2 Package Dimensions (DP-64S)





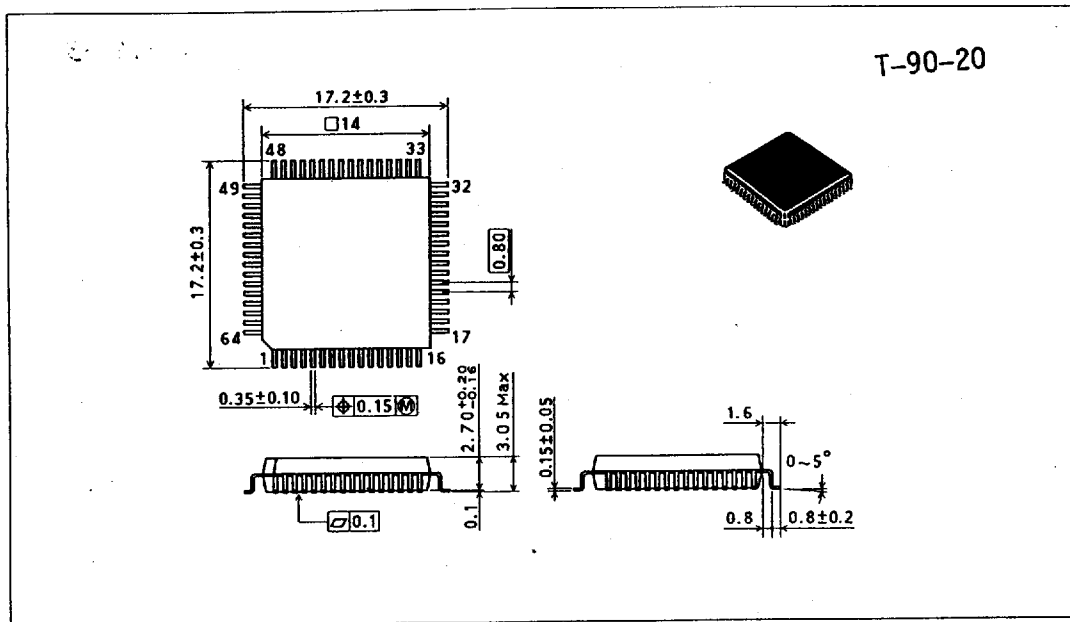


Figure F-3 Package Dimensions (FP-64A)

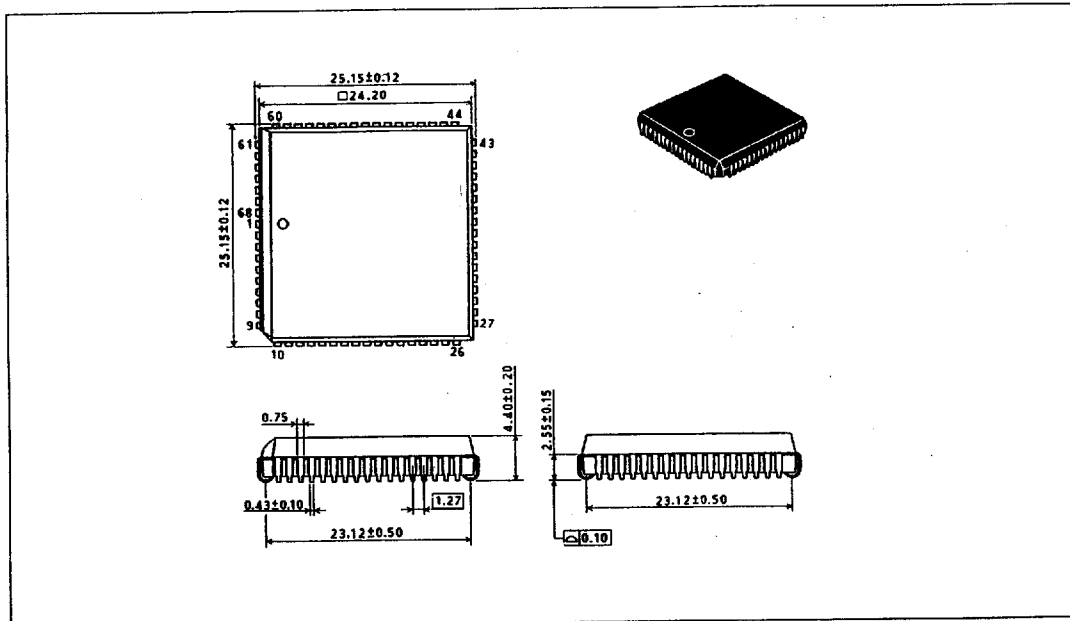


Figure F-4 Package Dimensions (CP-68)

