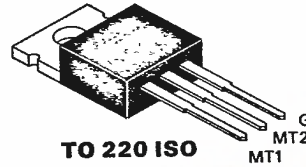


TAG SEMICONDUCTORS LTD

**T1213BJ -
T1213NJ TRIACS****12.0 A 200-800 V
50/50/50/75 mA**

The T1213 series isolated TRIAC's are high performance glass passivated PNP devices. These parts are intended for general purpose high current applications where high gate insensitivity is required.

U. L. Recognized, File Nr. E72763 (M)



TO 220 ISO

Absolute Maximum Ratings $T_A = 25^\circ\text{C}$ unless otherwise noted

Parameter	Part Nr.	Symbol	Min.	Max.	Unit	Test Conditions
Repetitive Peak Off State Voltage	T1213BJ	V_{DRM}	200		V	[$T_j = -40^\circ\text{C}$ to 125°C $R_{GK} = 1\text{K}\Omega$]
	T1213DJ		400		V	
	T1213MJ		600		V	
	T1213NJ		800		V	
On-State Current		$I_{T(RMS)}$	12		A	All Conduction Angles $T_C = 85^\circ\text{C}$
Nonrept. On-State Current		I_{TSM}	135		A	Half Cycle, 60 Hz
Nonrept. On-State Current		I_{TSM}	120		A	Half Cycle, 50 Hz
Fusing Current		I^2t	72		A^2s	$t = 10\text{ ms}$
Peak Gate Current		I_{GM}	4		A	$10\mu\text{s}$ max.
Peak Gate Dissipation		P_{GM}	10		W	$10\mu\text{s}$ max.
Gate Dissipation		$P_{G(AV)}$	1		W	20 ms max.
Isolation Voltage		V_{iso}	2500		VAC	
Operating Temperature		T_j	-40	125	$^\circ\text{C}$	
Storage Temperature		T_{stg}	-40	125	$^\circ\text{C}$	
Soldering Temperature		T_{sld}		250	$^\circ\text{C}$	1.6 mm from case, 10 s max.

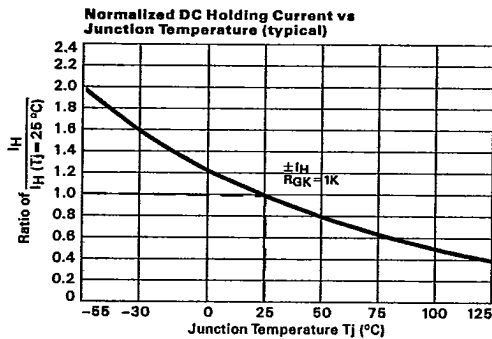
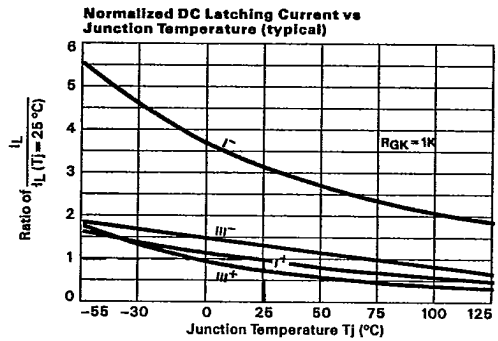
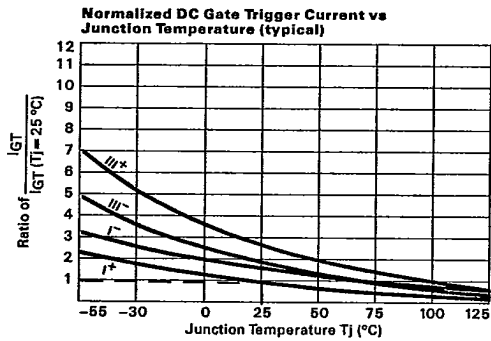
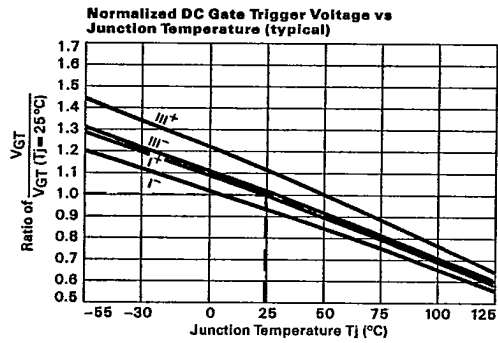
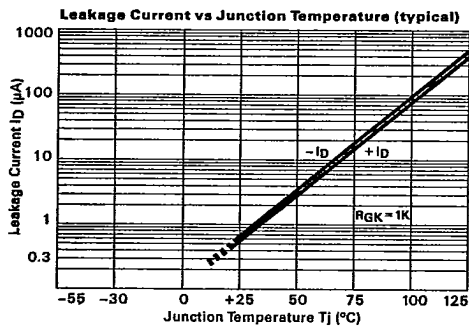
Electrical Characteristics $T_A = 25^\circ\text{C}$ unless otherwise noted

Parameter	Symbol	Min.	Max.	Unit	Test Conditions
Off-State Leakage Current	I_{DRM}		2.5	mA	$V_D = V_{DRM}$ $R_{GK} = 1\text{K}\Omega$ $T_j = 125^\circ\text{C}$
Off-State Leakage Current	I_{DRM}		10	μA	$V_D = V_{DRM}$ $R_{GK} = 1\text{K}\Omega$ $T_j = 25^\circ\text{C}$
On-State Voltage	V_T		1.36	V	at $I_T = 18\text{ A}$, $T_j = 25^\circ\text{C}$
On-State Threshold Voltage	$V_{T(TO)}$		0.9	V	$T_j = 125^\circ\text{C}$
On-State Slope Resistance	r_T		25	$\text{m}\Omega$	$T_j = 125^\circ\text{C}$
Gate Trigger Current	$I_{GT I+}$ (1)		50	mA	$V_D = 12\text{ V}$
	$I_{GT I-}$ (2)		50	mA	$V_D = 12\text{ V}$
	$I_{GT III-}$ (3)		50	mA	$V_D = 12\text{ V}$
	$I_{GT III+}$ (4)		75	mA	$V_D = 12\text{ V}$
Gate Trigger Voltage	V_{GT}		2.5	V	$V_D = 12\text{ V}$ All Quadrants
Holding Current	I_H		75	mA	$R_{GK} = 1\text{K}\Omega$
Critical Rate of Voltage Rise	dv/dt	500		$\text{V}/\mu\text{s}$	$V_D = .67 \times V_{DRM}$ $R_{GK} = 1\text{K}\Omega$ $T_j = 125^\circ\text{C}$
Critical Rate of Rise, Off-State	dv/dt_c	5		$\text{V}/\mu\text{s}$	$I_T = 12\text{ A}$ $di/dt = 5.33\text{ A/ms}$ $T_C = 85^\circ\text{C}$
Thermal Resistance junc. to case	$R_{\theta jc}$		2.8	K/W	
Thermal Resistance junc. to amb.	$R_{\theta ja}$		60	K/W	

T12

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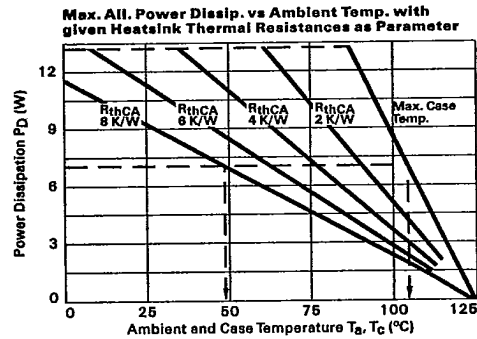
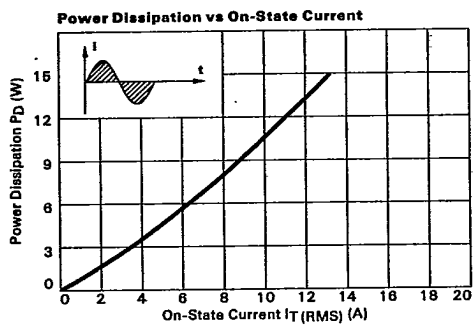
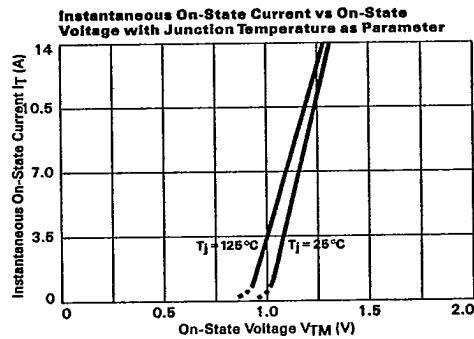
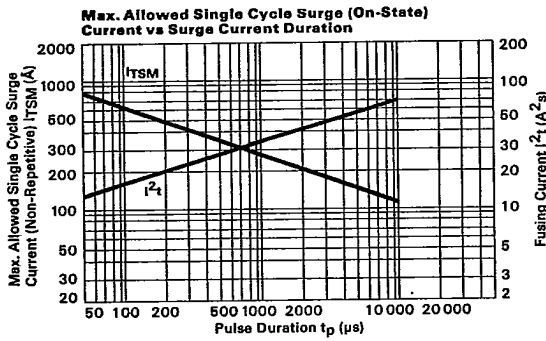
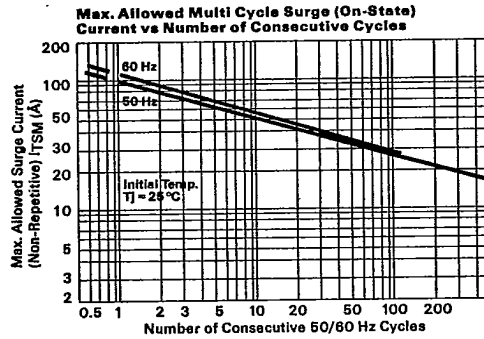
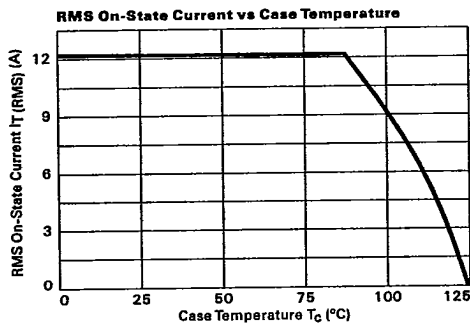
**Typical Characteristics
T12 - Chips**



T12

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**Typical Characteristics
T12 - Packaged Parts**



T12