SC1476
PORTABLE IMVP-IV™ DUAL PHASE POWER SUPPLY CONTROLLER

POWER MANAGEMENT **TARGET**

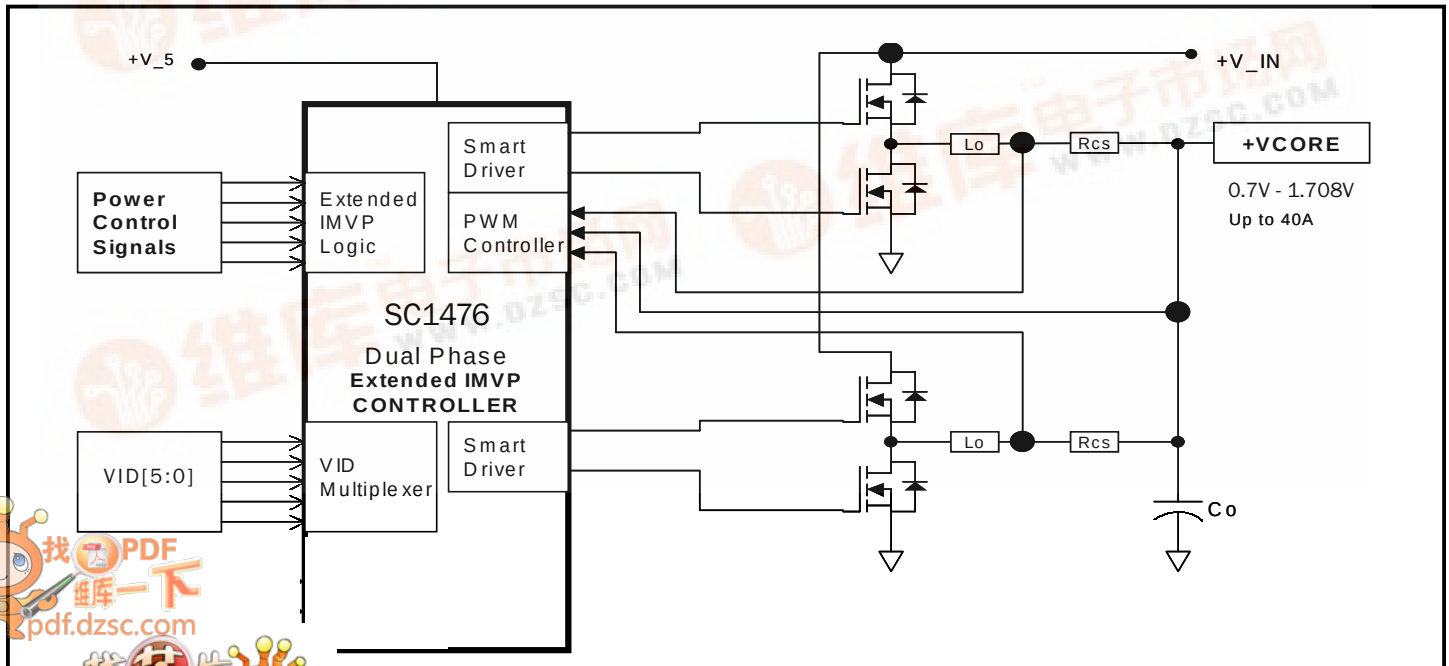
Description

The SC1476 PowerStep IV™ IC is a single chip high-performance Hysteretic PWM controller. With its integrated Smart™ Driver, it powers advanced Pentium® IV processors. The SC1476 features extended Intel Mobile Voltage Positioning (IMVP™) to increase battery life by reducing the voltage at the processor when it is heavily loaded. It directly supports Intel's SpeedStep™ processors for even longer battery life. The SC1476 fully supports the Intel® Geyserville-III™ core voltage specification. It provides direct "deeper sleep" mode and boot voltage support. Automatic "power-save" is present to prevent negative current flow in the low-side FET during light loading conditions, saving even more power.

A 6-bit DAC, accurate to 0.85%, sets the output voltage reference, and implements the 0.700V to 1.708V range required by the processor. The hysteretic converter uses a comparator without an error amplifier, and therefore provides the fastest possible transient response, while avoiding the stability issues inherent to classical PWM controllers.

The SC1476 operates from 3Vdc and 5Vdc and also features soft-start, an open-drain PWRGD signal with power-good blanking, and an enable input. Programmable current limiting shuts down the SC1476 after 32 current limit pulses. In addition, it comes in a space-saving TSSOP-38 package.

Typical Application Circuit



Features

- IMVP-IV™ compliant single chip solution
- High speed hysteretic controller
- Selectable single/dual phase operation
- Selectable constant-ripple or constant-frequency operation
- Selectable analog or VID controlled DeeperSleep setting
- 6 bit VID programmable output
- Integrated drivers
- Programmable softStart
- Programmable Boot voltage
- Programmable DeeperSleep voltage
- Dynamic phase current matching
- Under-voltage lock out on VccA
- Over-voltage protection on CORE
- Current Limit protection on CORE
- Thermal protection
- Powergood flag with blanking during VID or DeeperSleep mode changes
- Automatic powersave at light load
- TSSOP-38 package

Applications

- Notebook and Laptop computers

Absolute Maximum Ratings

Parameter	Name	Conditions	Min	Max	Units
Supply Voltages	V_{CCA}, V5_1, V5_2		-0.3	7	V
Input & Output Voltages	V_{VDPR}, V_{DPRSL}, V_{VID}[0..5], V_{DAC}, V_{CMPRF}, $V_{CMP1,2}$, V_{HYS}, V_{CORE}, $V_{CL1,2}$, V_{CLRF}, V_{PWRGD}, V_{PBOOT}, $V_{ISH1,2}$, V_{SS}, V_{GND}, $V_{BG1,2,}$ V_{CLSET}		-0.3	V_{CCA} + 0.3	V
EN	V_{EN}			7	V
BST1 to PGND1 BST2 to PGND2		static		36	V
BST1 to PGND1 BST2 to PGND2		transient < 100ns		40	V
BST1 to DRN1 BST2 to DRN2			-0.3	7	V
DRN1 to PGND1 DRN2 to PGND2		static	-2	30	V
DRN1 to PGND1 DRN2 to PGND2		transient < 100ns	-2	34	V
TG1, TG2			-2	BST1+0.3	V

Electrical Characteristics

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Supply (VCCA, V5_1, V5_2, GND)						
V5_1, V5_2 Supply Voltage Range	$V_{5\_1,\ V5\_2}$		4.3	5	6	V
VCCA Supply Voltage Range	V_{CCA}		2.9	3.3	6.0	V
VCCA Quiscent Current	I_{CCQ}	EN is low			10	µA
		EN is high, and in V_{CCA} UVLO		400		
VCCA Operating Current (static)	I_{CC}	When EN is high, not in UVLO		5		mA

Electrical Characteristics Cont.

Parameter	Symbol	Conditions		Min	Typ	Max	Units
Under Voltage Lock Out Circuits (VccA, V5_1, V5_2)							
Threshold (V_{CC}A falling)	V_{HCCA}			2.75	2.85	2.95	V
V_{CC}A Hysteresis	$V_{HYST\ CCA}$				110		mV
Threshold (V5_1, V5_2 falling)	V_{HV5}			3.9	4.1	4.3	V
V5_1, V5_2 Hysteresis	$V_{HYST\ V5}$				240		mV
Fixed Over Voltage Protection (CORE)							
Threshold (CORE rising)	$V_{TH\ CORE\ FIXED}$			1.95	2.0	2.05	V
Enable Input (EN)							
Input high	Ven ih	V_{CC}A = 2.7V -> 3.6V		2			V
		V_{CC}A > 3.6V		0.7*V_{CC}A			
Input low	Ven il					0.8	V
VCORE Power Good Generator (PWRGD, CORE)							
CORE Input threshold	$V_{TH\ CORE}$	V_{DAC} = 0.6 - 1.75V. Note that during UVLO, the output level of this signal is undefined.	upper threshold	1.1*V_{DAC}		1.14*V_{DAC}	V
			lower threshold	0.9*V_{DAC}		0.86*V_{DAC}	
			hysteresis		1		%
PWRGD Output Voltage	V_{PWRGD}	V_{CORE} = V_{DAC} Pulled-up with external resistor to VTT (1.2V)		0.95*V_{TT}			V
		Either V_{CORE} < 0.88*V_{DAC} or V_{CORE} > 1.12*V_{DAC}				0.4	
		EN is low or EN is high but UVLO condition				0.8	

Electrical Characteristics Cont.

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Core Converter Soft Start (SS)						
V_{SS_CORE} Soft Start Termination Threshold	V_{SS_TERM}		1.8	2.0	2.2	V
Core Converter Soft Start Current NOTE Soft Start cap is not discharged until Enable goes low or UVLO cuts in. To enable bias and soft-start, VSSCORE has to drop below V_{SS_EN}	I_{SS}	CORE Charge (Source) Current, V_{SS_CORE} = 0V	2.5	4	6	mA
		Discharge (Sink) Current, V_{SS_CORE} = 1.7V	5	10		mA
V_{SS_CORE} Soft Start Enable Threshold	V_{SS_EN}			40	100	mV
DAC (VID[5..0])						
VID Input Threshold	V_{VID_IH}		0.55			V
	V_{VID_IL}				0.45	
DAC Output Voltage Accuracy	V_{DAC_ERR}	0 < T_A < 85 °C I_{DAC} = 0 VID[5..0] = 000000 ... 111000 (1.708V ... 0.812V)	-0.85		+0.85	%
		-40 < T_A < 85 °C I_{DAC} = 0 VID[5..0] = 000000 ... 111000 (1.708V ... 0.812V)	-1.5		+1.5	
		VID[5..0] = 111001 ... 111111 (0.796V ... 0.700V)	-2.0		+2.0	
Settling Time (guaranteed by design)	$T_{SET\_VID\_DAC}$	C_{DAC} = 1000pF, R_{DAC} = 100kΩ, VID is set to change VCORE from 1.30V to 1.45V or 1.45V to 1.30V. Measured from VID[0..5] code transient to VDAC settling within ± 1% of its steady state value.			35	ms
BOOT VOLTAGE (PBOOT)						
Input voltage offset	$\|V_{PBOOT}-V_{DAC}\|$	PBOOT=1.2V			|±3|	%
BOOT delay	T_{BOOT}		10			ms

Electrical Characteristics Cont.

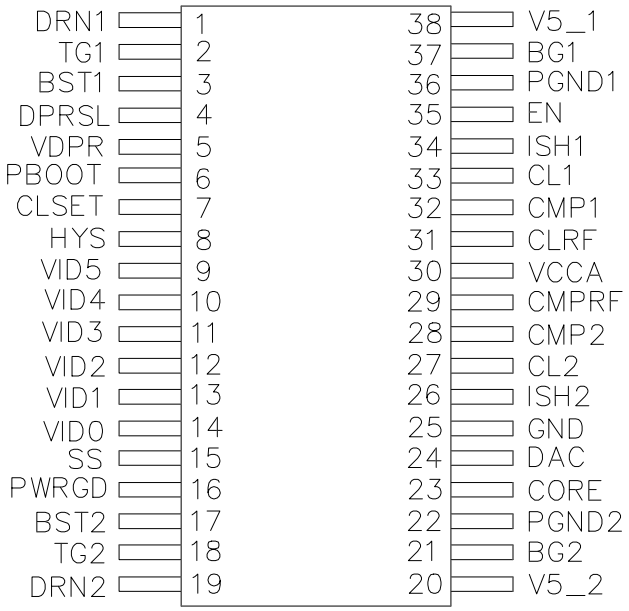
Parameter	Symbol	Conditions		Min	Typ	Max	Units
Deeper Sleep (DPRSL, VDPR)							
Input Offset Voltage	$\|V_{VDPR} - V_{DAC}\|$	V_{VDPR} = 0.75V				|±3|	%
Dprsl logic Threshold	V_{DPRSL_IH}			2			V
	V_{DPRSL_IL}					0.8	
VDPR VDPR/VID Mode select logic Threshold	V_{VDPR_IL}	status is latched when part is enabled		2.1			V
CORE Comparator (CMP1, CMP2, CMPRF, HYS)							
Input Bias Current	I_{CMPRF}	$V_{CMP} = V_{CMPREF}$ = 1.3V				|±2|	mA
Input Offset Voltage	$\|V_{CMP1,2} - V_{CPMREF}\|$				|±1.5|	|±3|	mV
Hysteresis Setting Current Constant Ripple Mode	$I_{R\_CMP1,2}$	R_{HYS} = 17 kΩ,		|±90|	|±100|	|±110|	mA
			dual phase $V_{cmp}>V_{cmprf}$	-2		+6	
		R_{HYS} = 170 kΩ		|±7|	|±10|	|±13|	
			dual phase $V_{cmp}>V_{cmprf}$	-1.5		2	
Hysteresis Setting Current Constant Frequency Mode	$I_{F\_CMP1,2}$	R_{HYS} = 17 kΩ,	VID=000000	|±90|	|±100|	|±110|	mA
			VID=111111	|±35|	|±41|	|±47|	
Propagation Delay Time** **Guaranteed by Characterization	$T_{pd\ CMP1-BG1}$, $T_{pd\ CMP2-BG2}$,	V_{CMPREF} = 1.3V D $V_{CMP1,2}$ = 40 mV input step with 20 mV overdrive. Measured at device pins, from the trip point to 10% of BG transition.	T_A = 25 °C			40	ns
			T_A = full range.			50	
Current Limit Comparator (CL1, CL2, CLRF, CLSET)							
Input Bias Current	$\|±I_{CL1,2}\|$	V_{CL} = 1.3V				|±5|	mA
Current Limit Setting Current	$\|±I_{CLREF}\|$	R_{GYS} = 17 kΩ	$V_{CLREF} - V_{CL}$ = -10mV		200		mA
			$V_{CLREF} - V_{CL}$ = 10mV		300		
CLSET Constant Ripple/Constant Frequency Mode select threshold	V_{CLSET_IH}	status is latched when part is enabled		2.1			V

Electrical Characteristics Cont.

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Current Limit Comparator (CL1, CL2, CLRF, CLSET) Cont.						
Input Offset Voltage	$\|V_{CL1,2} - V_{CLREF}\|$	V_{CLREF} = 1.3V		|±4|	|±6|	mV
CL2 Single/Dual phase mode select logic threshold	V_{CL2_IH}	status is latched when part is enabled	2.1			V
High-Side Drivers (TG1, TG2)						
Peak Output Current	I_{pkh}			2		A
Output Resistance	R_{SRC}			1	3	Ω
	R_{SINK}			1	3	
Rise Time	tr_{TG}	CL = 3nF, $V_{BST} - V_{DRN}$ = 5V		15	24	ns
Fall Time	tf_{TG}			15	24	ns
Propagation delay, TG going high				20	32	ns
Propagation delay, TG going low				15	24	ns
Low-Side Driver (BG1, BG2)						
Peak Output Current	I_{pkl}			4		A
Output Resistance	R_{SRC}			1	3	Ω
	R_{SINK}			0.5	2	
Rise Time	tr_{BG}	Cl = 3nF, V_{V5} = 5V		15	24	ns
Fall Tlme	tf_{BG}			10	17	ns
Propagation delay, BG going high				12	19	ns
Propagation delay, BG going low				7	12	ns
Powersave Comparators (CORE, CL1, CL2)						
Comparator offset	$V_{CL1,2}$-V_{CORE}		-5	0	+5	mV
Dynamic Current Sharing (ISH1, ISH2)						
I_{SHARE} enable logic threshold	V_{ISH1_IL}		0.3	0.4	0.5	V
I_{SHARE} range			12	17	27	$\%I_{CLSET}$

Pin Configuration

Top View



(38 pin TSSOP)

Ordering Information

DEVICE	PACKAGE	TEMP RANGE (T_J)
SC1476ITSTR	TSSOP-38	-40°C to 125°C

Pin Descriptions

Pin #	Pin Name	Pin Description
1	DRN1	This pin connects to the junction of the phase 1 switching and synchronous MOSFETs.
2	TG1	Output gate drive for the phase 1 switching (high-side) MOSFET.
3	BST1	Bootstrap pin for phase 1. A capacitor is connected between BST2 and DRN2 pins to develop the floating bootstrap voltage for the high-side MOSFET.
4	DPRSL	DeeperSleep logic input signal.
5	VDPR	Connect this pin to VccA to select "VID DeeperSleep Mode" . Otherwise, "VDPR DeeperSleep Mode" is selected and the voltage on this pin sets the DAC output during DeeperSleep.
6	PBOOT	The voltage on this pin sets the Boot Up voltage.
7	CLSET	Connect this pin to VccA to enable ""Constant Ripple Mode"". Otherwise, connect to ground thru an external resistor, called RCLSET to enable ""Constant Frequency Mode"". Current Limit Hysteresis current is established by an internal VREF voltage, 1.7V, divided by RCLSET in ""Constant Frequency Mode"".
8	HYS	Core Comparator Hysteresis. Connect to ground thru an external resistor, called RHYS. In ""Constant Ripple Mode"", Hysteresis current is established by an internal VREF voltage, 1.7V, divided by RHYS. In ""Constant Frequency Mode"", Hysteresis current is established by an internal voltage equal to VDAC divided by RHYS.

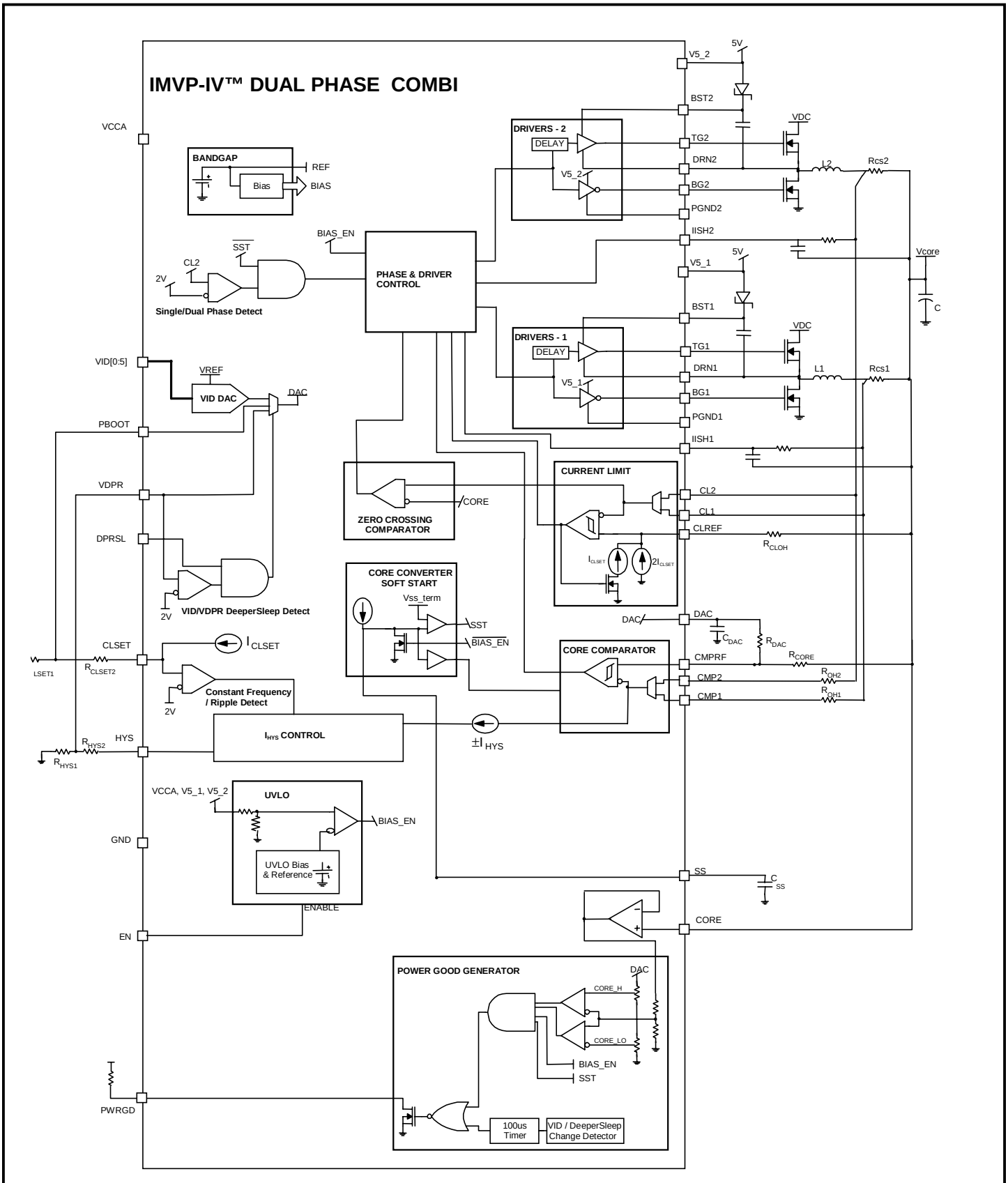
Pin Descriptions Cont.

Pin #	Pin Name	Pin Description
9	VID5	VID most significant bit main controller voltage programming DAC input.
10	VID4	VID input
11	VID3	VID input
12	VID2	VID input
13	VID1	VID input
14	VID0	VID least significant bit main controller voltage programming DAC input.
15	SS	Soft Start. An external cap defines the soft start ramp.
16	PWRGD	Power Good - open drain output. When the Main Converter Output approaches and stays within ± 14% of the VID_DAC setting, and the soft-start period has terminated, this signal is pulled high by an external resistor.
17	BST2	Bootstrap pin for phase 2. A capacitor is connected between BST2 and DRN2 pins to develop the floating bootstrap voltage for the high-side MOSFET.
18	TG2	Output gate drive for the phase 2 switching (high-side) MOSFET.
19	DRN2	This pin connects to the junction of the phase 2 switching and synchronous MOSFETs.
20	V5_2	5V supply for phase 2. A capacitor should be connected from V5_2 to PGND2.
21	BG2	Output drive for the phase 2 synchronous (low-side) FET.
22	PGND2	Power ground for phase 2. Connect to the synchronous FET power ground.
23	CORE	Main CORE Converter Output Feedback to the power-good generator. A small RC filter should be used to filter out any HF component to prevent faulty trip condition.
24	DAC	Main controller Digital-to-Analog Output.
25	GND	Ground.
26	ISH2	Driver 2 current sharing filter pin.
27	CL2	Current Limit Input Pin for phase 2. Hold this pin at VccA during softStart to enable Single Phase operation.
28	CMP2	Core Comparator input pin for phase 2.
29	CMPRF	Shared Core Comparator Reference input pin.
30	VCCA	3.3V or 5V supply for precision analog circuitry.

Pin Descriptions Cont.

Pin #	Pin Name	Pin Description
31	CLRF	Shared Current Limit Reference Input Pin.
32	CMP1	Core Comparator input pin for phase 1.
33	CL1	Current Limit Input Pin for phase 1.
34	ISH1	Driver 1 current sharing filter pin. Pull this pin to Gnd to disable current sharing.
35	EN	Enable - active high. This is capable of accepting a 5.0V signal level.
36	PGND1	Power ground for phase 1. Connect to the synchronous FET power ground.
37	BG1	Output drive for the phase 1 synchronous (low-side) FET.
38	V5_1	5V supply for phase 1. A capacitor should be connected from V5 to PGND.

Block Diagram



Applications Information

SUPPLY, BIAS, UVLO, POWERGOOD GENERATOR

Supply

The chip is optimized to operate from a 3.3 V ± 5% rail but also designed to work up to 6V maximum supply voltage. If VccA is out of the 3.3V ± 5% voltage range, the quiescent current will increase somewhat and slight degradation of line regulation is expected.

Under Voltage Lock-Out Circuit

The Under-Voltage-Lock-Out Circuit consists of comparators which monitor the VCCA, V5_1 and V5_2 voltage levels. The SC1476 is in UVLO mode whilst any of the supplies has not ramped above the upper threshold or has dropped below the lower threshold. During UVLO, the external FETs are held off, tri-stating the output.

Power Good Generator

If the chip is enabled but not in UVLO condition, and the core voltage gets within ± 14% vicinity of the VID programmed value, then a high level Power Good signal is generated on the PWRGD pin to trigger the processor power up sequence. If the chip is either disabled or enabled but in UVLO condition, then PWRGD is undefined. This is an open-drain output and will be pulled-up externally by a resistor.

During soft start, PWRGD stays low independently from the status of Vcore voltage. During VID code change latency time or a DeeperSleep transition, PWRGD is forced high (open drain) by logic circuits.

Over-voltage Protection

If the CORE voltage is greater than +14% of the DAC (i.e. out of the powergood window), the SC1476 will latch off and hold the low-side driver on permanently. Either the power or EN must be recycled to clear the latch. The latch is disabled during softstart and VID/DeeperSleep transitions. For safety, the latch is enabled if the CORE voltage exceeds 2V even during VID/DeeperSleep transitions.

Thermal Shutdown

The device will be disabled and latched off when the internal junction temperature reaches approximately 160°C. Either the power or EN must be recycled to clear the latch.

CORE CONVERTER CONTROLLER

Precision VID DAC Reference

This 6-bit digital-to-analog converter (DAC) serves as the programmable reference source of the Core Comparator. Programming is accomplished by logic voltage levels applied to the DAC inputs. The VID code vs. the DAC output is shown in the table below. The accuracy of the VID DAC is maintained on the same level as of the Band Gap Reference.

VID						V_{DAC}	VID						V_{DAC}
5	4	3	2	1	0	V	5	4	3	2	1	0	V
0	0	0	0	0	0	1.708	1	0	0	0	0	0	1.196
0	0	0	0	0	1	1.692	1	0	0	0	0	1	1.180
0	0	0	0	1	0	1.676	1	0	0	0	1	0	1.164
0	0	0	0	1	1	1.660	1	0	0	0	1	1	1.148
0	0	0	1	0	0	1.644	1	0	0	1	0	0	1.132
0	0	0	1	0	1	1.628	1	0	0	1	0	1	1.116
0	0	0	1	1	0	1.612	1	0	0	1	1	0	1.100
0	0	0	1	1	1	1.596	1	0	0	1	1	1	1.084
0	0	1	0	0	0	1.580	1	0	1	0	0	0	1.068
0	0	1	0	0	1	1.564	1	0	1	0	0	1	1.052
0	0	1	0	1	0	1.548	1	0	1	0	1	0	1.036
0	0	1	0	1	1	1.532	1	0	1	0	1	1	1.020
1	0	1	1	0	0	1.516	1	0	1	1	0	0	1.004
0	0	1	1	0	1	1.500	1	0	1	1	0	1	0.988
0	0	1	1	1	0	1.484	1	0	1	1	1	0	0.972
0	0	1	1	1	1	1.468	1	0	1	1	1	1	0.956
0	1	0	0	0	0	1.452	1	1	0	0	0	0	0.940
0	1	0	0	0	1	1.436	1	1	0	0	0	1	0.924
0	1	0	0	1	0	1.420	1	1	0	0	1	0	0.908
0	1	0	0	1	1	1.404	1	1	0	0	1	1	0.892
0	1	0	1	0	0	1.388	1	1	0	1	0	0	0.876
0	1	0	1	0	1	1.372	1	1	0	1	0	1	0.860
0	1	0	1	1	0	1.356	1	1	0	1	1	0	0.844
0	1	0	1	1	1	1.340	1	1	0	1	1	1	0.828
0	1	1	0	0	0	1.324	1	1	1	0	0	0	0.812
0	1	1	0	0	1	1.308	1	1	1	0	0	1	0.796
0	1	1	0	1	0	1.292	1	1	1	0	1	0	0.780
0	1	1	0	1	1	1.276	1	1	1	0	1	1	0.764
0	1	1	1	0	0	1.260	1	1	1	1	0	0	0.748
0	1	1	1	0	1	1.244	1	1	1	1	0	1	0.732
0	1	1	1	1	0	1.228	1	1	1	1	1	0	0.716
0	1	1	1	1	1	1.212	1	1	1	1	1	1	0.700

Applications Information Cont.

Core Comparator

This is an ultra-fast hysteretic comparator with a typical propagation delay of about 20ns at a 20mV overdrive. Hysteresis is generated by the current set at the HYS pin impressed upon an external resistor connected to the CMP1 and CMP2 pins.

In "Constant Frequency Mode", the hysteresis current will vary with DAC voltage.

Current Limit Comparator

The Current Limit Comparator monitors the core converter output current in each phase and turns the high side switch off when the current in either phase exceeds the upper current limit threshold, V_{HCL} and re-enabled only if the phase current drops below the lower current limit threshold, V_{LCL}. Each current is sensed by monitoring the voltage drop across the current sense resistor, R_{CS} connected in series with the core converter inductor.

In "Constant Frequency" mode, V_{HCL} and V_{LCL} are fixed by the current set at the CLSET pin impressed upon an external resistor connected to the CLRF pin. In "Constant Ripple" mode, V_{HCL} and V_{LCL} are fixed by the current set at the HYS pin impressed upon an external resistor connected to the CLRF pin.

The Current Limit hysteresis current is always a fixed (programmable) value and does not vary with DAC voltage, even in "Constant Frequency Mode".

Current limit Latch

If the CORE voltage goes lower than 14% below the VID (i.e. out of the powergood window), then sustained current limiting (32 current limit pulses) will cause the part to permanently latch off. The latch is inhibited during soft-start.

Core Converter Soft Start Timer

This block controls the start-up ramp time of the CORE voltage up to the boot voltage. The primary purpose is to reduce the initial in-rush current on the core input voltage (battery) rail. The timer also sets the delay before allowing the PWRGD signal to transition high.

Powergood blanking

On any VID change or DeeperSleep change, the PowerGood signal is blanked for 32 phase 1 switching cycles to prevent glitching on the PowerGood during the transition.

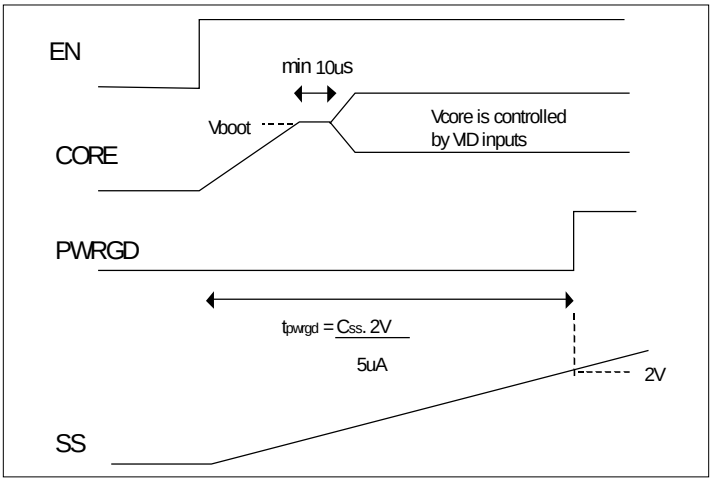
Deeper Sleep function

In "VDPR DeeperSleep" mode, the DAC output is set by the voltage on the VDPR pin when the DPRSL pin is held high. In "VID DeeperSleep" mode, the DAC output is set by the VID bits when DPRSL is held high.

On a DPRSL transition, the PWGD pin is forced high (blanked) for 32 phase 1 switching cycles.

Cycle-by-cycle Power-Save

Two zero-crossing comparators detect when the currents thru the external sense resistors reduce to zero. When either of the phase currents are at zero, the bottom FET for that particular phase is latched off. The latch is reset when the controller decides to switch on the associated top FET. This prevents excessive switching at light loads and hence saves switching power losses.



Dynamic Current Sharing

Using Semtech's proprietary algorithm, Dynamic Current Sharing is achieved by comparing the average current in each phase dynamically altering the switching set-points to match the phase currents. This helps to reduce hotspotsin the application.

Dynamic current sharing may be disabled by holding the ISH1 pin at GND. In this case, the controller will still deliver a certain amount of inherent current sharing.

Applications Information Cont.

Program Boot

On start-up, Vcore ramps to the Boot voltage set by the PBOOT pin irrespective of the status of the VID pins. After a minimum of 10us, Vcore responds to the VID inputs.

Single/Dual phase Mode

By default the controller operates in “Dual Phase” mode. “Single phase” mode is selected by holding the CL2 pin at VccA during start-up. In single phase mode, Driver 1 is active. But V5_2 must still be connected to supply to prevent faulty UVLO trips.

Constant Frequency/Constant Ripple Mode

By default, the controller operates in “Constant Frequency“ mode. In this mode, the DAC voltage is applied to the HYS pin causing the hysteresis current for the Core Comparator to track the DAC voltage. This maintains a pseudo constant frequency with respect to Vcore voltage as long as there is continuous conduction. However, the output ripple voltage will vary.

“Constant Ripple” Mode is selected by holding the CLSET pin at VccA during start-up. In this mode, the voltage at the HYS pin is a fixed 1.7V and the Core Comparator hysteresis current is static, irrespective of DAC voltage. This controls the output ripple to a constant value but allows the frequency to vary.

VDPR/VID DeeperSleep Mode

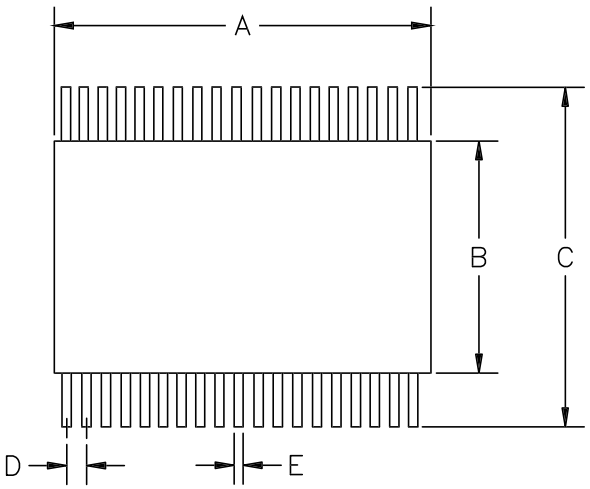
By default, the controller is in “VDPR controlled DeeperSleep” mode. In this mode, the voltage applied to the VDPR pin appears at the DAC output when DPRSL is asserted.

By holding the VDPR pin at VccA during start-up, “VID controlled DeeperSleep” mode is engaged. In this mode, the DAC output continues to be set by the VID inputs even when DPRSL is asserted.

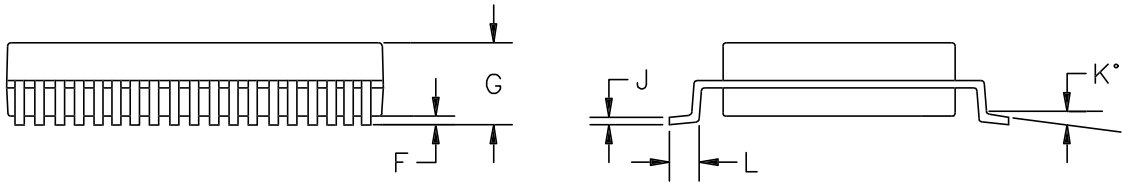
Summary of Fault Conditions

Protection Mode	Latched	When Active	Driver Status	SS Pin Status
Supply UVLO (VccA, V5_1, V5_2)	no	always	all low	low
32 cycle current limit	yes	SoftStart has terminated and PWRGD is low	TG1,TG2 low	sawtooth
114% Vcore OVP	yes	SoftStart has terminated and PWRGD is low	BG1, BG2 high	high
2.0V Vcore OVP	yes	always	BG1, BG2 high	high
Thermal Shutdown	yes	always	all low	high

Outline Drawing TSSOP-38



DIMENSIONS ①					
DIM	INCHES		MM		NOTE
	MIN	MAX	MIN	MAX	
A	.3779	.3858	9.60	9.80	②
B	.169	.177	4.30	4.50	②
C	.252 BSC		6.40 BSC		—
D	.0197 BSC		.50 BSC		—
E	.007	.012	.19	.30	—
F	.0020	.0060	.05	.15	—
G		.047		1.20	—
J	.0035	.0079	.09	.20	—
K	0°	8°	0°	8°	—
L	.018	.030	.45	.75	—



② DIMENSIONS A AND B DO NOT INCLUDE MOLD PROTRUSIONS.

① CONTROLLING DIMENSIONS: MILLIMETERS.

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