BUILT-IN DELAY CIRCUIT HIGH-PRECISION VOLTAGE DETECTOR

S-809xxC Series

The S-809xxC Series is a high-precision voltage detector developed using CMOS process. The detection voltage is fixed internally with an accuracy of ±2.0%. A time delayed reset can be accomplished with the addition of an external capacitor. Two output forms, N-channel open-drain and CMOS output, are available.

■ Features

- Ultra-low current consumption
  1.0 µA typ. (V_{DD}=2.0 V)
  ; Detection voltage ≤ 1.4 V
  1.1 µA typ. (V_{DD}=3.5 V)
  ; Detection voltage ≥ 1.5 V
- High-precision detection voltage ±2.0%
- Operating voltage range 0.7V to 10.0V
- Detection voltage 1.3 V to 6.0 V (0.1 V step)
- Hysteresis characteristics 5% typ.
- Two output forms CMOS output active “L”
  Open-drain output active “L”

■ Applications

- Power supply monitor for portable equipment such as electronic organizers, notebook PCs, cellular phones, digital cameras
- Constant voltage power monitor for cameras, communication equipment and video equipment
- Power monitor and reset for CPUs and microcomputers

■ Packages

SC-82AB	(Package drawing code, NP004-A)
4-pin SNB(B)	(Package drawing code, BB004-A)
SOT-23-5	(Package drawing code, MP005-A)

■ Block Diagrams

(1) Open-drain output

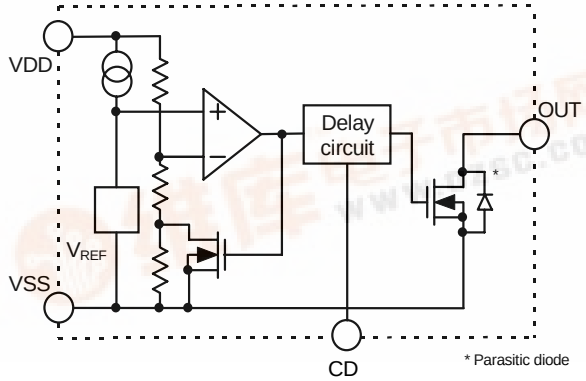


Figure 1

(2) CMOS output

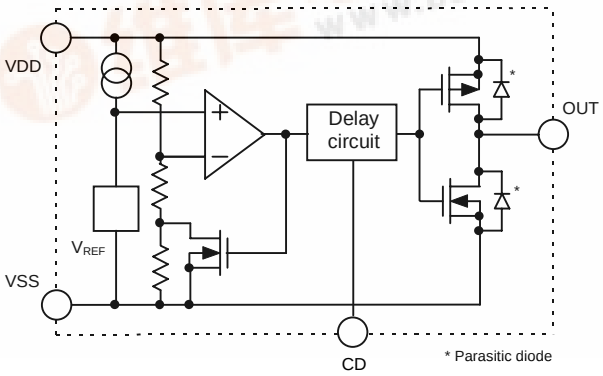


Figure 2

■ Selection Guide

S–809xx C N NB – xxx – T2

- T2: Direction of the IC in taping specifications
- xxx: Product code
- NB: Package code
  - NB: SC-82AB BB: 4-pin SNB(B)
  - MP: SOT-23-5
- N: Output form
  - N: Open-drain (active low output)
  - L: CMOS (active low output)
- xx: Detection voltage (×10)

Table 1.1

Detection voltage range (V)	Hysteresis width typ.	Open-Drain (Low)		
		SC-82AB	SOT-23-5	4-pin SNB(B)
1.3 V ± 2.0%	0.065 V	S-80913CNNB-G8H-T2	S-80913CNMC-G8H-T2	S-80913CNBB-G8H-TF
1.4 V ± 2.0%	0.070 V	S-80914CNNB-G8J-T2	S-80914CNMC-G8J-T2	S-80914CNBB-G8J-TF
1.5 V ± 2.0%	0.075 V	S-80915CNNB-G8K-T2	S-80915CNMC-G8K-T2	S-80915CNBB-G8K-TF
1.6 V ± 2.0%	0.080 V	S-80916CNNB-G8L-T2	S-80916CNMC-G8L-T2	S-80916CNBB-G8L-TF
1.7 V ± 2.0%	0.085 V	S-80917CNNB-G8M-T2	S-80917CNMC-G8M-T2	S-80917CNBB-G8M-TF
1.8 V ± 2.0%	0.090 V	S-80918CNNB-G8N-T2	S-80918CNMC-G8N-T2	S-80918CNBB-G8N-TF
1.9 V ± 2.0%	0.095 V	S-80919CNNB-G8P-T2	S-80919CNMC-G8P-T2	S-80919CNBB-G8P-TF
2.0 V ± 2.0%	0.100 V	S-80920CNNB-G8Q-T2	S-80920CNMC-G8Q-T2	S-80920CNBB-G8Q-TF
2.1 V ± 2.0%	0.105 V	S-80921CNNB-G8R-T2	S-80921CNMC-G8R-T2	S-80921CNBB-G8R-TF
2.2 V ± 2.0%	0.110 V	S-80922CNNB-G8S-T2	S-80922CNMC-G8S-T2	S-80922CNBB-G8S-TF
2.3 V ± 2.0%	0.115 V	S-80923CNNB-G8T-T2	S-80923CNMC-G8T-T2	S-80923CNBB-G8T-TF
2.4 V ± 2.0%	0.120 V	S-80924CNNB-G8U-T2	S-80924CNMC-G8U-T2	S-80924CNBB-G8U-TF
2.5 V ± 2.0%	0.125 V	S-80925CNNB-G8V-T2	S-80925CNMC-G8V-T2	S-80925CNBB-G8V-TF
2.6 V ± 2.0%	0.130 V	S-80926CNNB-G8W-T2	S-80926CNMC-G8W-T2	S-80926CNBB-G8W-TF
2.7 V ± 2.0%	0.135 V	S-80927CNNB-G8X-T2	S-80927CNMC-G8X-T2	S-80927CNBB-G8X-TF
2.8 V ± 2.0%	0.140 V	S-80928CNNB-G8Y-T2	S-80928CNMC-G8Y-T2	S-80928CNBB-G8Y-TF
2.9 V ± 2.0%	0.145 V	S-80929CNNB-G8Z-T2	S-80929CNMC-G8Z-T2	S-80929CNBB-G8Z-TF
3.0 V ± 2.0%	0.150 V	S-80930CNNB-G80-T2	S-80930CNMC-G80-T2	S-80930CNBB-G80-TF
3.1 V ± 2.0%	0.155 V	S-80931CNNB-G81-T2	S-80931CNMC-G81-T2	S-80931CNBB-G81-TF
3.2 V ± 2.0%	0.160 V	S-80932CNNB-G82-T2	S-80932CNMC-G82-T2	S-80932CNBB-G82-TF
3.3 V ± 2.0%	0.165 V	S-80933CNNB-G83-T2	S-80933CNMC-G83-T2	S-80933CNBB-G83-TF
3.4 V ± 2.0%	0.170 V	S-80934CNNB-G84-T2	S-80934CNMC-G84-T2	S-80934CNBB-G84-TF
3.5 V ± 2.0%	0.175 V	S-80935CNNB-G85-T2	S-80935CNMC-G85-T2	S-80935CNBB-G85-TF
3.6 V ± 2.0%	0.180 V	S-80936CNNB-G86-T2	S-80936CNMC-G86-T2	S-80936CNBB-G86-TF
3.7 V ± 2.0%	0.185 V	S-80937CNNB-G87-T2	S-80937CNMC-G87-T2	S-80937CNBB-G87-TF
3.8 V ± 2.0%	0.190 V	S-80938CNNB-G88-T2	S-80938CNMC-G88-T2	S-80938CNBB-G88-TF
3.9 V ± 2.0%	0.195 V	S-80939CNNB-G89-T2	S-80939CNMC-G89-T2	S-80939CNBB-G89-TF
4.0 V ± 2.0%	0.200 V	S-80940CNNB-G9A-T2	S-80940CNMC-G9A-T2	S-80940CNBB-G9A-TF
4.1 V ± 2.0%	0.205 V	S-80941CNNB-G9B-T2	S-80941CNMC-G9B-T2	S-80941CNBB-G9B-TF
4.2 V ± 2.0%	0.210 V	S-80942CNNB-G9C-T2	S-80942CNMC-G9C-T2	S-80942CNBB-G9C-TF
4.3 V ± 2.0%	0.215 V	S-80943CNNB-G9D-T2	S-80943CNMC-G9D-T2	S-80943CNBB-G9D-TF
4.4 V ± 2.0%	0.220 V	S-80944CNNB-G9E-T2	S-80944CNMC-G9E-T2	S-80944CNBB-G9E-TF
4.5 V ± 2.0%	0.225 V	S-80945CNNB-G9F-T2	S-80945CNMC-G9F-T2	S-80945CNBB-G9F-TF
4.6 V ± 2.0%	0.230 V	S-80946CNNB-G9G-T2	S-80946CNMC-G9G-T2	S-80946CNBB-G9G-TF
4.7 V ± 2.0%	0.235 V	S-80947CNNB-G9H-T2	S-80947CNMC-G9H-T2	S-80947CNBB-G9H-TF
4.8 V ± 2.0%	0.240 V	S-80948CNNB-G9J-T2	S-80948CNMC-G9J-T2	S-80948CNBB-G9J-TF
4.9 V ± 2.0%	0.245 V	S-80949CNNB-G9K-T2	S-80949CNMC-G9K-T2	S-80949CNBB-G9K-TF
5.0 V ± 2.0%	0.250 V	S-80950CNNB-G9L-T2	S-80950CNMC-G9L-T2	S-80950CNBB-G9L-TF
5.1 V ± 2.0%	0.255 V	S-80951CNNB-G9M-T2	S-80951CNMC-G9M-T2	S-80951CNBB-G9M-TF
5.2 V ± 2.0%	0.260 V	S-80952CNNB-G9N-T2	S-80952CNMC-G9N-T2	S-80952CNBB-G9N-TF
5.3 V ± 2.0%	0.265 V	S-80953CNNB-G9P-T2	S-80953CNMC-G9P-T2	S-80953CNBB-G9P-TF
5.4 V ± 2.0%	0.270 V	S-80954CNNB-G9Q-T2	S-80954CNMC-G9Q-T2	S-80954CNBB-G9Q-TF
5.5 V ± 2.0%	0.275 V	S-80955CNNB-G9R-T2	S-80955CNMC-G9R-T2	S-80955CNBB-G9R-TF
5.6 V ± 2.0%	0.280 V	S-80956CNNB-G9S-T2	S-80956CNMC-G9S-T2	S-80956CNBB-G9S-TF
5.7V ± 2.0%	0.285 V	S-80957CNNB-G9T-T2	S-80957CNMC-G9T-T2	S-80957CNBB-G9T-TF
5.8 V ± 2.0%	0.290 V	S-80958CNNB-G9U-T2	S-80958CNMC-G9U-T2	S-80958CNBB-G9U-TF
5.9 V ± 2.0%	0.295 V	S-80959CNNB-G9V-T2	S-80959CNMC-G9V-T2	S-80959CNBB-G9V-TF
6.0 V ± 2.0%	0.300 V	S-80960CNNB-G9W-T2	S-80960CNMC-G9W-T2	S-80960CNBB-G9W-TF

Table 1.2

Detection voltage range (V)	Hysteresis width typ.	CMOS output (Low)		
		SC-82AB	SOT-23-5	4-pin SNB(B)
1.3 V ± 2.0%	0.065 V	S-80913CLNB-G6H-T2	S-80913CLMC-G6H-T2	S-80913CLBB-G6H-TF
1.4 V ± 2.0%	0.070 V	S-80914CLNB-G6J-T2	S-80914CLMC-G6J-T2	S-80914CLBB-G6J-TF
1.5 V ± 2.0%	0.075 V	S-80915CLNB-G6K-T2	S-80915CLMC-G6K-T2	S-80915CLBB-G6K-TF
1.6 V ± 2.0%	0.080 V	S-80916CLNB-G6L-T2	S-80916CLMC-G6L-T2	S-80916CLBB-G6L-TF
1.7 V ± 2.0%	0.085 V	S-80917CLNB-G6M-T2	S-80917CLMC-G6M-T2	S-80917CLBB-G6M-TF
1.8 V ± 2.0%	0.090 V	S-80918CLNB-G6N-T2	S-80918CLMC-G6N-T2	S-80918CLBB-G6N-TF
1.9 V ± 2.0%	0.095 V	S-80919CLNB-G6P-T2	S-80919CLMC-G6P-T2	S-80919CLBB-G6P-TF
2.0 V ± 2.0%	0.100 V	S-80920CLNB-G6Q-T2	S-80920CLMC-G6Q-T2	S-80920CLBB-G6Q-TF
2.1 V ± 2.0%	0.105 V	S-80921CLNB-G6R-T2	S-80921CLMC-G6R-T2	S-80921CLBB-G6R-TF
2.2 V ± 2.0%	0.110 V	S-80922CLNB-G6S-T2	S-80922CLMC-G6S-T2	S-80922CLBB-G6S-TF
2.3 V ± 2.0%	0.115 V	S-80923CLNB-G6T-T2	S-80923CLMC-G6T-T2	S-80923CLBB-G6T-TF
2.4 V ± 2.0%	0.120 V	S-80924CLNB-G6U-T2	S-80924CLMC-G6U-T2	S-80924CLBB-G6U-TF
2.5 V ± 2.0%	0.125 V	S-80925CLNB-G6V-T2	S-80925CLMC-G6V-T2	S-80925CLBB-G6V-TF
2.6 V ± 2.0%	0.130 V	S-80926CLNB-G6W-T2	S-80926CLMC-G6W-T2	S-80926CLBB-G6W-TF
2.7 V ± 2.0%	0.135 V	S-80927CLNB-G6X-T2	S-80927CLMC-G6X-T2	S-80927CLBB-G6X-TF
2.8 V ± 2.0%	0.140 V	S-80928CLNB-G6Y-T2	S-80928CLMC-G6Y-T2	S-80928CLBB-G6Y-TF
2.9 V ± 2.0%	0.145 V	S-80929CLNB-G6Z-T2	S-80929CLMC-G6Z-T2	S-80929CLBB-G6Z-TF
3.0 V ± 2.0%	0.150 V	S-80930CLNB-G60-T2	S-80930CLMC-G60-T2	S-80930CLBB-G60-TF
3.1 V ± 2.0%	0.155 V	S-80931CLNB-G61-T2	S-80931CLMC-G61-T2	S-80931CLBB-G61-TF
3.2 V ± 2.0%	0.160 V	S-80932CLNB-G62-T2	S-80932CLMC-G62-T2	S-80932CLBB-G62-TF
3.3 V ± 2.0%	0.165 V	S-80933CLNB-G63-T2	S-80933CLMC-G63-T2	S-80933CLBB-G63-TF
3.4 V ± 2.0%	0.170 V	S-80934CLNB-G64-T2	S-80934CLMC-G64-T2	S-80934CLBB-G64-TF
3.5 V ± 2.0%	0.175 V	S-80935CLNB-G65-T2	S-80935CLMC-G65-T2	S-80935CLBB-G65-TF
3.6 V ± 2.0%	0.180 V	S-80936CLNB-G66-T2	S-80936CLMC-G66-T2	S-80936CLBB-G66-TF
3.7 V ± 2.0%	0.185 V	S-80937CLNB-G67-T2	S-80937CLMC-G67-T2	S-80937CLBB-G67-TF
3.8 V ± 2.0%	0.190 V	S-80938CLNB-G68-T2	S-80938CLMC-G68-T2	S-80938CLBB-G68-TF
3.9 V ± 2.0%	0.195 V	S-80939CLNB-G69-T2	S-80939CLMC-G69-T2	S-80939CLBB-G69-TF
4.0 V ± 2.0%	0.200 V	S-80940CLNB-G7A-T2	S-80940CLMC-G7A-T2	S-80940CLBB-G7A-TF
4.1 V ± 2.0%	0.205 V	S-80941CLNB-G7B-T2	S-80941CLMC-G7B-T2	S-80941CLBB-G7B-TF
4.2 V ± 2.0%	0.210 V	S-80942CLNB-G7C-T2	S-80942CLMC-G7C-T2	S-80942CLBB-G7C-TF
4.3 V ± 2.0%	0.215 V	S-80943CLNB-G7D-T2	S-80943CLMC-G7D-T2	S-80943CLBB-G7D-TF
4.4 V ± 2.0%	0.220 V	S-80944CLNB-G7E-T2	S-80944CLMC-G7E-T2	S-80944CLBB-G7E-TF
4.5 V ± 2.0%	0.225 V	S-80945CLNB-G7F-T2	S-80945CLMC-G7F-T2	S-80945CLBB-G7F-TF
4.6 V ± 2.0%	0.230 V	S-80946CLNB-G7G-T2	S-80946CLMC-G7G-T2	S-80946CLBB-G7G-TF
4.7 V ± 2.0%	0.235 V	S-80947CLNB-G7H-T2	S-80947CLMC-G7H-T2	S-80947CLBB-G7H-TF
4.8 V ± 2.0%	0.240 V	S-80948CLNB-G7J-T2	S-80948CLMC-G7J-T2	S-80948CLBB-G7J-TF
4.9 V ± 2.0%	0.245 V	S-80949CLNB-G7K-T2	S-80949CLMC-G7K-T2	S-80949CLBB-G7K-TF
5.0 V ± 2.0%	0.250 V	S-80950CLNB-G7L-T2	S-80950CLMC-G7L-T2	S-80950CLBB-G7L-TF
5.1 V ± 2.0%	0.255 V	S-80951CLNB-G7M-T2	S-80951CLMC-G7M-T2	S-80951CLBB-G7M-TF
5.2 V ± 2.0%	0.260 V	S-80952CLNB-G7N-T2	S-80952CLMC-G7N-T2	S-80952CLBB-G7N-TF
5.3 V ± 2.0%	0.265 V	S-80953CLNB-G7P-T2	S-80953CLMC-G7P-T2	S-80953CLBB-G7P-TF
5.4 V ± 2.0%	0.270 V	S-80954CLNB-G7Q-T2	S-80954CLMC-G7Q-T2	S-80954CLBB-G7Q-TF
5.5 V ± 2.0%	0.275 V	S-80955CLNB-G7R-T2	S-80955CLMC-G7R-T2	S-80955CLBB-G7R-TF
5.6 V ± 2.0%	0.280 V	S-80956CLNB-G7S-T2	S-80956CLMC-G7S-T2	S-80956CLBB-G7S-TF
5.7V ± 2.0%	0.285 V	S-80957CLNB-G7T-T2	S-80957CLMC-G7T-T2	S-80957CLBB-G7T-TF
5.8 V ± 2.0%	0.290 V	S-80958CLNB-G7U-T2	S-80958CLMC-G7U-T2	S-80958CLBB-G7U-TF
5.9 V ± 2.0%	0.295 V	S-80959CLNB-G7V-T2	S-80959CLMC-G7V-T2	S-80959CLBB-G7V-TF
6.0 V ± 2.0%	0.300 V	S-80960CLNB-G7W-T2	S-80960CLMC-G7W-T2	S-80960CLBB-G7W-TF

■ Pin Assignment

See the detailed drawing of the package at the end of this document.

SC-82AB
Top view

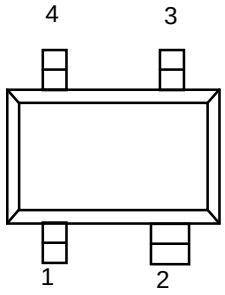


Figure 3

Table 2

No.	Symbol	Description
1	VSS	Ground pin
2	VDD	Voltage input pin
3	CD	Connection pin for delay capacitor
4	OUT	Voltage detection output pin

SOT-23-5
Top view

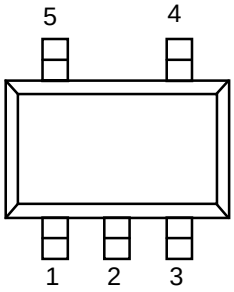


Figure 4

Table 3

No.	Symbol	Description
1	OUT	Voltage detection output pin
2	VDD	Voltage input pin
3	VSS	Ground pin
4	NC [1)]	No connection
5	CD	Connection pin for delay capacitor

1) NC pin is electrically open. Connecting this pin to VDD or VSS is allowed.

4-pin SNB(B)
Top view

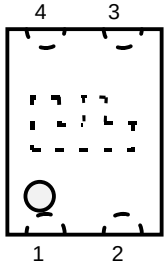


Figure 5

Table 4

No.	Symbol	Description
1	VSS	Ground pin
2	OUT	Voltage detection output pin
3	CD	Connection pin for delay capacitor
4	VDD	Voltage input pin

■ Absolute Maximum Ratings

Table 5

(Unless otherwise specified: Ta=25°C)

Parameter		Symbol		Ratings	Unit
Power supply voltage		V_{DD}–V_{SS}		12	V
CD pin Input voltage		V_{CD}		V_{SS}-0.3 to V_{DD} +0.3	V
Output voltage	Nch open-drain	V_{OUT}		V_{SS}-0.3 to 12	V
	CMOS			V_{SS}-0.3 to V_{DD}+0.3	V
Output current		I_{OUT}		50	mA
Power dissipation		P_D	SC-82AB,SOT-23-5	150	mW
			4-pin SNB(B)	60	mW
Operating temperature		T_{opr}		–40 to +85	°C
Storage temperature		T_{stg}		–40 to +125	°C

Note: Although the IC contains protection circuit against static electricity, excessive static electricity or voltage which exceeds the limit of the protection circuit should not be applied to.

■ Electrical Characteristics (1)

Table 6.1

Open-drain output products (Unless otherwise specified: Ta=25°C)

Parameter	Symbol	Conditions		Min.	Typ.	Max.	Unit	Test circuit
Detection voltage [1]	$-V_{DET}$	—		$-V_{DET}(S)$ ×0.98	$-V_{DET}(S)$	$-V_{DET}(S)$ ×1.02	V	1
Hysteresis width	V_{HYS}	S-80913 to 14		$-V_{DET}$ ×0.03	$-V_{DET}$ ×0.05	$-V_{DET}$ ×0.08	V	1
		S-80915 to 60		$-V_{DET}$ ×0.03	$-V_{DET}$ ×0.05	$-V_{DET}$ ×0.07		
Current consumption	I_{SS}	V_{DD}=2.0V	S-80913 to 14	—	1.0	2.5	μA	2
		V_{DD}=3.5V	S-80915 to 26	—	1.1	2.8		
		V_{DD}=4.5V	S-80927 to 39	—	1.2	3.0		
		V_{DD}=6.0V	S-80940 to 54	—	1.3	3.3		
		V_{DD}=7.5V	S-80955 to 60	—	1.4	3.5		
Operating voltage	V_{DD}	—		0.7	—	10.0	V	1
Output current of output transistor	I_{OUT}	N-channel V_{OUT}=0.5V	V_{DD}=0.95V S-80913 to 14	0.23	0.64	—	mA	3
			V_{DD}=1.2V S-80915 to 60	0.59	1.36	—		
			V_{DD}=2.4V S-80927 to 60	2.88	4.98	—		
Leakage current of output transistor	I_{LEAK}	N-channel V_{DS}=10.0V, V_{DD}=10.0V		—	—	0.1	μA	3
Delay time	td	C_D=4.7nF	V_{DD}=2.0V S-80913 to 14	2.7	3.6	4.5	ms	4
			V_{DD}=3.5V S-80915 to 26	20	27	34		
			V_{DD}=4.5V S-80927 to 39					
			V_{DD}=6.0V S-80940 to 54					
			V_{DD}=7.5V S-80955 to 60					
Temperature coefficient for $-V_{DET}$ [2]	$\frac{\Delta - V_{DET}}{\Delta Ta \bullet -V_{DET}}$	Ta=-40°C to +85°		—	±100	±350	ppm/°C	1

1) $-V_{DET}$; Actual detection voltage
$-V_{DET}(S)$; Specified detection voltage

2) Temperature change in the detection voltage is caluculated by using the following equation.

$$\frac{\Delta - V_{DET}}{\Delta Ta}[mV/°C] = -V_{DET}(S)[V] \times \frac{\Delta - V_{DET}}{\Delta Ta \bullet -V_{DET}}[ppm/°C] \div 1000$$

Temperature change in detection voltage | Detection voltage | Detection voltage temperature coefficient

■ Electrical Characteristics (2)

Table 6.2

CMOS output products (Unless otherwise specified: Ta=25°C)

Parameter	Symbol	Conditions		Min.	Typ.	Max.	Unit	Test circuit
Detection voltage [1]	$-V_{DET}$	—		$-V_{DET}(S)$ ×0.98	$-V_{DET}(S)$	$-V_{DET}(S)$ ×1.02	V	1
Hysteresis width	V_{HYS}	S-80913 to 14		$-V_{DET}$ ×0.03	$-V_{DET}$ ×0.05	$-V_{DET}$ ×0.08	V	1
		S-80915 to 60		$-V_{DET}$ ×0.03	$-V_{DET}$ ×0.05	$-V_{DET}$ ×0.07		
Current consumption	I_{SS}	V_{DD}=2.0V	S-80913 to 14	—	1.0	2.5	µA	2
		V_{DD}=3.5V	S-80915 to 26	—	1.1	2.8		
		V_{DD}=4.5V	S-80927 to 39	—	1.2	3.0		
		V_{DD}=6.0V	S-80940 to 54	—	1.3	3.3		
		V_{DD}=7.5V	S-80955 to 60	—	1.4	3.5		
Operating voltage	V_{DD}	—		0.7	—	10.0	V	1
Output current of output transistor	I_{OUT}	N-channel V_{OUT}=0.5V	V_{DD}=0.95V S-80913 to 14	0.23	0.64	—	mA	3
			V_{DD}=1.2V S-80915 to 60	0.59	1.36	—		
			V_{DD}=2.4V S-80927 to 60	2.88	4.98	—		
		P-channel V_{DD}-V_{OUT} =0.5V	V_{DD}=4.8V S-80913 to 39	1.43	2.39	—	mA	5
			V_{DD}=6.0V S-80940 to 54	1.68	2.78	—		
			V_{DD}=8.4V S-80955 to 60	2.08	3.42	—		
Delay time	td	C_D=4.7nF	V_{DD}=2.0V S-80913 to 14	2.7	3.6	4.5	ms	4
			V_{DD}=3.5V S-80915 to 26	18	24	30		
			V_{DD}=4.5V S-80927 to 39					
			V_{DD}=6.0V S-80940 to 54					
			V_{DD}=7.5V S-80955 to 60					
Temperature characteristic of $-V_{DET}$ [2]	$\frac{\Delta - V_{DET}}{\Delta Ta \bullet -V_{DET}}$	Ta=-40°C to +85°		—	±100	±350	ppm/°C	1

1) $-V_{DET}$; Actual detection voltage
$-V_{DET}(S)$; Specified detection voltage

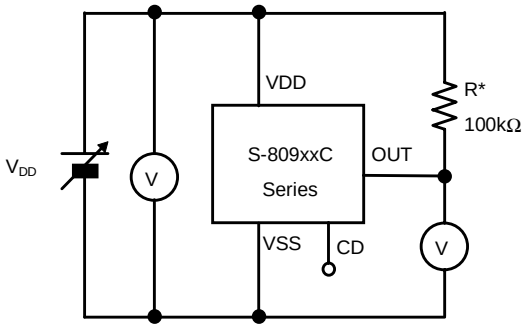
2) Temperature change in the detection voltage is caluculated by using the following equation.

$$\frac{\Delta - V_{DET}}{\Delta Ta}[mV/°C] = -V_{DET}(S)[V] \times \frac{\Delta - V_{DET}}{\Delta Ta \bullet -V_{DET}}[ppm/°C] \div 1000$$

Temperature change in detection voltage | Detection voltage | Detection voltage temperature coefficient

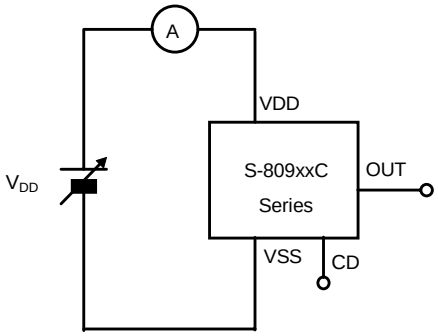
■ Test Circuits

(1)

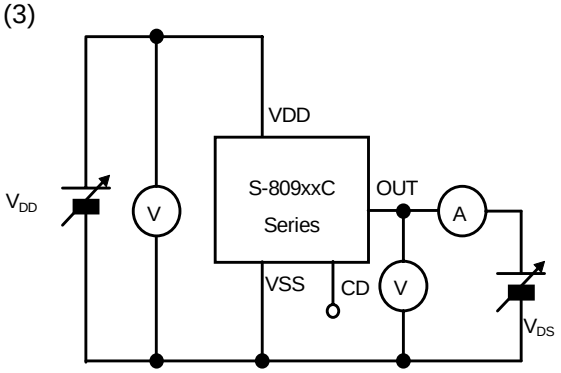


* R is unnecessary for CMOS output products.

(2)



(3)



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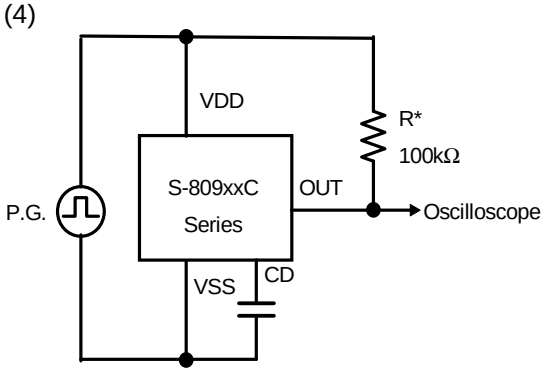


* R is unnecessary for CMOS output products.

(5)

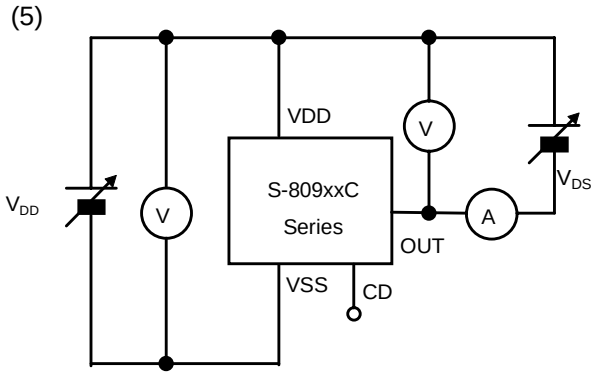


Figure 6

■ Definition of Technical Terms

1. Detection voltage ($-V_{DET}$)

Detection voltage $-V_{DET}$ is a voltage at which the output turns to low. This detection voltage varies slightly among products of the same specification. The variation of detection voltage between the specified minimum [$(-V_{DET})$min.] and maximum [$(-V_{DET})$max.] is called the detection voltage range (See Figure 7).

Example : For the S-80927CN, detection voltage lies in the range of $2.646 \leq (-V_{DET}) \leq 2.754$. This means that some S-80927CNs have 2.646 V for $-V_{DET}$ and some have 2.754 V.

2. Release voltage ($+V_{DET}$)

Release voltage $+V_{DET}$ is a voltage at which the output turns to high. This release voltage varies slightly among products of the same specification. The variation of release voltage between the specified minimum [$(+V_{DET})$min.] and maximum [$(+V_{DET})$max.] is called the release voltage range (See Figure 8). The range is calculated from the actual detection voltage $-V_{DET}$ of a product and is expressed by $-V_{DET}\times1.03 \le +V_{DET} \le -V_{DET}\times1.08$ for S-80913 to S-80914, and by $-V_{DET}\times1.03 \le +V_{DET} \le -V_{DET}\times1.07$ for S-80915 to S-80960.

Example : For the S-80927CN, the release voltage lies in the range of $2.725 \le (+V_{DET}) \le 2.947$. This means that some S-80927CNs have 2.725 V for $+V_{DET}$ and some have 2.947 V.

Remark: Although the detection voltage and release voltage overlap in the range of 2.725 V to 2.754 V, $+V_{DET}$ is always larger than $-V_{DET}$.

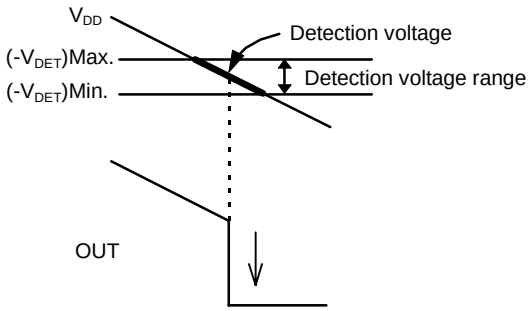


Figure 7

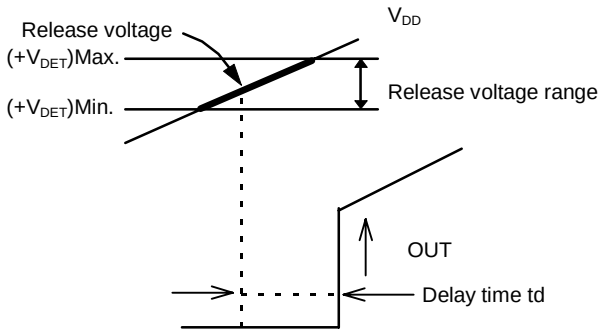


Figure 8

3. Hysteresis width (V_{HYS})

Hysteresis width is the voltage difference between the detection voltage and the release voltage. The existence of the hysteresis width avoids malfunction caused by noise on input signal.

4. Delay time (td)

Delay time is a time internally measured from the instant at which V_{DD} pin exceeds the release voltage ($+V_{DET}$) to the point at which the output of the OUT pin inverts. The delay time changes according to the external capacitor C_D.

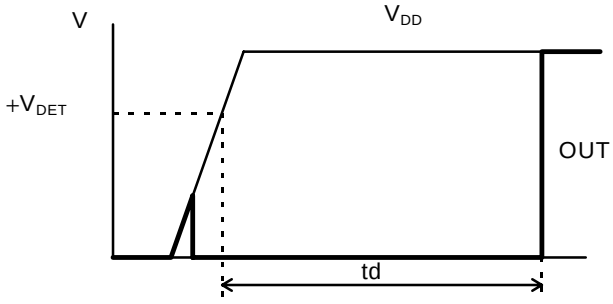


Figure 9

5. Short-circuit current

Short-circuit current refers to the current which flows instantaneously at the time of detection and release of a voltage detector. Short-circuit current is large in CMOS output products, and small in N channel open-drain output products.

6. Oscillation

In applications where a resistor is connected to the voltage detector input as shown in Figure 11, taking a CMOS active low product for example, the short-circuit current, which flows at release when the output goes from low to high, causes a voltage drop equal to [short-circuit current] × [input resistance] across the resistor. When the input voltage falls below the detection voltage -VDET as a result, the output voltage goes to low level. In this state, the short-circuit current stops and its resultant voltage drop the output goes from low to high. Short-circuit current again starts flowing, a voltage

drop appears, and oscillation is finally induced by repeating the process.

Following is an example for bad implementation: input voltage divider for a CMOS output product.

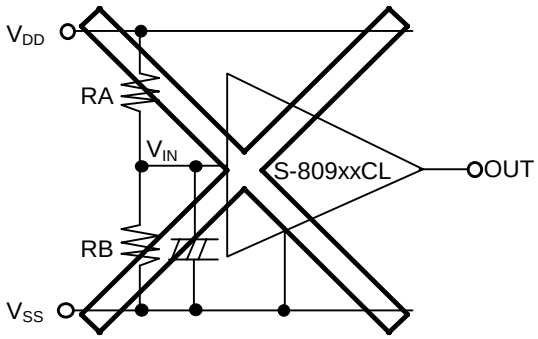
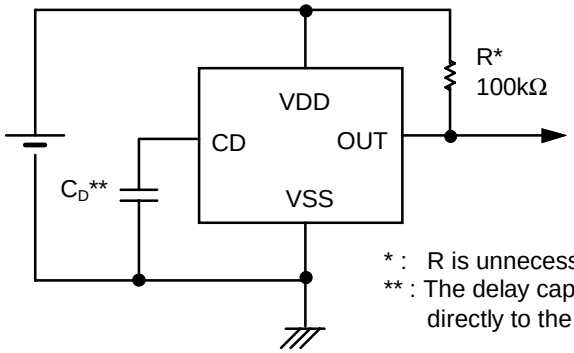


Figure 10 An example for bad implementation

■ Standard Circuit



* : R is unnecessary for CMOS output products.
** : The delay capacitor C_D should be connected directly to the CD pin and to the VSS pin.

Figure 11

■ Operation

1. Basic operation : CMOS active low output

(1) When the power supply voltage V_{DD} is higher than the release voltage $+V_{DET}$, the N-channel transistor is off and the P-channel transistor is on to provide V_{DD} (high) at the output. Since the N-channel transistor N1 in Figure 12 is off, the comparator input voltage is $(RB+RC)/(RA+RB+RC)\times V_{DD}$.

(2) When the V_{DD} goes below $+V_{DET}$, the output provides the V_{DD} level, as long as the V_{DD} remains above the detection voltage $-V_{DET}$. When the V_{DD} falls below $-V_{DET}$ (point A in Figure 13), the N-channel transistor becomes on, the P-channel transistor becomes off, and the V_{SS} level appears at the output. At this time the N-channel transistor N1 in Figure 12 becomes on, the comparator input voltage is changed to $RB/(RA+RB)\times V_{DD}$.

(3) When the V_{DD} falls below the minimum operating voltage, the output becomes undefined, or goes to the V_{DD} when the output is pulled up to the V_{DD}.

(4) The V_{SS} level appears when the V_{DD} rises above the minimum operating voltage. The V_{SS} level still appears even when the V_{DD} surpasses $-V_{DET}$, as long as it does not exceed the release voltage $+V_{DET}$.

(5) When V_{DD} rises above $+V_{DET}$ (point B in Figure 13), the N-channel transistor goes off, the P-channel transistor goes on, and V_{DD} appears at the output after the delay time td counted by the delay circuit.

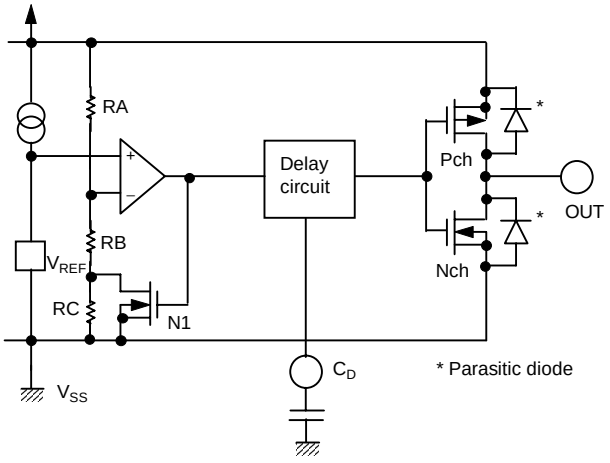


Figure 12

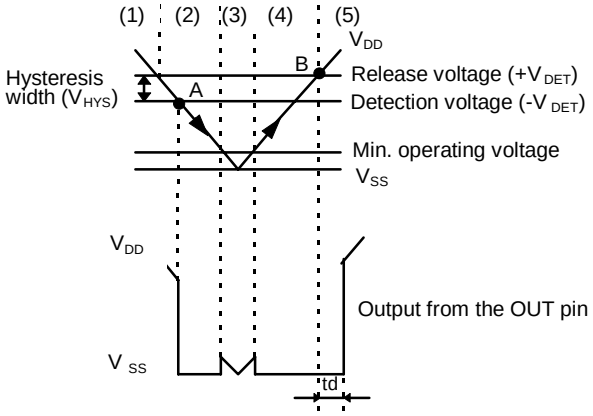


Figure 13

2. Delay circuit

The delay circuit delays the output signal from the time at which the power voltage V_{DD} exceeds the release voltage ($+V_{DET}$) when V_{DD} is turned on. The output signal is not delayed when the V_{DD} goes below the detection voltage ($-V_{DET}$). See Figure 13. The delay time(td) is determined by the time constant of the built-in constant current (approx. 100nA) and the attached external capacitor (C_D), and calculated from the following equation.

td (ms) = Delay coefficient $\times$ C_D (nF)

Delay coefficient: (25°C)

Detection votage $-V_{DET} \leq 1.4V$		Min. 0.57,	Typ. 0.77,	Max. 0.96
Detection voltage $-V_{DET} \geq 1.5V$	Open-drain output :	Min. 4.3,	Typ. 5.7,	Max. 7.2
	CMOS output :	Min. 3.8,	Typ. 5.1,	Max. 6.4

[Cautions]

- When the CD pin is open, a double pulse shown in Figure 14 may appear at release. To avoid the double pulse, attach 20pF or larger capacitor to the C_D pin. Do not apply voltage to the C_D pin.

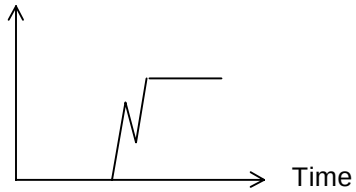


Figure 14

- Print circuit board layout should be made in such a way that no current flows into or flows from the CD pin since the impedance of the CD pin is high, otherwise correct delay time can not be provided.
- There is no limit for the capacitance of the external capacitor CD as long as the leakage current of the capacitor can be ignored against the built-in constant current value. Leakage current causes deviation in delay time. When the leakage current is larger than the built-in constant current, no relaese takes place.

3. Other characteristics

(1) Temperature characteristic of detection voltage

The temperature characteristics of the detection voltage are expressed by the shaded parts in Figure 15

ex) ;S-80927C:

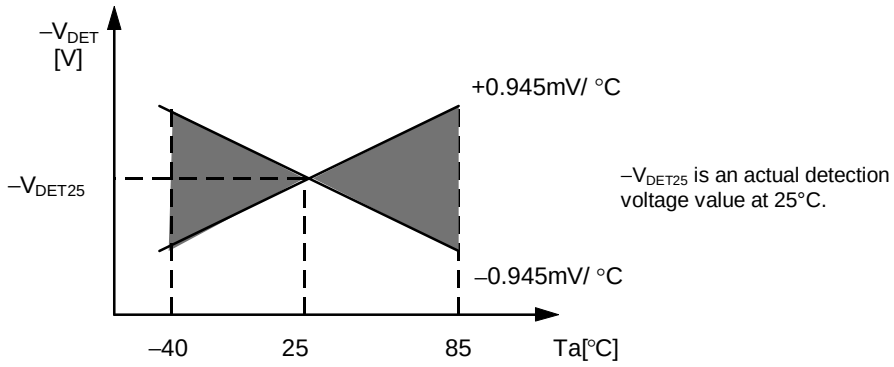


Figure 15

(2) Temperature characteristics of release voltage

The temperature coefficient $\left(\frac{\Delta + V_{DET}}{\Delta Ta}\right)$ for the release voltage is calculated by the temperature coefficient for the detection voltage $\left(\frac{\Delta - V_{DET}}{\Delta Ta}\right)$ as follows:

$$\left(\frac{\Delta + V_{DET}}{\Delta Ta}\right) = \frac{+V_{DET}}{-V_{DET}} \times \frac{\Delta - V_{DET}}{\Delta Ta}$$

The temperature coefficient for the release voltage has hence the same sign as the temperature coefficient for the detection voltage.

(3) Temperature characteristics of hysteresis voltage

The temperature coefficient for the hysteresis voltage $\frac{\Delta + V_{DET}}{\Delta Ta} - \frac{\Delta - V_{DET}}{\Delta Ta}$ is calculated as follows:

$$\frac{\Delta + V_{DET}}{\Delta Ta} - \frac{\Delta - V_{DET}}{\Delta Ta} = \frac{V_{HYS}}{-V_{DET}} \times \frac{\Delta - V_{DET}}{\Delta Ta}$$

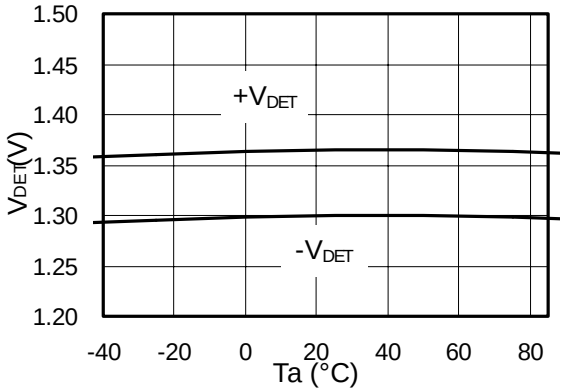
■ Notes

- In CMOS output products of the S-808xxC series, the short-circuit current flows at the detection and the release. If the input impedance is high, oscillation may occur due to the voltage drop by the short-circuit current during releasing.
- When designing for mass production using an application circuit described herein, parts deviation and temperature characteristics should be taken into consideration.
- Seiko Instruments Inc. shall not bear any responsibility for the patents on the circuits described herein.

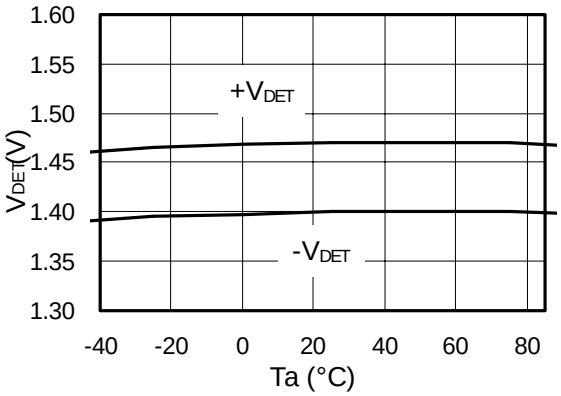
■ Typical Characteristics

(1) Detection voltage (V_{DET}) - Temperature (Ta)

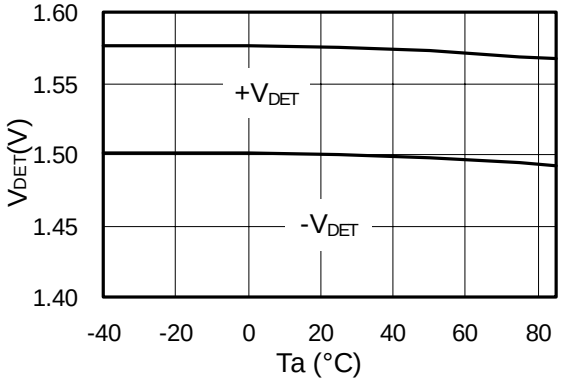
S-80913CN



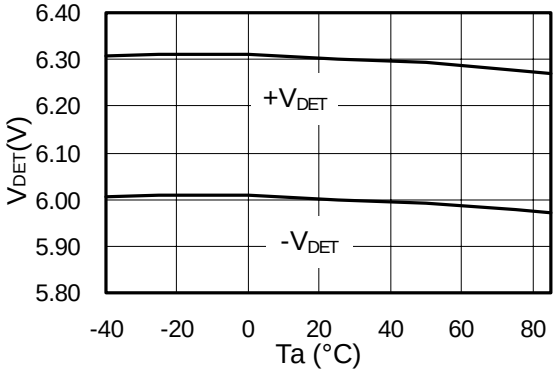
S-80914CN



S-80915CN

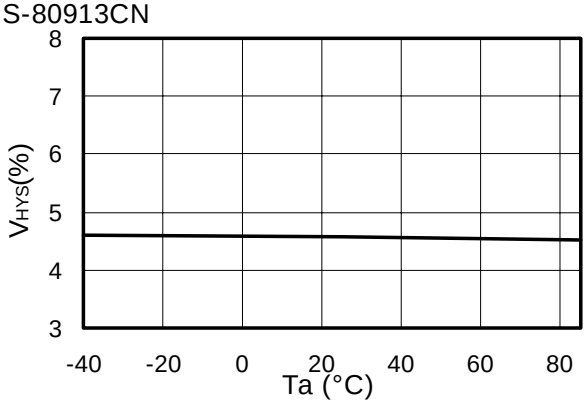


S-80960CN

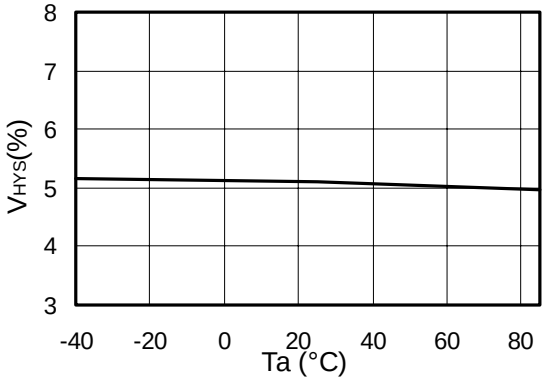


(2) Hysteresis voltage width (V_{HYS}) - Temperature (Ta)

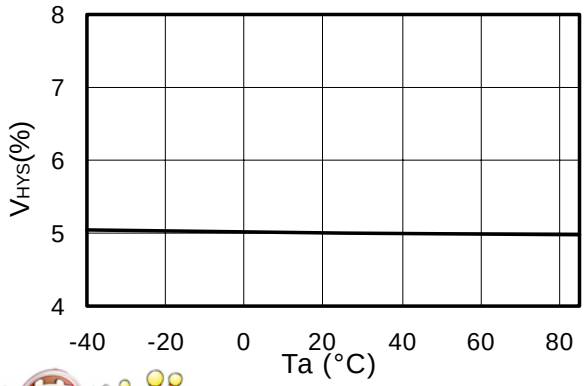
S-80913CN



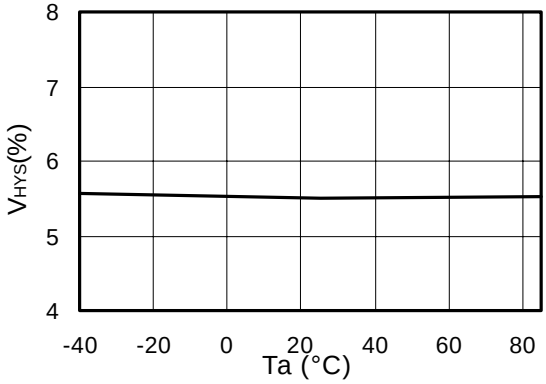
S-80914CN



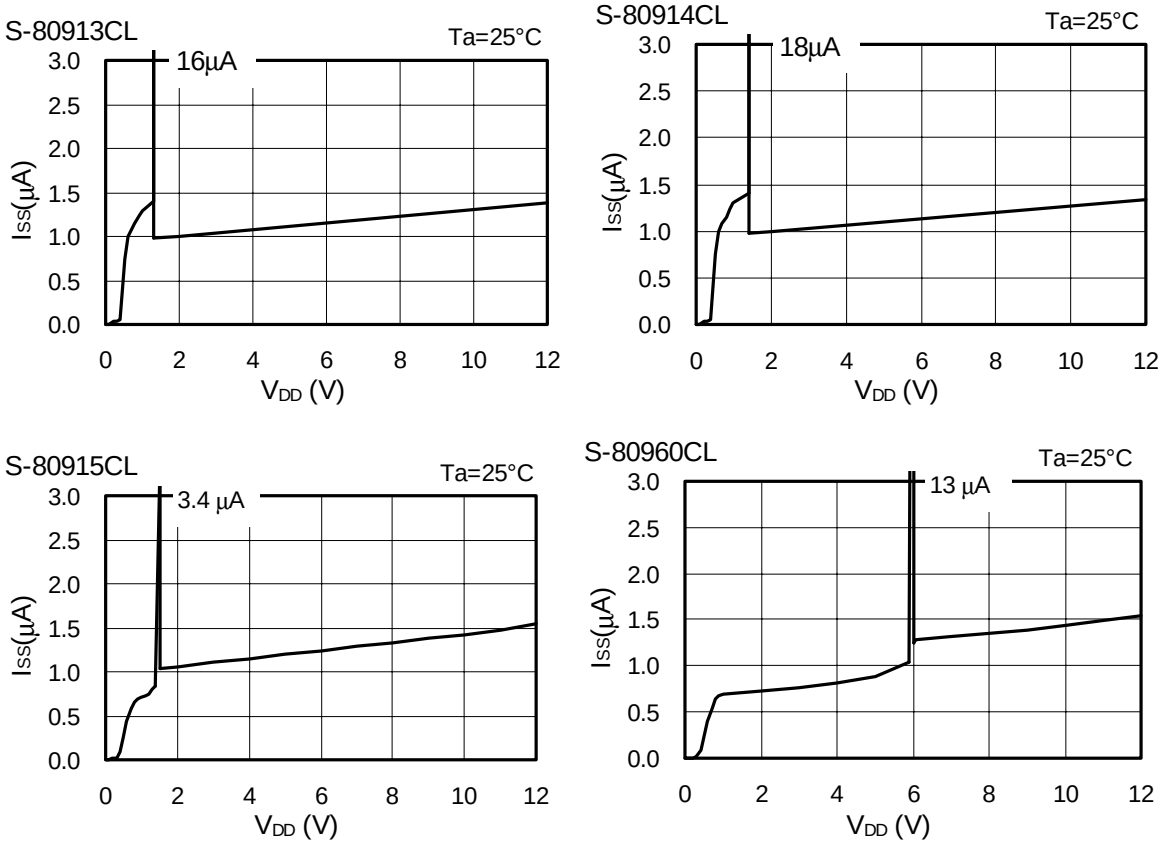
S-80915CN



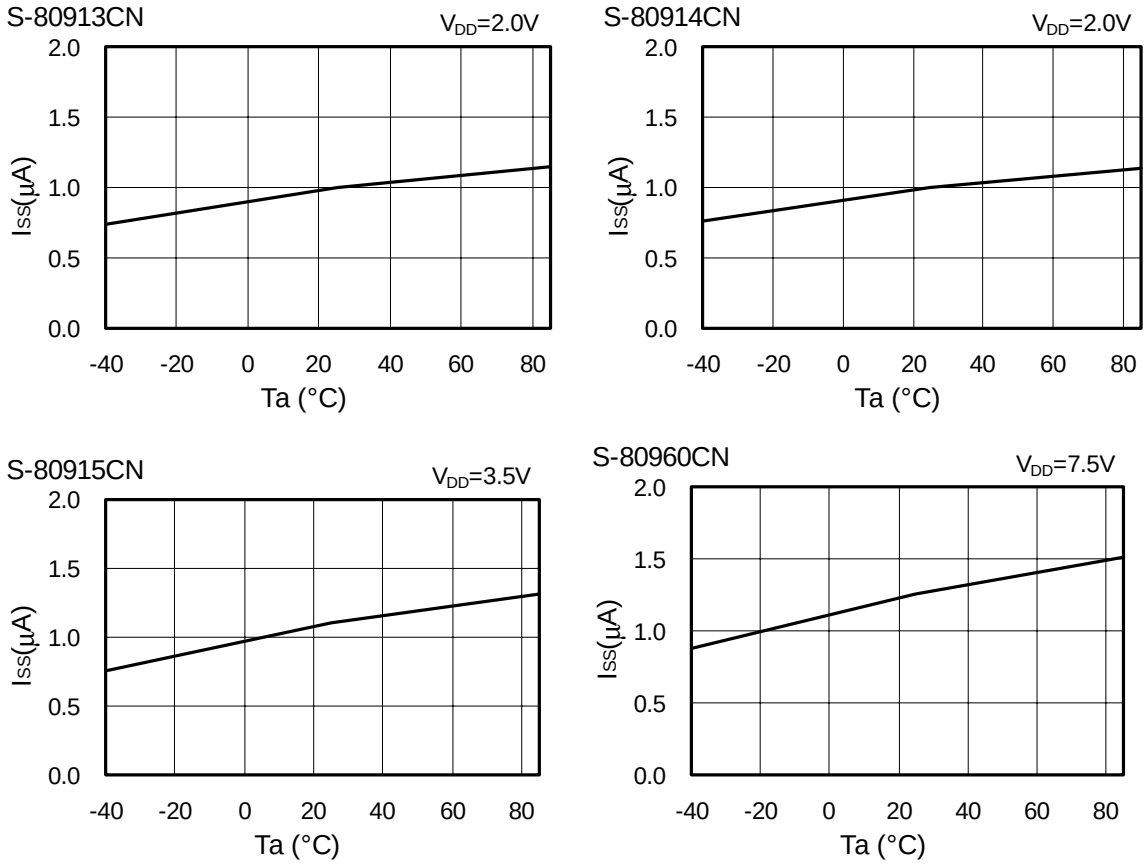
S-80960CN



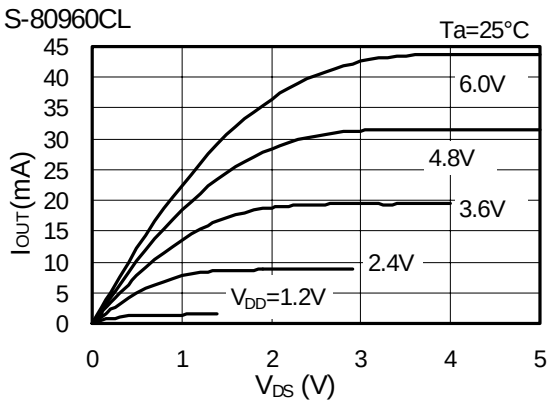
(3) Current consumption (I_{SS}) - Input voltage (V_{DD})



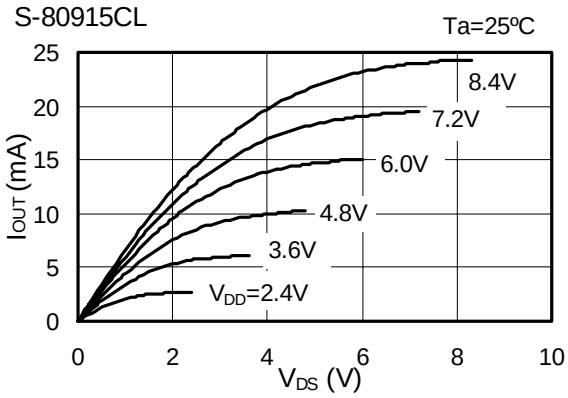
(4) Current consumption (I_{SS}) - Temperature (Ta)



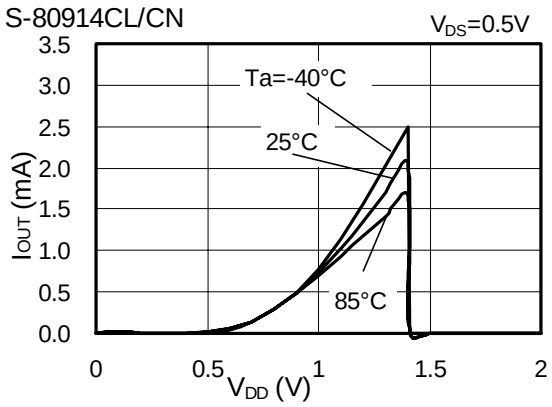
(5) Nch transistor output current (I_{OUT}) - V_{DS}

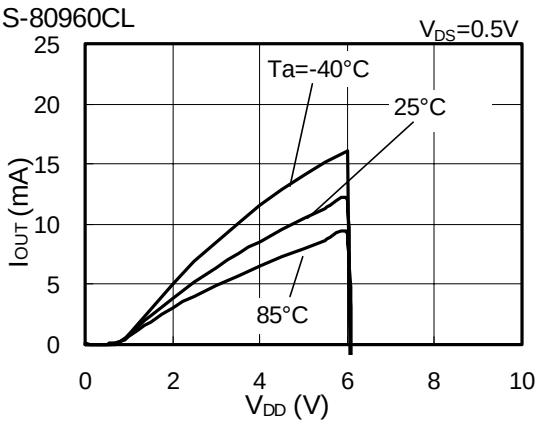


(6) Pch transistor output current (I_{OUT}) - V_{DS}

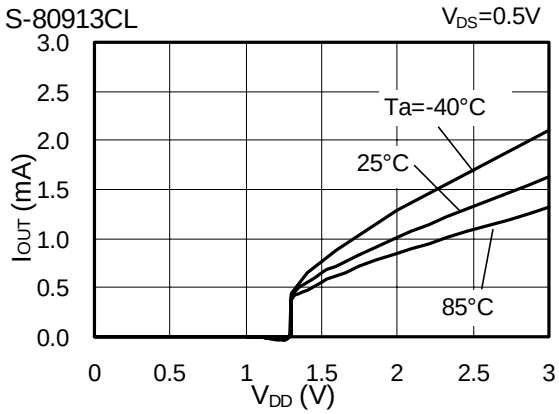


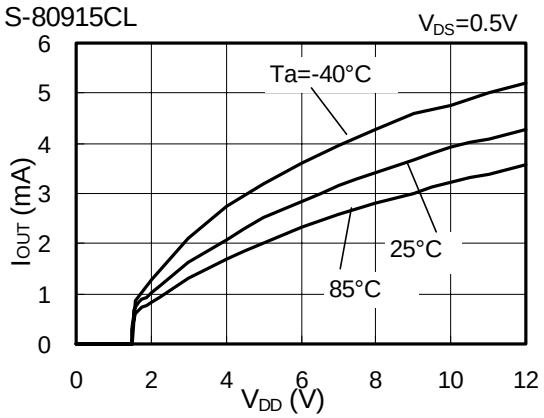
(7) Nch transistor output current (I_{OUT}) - Input voltage(V_{DD})



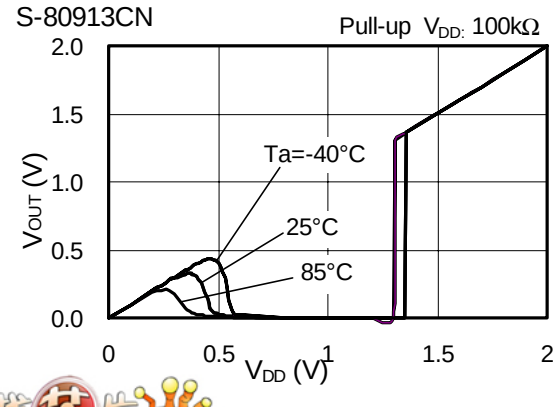


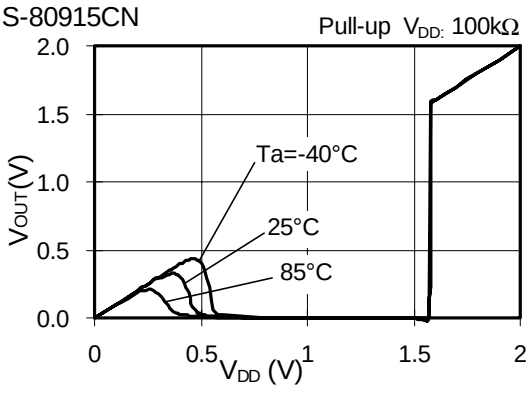
(8) Pch transistor output current(I_{OUT}) - Input voltage(V_{DD})





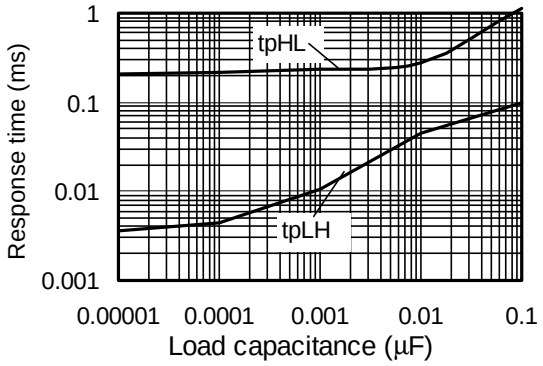
(9) Minimum operating voltage - Input voltage(V_{DD})



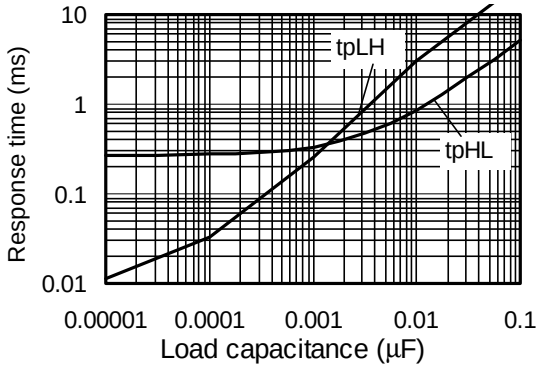


(10) Dynamic response - C_{OUT} (CD pin; open)

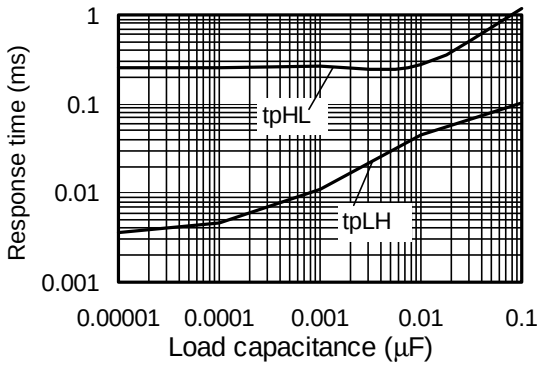
S-80813CL CMOS Ta=25°C



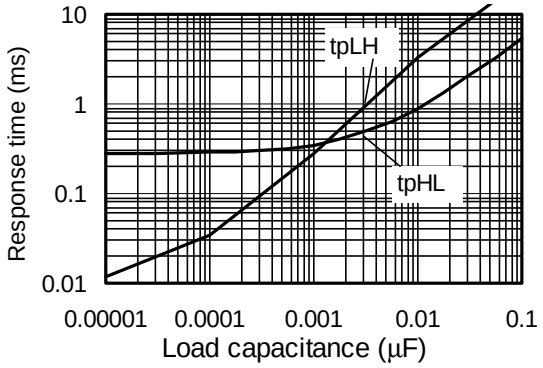
S-80913CN Nch Ta=25°C



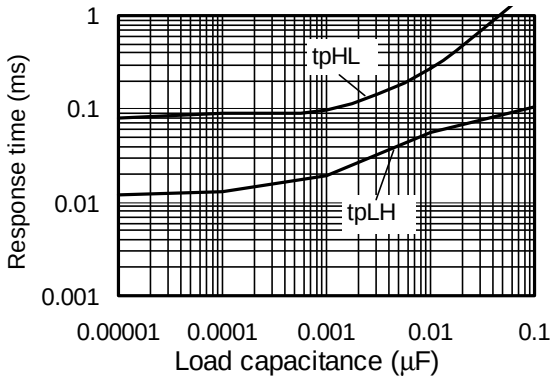
S-80914CL CMOS Ta=25°C



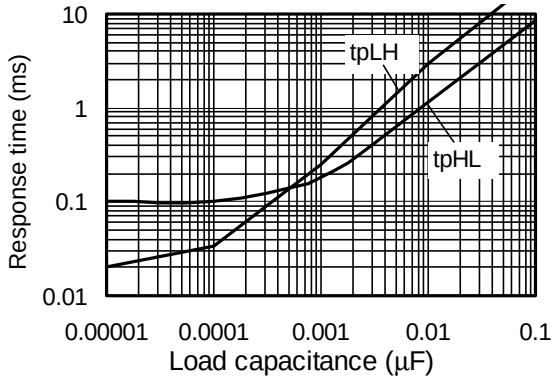
S-80914CN Nch Ta=25°C



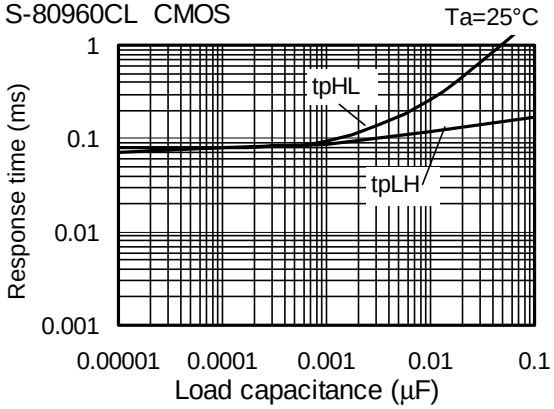
S-80815CL CMOS Ta=25°C



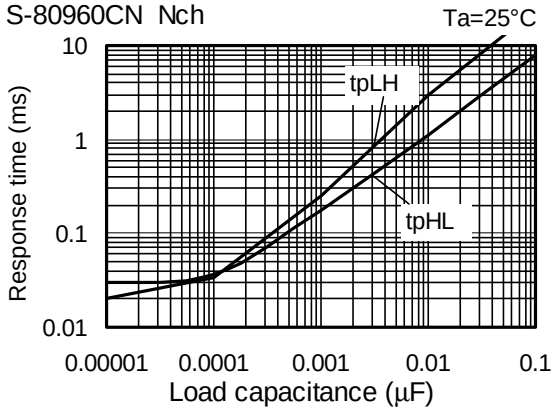
S-80915CN Nch Ta=25°C



S-80960CL CMOS Ta=25°C



S-80960CN Nch Ta=25°C



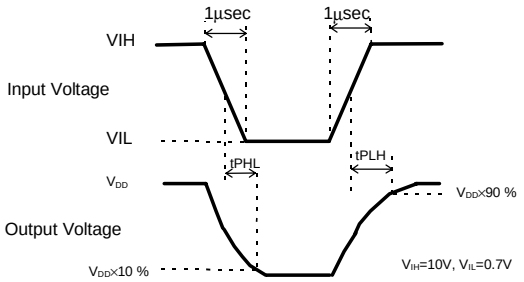
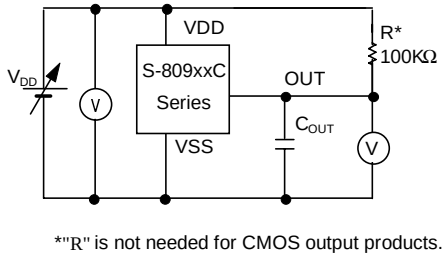


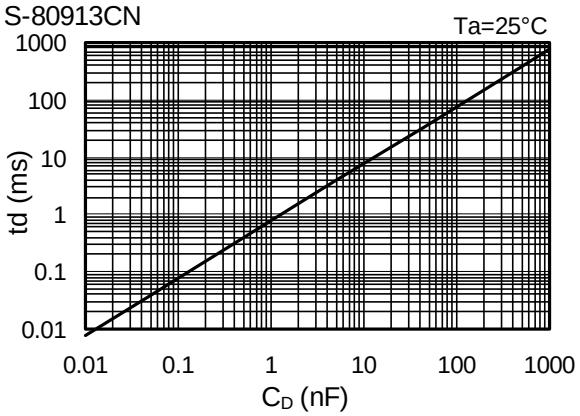
Figure 16 Measurement condition for response time

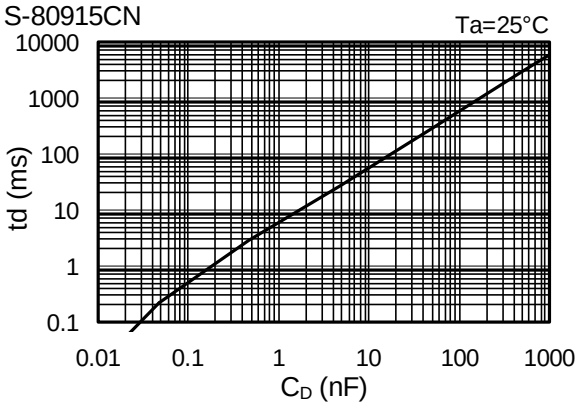


*"R" is not needed for CMOS output products.

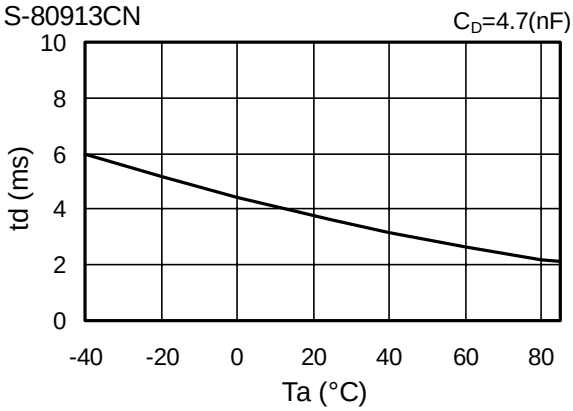
Figure 17 Measurement circuit for response time

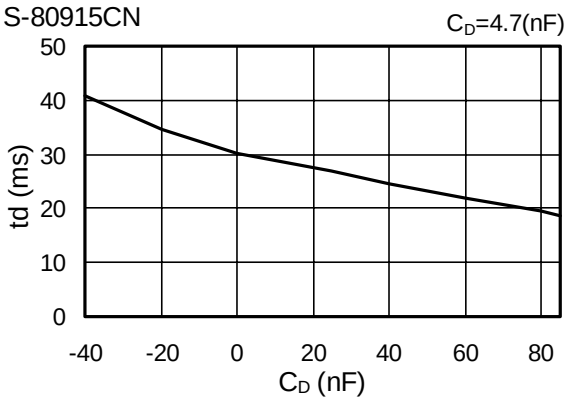
(11) Delay time - CD pin capacitance characteristics(C_D)(No output pin capacitance)





(12) Delay time - Temperature characteristics(Ta)





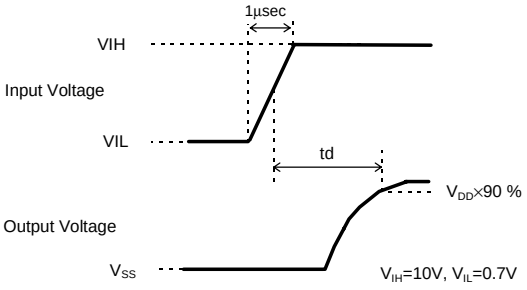
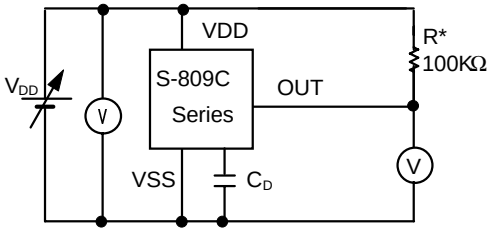


Figure 18 Measuring conditions of delay time



*"R" is not needed for CMOS output products.

Figure 19 Measurement circuit for delay time

■ Application Circuit Examples

1. Microcomputer reset circuits

With the S-809xxC Series which has a low operating voltage, a high-precision detection voltage and hysteresis characteristic, the reset circuits shown in Figures 20 to 21 can be easily constructed.

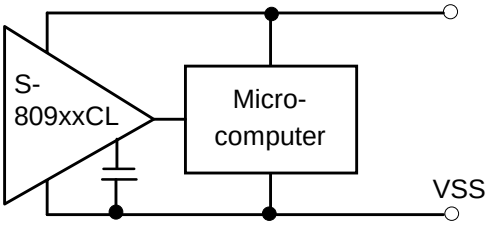
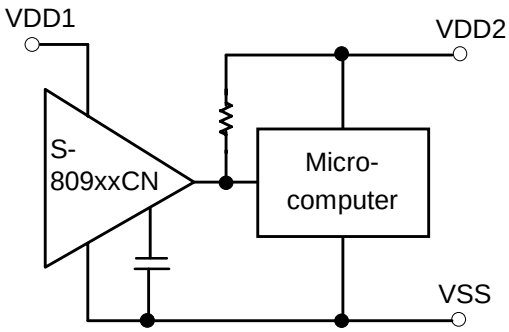


Figure 20

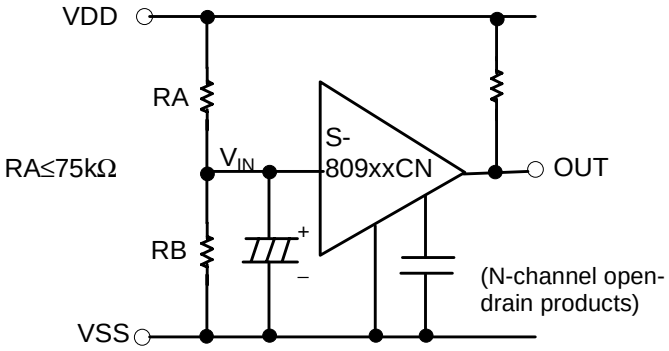


(Nch open-drain output products only)

Figure 21

2. Change of detection voltege

In Nch open-drain output products of the S-809xxC Series, detection voltage can be changed using resistance dividers or diodes as shown in Figures 22 and 23. In Figure 20, hysteresis width is also changed.



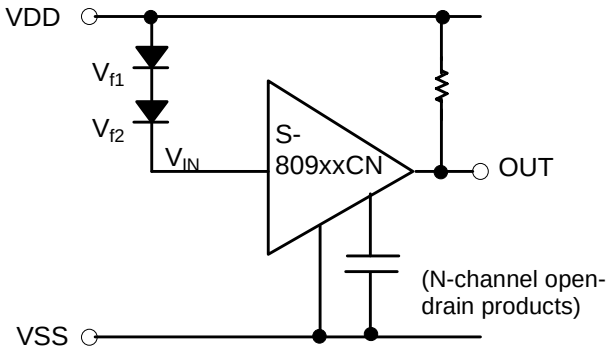
$$\text{Detection voltage} = \frac{RA+RB}{RB} \cdot -V_{DET}$$

$$\text{Hysteresis width} = \frac{RA+RB}{RB} \cdot V_{HYS}$$

Note1: If RA and RB are large, the hysteresis width may also be larger than the value given by the equation above due to short-circuit current (which flows slightly in an N channel open-drain produnt).

Note2: RA should be 75k Ω or less to prevent oscilation.

Figure 22



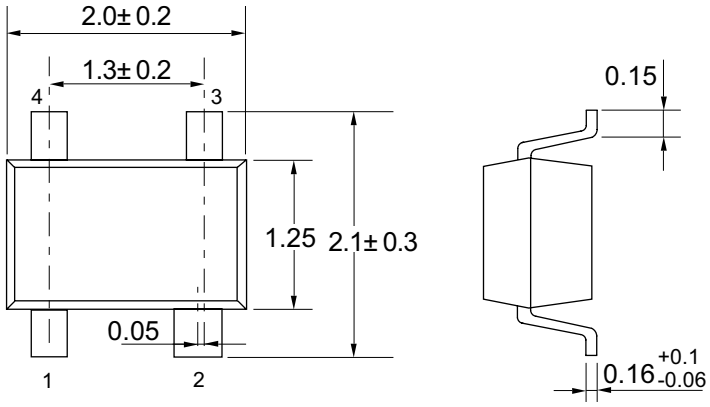
Detection voltage $=V_{f1}+V_{f2}+(-V_{DET})$

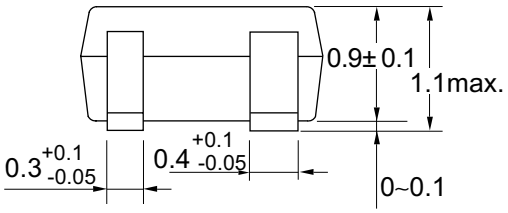
Figure 23

■ SC-82AB

Unit:mm

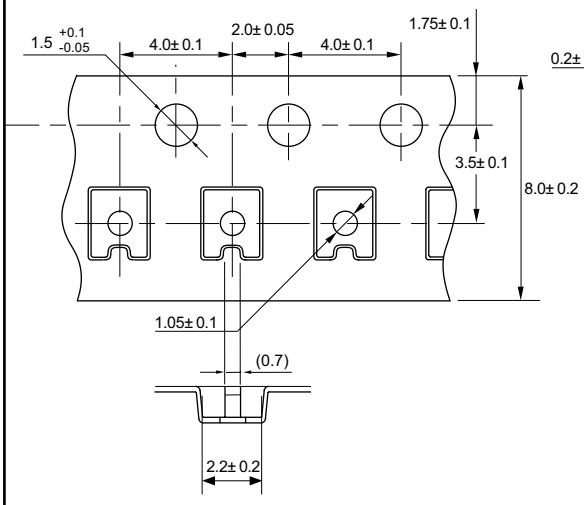
●Dimensions

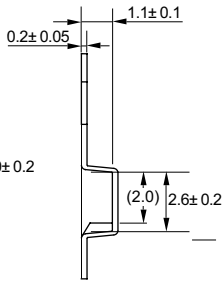


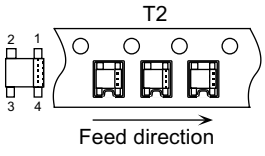


No. NP004-A-P-SD-1.0

●Taping Specifications



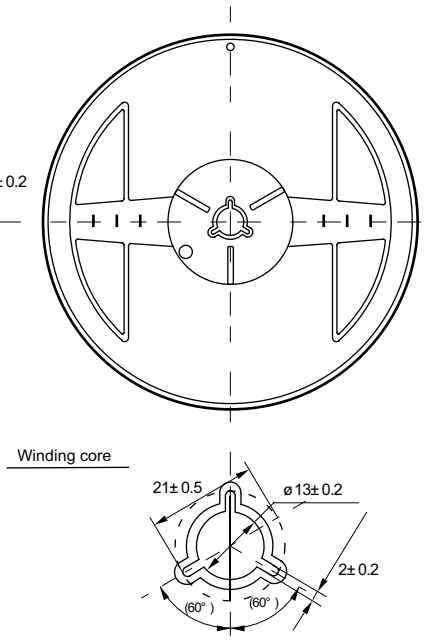


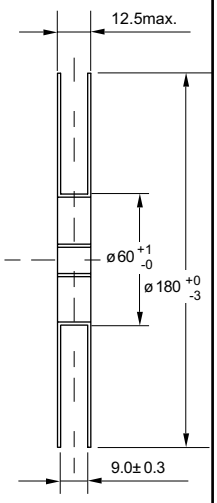


No. NP004-A-C-SD-1.0

●Reel Specifications

3000 pcs./ reel





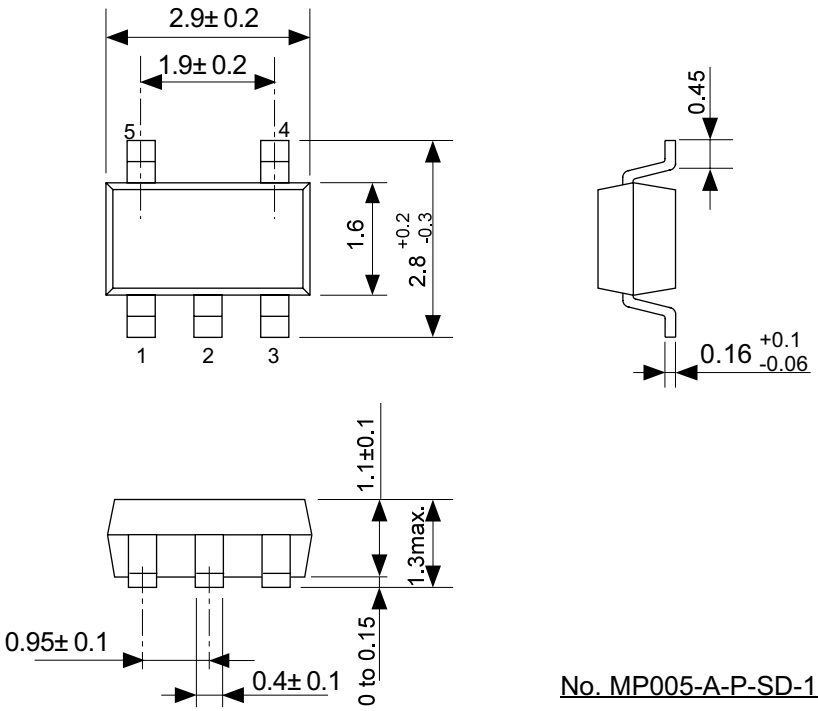
No. NP004-A-R-SD-1.0

■ SOT-23-5

MP005-A 010907

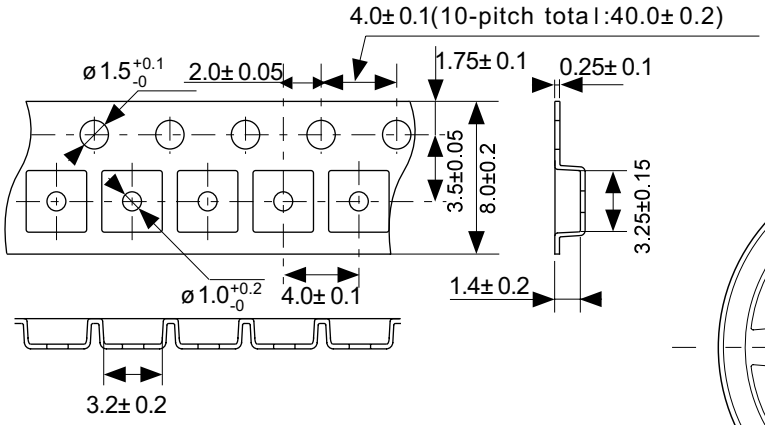
● Dimensions

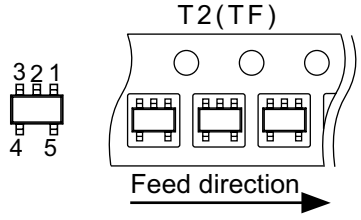
Unit : mm



No. MP005-A-P-SD-1.1

● Tape Specifications

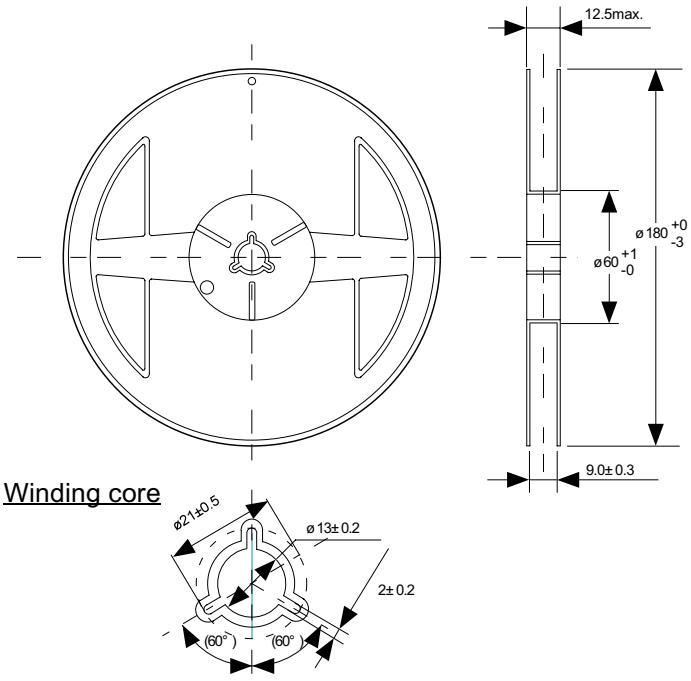




No. : MP005-A-C-SD-2.0

● Reel Specifications

3000 pcs./reel



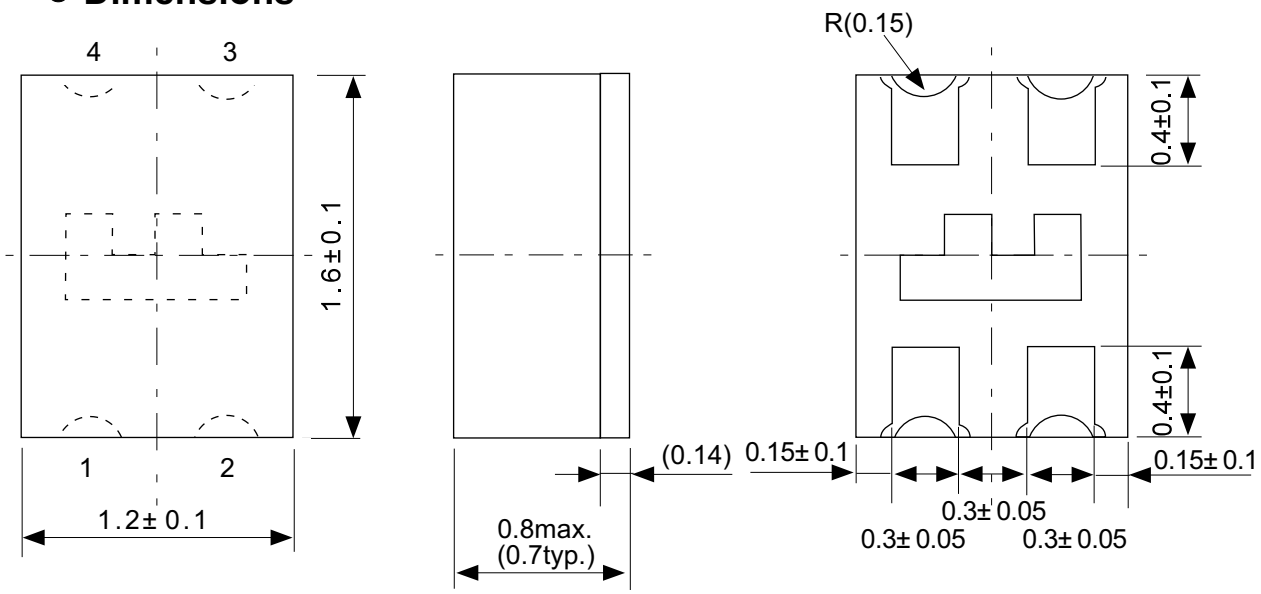
No. MP005-A-R-SD-1. 0

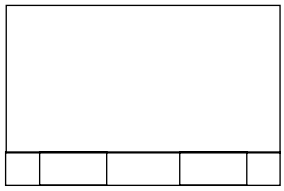
■ 4-Pin SNB(B) [SNB4B(1216)]

BB004-A 010801

Unit : mm

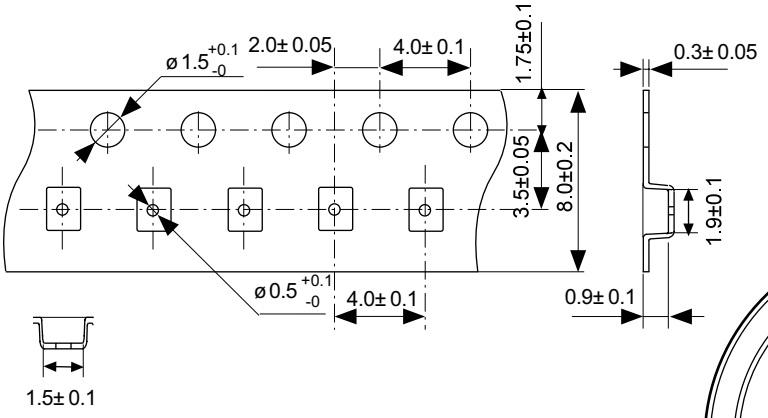
● Dimensions

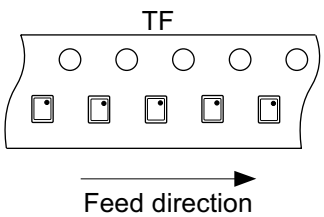




No. : BB004-A-P-SD-1.0

● Tape Specifications

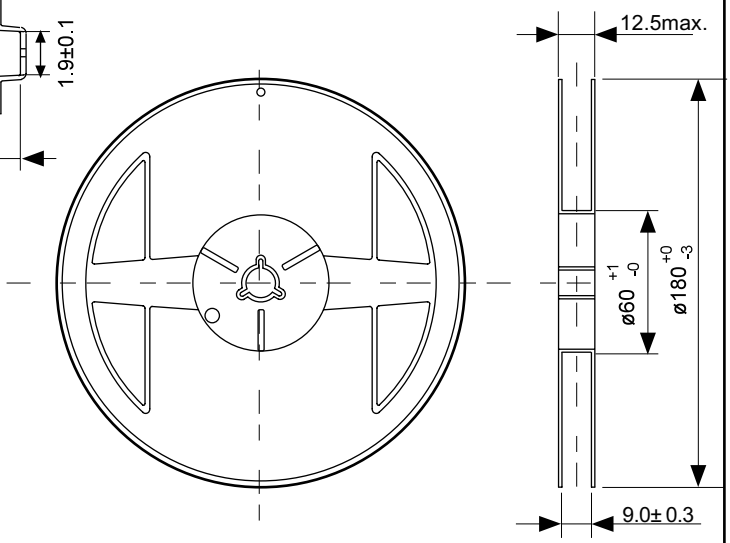




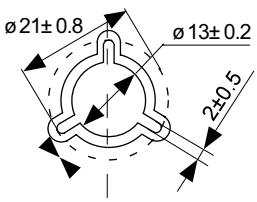
No. : BB004-A-C-SD-1.0

● Reel Specifications

5000 pcs./ reel



Winding core



No. : BB004-A-R-SD-1.0

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