



**MOTOROLA**

# Advance Information 8K x 8 Bit Static Random Access Memory

ELECTRICALLY TESTED PER:  
 MPG6264C

The 6264C is a 65,536-bit static random access memory organized as 8192 words of 8 bits, fabricated using Motorola's second-generation high-performance silicon-gate CMOS technology. Static design eliminates the need for external clocks or timing strobes, while CMOS circuitry reduces power consumption and provides for greater reliability.

The chip enable pins ( $\overline{E1}$  and  $\overline{E2}$ ) are not clocks. Either pin, when asserted false, causes the part to enter a low-power standby mode. The part will remain in standby mode until both pins are asserted true again. The availability of active high and active low chip enable pins provides more system design flexibility than single chip enable devices.

The 6264C is available in a 600 mil, 28-pin ceramic DIL, and a 32-terminal ceramic LCCC package and features the standard JEDEC pinout.

- Single 5.0 V  $\pm$  10% Power Supply
- Output Enable (G) Feature for Increased System Flexibility and to Eliminate Bus Contention Problems
- 8K x 8 Organization
- Fully Static — No Clock or Timing Strokes Necessary
- Fast Access Time — 15, 20, 25, 35, 45, 55, 70 ns
- Low Power Dissipation — 825 mW
- Fully TTL Compatible
- Three State Data Outputs

**6264C**

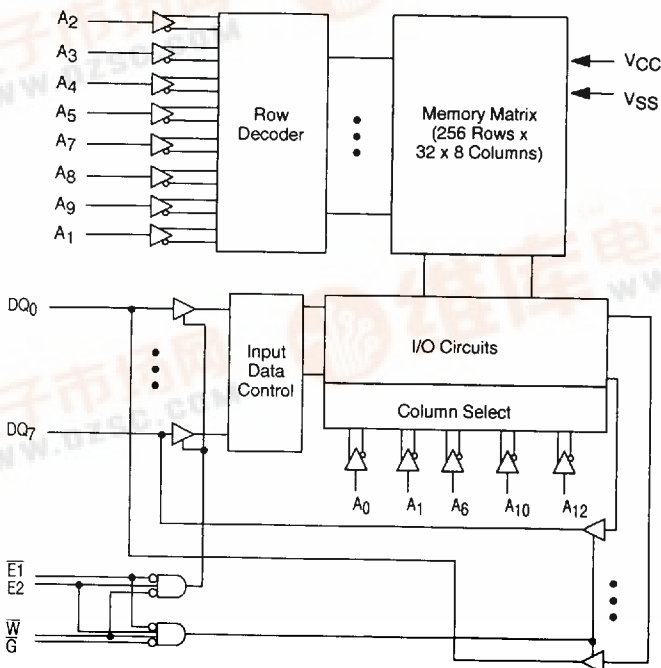
**Commercial Plus  
 and  
 Mil/Aero Applications**

## AVAILABLE AS

- 1) JAN: N/A
  - 2) SMD: Pending
  - 3) 883: 6264C - XX/BXAJC
- X = CASE OUTLINE AS FOLLOWS:  
 PACKAGE: DIL: X  
 LCC: U  
 XX = Speed in ns  
 (15, 20, 25, 35, 45, 55, 70)

The letter "M" appears after the speed on LCC

## BLOCK DIAGRAM



**BURN-IN CONDITIONS:**

$V_{CC} = 5.0 \text{ V(min)}/6.0 \text{ V(max)}$ ,  $R_1 = 39.2 \text{ k}\Omega \pm 20\%$ ,  $C_1 = 0.1 \mu\text{F} \pm 20\%$ ,  
 $V_H = 3.0 \text{ V(min)}/5.0 \text{ V(max)}$ ,  $V_L = -0.5 \text{ V(min)}/0.0 \text{ V(max)}$ ,

|               |                 |                |                |
|---------------|-----------------|----------------|----------------|
| CP1: 100 kHz  | CP6: 3.125 kHz  | CP11: 97.66 Hz | CP16: 3.052 Hz |
| CP2: 50 kHz   | CP7: 1.563 kHz  | CP12: 48.83 Hz | CP17: 1.526 Hz |
| CP3: 25 kHz   | CP8: 0.781 kHz  | CP13: 24.41 Hz | CP18: 0.763 Hz |
| CP4: 12.5 kHz | CP9: 0.391 kHz  | CP14: 12.21 Hz | CP19: 0.382 Hz |
| CP5: 6.25 kHz | CP10: 0.195 kHz | CP15: 6.104 Hz | CP20: 0.191 Hz |

**PIN NAME and FUNCTIONS**

|                                   |                      |
|-----------------------------------|----------------------|
| A <sub>0</sub> – A <sub>12</sub>  | Address Inputs       |
| $\bar{W}$                         | Write Enable         |
| E <sub>1</sub> , E <sub>2</sub>   | Chip Enable          |
| $\bar{G}$                         | Output Enable        |
| DQ <sub>0</sub> – DQ <sub>7</sub> | Data Input/Output    |
| V <sub>CC</sub>                   | + 5.0 V Power Supply |
| V <sub>SS</sub>                   | Ground               |
| N.C.                              | No Connection        |

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltages higher than maximum rated voltages to this high-impedance circuit.

**TRUTH TABLE**

| $\bar{E}_1$ | E <sub>2</sub> | $\bar{G}$ | $\bar{W}$ | Mode            | Supply Current  | I/O Pin          |
|-------------|----------------|-----------|-----------|-----------------|-----------------|------------------|
| H           | X              | X         | X         | Not Selected    | I <sub>SB</sub> | High Z           |
| X           | L              | X         | X         | Not Selected    | I <sub>SB</sub> | High Z           |
| L           | H              | H         | H         | Output Disabled | I <sub>CC</sub> | High Z           |
| L           | H              | L         | H         | Read            | I <sub>CC</sub> | D <sub>OUT</sub> |
| L           | H              | X         | L         | Write           | I <sub>CC</sub> | D <sub>IN</sub>  |

X = Don't Care

**PIN ASSIGNMENTS**

| Function        | DIL | LCC<br>766A-01 | Burn-In<br>(Condition-D)                |
|-----------------|-----|----------------|-----------------------------------------|
| N.C.            | 1   | 2              | N.C.                                    |
| A <sub>12</sub> | 2   | 3              | CP4                                     |
| A <sub>7</sub>  | 3   | 4              | CP5                                     |
| A <sub>8</sub>  | 4   | 5              | CP6                                     |
| A <sub>5</sub>  | 5   | 6              | CP7                                     |
| A <sub>4</sub>  | 6   | 7              | CP8                                     |
| A <sub>3</sub>  | 7   | 8              | CP9                                     |
| A <sub>2</sub>  | 8   | 9              | CP10                                    |
| A <sub>1</sub>  | 9   | 10             | CP11                                    |
| A <sub>0</sub>  | 10  | 11             | CP12                                    |
| DQ <sub>0</sub> | 11  | 13             | R <sub>1</sub> to CP17                  |
| DQ <sub>1</sub> | 12  | 14             | R <sub>1</sub> to CP17                  |
| DQ <sub>2</sub> | 13  | 15             | R <sub>1</sub> to CP17                  |
| V <sub>SS</sub> | 14  | 16             | GND                                     |
| DQ <sub>3</sub> | 15  | 18             | R <sub>1</sub> to CP17                  |
| DQ <sub>4</sub> | 16  | 19             | R <sub>1</sub> to CP17                  |
| DQ <sub>5</sub> | 17  | 20             | R <sub>1</sub> to CP17                  |
| DQ <sub>6</sub> | 18  | 21             | R <sub>1</sub> to CP17                  |
| DQ <sub>7</sub> | 19  | 22             | R <sub>1</sub> to CP17                  |
| $\bar{E}_1$     | 20  | 23             | CP2                                     |
| A <sub>10</sub> | 21  | 24             | CP13                                    |
| $\bar{G}$       | 22  | 25             | CP1                                     |
| A <sub>11</sub> | 23  | 27             | CP14                                    |
| A <sub>9</sub>  | 24  | 28             | CP15                                    |
| A <sub>6</sub>  | 25  | 29             | CP16                                    |
| E <sub>2</sub>  | 26  | 30             | CP3                                     |
| $\bar{W}$       | 27  | 31             | CP1                                     |
| V <sub>CC</sub> | 28  | 32             | V <sub>CC</sub> , C <sub>1</sub> to GND |

**ABSOLUTE MAXIMUM RATINGS** (See Note)

| Rating                                                                 | Symbol                             | Value                          | Unit |
|------------------------------------------------------------------------|------------------------------------|--------------------------------|------|
| Power Supply Voltage                                                   | V <sub>CC</sub>                    | – 0.5 to + 7.0                 | V    |
| Voltage Relative to V <sub>SS</sub> for Any Pin Except V <sub>CC</sub> | V <sub>IN</sub> , V <sub>OUT</sub> | – 0.5 to V <sub>CC</sub> + 0.5 | V    |
| Output Current (per I/O)                                               | I <sub>OUT</sub>                   | ±20                            | mA   |
| Power Dissipation (T <sub>A</sub> = 25°C)                              | P <sub>D</sub>                     | 1.0                            | W    |
| Temperature Under Bias                                                 | T <sub>bias</sub>                  | – 55 to +125                   | °C   |
| Storage Temperature Range                                              | T <sub>stg</sub>                   | – 65 to +150                   | °C   |
| Operating Temperature Range                                            | T <sub>A</sub>                     | – 55 to +125                   | °C   |

**NOTE:** Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to RECOMMENDED OPERATING CONDITIONS. Exposure to higher than recommended voltages for extended periods of time could affect device reliability.

MOTOROLA SC MEMORY/ASI 65E D

**DC OPERATING CONDITIONS AND CHARACTERISTICS**(V<sub>CC</sub> = 5.0 V ± 10%, T<sub>A</sub> = -55°C to +125°C, Unless Otherwise Noted)**RECOMMENDED OPERATING CONDITIONS**

| Parameter                                | Symbol          | Min    | Max                   | Unit |
|------------------------------------------|-----------------|--------|-----------------------|------|
| Supply Voltage (Operating Voltage Range) | V <sub>CC</sub> | 4.5    | 5.5                   | V    |
| Input High Voltage                       | V <sub>IH</sub> | 2.2    | V <sub>CC</sub> + 0.3 | V    |
| Input Low Voltage                        | V <sub>IL</sub> | -0.3 * | 0.8                   | V    |

\* V<sub>IL</sub> (min) = -0.5 Vdc; V<sub>IL</sub> (min) = -3.0 Vdc (pulse width ≤ 20 ns)**DC CHARACTERISTICS**

| Parameter                                                                                                       | Symbol           | Min | Max | Unit |
|-----------------------------------------------------------------------------------------------------------------|------------------|-----|-----|------|
| Input Leakage Current (All Inputs, V <sub>in</sub> = 0 to V <sub>CC</sub> )                                     | I <sub>IL</sub>  | —   | 2.0 | μA   |
| Output Leakage Current ( $\bar{E}1 = V_{IH}$ , E2 = V <sub>IL</sub> , V <sub>OUT</sub> = 0 to V <sub>CC</sub> ) | I <sub>OZL</sub> | —   | 2.0 | μA   |
| Operating Supply Current Cycle = Min, Duty = 100%                                                               | I <sub>CCA</sub> | —   | 150 | mA   |
| +25, +125°C (15)                                                                                                | I <sub>CCA</sub> | —   | 135 | mA   |
| -55°C (25)                                                                                                      | I <sub>CCA</sub> | —   | 135 | mA   |
| TTL Standby Current ( $\bar{E}1 = V_{IH}$ , or E2 = V <sub>IL</sub> )                                           | I <sub>SB1</sub> | —   | 35  | mA   |
| CMOS Standby Current ( $\bar{E}1 \geq V_{CC} - 2.0$ V, E2 ≥ 0.2 V)                                              | I <sub>SB2</sub> | —   | 20  | mA   |
| Output Low Voltage (I <sub>OL</sub> = 8.0 mA)                                                                   | V <sub>OL</sub>  | —   | 0.4 | V    |
| Output High Voltage (I <sub>OH</sub> = -4.0 mA)                                                                 | V <sub>OH</sub>  | 2.4 | —   | V    |

**CAPACITANCE** (f = 1.0 MHz, T<sub>A</sub> = 25°C, Sampled at initial device qualification and major redesign rather than 100% tested)

| Characteristic                         | Symbol           | Min | Typ | Max | Unit |
|----------------------------------------|------------------|-----|-----|-----|------|
| Input Capacitance All Inputs Except DQ | C <sub>in</sub>  | —   | 5.0 | 10  | pF   |
| I/O Capacitance DQ                     | C <sub>I/O</sub> | —   | 6.0 | 12  | pF   |

**AC OPERATING CONDITIONS AND CHARACTERISTICS**(V<sub>CC</sub> = 5.0 V ± 10%, T<sub>A</sub> = -55°C to +125°C, Unless Otherwise Noted)

|                        |              |
|------------------------|--------------|
| Input Reference Level  | 1.5 V        |
| Input Pulse levels     | 0 to 3.0 V   |
| Input Rise/Falls Time  | 5.0 ns       |
| Output Reference Level | 1.5 V        |
| Output Load            | See Figure 1 |

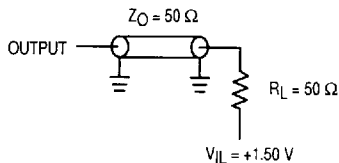


Figure 1A.

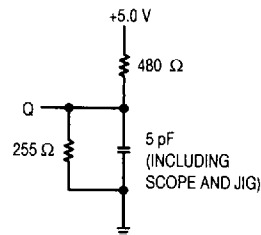
**AC TEST LOADS OR EQUIVALENT**

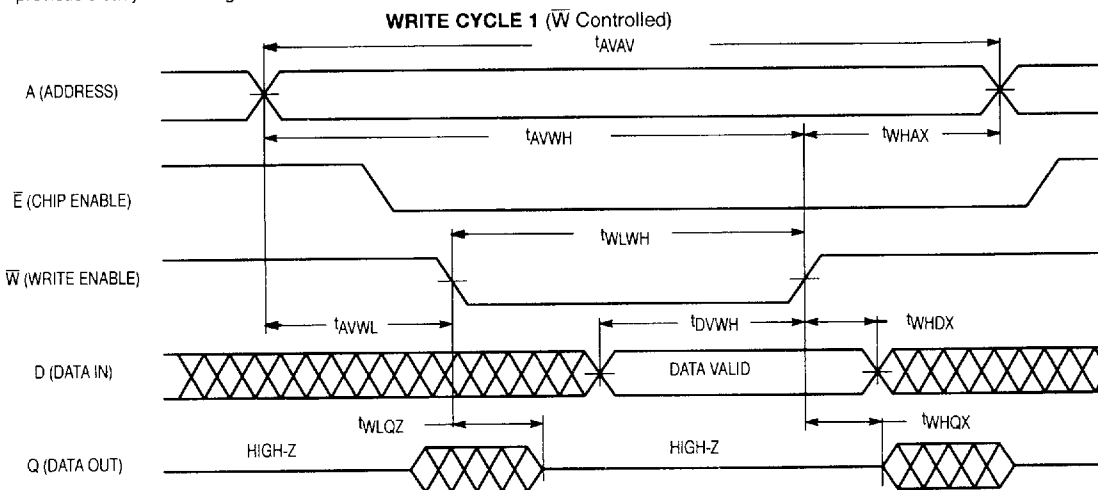
Figure 1B.

| WRITE CYCLE 1 (W Controlled, See Note 1) |                 |                  |          |     |          |     |          |     |          |     |      |       |
|------------------------------------------|-----------------|------------------|----------|-----|----------|-----|----------|-----|----------|-----|------|-------|
| Parameter                                | Symbol Standard | Symbol Alternate | 6264C-15 |     | 6264C-20 |     | 6264C-25 |     | 6264C-35 |     | Unit | Notes |
|                                          |                 |                  | Min      | Max | Min      | Max | Min      | Max | Min      | Max |      |       |
| Write Cycle Time                         | tAVAV           | tWC              | 15       | —   | 20       | —   | 25       | —   | 35       | —   | ns   | —     |
| Address Setup Time                       | tAVWL           | tAS              | 0        | —   | 0        | —   | 0        | —   | 0        | —   | ns   | —     |
| Address Valid to End of Write            | tAVWH           | tAW              | 10       | —   | 15       | —   | 20       | —   | 30       | —   | ns   | —     |
| Write Pulse Width                        | tWLWH           | tWP              | 10       | —   | 15       | —   | 20       | —   | 30       | —   | ns   | 2     |
| Data Valid to End of Write               | tDVWH           | tDW              | 5.0      | —   | 10       | —   | 15       | —   | 25       | —   | ns   | —     |
| Data Hold Time                           | tWHDX           | tDH              | 0        | —   | 0        | —   | 0        | —   | 0        | —   | ns   | 3     |
| Write High to Output Low-Z               | tWHQX           | tWLZ             | 0        | —   | 0        | —   | 0        | —   | 0        | —   | ns   | 4     |

| WRITE CYCLE 1 ( $\overline{W}$ Controlled, See Note 1) |                   |                  |          |     |          |     |          |     |      |       |
|--------------------------------------------------------|-------------------|------------------|----------|-----|----------|-----|----------|-----|------|-------|
| Parameter                                              | Symbol Standard   | Symbol Alternate | 6264C-45 |     | 6264C-55 |     | 6264C-70 |     | Unit | Notes |
|                                                        |                   |                  | Min      | Max | Min      | Max | Min      | Max |      |       |
| Write Cycle Time                                       | t <sub>AVAV</sub> | t <sub>WC</sub>  | 45       | —   | 55       | —   | 70       | —   | ns   | —     |
| Address Setup Time                                     | t <sub>AVWL</sub> | t <sub>AS</sub>  | 0        | —   | 0        | —   | 0        | —   | ns   | —     |
| Address Valid to End of Write                          | t <sub>AVWH</sub> | t <sub>AW</sub>  | 40       | —   | 50       | —   | 65       | —   | ns   | —     |
| Write Pulse Width                                      | t <sub>WLWH</sub> | t <sub>WP</sub>  | 40       | —   | 50       | —   | 65       | —   | ns   | 2     |
| Data Valid to End of Write                             | t <sub>DVWH</sub> | t <sub>DW</sub>  | 35       | —   | 45       | —   | 60       | —   | ns   | —     |
| Data Hold Time                                         | t <sub>WHDX</sub> | t <sub>DH</sub>  | 0        | —   | 0        | —   | 0        | —   | ns   | 3     |
| Write High to Output Low-Z                             | t <sub>WHQX</sub> | t <sub>WLZ</sub> | 0        | —   | 0        | —   | 0        | —   | ns   | 4     |

**NOTES:**

1. A write cycle starts at the latest transition of a low  $\bar{E}1$ , or low  $\bar{W}$  or high  $E2$ . A write cycle ends at the earliest transition of a high  $\bar{E}1$ , high  $\bar{W}$  or low  $E2$ .
2. If  $\bar{W}$  goes low coincident with or prior to  $\bar{E}1$  low or  $E2$  high then the outputs will remain in a high impedance state.
3. During this time the output pins may be in the output state. Signals of opposite phase to the outputs must not be applied at this time.
4. All high-Z AND low-Z parameters are considered in a high or low impedance state when the output has made a 500 mW transition from the previous steady state voltage.

**TIMING LIMITS**

The table of timing values shows either a minimum or a maximum limit for each parameter. Input requirements are specified from the external system point of view. Thus, address setup time is shown as a minimum since the system must supply at least that much time (even though most devices do not require it). On the other hand, responses from the memory are specified from the device point of view. Thus, the access time is shown as a maximum since the device never provides data later than that time.



**WRITE CYCLE 2** (See Note 1)

| Parameter          | Symbol Standard   | Symbol Alternate | 6264C-15 |     | 6264C-20 |     | 6264C-25 |     | 6264C-35 |     | Unit | Notes |
|--------------------|-------------------|------------------|----------|-----|----------|-----|----------|-----|----------|-----|------|-------|
|                    |                   |                  | Min      | Max | Min      | Max | Min      | Max | Min      | Max |      |       |
| Write Cycle Time   | t <sub>AVAV</sub> | t <sub>WC</sub>  | 15       | —   | 20       | —   | 25       | —   | 35       | —   | ns   | —     |
| Address Setup Time | t <sub>AVEL</sub> | t <sub>AS</sub>  | 0        | —   | 0        | —   | 0        | —   | 0        | —   | ns   | —     |

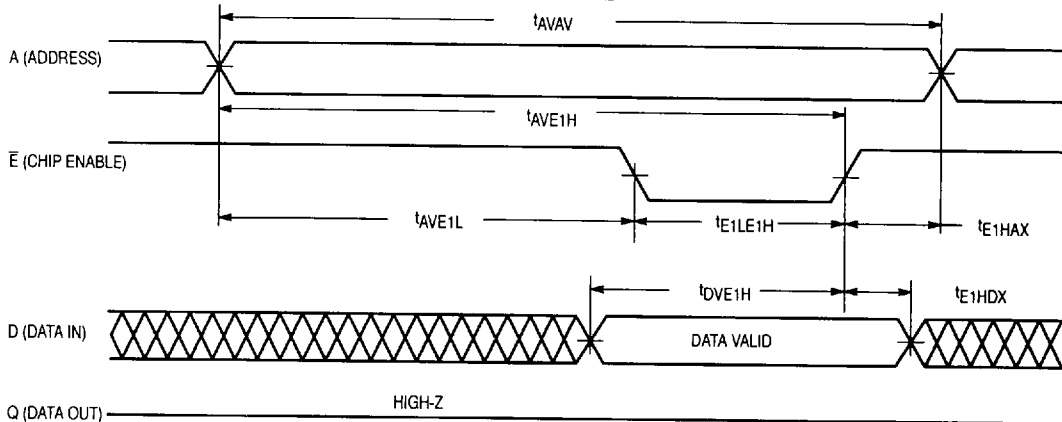
**WRITE CYCLE 2** (See Note 1)

| Parameter          | Symbol Standard   | Symbol Alternate | 6264C-45 |     | 6264C-55 |     | 6264C-70 |     | Unit | Notes |
|--------------------|-------------------|------------------|----------|-----|----------|-----|----------|-----|------|-------|
|                    |                   |                  | Min      | Max | Min      | Max | Min      | Max |      |       |
| Write Cycle Time   | t <sub>AVAV</sub> | t <sub>WC</sub>  | 45       | —   | 55       | —   | 70       | —   | ns   | —     |
| Address Setup Time | t <sub>AVEL</sub> | t <sub>AS</sub>  | 0        | —   | 0        | —   | 0        | —   | ns   | —     |

**NOTES:**

- A write cycle starts at the latest transition of a low  $\overline{E1}$ , or low  $\overline{W}$  or high E2. A write cycle ends at the earliest transition of a high  $\overline{E1}$ , high  $\overline{W}$  or low E2.
- $\overline{E1}$  and E2 timing are identical when E2 signals are inverted.

MOTOROLA SC MEMORY/ASI 65E D

**WRITE CYCLE 2****READ CYCLE** (See Note 1)

| Parameter                      | Symbol Standard                         | Symbol Alternate | 6264C-15 |     | 6264C-20 |     | 6264C-25 |     | 6264C-35 |     | Unit | Notes |
|--------------------------------|-----------------------------------------|------------------|----------|-----|----------|-----|----------|-----|----------|-----|------|-------|
|                                |                                         |                  | Min      | Max | Min      | Max | Min      | Max | Min      | Max |      |       |
| Read Cycle Time                | t <sub>AVAV</sub>                       | t <sub>RC</sub>  | 15       | —   | 20       | —   | 25       | —   | 35       | —   | ns   | —     |
| Address Access Time            | t <sub>AVQV</sub>                       | t <sub>AA</sub>  | —        | 15  | —        | 20  | —        | 25  | —        | 35  | ns   | —     |
| E1 Access Time                 | t <sub>E1LQV</sub>                      | t <sub>AC1</sub> | —        | 15  | —        | 20  | —        | 25  | —        | 35  | ns   | —     |
| E2 Access Time                 | t <sub>E2HQV</sub>                      | t <sub>AC2</sub> | —        | 15  | —        | 20  | —        | 25  | —        | 35  | ns   | —     |
| $\overline{Q}$ Access Time     | t <sub>GLQV</sub>                       | t <sub>OE</sub>  | —        | 12  | —        | 15  | —        | 20  | —        | 25  | ns   | —     |
| Chip Enable to Output Low-Z    | t <sub>E1LQX</sub> , t <sub>E2HQX</sub> | t <sub>CLZ</sub> | 5.0      | —   | 5.0      | —   | 5.0      | —   | 5.0      | —   | ns   | 2     |
| Output Enable to Output Low-Z  | t <sub>GLQX</sub>                       | t <sub>OLZ</sub> | 0        | —   | 0        | —   | 0        | —   | 0        | —   | ns   | 2     |
| Chip Enable to Output High-Z   | t <sub>E1HQZ</sub> , t <sub>E2LQZ</sub> | t <sub>CHZ</sub> | —        | 5.0 | —        | 10  | —        | 15  | —        | 20  | ns   | 2, 3  |
| Output Enable to Output High-Z | t <sub>GHQZ</sub>                       | t <sub>OHZ</sub> | —        | 5.0 | —        | 10  | —        | 15  | —        | 20  | ns   | 2, 3  |

**NOTES:**

- $\overline{W}$  is high at all times for read cycles.
- All high-Z and low-Z parameters are considered in a high or low impedance state when the output has made a 500 mV transition from the previous steady state voltage.
- This parameter is sampled and not 100% tested.



**READ CYCLE** (See Note 1)

| Parameter                      | Symbol Standard        | Symbol Alternate | 6264C-45 |     | 6264C-55 |     | 6264C-70 |     | Unit | Notes |
|--------------------------------|------------------------|------------------|----------|-----|----------|-----|----------|-----|------|-------|
|                                |                        |                  | Min      | Max | Min      | Max | Min      | Max |      |       |
| Read Cycle Time                | $t_{AVAV}$             | $t_{RC}$         | 45       | —   | 55       | —   | 70       | —   | ns   | —     |
| Address Access Time            | $t_{AVQV}$             | $t_{AA}$         | —        | 45  | —        | 55  | —        | 70  | ns   | —     |
| $\overline{E1}$ Access Time    | $t_{E1LQV}$            | $t_{AC1}$        | —        | 45  | —        | 55  | —        | 70  | ns   | —     |
| $E2$ Access Time               | $t_{E2HQV}$            | $t_{AC2}$        | —        | 45  | —        | 55  | —        | 70  | ns   | —     |
| $\overline{G}$ Access Time     | $t_{GLQV}$             | $t_{OE}$         | —        | 30  | —        | 35  | —        | 40  | ns   | —     |
| Chip Enable to Output Low-Z    | $t_{E1LQX}, t_{E2HQX}$ | $t_{CLZ}$        | 5.0      | —   | 5.0      | —   | 5.0      | —   | ns   | 2     |
| Output Enable to Output Low-Z  | $t_{GLQX}$             | $t_{OLZ}$        | 0        | —   | 0        | —   | 0        | —   | ns   | 2     |
| Chip Enable to Output High-Z   | $t_{E1HQZ}, t_{E2LQZ}$ | $t_{CHZ}$        | —        | 25  | —        | 30  | —        | 35  | ns   | 2, 3  |
| Output Enable to Output High-Z | $t_{GHQZ}$             | $t_{OHZ}$        | —        | 25  | —        | 30  | —        | 35  | ns   | 2, 3  |

**NOTES:**

- $\overline{W}$  is high at all times for read cycles.
- All high-Z and low-Z parameters are considered in a high or low impedance state when the output has made a 500 mV transition from the previous steady state voltage.
- This parameter is sampled and not 100% tested.

**READ CYCLE**

MOTOROLA SC (MEMORY/ASI 65E D

