TA7282AP

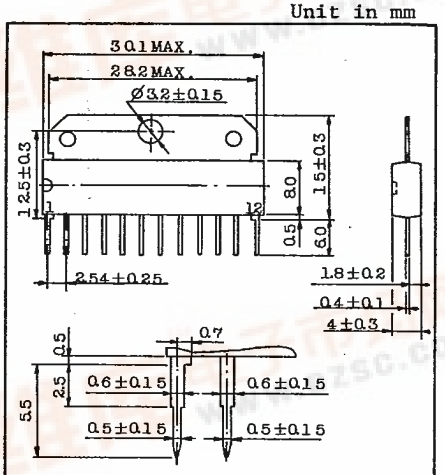
T-74-05-01

LOW FREQUENCY POWER AMPLIFIER

TA7282AP is an audio power IC with built-in two channels developed for portable radio cassette tape recoder with power ON/OFF switch.
Because of the parts reduction and SIP (Single Inline Package), space merit is remarkable.
Thermal shut down protection circuit is built in.

- High Power: P_{OUT}=2.5W/CH (Typ.)
  (V_{CC}=9V, R_L=4Ω, f=1kHz, THD=10%)
  : P_{OUT}=4.6W/CH (Typ.)
  (V_{CC}=12V, R_L=4Ω, f=1kHz, THD=10%)
- Low Popping Noise at Power ON
- Small Quiescent Current
  : I_{CCQ}=19mA (Typ.) (V_{CC}=9V, V_{IN}=0)
- Soft Clip
- Built-in Thermal Shut Down Protection Circuit
- Best for Supply Voltage 9V, 12V
- Operation Supply Voltage Range : V_{CC}=6～15V

Unit in mm



Lead pitch is 2.54 and tolerance is ±0.25 against theoretical center of each lead that is obtained on the basis of No.1 lead.

JEDEC	—
TOSHIBA	S12CP-P

Weight: 3.2g (Typ.)

MAXIMUM RATINGS (Ta=25°C)

CHARACTERISTIC	SYMBOL	RATING	UNIT
Supply Voltage	V_{CC}	16	V
Output Current (Peak/CH)	$I_{O(peak)}$	2.5	A
Power Dissipation	P_D	12.5	W
Operating Temperature	T_{opr}	-20～75	°C
Storage Temperature	T_{stg}	-55～150	°C

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ELECTRICAL CHARACTERISTICS

(Unless otherwise specified, V_{CC}=9V, R_L=4Ω, R_g=600Ω, f=1kHz, Ta=25°C)

CHARACTERISTIC	SYMBOL	TEST CIR-CUIT	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
Quiescent Current	I_{CCQ}	-	V_{in}=0	-	19	45	mA
Output Power	P_{OUT}(1)	-	THD=10%	2.0	2.5	-	W
	P_{OUT}(2)	-	THD=10%, V_{CC}=12V	-	4.6	-	
Total Harmonic Distortion	THD	-	P_{OUT}=1W/CH.	-	0.25	1.0	%
Voltage Gain	G_V(1)	-	R_f=82Ω V_{OUT}=0.775V_{rms}	43	45	47	dB
	G_V(2)	-	R_f=0, V_{OUT}=0.775V_{rms}	-	56	-	
Input Resistance	R_{IN}	-	-	-	30	-	kΩ
Output Noise Voltage	V_{NO}	-	R_g=10kΩ BW=20Hz ~ 20kHz	-	0.3	1.0	mV_{rms}
Ripple Rejection Ratio	R.R.	-	R_g=600Ω f_{ripple}=100Hz	-	54	-	dB
Cross Talk	C.T.	-	R_g=10kΩ, Ampl↔2 V_{OUT}=0dBm, f=1kHz	-	45	-	dB
Input Offset Voltage	V_6,V_7	-	-	-	20	60	mV

TYPICAL DC VOLTAGE OF EACH TERMINAL (V_{CC}=9V, Ta=25°C)

TERMINAL No.	1	2	3	4	5	6	7	8	9	10	11	12
DC Voltage (V)	8.2	4.5	V_{CC}	8.9	0.6	0.01	0.01	0.6	GND	4.5	8.2	V_{CC}

* 3 pin is connected to V_{CC}.

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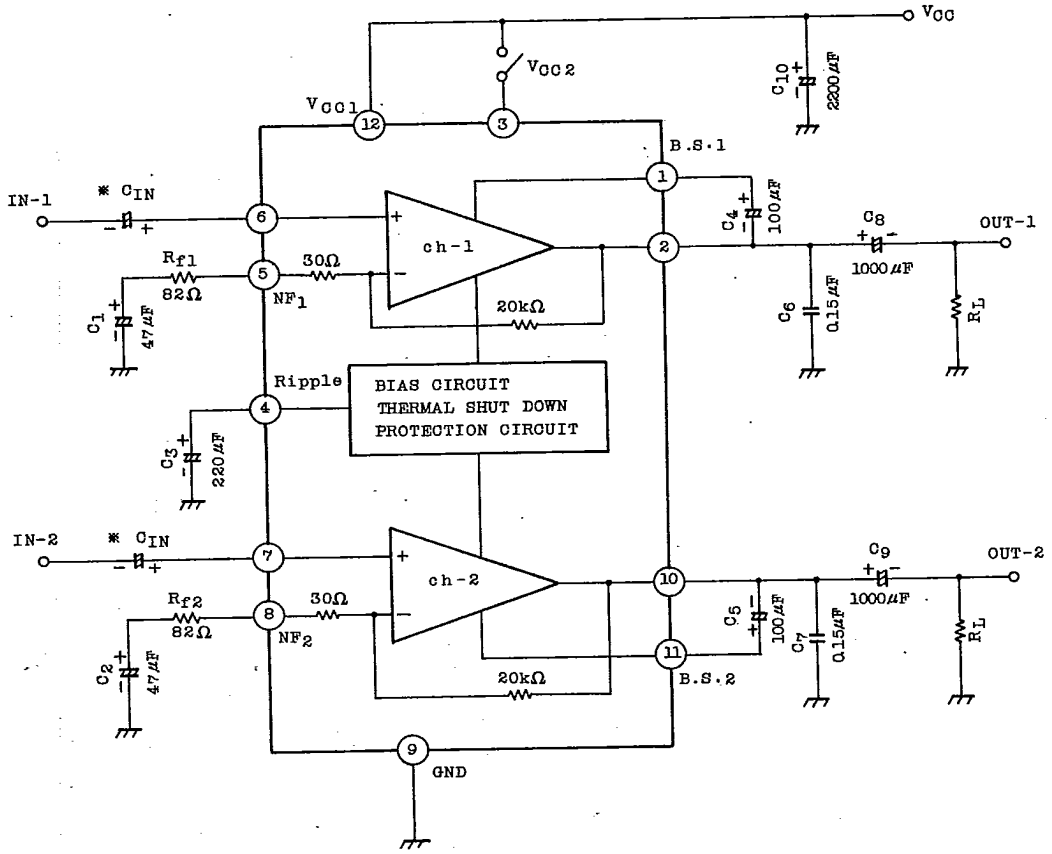
BLOCK DIAGRAM/TEST CIRCUIT



* This IC can be used without coupling capacitor (C_{in}). If volume slide noise occured by input offset voltage is undesirable, it needs to use the capacitor (C_{in}).

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APPLICATION INFORMATION AND APPLICATION METHOD

1. ADJUSTMENT OF VOLTAGE GAIN

The voltage gain G_V is obtained as follows by R_1, R_2 and R_f in Fig. 1.

$$G_V = 20\log \frac{R_f+R_1+R_2}{R_f+R_1}$$

When $R_f=0$ $G_V=56$dB(Typ.)
When $R_f=82\Omega$ $G_V=45$dB (Typ.)
By increasing R_f, reduction of G_V is possible. However, since the feedback increase is liable to produce oscillation, it is recommended to use this at 40dB or over.

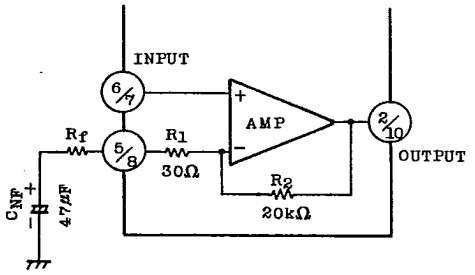

Fig. 1

2. THERMAL SHUT-DOWN CIRCUIT

The thermal shut-down circuit is built in for the purpose of preventing the destruction of IC due to the abnormal temperature rise when the heat radiation is insufficient..
The operation temperature is set at radiation Fin temperature 175°C(Typ.).
At this temperature or over the bias is interrupted to prevent the destruction of IC.

3. INPUT STAGE

The input circuit of this IC is as shown in Fig. 2.
PNP Tr:Q_1 is provided in the input circuit so as to make its usage possible without the input coupling capacitor.
However, at pins ⑥ and ⑦, max 60mV offset voltage is produced.

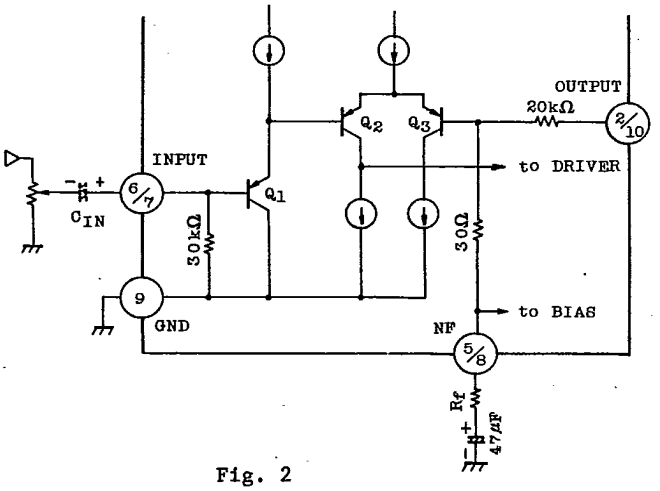

Fig. 2

Application after checking volume slide noise is recommended.
For cutting the volume slide noise, insert the input capacitor:C_{in} in series to interrupt the DC compornent.

4. OSCILLATION PREVENTIVE MEASURES

For oscillation preventive capacitor C_6 and C_7 between the output terminal and GND, it is recommended to use polyester film capacitor having good characteristics for temperature and for high frequency.
Since the characteristics of the capacitor is liable to be influenced the temperature, use this capacitor after the temperature test to check the oscillation allowance.
In addition, as the position of the electrolytic capacitor has a remarkable influence on the oscillation, connect C_{10} to V_{CC} at the nearest possible position from power GND.
At using this application with the voltage gain reduced, oscillation is liable to be produced. Apply the capacitor after cheking enough for its capacity, type and mounting position.
* As the oscillation allowance varies according to the printed pattern layout, the standard printed board of TOSHIBA is recommended to be referred to for design it.

5. POWER ON/OFF SWITCH

There is power ON/OFF switch at ③ pin. However, output power is changed by ③ pin supply voltage when ③ pin supply voltage is not same ⑫ pin supply voltage, after referring to attached date, select ③ pin supply voltage.

6. INPUT VOLTAGE

When the excessive signal is input, turning-up is produced in the clip waveform. The turning-up point is V_{in}=300mV_{rms}(Typ.):V_{CC}=9V, R_L=4Ω, f=1kHz:Enough care must be taken for this phenomenon.

7. GND LINE

GND pin is not separated for Pre-GND and for P_W-GND. That is liable to cause distortion and cross talk worse. Before use this IC, please chack it.

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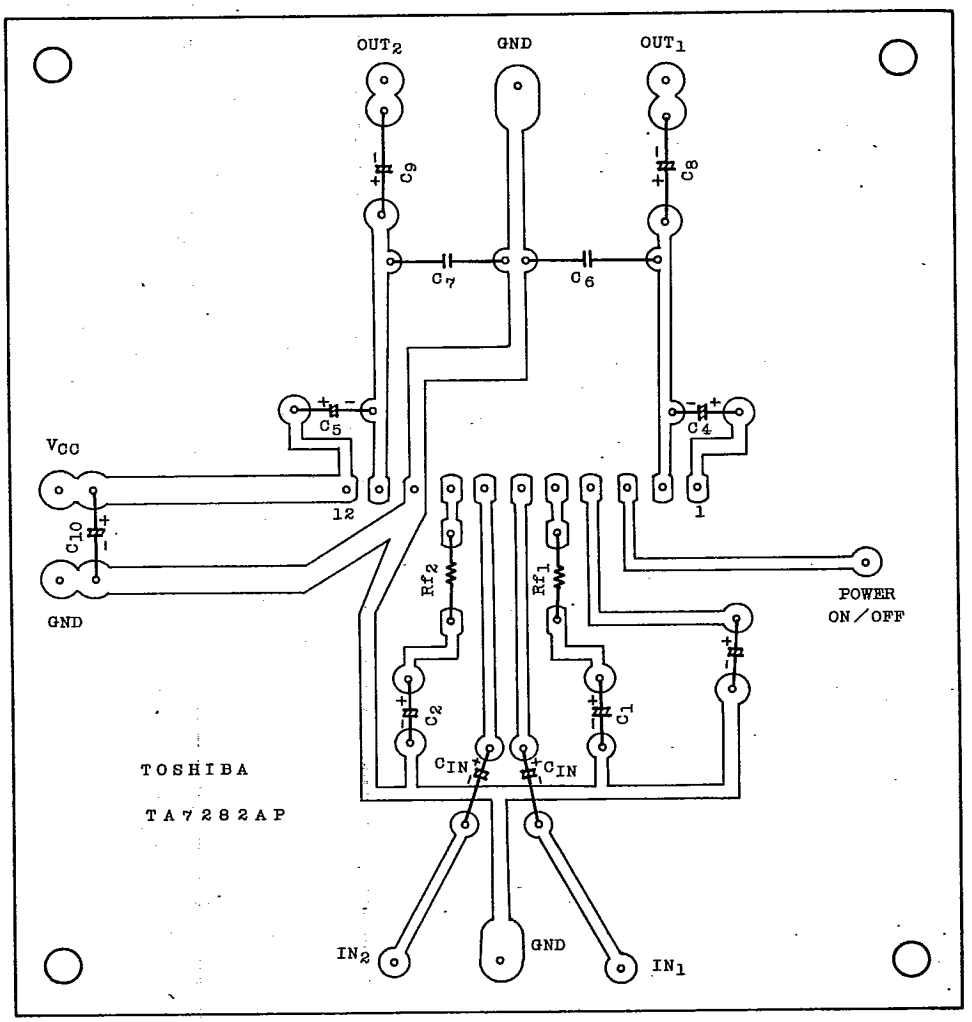
STANDARD PRINT PATTERN



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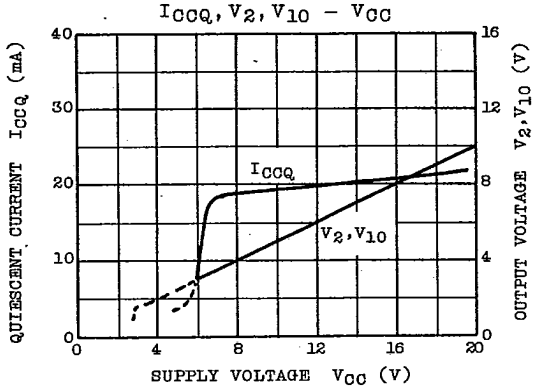
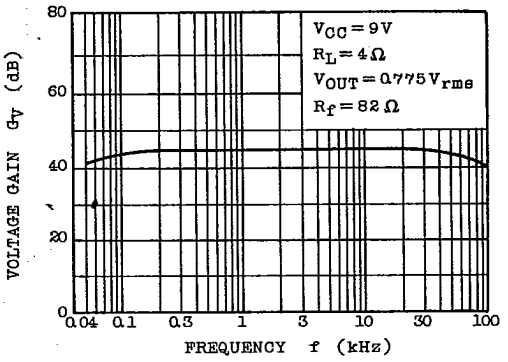
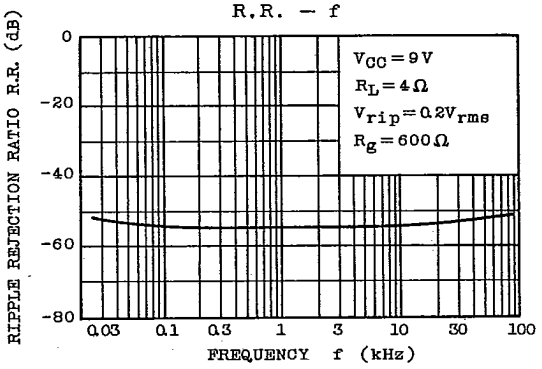
I_{CCQ}, V_2, V_{10} – V_{CC}



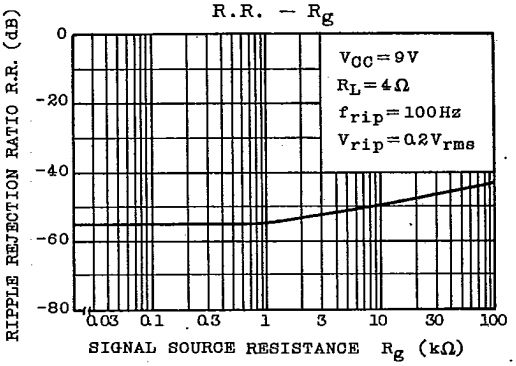
G_V – f



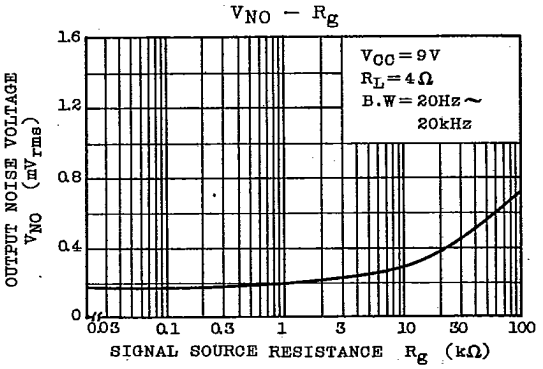
R.R. – f



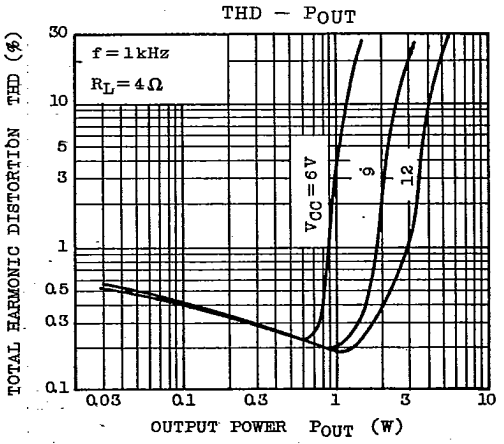
R.R. – R_g



V_{NO} – R_g



THD – P_{OUT}



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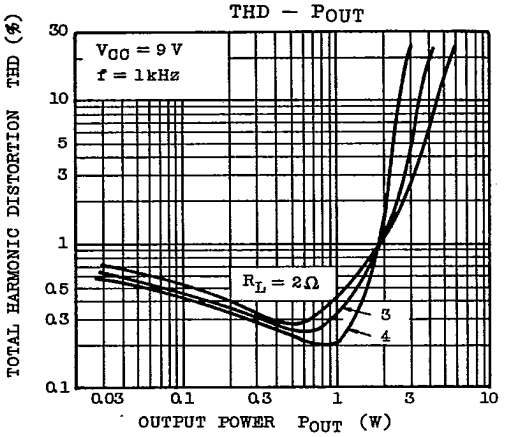
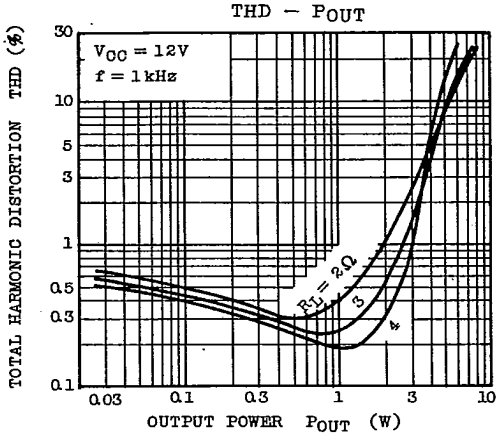
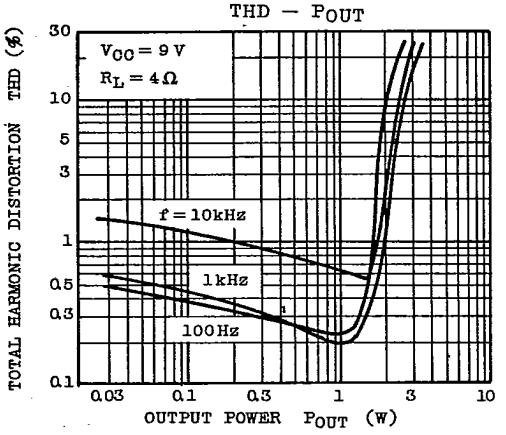
THD – P_{OUT}



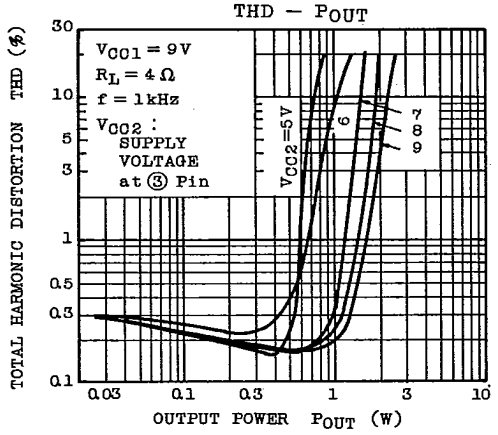
THD – P_{OUT}



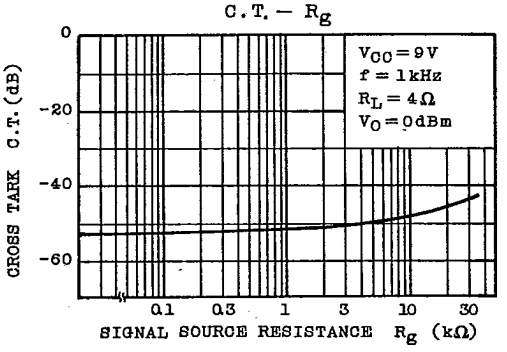
THD – P_{OUT}



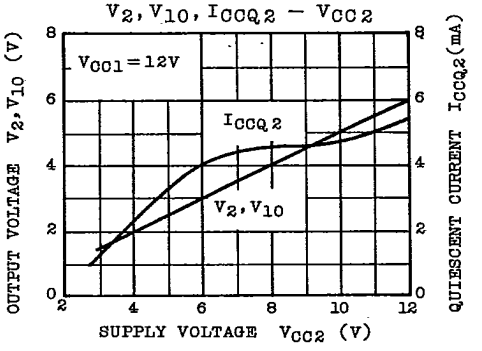
THD – P_{OUT}



C.T. – R_g



V_2, V_{10}, I_{CCQ2} – V_{CC2}



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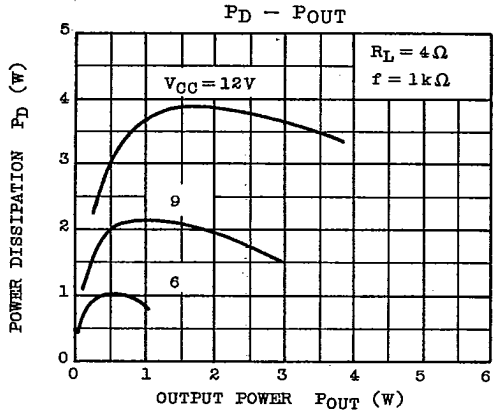
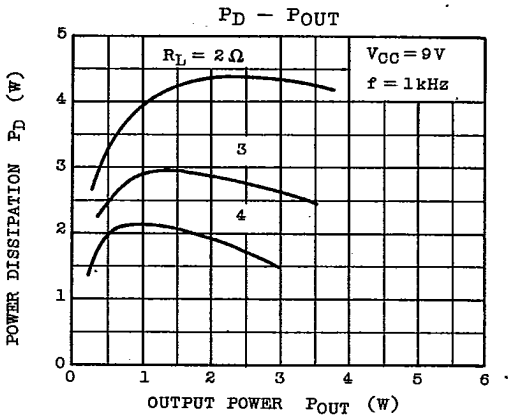
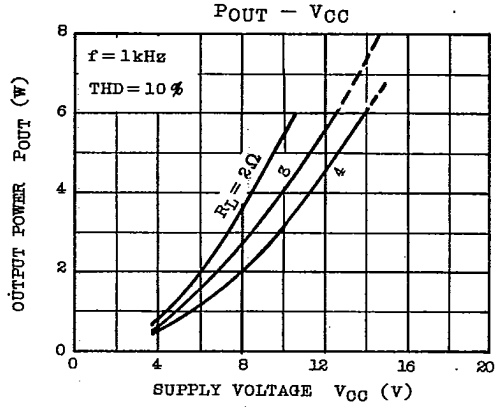
$P_D - P_{OUT}$



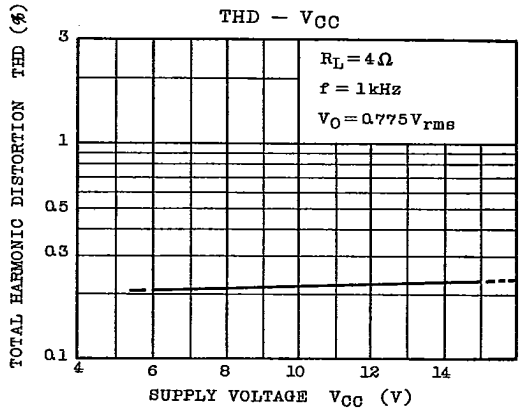
$P_D - P_{OUT}$



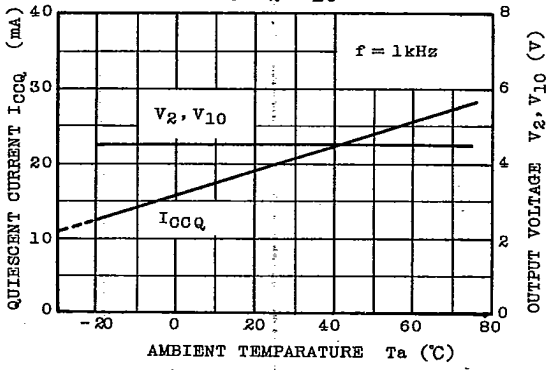
$P_{OUT} - V_{CC}$



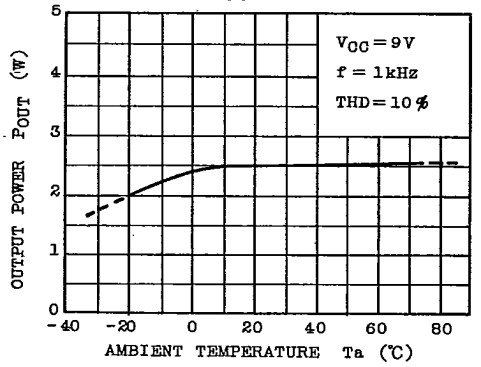
THD – V_{CC}



I_{CCQ}, V_2, V_{10} – Ta



P_{OUT} – Ta



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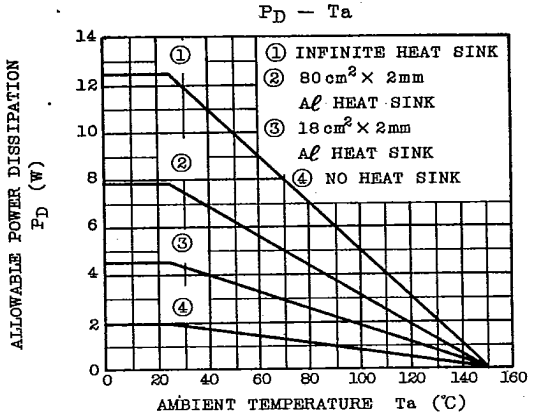
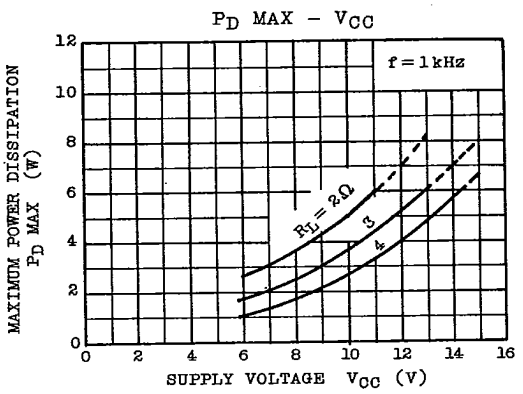
P_D – Ta



P_D MAX – V_{CC}



THD – Ta