



捷多那, 专业PCB打样工厂, 24小时加急出货

MC12012

S-2

ORIG

003406

T-3406

met

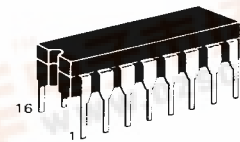
MECL PLL COMPONENTS

TWO-MODULUS PRESCALER

The MC12012 is a two-modulus prescaler which consists of three functional blocks: 1) a controllable divide-by-5/divide-by-6 prescaler; 2) a divide-by-2 prescaler, and 3) a MECL to MTTL translator. When used with the MC12014 Counter Control Logic function and the MC4016 programmable counter, a divide-by-N programmable counter can be constructed for operation to 200 MHz. This arrangement is especially useful in frequency synthesizer applications.

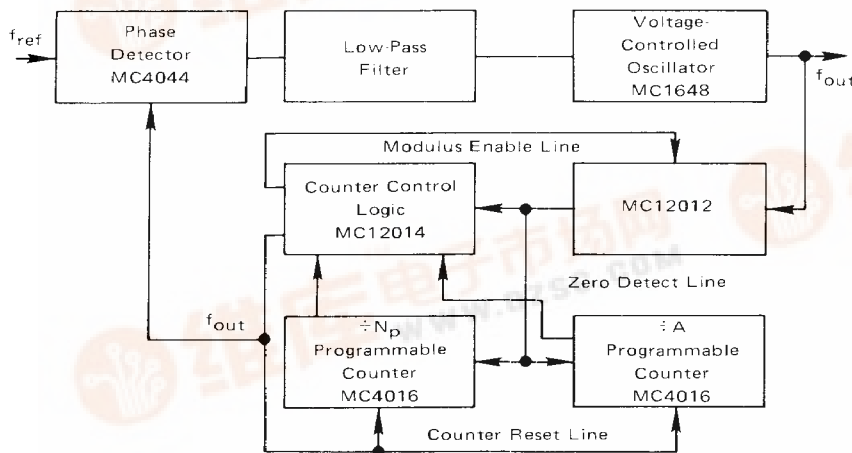
- $\div 2, \div 5/\div 6, \div 10/\div 11, \div 10/\div 12$
- MECL to MTTL Translator on Chip
- +5.0 or -5.2 V Operation*
- 200 MHz (Typ) Toggle Frequency

*When using +5.0 V supply, apply +5.0 V to pin 16 (V_{CC}) and ground pin 8 (V_{EE}). When using -5.2 supply, ground pin 16 (V_{CC}) and apply -5.2 V to pin 8 (V_{EE}).



L SUFFIX
CERAMIC PACKAGE
CASE 620

FIGURE 1 — TYPICAL FREQUENCY SYNTHESIZER APPLICATION



PIN ASSIGNMENT

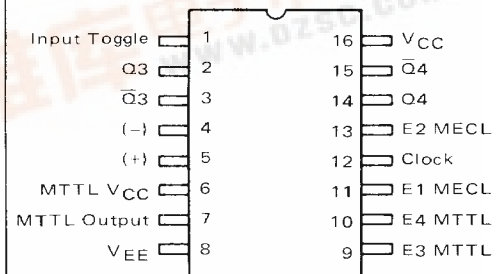
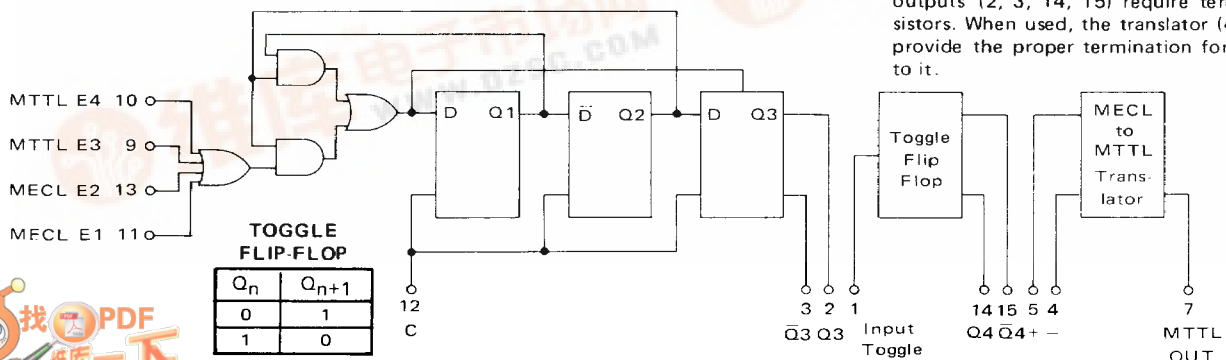


FIGURE 2 — LOGIC DIAGRAM



To obtain an MTTL output connect 5 and 4 to 2 and 3 or 14 and 15 respectively. The MECL outputs (2, 3, 14, 15) require terminating resistors. When used, the translator (4 and 5) will provide the proper termination for connection to it.

MAXIMUM RATINGS

Characteristic	Symbol	Rating	Unit
(Ratings above which device life may be impaired)			
Power Supply Voltage (VCC - 0)	V _{EE}	-8.0	V _{dc}
Input Voltage (VCC - 0)	V _{in}	0 to V _{EE}	V _{dc}
Output Source Current Continuous	I _O	50	mA _{dc}
Storage Temperature Range	T _{stg}	-65 to +150	°C

(Recommended Maximum Ratings, above which performance may be degraded)
Operating Temperature Range

ELECTRICAL CHARACTERISTICS

Supply Voltage -5.2 V

Characteristic		Symbol	Pin Under Test	MC12012						Unit	TEST VOLTAGE/CURRENT APPLIED TO PINS LISTED BELOW																																																																																																																																																																																																																																																																																																																																																								
				0°C		+25°C		+75°C			V _{IHmax}	V _{IHmin}	V _{IHAmax}	V _{IHL}	V _{IHH}	V _{IL}	V _{OL}	V _{OL}	V _{OL}	V _{OL}	V _{OL}	V _{OL}	V _{OL}	V _{OL}	V _{OL}	V _{OL}	V _{OL}	V _{OL}	V _{OL}	V _{OL}	V _{OL}	V _{OL}	V _{OL}	V _{OL}	V _{OL}	V _{OL}	V _{OL}	V _{OL}	V _{OL}	V _{OL}	V _{OL}	V _{OL}	V _{OL}	V _{OL}	V _{OL}	V _{OL}	V _{OL}	V _{OL}	V _{OL}	V _{OL}	V _{OL}	V _{OL}	V _{OL}	V _{OL}	V _{OL}	V _{OL}	V _{OL}	V _{OL}	V _{OL}	V _{OL}	V _{OL}	V _{OL}	V _{OL}	V _{OL}	V _{OL}	V _{OL}	V _{OL}	V _{OL}	V _{OL}	V _{OL}	V _{OL}	V _{OL}	V _{OL}	V _{OL}	V _{OL}	V _{OL}	V _{OL}	V _{OL}	V _{OL}	V _{OL}	V _{OL}	V _{OL}	V _{OL}	V _{OL}	V _{OL}	V _{OL}	V _{OL}	V _{OL}	V _{OL}	V _{OL}	V _{OL}	V _{OL}	V _{OL}	V _{OL}	V _{OL}	V _{OL}	V _{OL}	V _{OL}	V _{OL}	V _{OL}	V _{OL}	V _{OL}	V _{OL}	V _{OL}	V _{OL}	V _{OL}	V _{OL}	V _{OL}	V _{OL}	V _{OL}	V _{OL}	V _{OL}	V _{OL}	V _{OL}	V _{OL}	V _{OL}	V _{OL}	V _{OL}	V _{OL}	V _{OL}	V _{OL}	V _{OL}	V _{OL}	V _{OL}	V _{OL}	V _{OL}	V _{OL}	V _{OL}	V _{OL}	V _{OL}	V _{OL}	V _{OL}	V _{OL}	V _{OL}	V _{OL}	V _{OL}	V _{OL}	V _{OL}	V _{OL}	V _{OL}	V _{OL}	V _{OL}	V _{OL}	V _{OL}	V _{OL}	V _{OL}	V _{OL}	V _{OL}	V _{OL}	V _{OL}	V _{OL}	V _{OL}	V _{OL}	V _{OL}	V _{OL}	V _{OL}	V _{OL}	V _{OL}	V _{OL}	V _{OL}	V _{OL}	V _{OL}	V _{OL}	V _{OL}	V _{OL}	V _{OL}	V _{OL}	V _{OL}	V _{OL}	V _{OL}	V _{OL}	V _{OL}	V _{OL}	V _{OL}	V _{OL}	V _{OL}	V _{OL}	V _{OL}	V _{OL}	V _{OL}	V _{OL}	V _{OL}	V _{OL}	V _{OL}	V _{OL}	V _{OL}	V _{OL}	V _{OL}	V _{OL}	V _{OL}	V _{OL}	V _{OL}	V _{OL}	V _{OL}	V _{OL}	V _{OL}	V _{OL}	V _{OL}	V _{OL}	V _{OL}	V _{OL}	V _{OL}	V _{OL}	V _{OL}	V _{OL}	V _{OL}	V _{OL}	V _{OL}	V _{OL}	V _{OL}	V _{OL}	V _{OL}	V _{OL}	V _{OL}	V _{OL}	V _{OL}	V _{OL}	V _{OL}	V _{OL}	V _{OL}	V _{OL}	V _{OL}	V _{OL}	V _{OL}	V _{OL}	V _{OL}	V _{OL}	V _{OL}	V _{OL}	V _{OL}	V _{OL}	V _{OL}	V _{OL}	V _{OL}	V _{OL}	V _{OL}	V _{OL}	V _{OL}	V _{OL}	V _{OL}	V _{OL}	V _{OL}	V _{OL}	V _{OL}	V _{OL}	V _{OL}	V _{OL}	V _{OL}	V _{OL}	V _{OL}	V _{OL}	V _{OL}	V _{OL}	V _{OL}	V _{OL}	V _{OL}	V _{OL}	V _{OL}	V _{OL}	V _{OL}	V _{OL}	V _{OL}	V _{OL}	V _{OL}	V _{OL}	V _{OL}	V _{OL}	V _{OL}	V _{OL}	V _{OL}	V _{OL}	V _{OL}	V _{OL}	V _{OL}	V _{OL}	V _{OL}	V _{OL}	V _{OL}	V _{OL}	V _{OL}	V _{OL}	V _{OL}	V _{OL}	V _{OL}	V _{OL}	V _{OL}	V _{OL}	V _{OL}	V _{OL}	V _{OL}	V _{OL}	V _{OL}	V _{OL}	V _{OL}	V _{OL}	V _{OL}	V _{OL}	V _{OL}	V _{OL}	V _{OL}	V _{OL}	V _{OL}	V _{OL}	V _{OL}	V _{OL}	V _{OL}	V _{OL}	V _{OL}	V _{OL}	V _{OL}	V _{OL}	V _{OL}	V _{OL}	V _{OL}	V _{OL}	V _{OL}	V _{OL}	V _{OL}	V _{OL}	V _{OL}	V _{OL}	V _{OL}	V _{OL}	V _{OL}	V _{OL}	V _{OL}	V _{OL}	V _{OL}	V _{OL}	V _{OL}	V _{OL}	V _{OL}	V _{OL}	V _{OL}	V _{OL}	V _{OL}	V _{OL}	V _{OL}	V _{OL}	V _{OL}	V _{OL}	V _{OL}	V _{OL}	V _{OL}	V _{OL}	V _{OL}	V _{OL}	V _{OL}	V _{OL}	V _{OL}	V _{OL}	V _{OL}	V _{OL}	V _{OL}	



TEST VOLTAGE/CURRENT VALUES

Volts

② Test Temperature

0°C

25°C

75°C

ELECTRICAL CHARACTERISTICS

Supply Voltage +5.0 V

Characteristic	Symbol	Pin Under Test	MC12012						TEST VOLTAGE CURRENT APPLIED TO PINS LISTED BELOW										
			0°C		+25°C		+75°C		Unit	V _{IHmax}	V _{IHmin}	V _{IHAmix}	V _{IHmax}	V _{IHmin}	V _{IHAmix}	V _{ILmax}	V _{ILmin}	V _{ILAmix}	V _{ILmax}
			Min	Max	Min	Max	Min	Max											
Power Supply Drain Current	I _E	8	—	135	—	125	—	135	mAdc	12	—	—	—	—	—	—	—	—	—
	I _{INH1}	12	—	200	—	200	—	200	μAdc	1	—	—	—	—	—	—	—	—	
	I _{INH2}	11	—	100	—	100	—	100	μAdc	11	—	—	—	—	—	—	—	—	
	I _{INH3}	13	—	—	—	100	—	—	μAdc	13	—	—	—	—	—	—	—	—	
	I _{INH4}	9	—	40	—	40	—	40	μAdc	—	—	—	—	—	—	—	—	—	
Leakage Current	I _{INH4}	10	—	40	—	40	—	40	μAdc	—	—	—	—	—	—	—	—	—	
	I _{INH4}	4	4.0	6.5	4.0	6.5	4.0	6.5	mAdc	5	4	—	—	—	—	—	—	—	
	I _{INH4}	5	4.0	6.5	4.0	6.5	4.0	6.5	mAdc	5	4	—	—	—	—	—	—	—	
	I _{INL1}	1	—3.0	—	2.0	—	—	—3.0	μAdc	—	—	—	—	—	—	—	—	—	
	I _{INL1}	11	—	—	—	—	—	—	μAdc	—	—	—	—	—	—	—	—	—	
Logic "1" Output Voltage	I _{INL2}	13	—	—	—	—	—	—	μAdc	—	—	—	—	—	—	—	—	—	
	I _{INL2}	9	—2.5	—1.1	—2.5	—1.1	2.5	—1.1	mAdc	—	—	—	—	—	—	—	—	—	
	I _{INL2}	10	—2.5	—1.1	—2.5	—1.1	—2.5	—1.1	mAdc	—	—	—	—	—	—	—	—	—	
	I _{INL3}	4	4.0	7.0	4.0	7.0	4.0	7.0	mAdc	4	5	—	—	—	—	—	—	—	
	I _{INL3}	5	3.0	5.0	3.0	5.0	3.0	5.0	mAdc	4	5	—	—	—	—	—	—	—	
Logic "1" Output Voltage	V _{OH1}	2	4.000	4.160	4.040	4.190	4.100	4.280	Vdc	11,13	9,10	—	—	—	—	—	—	—	
	V _{OH1}	3	—	—	—	—	—	—	μAdc	—	—	—	—	—	—	—	—	—	
	V _{OH1}	14	—	—	—	—	—	—	μAdc	—	—	—	—	—	—	—	—	—	
	V _{OH1}	15	—	—	—	—	—	—	μAdc	—	—	—	—	—	—	—	—	—	
	V _{OH2}	7	2.400	—	2.400	—	2.400	—	Vdc	5	4	—	—	—	—	—	—	—	
Logic "0" Output Voltage	V _{OL1}	2	3.180	3.415	3.200	3.430	3.220	3.455	Vdc	11,13	9,10	—	—	—	—	—	—	—	
	V _{OL1}	3	—	—	—	—	—	—	μAdc	—	—	—	—	—	—	—	—	—	
	V _{OL1}	14	—	—	—	—	—	—	μAdc	—	—	—	—	—	—	—	—	—	
	V _{OL1}	15	—	—	—	—	—	—	μAdc	—	—	—	—	—	—	—	—	—	
	V _{OL2}	7	—	0.500	—	0.500	—	0.500	Vdc	4	5	—	—	—	—	—	—	—	
Logic "1" Threshold Voltage	V _{OH1}	2	3.980	—	4.020	—	4.080	—	Vdc	11,13	9,10	—	—	—	—	—	—	—	
	V _{OH1}	3	—	—	—	—	—	—	μAdc	—	—	—	—	—	—	—	—	—	
	V _{OH1}	14	—	—	—	—	—	—	μAdc	—	—	—	—	—	—	—	—	—	
	V _{OH1}	15	—	—	—	—	—	—	μAdc	—	—	—	—	—	—	—	—	—	
	V _{OL2}	7	—	0.500	—	0.500	—	0.500	Vdc	4	5	—	—	—	—	—	—	—	
Logic "0" Threshold Voltage	V _{OL1}	2	—	—	—	—	—	—	Vdc	11,13	9,10	—	—	—	—	—	—	—	
	V _{OL1}	3	—	—	—	—	—	—	μAdc	—	—	—	—	—	—	—	—	—	
	V _{OL1}	14	—	—	—	—	—	—	μAdc	—	—	—	—	—	—	—	—	—	
	V _{OL1}	15	—	—	—	—	—	—	μAdc	—	—	—	—	—	—	—	—	—	
	V _{OL2}	7	—	0.500	—	0.500	—	0.500	Vdc	4	5	—	—	—	—	—	—	—	
Short Circuit Current	I _{OS}	7	—20	—65	—20	—65	—20	—65	mAdc	5	4	—	—	—	—	—	—	—	



MOTOROLA Semiconductor Products Inc.

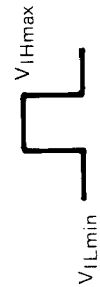
TEST VOLTAGES/WAVEFORMS APPLIED TO PINS LISTED BELOW									
Characteristic	Symbol	Pin Under Test	MC12012						Pulse Gen. 1
			0°C		+25°C		+75°C		Pulse Gen. 2
			Min	Max	Min	Typ	Max	Unit	
Propagation Delay (See Figures 3 and 4)	t ₁₂₊₂₊	12,2	—	—	—	3.0	4.0	ns	12
	t ₁₂₊₃₊	12,3	—	—	—	3.0	—	—	—
	t ₁₂₊	12,2	—	—	—	2.8	—	—	—
	t ₁₂₊₃₋	12,3	—	—	—	2.8	—	—	—
	t ₁₊₁₄₊	1,14	—	—	—	3.0	—	—	—
	t ₁₊₁₅₊	1,15	—	—	—	3.0	—	—	—
	t ₁₊₁₄₋	1,14	—	—	—	2.8	—	—	—
	t ₁₊₁₅₋	1,15	—	—	—	2.8	—	—	—
	t ₅₊₇₊	5,7	—	—	—	8.0	12.0	—	—
	t ₅₋₇₋	5,7	—	—	—	5.0	10.0	—	—
Output Rise Time (See Figure 4)	t ₂₊	2	—	—	—	—	3.0	ns	12
	t ₃₊	3	—	—	—	—	—	—	12
	t ₁₄₊	14	—	—	—	—	—	—	1
	t ₁₅₊	15	—	—	—	—	—	—	1
	t ₂₋	2	—	—	—	—	2.5	ns	12
Output Fall Time (See Figure 4)	t ₃₋	3	—	—	—	—	—	—	12
	t ₁₄₋	14	—	—	—	—	—	—	1
	t ₁₅₋	15	—	—	—	—	—	—	1
	t _{setup1}	11,13	—	4.0	—	2.4	3.0	ns	12
	t _{setup2}	9,10	—	7.0	—	5.0	7.0	ns	12
Setup Time (See Figure 5)	t _{rel1}	11,13	—	2.5	—	1.2	2.0	ns	12
	t _{rel2}	9,10	—	4.0	—	2.5	3.5	ns	12
Toggle Frequency Figure 6 (÷ 5) Figure 7 (÷ 2) Figure 7 (÷ 10 or 11)	f _{max}	2	—	—	175	200	—	MHz	—
	—	2	—	—	—	—	—	—	—
	—	14	—	—	—	—	—	—	—
	—	14	—	—	—	—	—	—	—
	—	14	—	—	—	—	—	—	—

① All MECL outputs (2, 3, 14, 15) are terminated to V_{EE} through an external 510 Ω resistor during the DC tests.

② Test outputs of the device must be tested by sequencing through the truth table. All input, power supply and ground voltages must be maintained between tests. The clock input is



③ In addition to meeting the output levels specified, the device must divide by 5 during this test. The clock input is



④ In addition to meeting the output levels specified the device must divide by 2 with a clock input of



⑤ In addition to meeting the output levels specified, the device must divide by 6 during this test. The clock input is

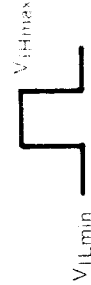


FIGURE 3 AC TEST CIRCUIT



All unused cables must be terminated with 50 ohms.

$C_T = 15 \text{ pF}$ = total parasitic capacitance which includes probe.

The 950-ohm resistor and the scope termination impedance constitute a 20:1 attenuator probe.

stitute a 2:1 attenuator probe.

FIGURE 4 — AC VOLTAGE WAVEFORMS



FIGURE 4 - SETUP AND RELEASE TIME WAVEFORMS

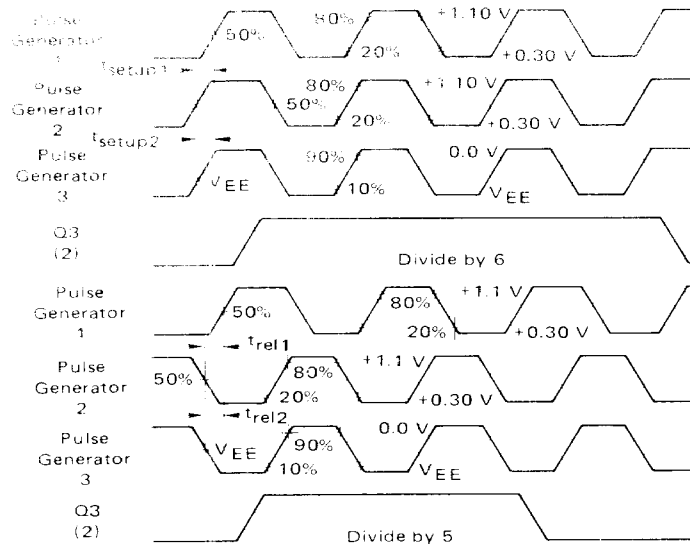
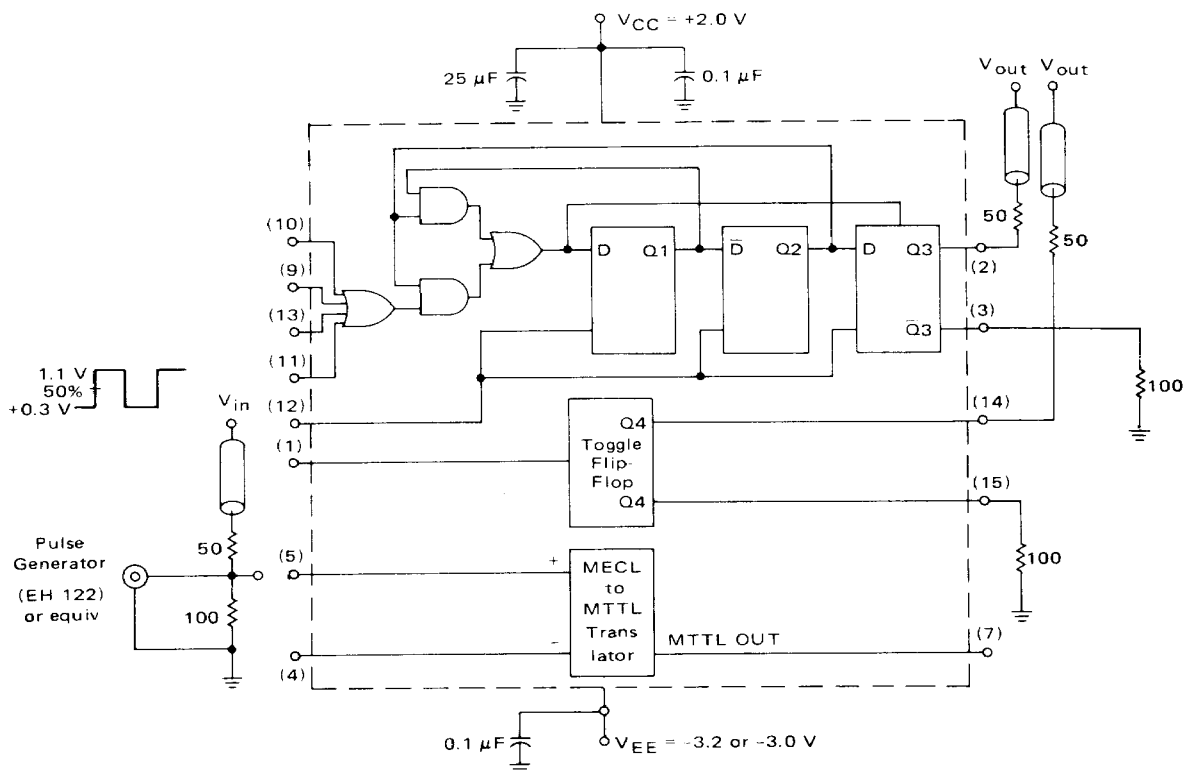


FIGURE 6 - MAXIMUM FREQUENCY TEST CIRCUIT

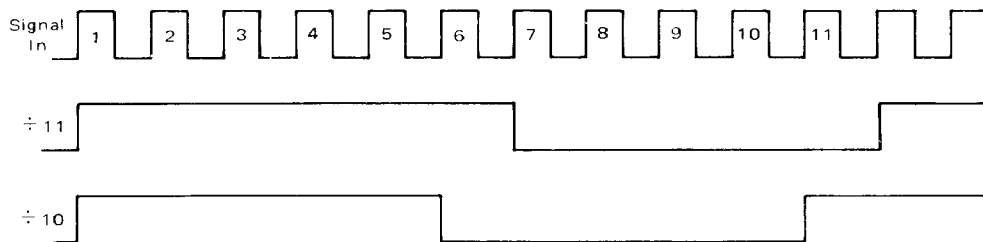
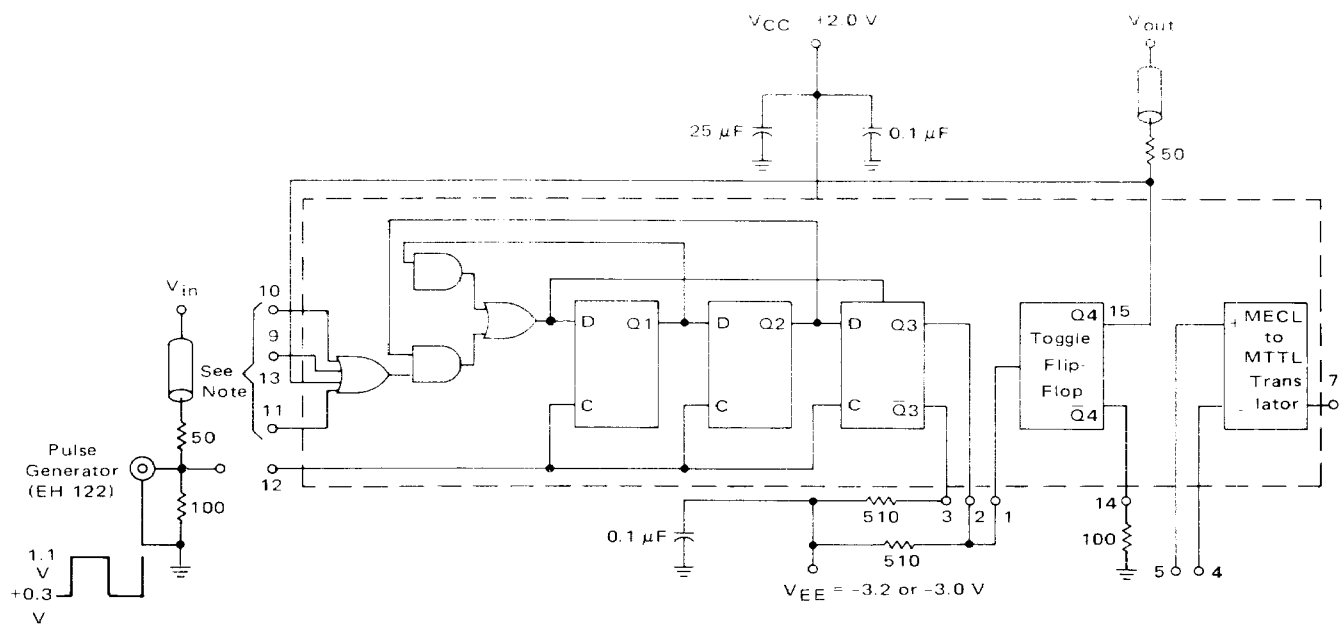


NOTE: Output Waveforms are same as shown in Figures 4 and 5.



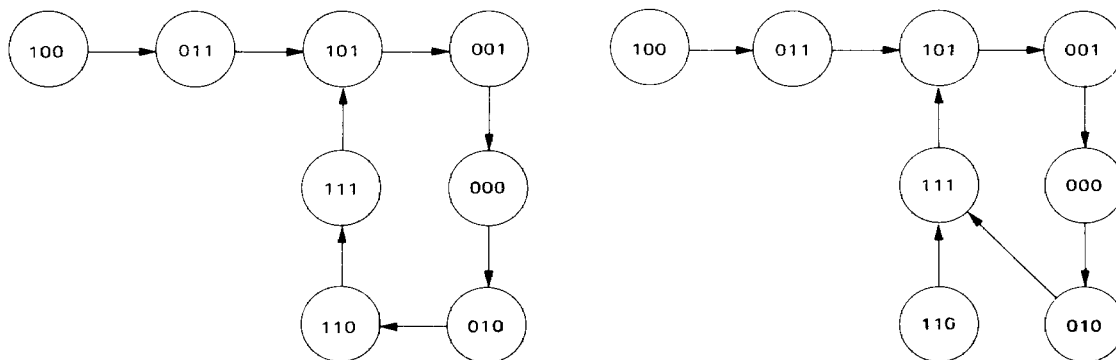
MOTOROLA Semiconductor Products Inc.

FIGURE 7 - TOGGLE FREQUENCY TEST CIRCUIT



NOTE: For divide by 11 connect 11 to $V_{IL} = +0.130$ and 9 and 10 to $V_F = -3.0$ V
For divide by 10 connect 11 to $V_{IH} = +1.160$ or 9 or 10 to $V_R = 0.0$ V

FIGURE 8 - STATE DIAGRAMS



FUNCTION DESCRIPTION

THE MC12012 TWO MODULUS PRESCALER

Three functional blocks are contained in the MC12012 variable modulus prescaler: 1) a controllable $\div 5/\div 6$ prescaler; 2) a $\div 2$ prescaler; and 3) an ECL to TTL translator (for single power supply operation).

Selection of division by 5 or by 6 is made by inputs to E1 through E4. If all E inputs are low before the transition of the clock pulse driving Q3 high, Q3 will stay high for 3 clock pulses, then will go low for 3 clock pulses. This provides a divide by 6 function.

On the other hand, if any one or all of the E inputs are high prior to the positive transition of the clock pulse driving Q3 high, Q3 will stay high for only 2 clock pulses, then will go low for 3 clock pulses. The result is division by 5.

For the $\div 5$ operation, at least one of the E inputs must go high sometime before the clock pulse. This time is referred to as the "setup time." Specifications for setup time are given in the electrical characteristics table: t_{setup1} and t_{setup2} for E1 and E2 (MECL inputs), and E3 and E4 (MTTL inputs).

For the divide by 6 operation all E inputs must be low for some time prior to the clock pulse. This time is referred to as the "release time." Data for release time is given in the electrical characteristics table; t_{re1} and t_{re2} for E1, E2, E3, E4.

The data given in the tables for setup and release times are referenced to the positive transition of the clock pulse

causing Q3 to go high. If it is necessary to reference the setup and release times to the positive transition of Q3, add $t_{\text{++}}$ (specified for Q3) to the setup/release times given. It should be noted that the logic states for the enable inputs are important only for only one clock pulse which causes Q3 to go high (within the limits specified by setup and release times).

The $\div 5/\div 6$ prescaler may be connected externally to the $\div 2$ prescaler to form a $\div 10/\div 11$ prescaler (Figure 10) or a $\div 10/\div 12$ prescaler (Figure 11).

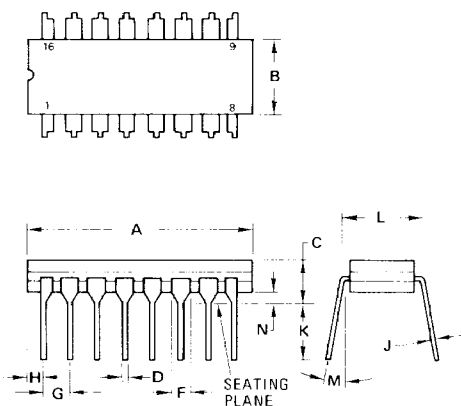
By way of an example showing how a $\div 10/\div 11$ prescaler operates, note that if E1, E3, and E4 (Figure 10) are held in a low state, the counter divides by 11. To do this, a feedback connection is established from Q4 to E2 (or to E1). With this feedback, the $\div 5/\div 6$ prescaler divides by 5 when Q4 is high, and by 6 when Q4 is low.

Since Q4 changes state with each positive transition of Q3, the prescaler alternates between $\div 5$ and $\div 6$ resulting in a $\div 11$ at Q4.

If any one or all of the E inputs are high (Figure 10), the $5/6$ prescaler always divides by 5 and a divide by 10 results at Q4.

With the addition of external flip-flops and counters (MECL or MTTL) various other modulus prescalers may be produced (20/21, 20/22, 20/24, 40/41, 50/51, 100/101, etc.).

OUTLINE DIMENSIONS



NOTES:

- LEADS WITHIN 0.13 mm (0.005) RADIUS OF TRUE POSITION AT SEATING PLANE
- AT MAXIMUM MATERIAL CONDITION PKG. INDEX: NOTCH IN LEAD NOTCH IN CERAMIC OR INK DOT
- DIM "L" TO CENTER OF LEADS WHEN FORMED PARALLEL

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	19.05	19.81	0.750	0.780
B	6.22	6.99	0.245	0.275
C	4.06	5.08	0.160	0.200
D	0.38	0.51	0.015	0.020
F	1.40	1.65	0.055	0.065
G	2.54 BSC		0.100 BSC	
H	0.51	1.14	0.020	0.045
J	0.20	0.31	0.008	0.012
K	3.18	4.06	0.125	0.160
L	7.37	7.87	0.290	0.310
M	—	15°	—	15°
N	0.51	1.02	0.020	0.040

CASE 620

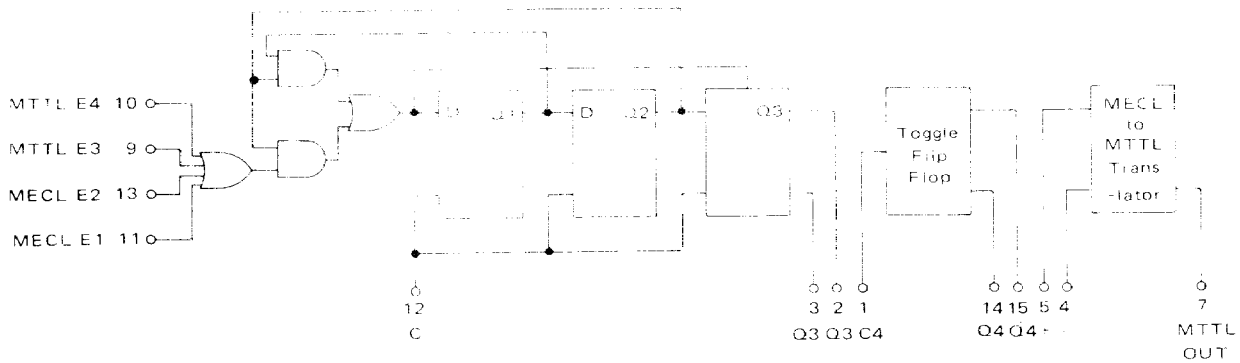
Motorola reserves the right to make changes to any products herein to improve reliability, function or design. Motorola does not assume any liability arising out of the application or use of any product or circuit described herein, neither does it convey any license under its patent rights nor the rights of others.



MOTOROLA Semiconductor Products Inc.

BOX 20912 • PHOENIX, ARIZONA 85036 • A SUBSIDIARY OF MOTOROLA INC.

FIGURE 9 - ÷ 5/6

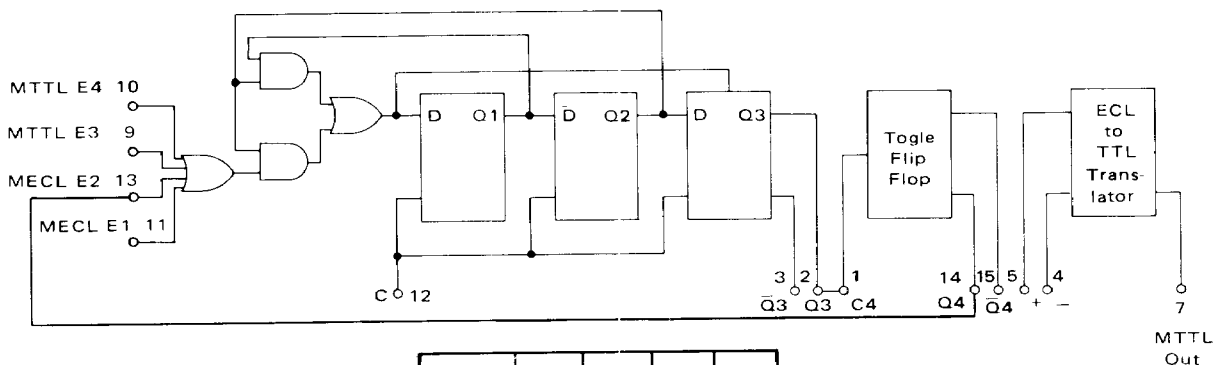


Divide by 2
use Toggle
Flip Flop

COUNT	Q1	Q2	Q3
6	0	1	1
7	1	1	1
5	1	0	1
1	1	0	0
0	0	0	0
2	0	1	0

To obtain an MTTL output connect 5 and 4 to 2 and 3 or 14 and 15, respectively.

FIGURE 10 - ÷ 10/11



COUNT	Q1	Q2	Q3	Q4
14	0	1	1	1
15	1	1	1	1
13	1	0	1	1
9	1	0	0	1
8	0	0	0	1
10	0	1	0	1
7	1	1	1	0
5	1	0	1	0
1	1	0	0	0
0	0	0	0	0
2	0	1	0	0

To obtain an MTTL output connect 5 and 4 to 14 and 15, respectively.



FIGURE 11 — 10/12

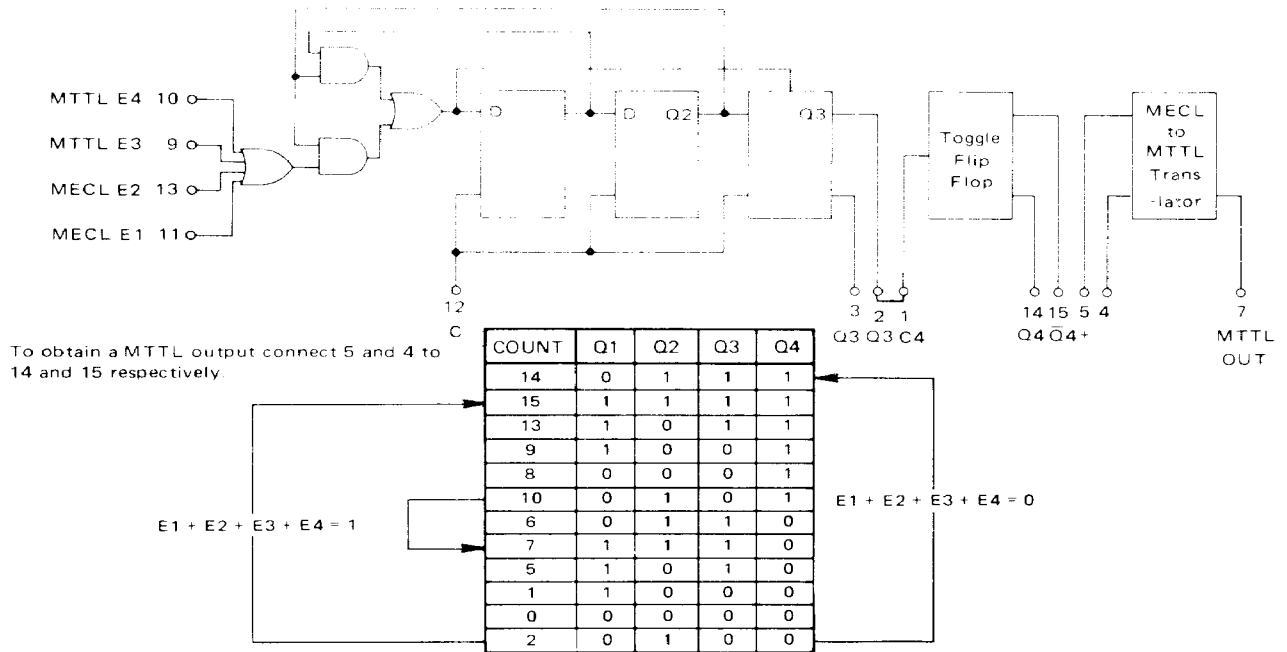


FIGURE 12 — 20/21

