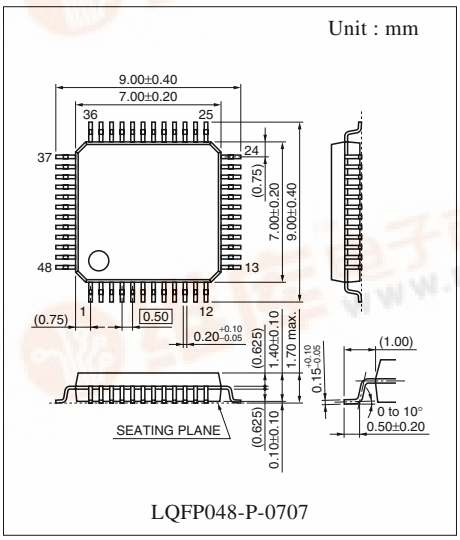
AN2104NFHQ

Digital Pre-Processing IC for Digital Cameras

■ Overview

The AN2104NFHQ is a digital pre-processing IC for CCD digital cameras. It is a single chip IC including a 10-bit A/D converter as well as CDS and AGC circuits. The CDS circuit achieves high-speed sampling at rates up to 25 MHz, and thus the AN2104NFHQ can support advanced CCD cameras developing in higher density pixels and image quality, such as XGA or SXGA resolutions. The AGC and OB circuits can be adjusted with 9-bit and 8-bit serial data respectively through on-chip D/A converter.



LQFP048-P-0707

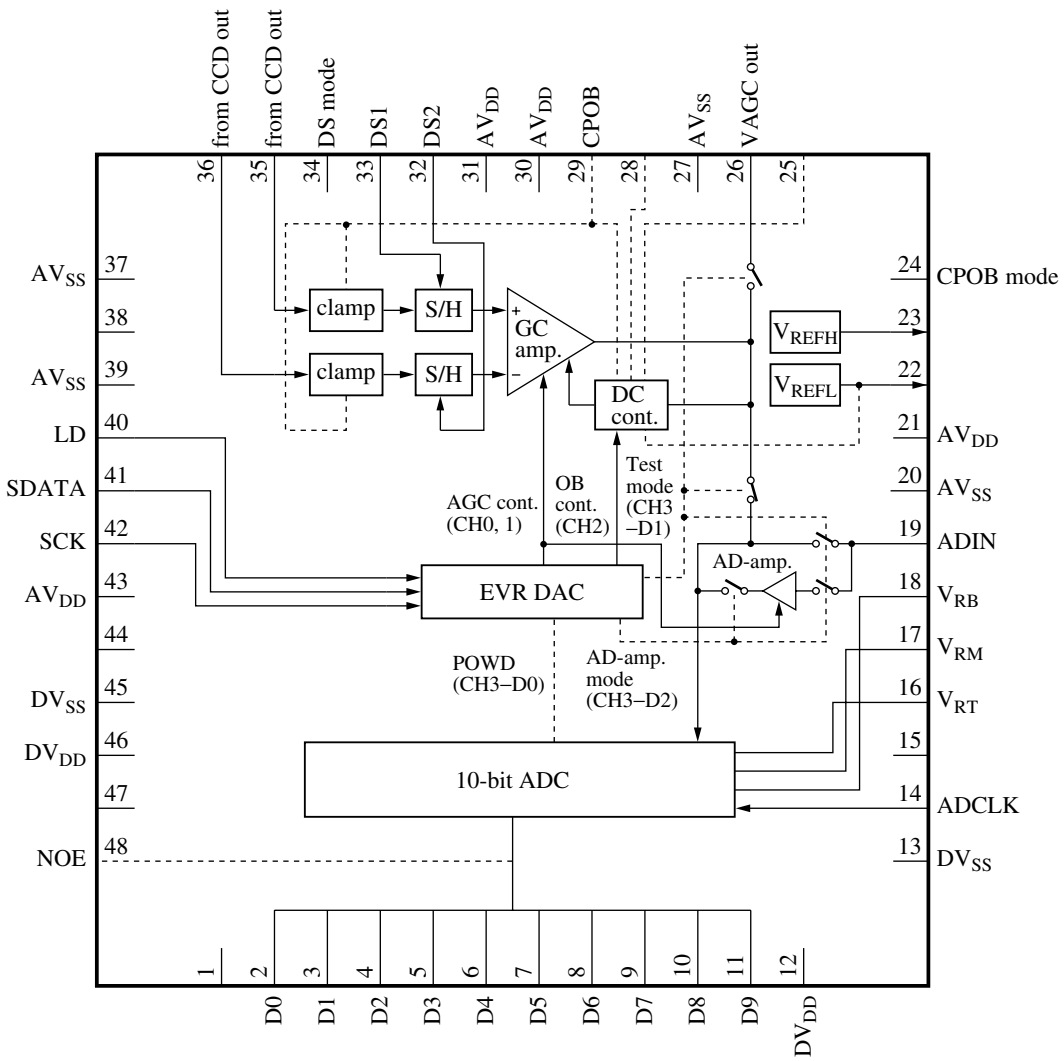
■ Features

- Low power (114 mW typ. at 3 V supply voltage)
- High-speed sample-and-hold circuit operates up to 25 MHz.
- The AGC can be adjusted over 0.5 dB to 36 dB range.
- The OB circuit is adjustable over a {V_{RB} to V_{RB}+(V_{RT} −V_{RB})/4} range.
- On-chip A/D converter reference voltage supply circuit (V_{RT} and V_{RB})
- On-chip 10-bit A/D converter (maximum conversion speed: 25 MSPS)
- Built-in 3-channel 8-bit D/A converter for adjustments and mode settings.

■ Applications

- Digital still cameras
- Video cameras
- PC input cameras
- Surveillance cameras
- Board cameras
- Cameras that use CCDs and digital signal processing.

■ Block Diagram



■ Pin Descriptions

Pin No.	Description	Pin No.	Description
1	Unused (Must be connected to ground.)	25	Output OB level stabilization
2	A/D converter output D0	26	AGC output in test mode
3	A/D converter output D1	27	Analog system ground 2
4	A/D converter output D2	28	Input DC level stabilization
5	A/D converter output D3	29	CPOB pulse input
6	A/D converter output D4	30	Analog system power supply 2
7	A/D converter output D5	31	Analog system power supply 3
8	A/D converter output D6	32	DS2 pulse input
9	A/D converter output D7	33	DS1 pulse input
10	A/D converter output D8	34	DS1 and DS2 pulse. Active high/active low setting
11	A/D converter output D9	35	CCD output signal input 1
12	Digital system power supply 1	36	CCD output signal input 2
13	Digital system ground 1	37	Analog system ground 3
14	A/D converter clock input	38	Unused (Must be connected to ground.)
15	Unused (Must be connected to ground.)	39	Analog system ground 4
16	A/D converter reference supply V_{RT} input	40	Load pulse input
17	A/D converter reference supply V_{RM}	41	Serial data input
18	A/D converter reference supply V_{RB} input	42	Serial clock input
19	AGC input in test mode	43	Analog system power supply 4
20	Analog system ground 1	44	Unused (Must be connected to ground.)
21	Analog system power supply 1	45	Digital system ground 2
22	Reference voltage supply V_{REFL} output (1.1 V typical)	46	Digital system power supply 2
23	Reference voltage supply V_{REFH} output (2.5 V typical)	47	Unused (Must be connected to ground.)
24	CPOB pulse. Active high/active low setting	48	A/D converter output enable setting

■ Absolute Maximum Ratings

Parameter	Symbol	Rating	Unit
Supply voltage	V_{DD}	− 0.3 to +4.6	V
Supply current	I_{DD}	—	mA
Power dissipation *2	P_D	226	mW
Operating temperature *1	T_{opr}	−20 to +75	°C
Storage temperature *1	T_{stg}	−55 to +125	°C

Notes: *1 : Except for the operating temperature and storage temperature, all items are measured at T_a = 25 °C.

*2 : The power dissipation is for the package at T_a = 75 °C in free air.

■ Recommended Operating Range

Parameter	Symbol	Range	Unit
Supply voltage	V_{CC}	2.7 to 3.0 to 3.6	V

■ Electrical Characteristics at AV_{DD} = DV_{DD} = 3.0 V, T_a = 25 °C

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Supply current (in CDS mode)	I_{DD1}	$AV_{DD} = DV_{DD} = 3.0$ V, $f_{CLK} = 25$ MHz	—	38	51	mA
Supply current (in AD amplifier mode)	I_{DD2}	$AV_{DD} = DV_{DD} = 3.0$ V, $f_{CLK} = 25$ MHz	—	24	39	mA
Low power mode supply current	I_{POWD}	f_{CLK} = 25 MHz	—	5.0	16	mA
Reference voltage (1)	V_{REFH}	$AV_{DD} = DV_{DD} = 3.0$ V	2.3	2.5	2.7	V
Reference voltage (2)	V_{REFL}	$AV_{DD} = DV_{DD} = 3.0$ V	0.8	1.0	1.2	V
CPOB pulse input voltage high level	$CPOB_H$	—	2.4	—	V_{DD}	V
CPOB pulse input voltage low level	$CPOB_L$	—	V_{SS}	—	0.8	V
DS1 pulse input voltage high level	$DS1_H$	—	2.4	—	V_{DD}	V
DS1 pulse input voltage low level	$DS1_L$	—	V_{SS}	—	0.8	V
DS2 pulse input voltage high level	$DS2_H$	—	2.4	—	V_{DD}	V
DS2 pulse input voltage low level	$DS2_L$	—	V_{SS}	—	0.8	V
AGC frequency characteristics	G_{fA}	10 MHz, with upper blanking, sine wave, 300 mV[p-p]	–2.9	– 0.4	2.1	dB
AGC input dynamic range	G_{AG3}	With upper BLK, sine wave, 600 mV[p-p]	–1.8	0	1.8	dB
Minimum AGC gain	G_{AG4}	With upper BLK, sine wave, 300 mV[p-p]	–2.0	0.5	3.0	dB
Maximum AGC gain	G_{AG5}	With upper BLK, sine wave, 20 mV[p-p]	32.0	36.0	40.0	dB
AGC output dynamic range	V_{AG6}	With upper BLK, sine wave, 50 mV[p-p]	1350	1700	—	mV[p-p]
AGC output DC (1)	V_{OFF1}	CH2 = 00, the difference with respect to V_{REF}	–70	0	70	mV
AGC output DC (2)	V_{OFF2}	CH2 = FF, the difference with respect to (V_{REFH} - V_{REFL})/4	–70	0	70	mV
CDS sampling capability	G_{CDS}	DS1 = DS2 = 25 MHz CDS input: 300 mV[p-p]	–2.0	0	2.0	dB
Reference resistor (V_{RB} to V_{RT})	R_{REF}	—	278	570	950	Ω
AD-amplifier maximum gain	G_{AA1}	3.58 MHz sine wave, 300 mV[p-p]	5.0	—	—	dB
AD-amplifier minimum gain	G_{AA2}	3.58 MHz sine wave, 300 mV[p-p]	—	—	–2.0	dB

■ Electrical Characteristics (continued) at $AV_{DD} = DV_{DD} = 3.0$ V, $T_a = 25$ °C

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Digital input current (high)	I_{DINH}	CLK and POWD pins Pin19 = 0.8 × V_{DD}	—	—	45	µA
Digital input current (low)	I_{DINL}	CLK and POWD pins Pin19 = 0.2 × V_{DD}	—	—	45	µA
Analog input current (high)	I_{AIH}	Pin19 = 3.0 V	—	—	200	µA
Analog input current (low)	I_{AIL}	Pin19 = 0.5 V	–200	—	—	µA
High-level digital input current	V_{IH}	—	2.4	—	V_{DD}	V
Low-level digital input current	V_{IL}	—	V_{SS}	—	0.8	V
High-level digital output current	I_{OH}	$V_{OH} = 0.8 \times V_{DD}$	—	—	–1.5	mA
Low-level digital output current	I_{OL}	$V_{OL} = -0.2 \times V_{DD}$	1.5	—	—	mA
Differential linearity error	E_D	—	—	± 0.5	±1.0	LSB
Dynamic linearity error	DE_L	f_{CLK} = 25 MHz, f_{IN} = 12.5 MHz	—	—	±13	LSB
Quantization noise *1	S/N	f_{CLK} = 20 MHz, f_{IN} = 3.58 MHz	42	47	—	dB

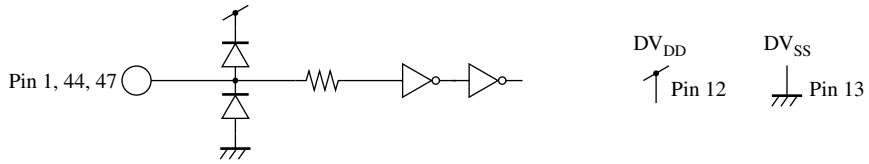
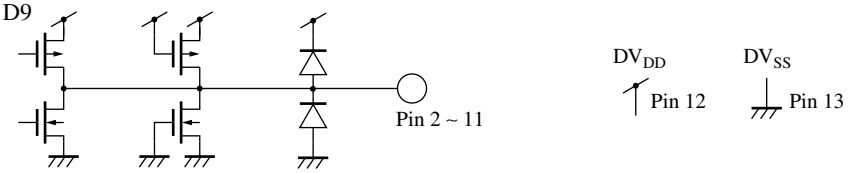
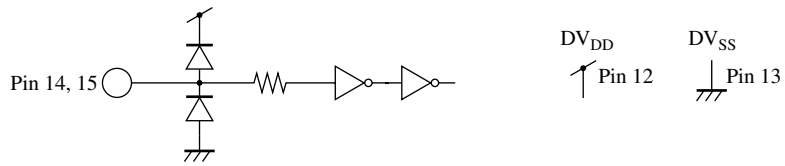
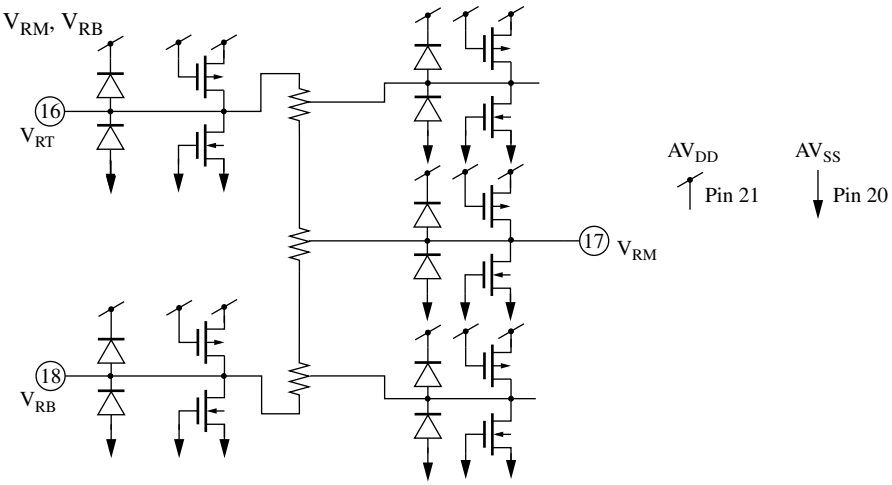
Note: *1. Including the total harmonic distortion.

• Design Reference Data

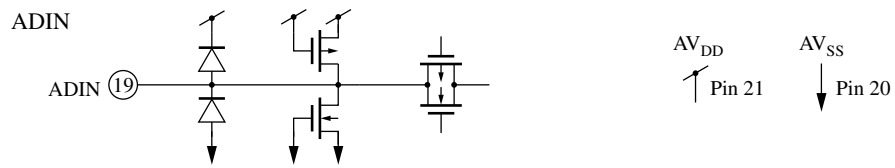
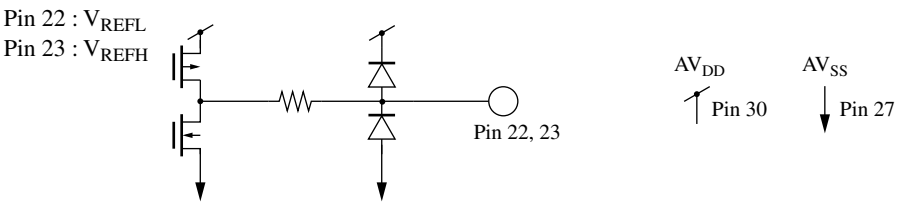
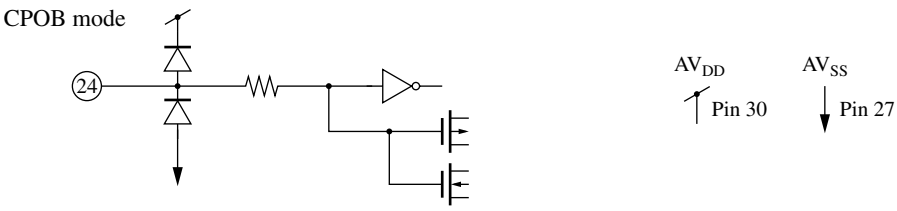
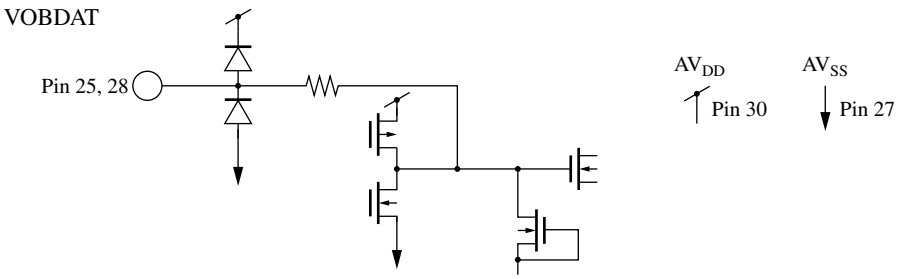
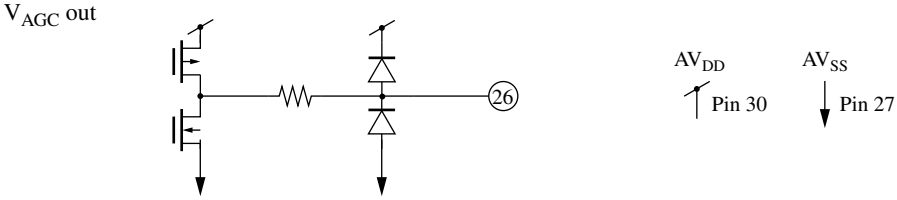
Note: The characteristics shown below are design reference values, and are not guaranteed.

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Maximum conversion rate	F_{CMAX}	—	25	—	—	MSPS
Reference voltage difference	V_{DELTA}	$AV_{DD} = DV_{DD} = 3.0$ V	1.38	1.48	1.58	V

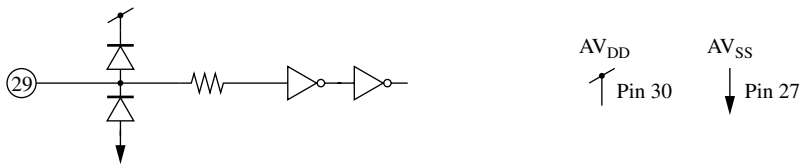
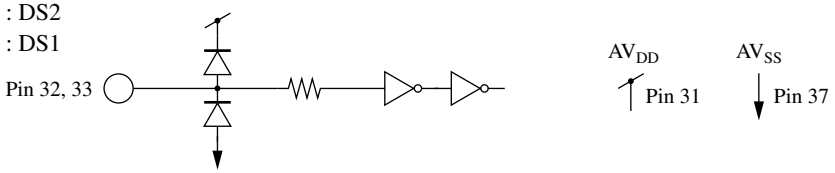
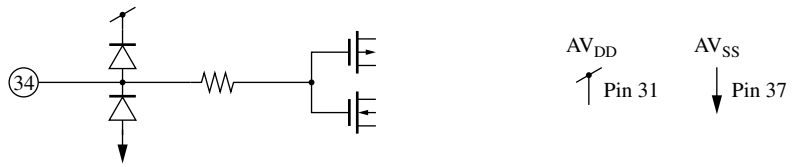
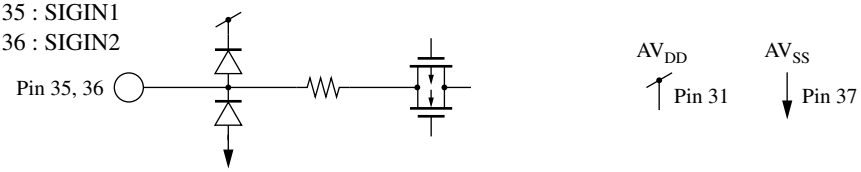
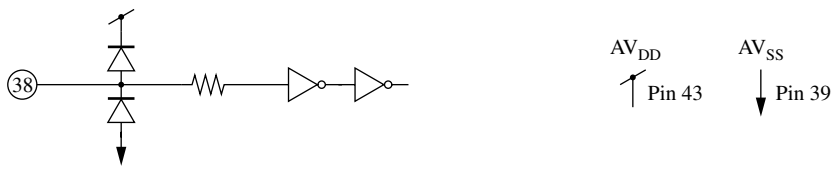
■ Terminal Equivalent Circuits

Pin No.	Equivalent circuit
1	N.C. (Ground to analog system ground) 
2 to 11	D0 to D9 
12 13	Pin 12 : DV_{DD} Pin 13 : DV_{SS} 
14 15	Pin 14 : ADCLK Pin 15 : N.C. (Ground to analog system ground) 
16 17 18	V_{RT}, V_{RM}, V_{RB} 

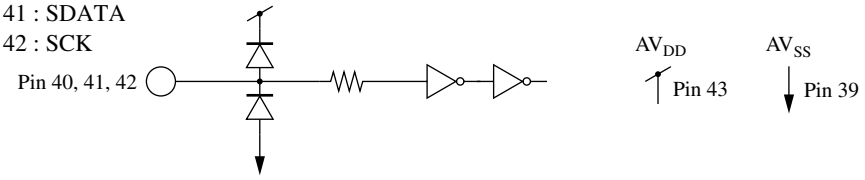
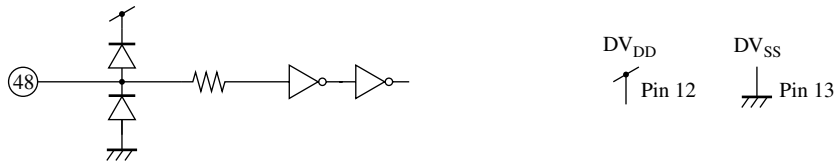
■ Pin Equivalent Circuits (continued)

Pin No.	Equivalent circuit
19	
20 21	
22 23	
24	
25	
26	

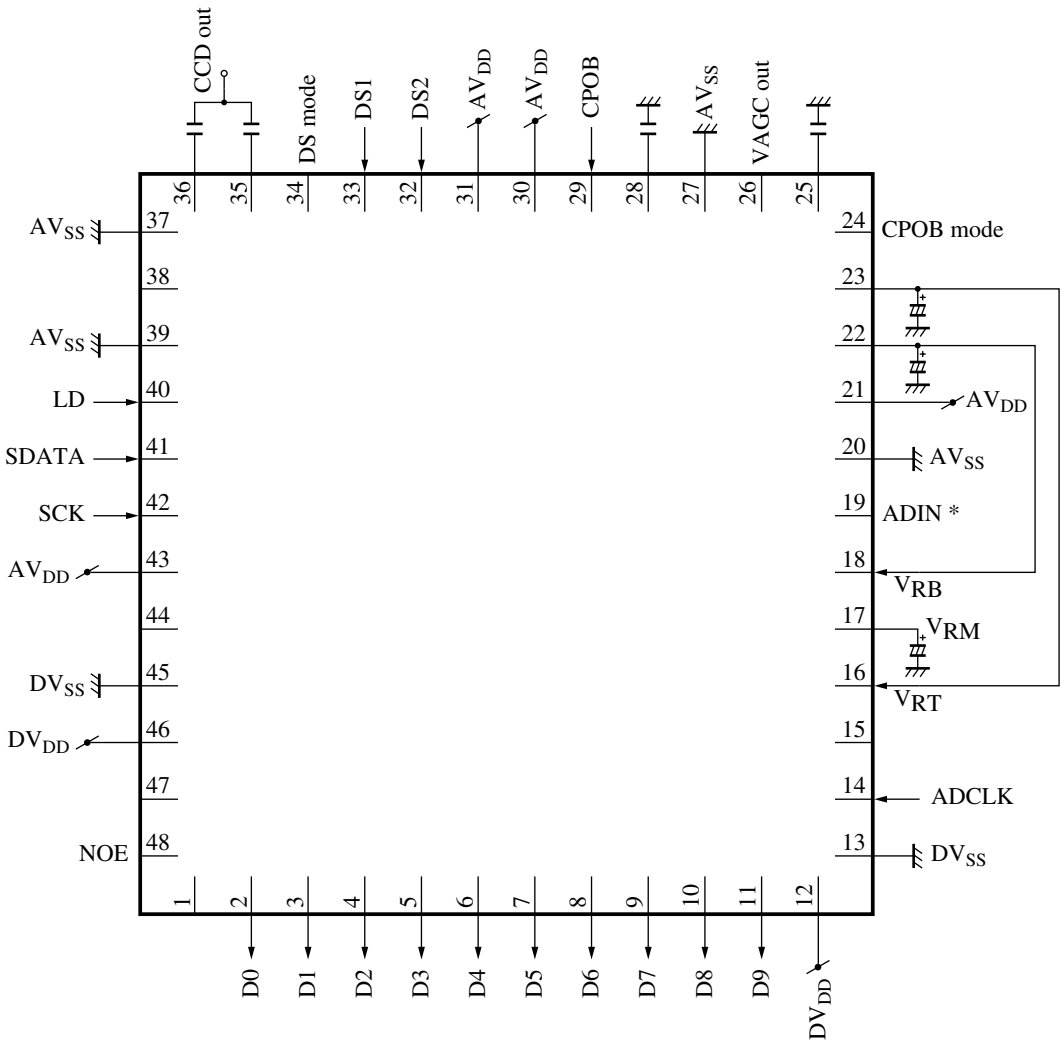
■ Pin Equivalent Circuits (continued)

Pin No.	Equivalent circuit
27	Analog ground
28	VCLIPDAT See pin 25
29	CPOB 
30	AV_{DD} (analog system power supply 2)
31	AV_{DD} (analog system power supply 3)
32 33	Pin 32 : DS2 Pin 33 : DS1 
34	DS mode 
35 36	Pin 35 : SIGIN1 Pin 36 : SIGIN2 
37	Analog ground3
38	Unused (Must be connected to ground.) 
39	Analog ground 4

■ Pin Equivalent Circuits (continued)

Pin No.	Equivalent circuit
40 41 42	Pin 40 : LD Pin 41 : SDATA Pin 42 : SCK 
43	Analog system power supply 4
44	Unused (Must be connected to ground.)
45	Digital system ground 2
46	Digital system power supply 2
47	Unused (Must be connected to ground.)
48	NOE 

■ Application Circuit Example



Note *: When the AD amplifier is used, signals should be input to pin 19 through a capacitor. (Assumed chrominance signal may be input.)

■ Usage Notes

The unused pins (pins 1, 15, 38, 44, and 47) are connected internally to the circuit shown in the "Pin Equivalent Circuits" table. Therefore, these pins must be held fixed at either V_{SS} or V_{DD}.

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