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74ALVC164245

16-bit dual supply translating transciever; 3-state

Rev. 02 — 1 June 2004

Product data sheet

1. General description

The 74ALVC164245 is a high-performance, low-power, low-voltage, Si-gate CMOS device, superior to most advanced CMOS compatible TTL families.

The 74ALVC164245 is a 16-bit (dual octal) dual supply translating transceiver featuring non-inverting 3-state bus compatible outputs in both send and receive directions. It is designed to interface between a 3 V and 5 V bus in a mixed 3 V and 5 V supply environment.

This device can be used as two 8-bit transceivers or one 16-bit transceiver.

The direction control inputs (1DIR and 2DIR) determine the direction of the data flow. nDIR (active HIGH) enables data from nA ports to nB ports. nDIR (active LOW) enables data from nB ports to nA ports. The output enable inputs ($1\overline{OE}$ and $2\overline{OE}$), when HIGH, disable both nA and nB ports by placing them in a high-impedance OFF-state. The nB ports interface with the 5 V bus. The nA ports interface with the 3 V bus.

In suspend mode, when one of the supply voltages is zero, there will be no current flow from the non-zero supply towards the zero supply. The A-outputs must be set 3-state and the voltage on the A-bus must be smaller than V_{diode} (typical 0.7 V). $V_{CCB} \geq V_{CCA}$ (except in suspend mode).

2. Features

- 5 V tolerant inputs/outputs for interfacing with 5 V logic
- Wide supply voltage range:
  - 3 V port (V_{CCA}): 1.5 V to 3.6 V
  - 5 V port (V_{CCB}): 1.5 V to 5.5 V.
- CMOS low power consumption
- Direct interface with TTL levels
- Control inputs voltage range from 2.7 V to 5.5 V
- Inputs accept voltages up to 5.5 V
- High-impedance outputs when V_{CCA} or V_{CCB} = 0 V
- Complies with JEDEC standard JESD8-B/JESD36
- ESD protection:
  - HBM EIA/JESD22-A114-B exceeds 2000 V
  - MM EIA/JESD22-A115-A exceeds 200 V.
- Specified from –40 °C to +85 °C and –40 °C to +125 °C.

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3. Quick reference data

Table 1: Quick reference data
GND = 0 V; T_{amb} = 25 °C; $t_r = t_f \leq 2.5$ ns.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
t_{PHL}, t_{PLH}	propagation delay nAn to nBn	C_L = 50 pF; V_{CCB} = 4.5 V to 5.5 V; V_{CCA} = 3.0 V to 3.6 V	-	2.9	-	ns
	propagation delay nBn to nAn	C_L = 50 pF; V_{CCB} = 4.5 V to 5.5 V; V_{CCA} = 3.0 V to 3.6 V	-	2.5	-	ns
	propagation delay nAn to nBn	C_L = 50 pF; V_{CCB} = 3.0 V to 3.6 V; V_{CCA} = 2.3 V to 2.7 V	-	3.3	-	ns
	propagation delay nBn to nAn	C_L = 50 pF; V_{CCB} = 3.0 V to 3.6 V; V_{CCA} = 2.3 V to 2.7 V	-	3.0	-	ns
C_I	input capacitance		-	4.0	-	pF
$C_{I/O}$	input/output capacitance A and B port		-	5.0	-	pF
C_{PD}	power dissipation capacitance 5 V port: nAn to nBn	V_{CCB} = 5 V; V_{CCA} = 3.3 V [1] [2]				
		outputs enabled	-	30	-	pF
		outputs disabled	-	15	-	pF
	power dissipation capacitance 3 V port: nBn to nA	V_{CCB} = 5 V; V_{CCA} = 3.3 V [1] [2]				
		outputs enabled	-	40	-	pF
		outputs disabled	-	5	-	pF

[1] C_{PD} is used to determine the dynamic power dissipation (P_D in μW).
$P_D = C_{PD} \times V_{CC}^2 \times f_i \times N + \Sigma(C_L \times V_{CC}^2 \times f_o)$ where:
f_i = input frequency in MHz;
f_o = output frequency in MHz;
C_L = output load capacitance in pF;
V_{CC} = supply voltage in Volts;
N = total load switching outputs;
$\Sigma(C_L \times V_{CC}^2 \times f_o)$ = sum of the outputs.

[2] The condition is V_I = GND to V_{CC}.

4. Ordering information

Table 2: Ordering information

Type number	Temperature range	Package		
		Name	Description	Version
74ALVC164245DGG	–40 °C to +125 °C	TSSOP48	plastic thin shrink small outline package; 48 leads; body width 6.1 mm	SOT362-1
74ALVC164245DL	–40 °C to +125 °C	SSOP48	plastic shrink small outline package; 48 leads; body width 7.5 mm	SOT370-1

5. Functional diagram

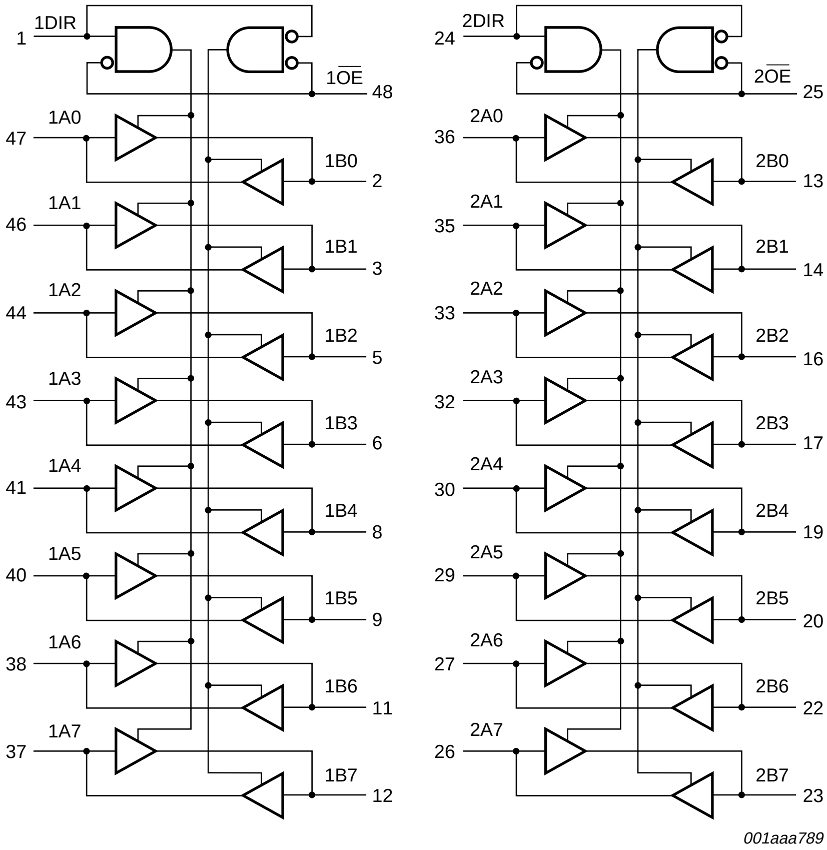

1DIR
1
1OE
48
1A0
47
1B0
2
1A1
46
1B1
3
1A2
44
1B2
5
1A3
43
1B3
6
1A4
41
1B4
8
1A5
40
1B5
9
1A6
38
1B6
11
1A7
37
1B7
12
2DIR
24
2OE
25
2A0
36
2B0
13
2A1
35
2B1
14
2A2
33
2B2
16
2A3
32
2B3
17
2A4
30
2B4
19
2A5
29
2B5
20
2A6
27
2B6
22
2A7
26
2B7
23
001aaa789

Fig 1. Logic symbol.

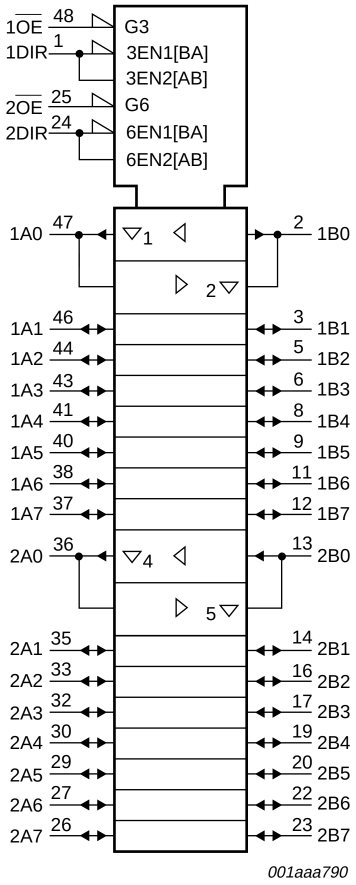

1OE 48
1DIR 1
2OE 25
2DIR 24
G3
3EN1[BA]
3EN2[AB]
G6
6EN1[BA]
6EN2[AB]
1A0 47
1
2
2 1B0
1A1 46
1A2 44
1A3 43
1A4 41
1A5 40
1A6 38
1A7 37
3 1B1
5 1B2
6 1B3
8 1B4
9 1B5
11 1B6
12 1B7
2A0 36
4
5
13 2B0
2A1 35
2A2 33
2A3 32
2A4 30
2A5 29
2A6 27
2A7 26
14 2B1
16 2B2
17 2B3
19 2B4
20 2B5
22 2B6
23 2B7
001aaa790

Fig 2. IEC logic symbol.

6. Pinning information

6.1 Pinning

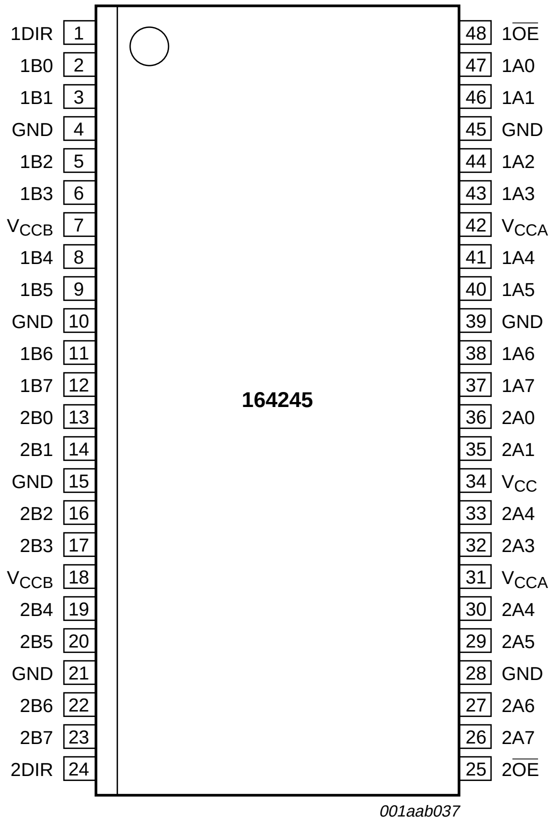

1DIR 1
1B0 2
1B1 3
GND 4
1B2 5
1B3 6
V_{CCB} 7
1B4 8
1B5 9
GND 10
1B6 11
1B7 12
2B0 13
2B1 14
GND 15
2B2 16
2B3 17
V_{CCB} 18
2B4 19
2B5 20
GND 21
2B6 22
2B7 23
2DIR 24
48 $1\overline{OE}$
47 1A0
46 1A1
45 GND
44 1A2
43 1A3
42 V_{CCA}
41 1A4
40 1A5
39 GND
38 1A6
37 1A7
36 2A0
35 2A1
34 V_{CC}
33 2A4
32 2A3
31 V_{CCA}
30 2A4
29 2A5
28 GND
27 2A6
26 2A7
25 $2\overline{OE}$
164245
001aab037

Fig 3. Pin configuration (T)SSOP48.

6.2 Pin description

Table 3: Pin description

Symbol	Pin	Description
1DIR	1	direction control input
1B0	2	data input/output
1B1	3	data input/output
GND	4, 10, 15, 21, 28, 34, 39, 45	ground (0 V)
1B2	5	data input/output
1B3	6	data input/output
V_{CCB}	7, 18	supply voltage (5 V bus)
1B4	8	data input/output
1B5	9	data input/output
1B6	11	data input/output
1B7	12	data input/output

Table 3: Pin description *…continued*

Symbol	Pin	Description
2B0	13	data input/output
2B1	14	data input/output
2B2	16	data input/output
2B3	17	data input/output
2B4	19	data input/output
2B5	20	data input/output
2B6	22	data input/output
2B7	23	data input/output
2DIR	24	direction control input
2$\overline{\text{OE}}$	25	output enable input (active LOW)
2A7	26	data input/output
2A6	27	data input/output
2A5	29	data input/output
2A4	30	data input/output
V_{CCA}	31, 42	supply voltage (3 V bus)
2A3	32	data input/output
2A2	33	data input/output
2A1	35	data input/output
2A0	36	data input/output
1A7	37	data input/output
1A6	38	data input/output
1A5	40	data input/output
1A4	41	data input/output
1A3	43	data input/output
1A2	44	data input/output
1A1	46	data input/output
1A0	47	data input/output
1$\overline{\text{OE}}$	48	output enable input (active LOW)
n.c.	-	not connected

7. Functional description

7.1 Function table

Table 4: Function table [1]

Inputs		**Outputs**	
n$\overline{\text{OE}}$	**nDIR**	**nAn**	**nBn**
L	L	A = B	inputs
L	H	inputs	B = A
H	X	Z	Z

[1] H = HIGH voltage level;
L = LOW voltage level;
X = don’t care;
Z = high-impedance OFF-state.

8. Limiting values

Table 5: Limiting values
In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to GND (ground = 0 V). See Table note 1.

Symbol	**Parameter**	**Conditions**		**Min**	**Max**	**Unit**
V_{CCB}	supply voltage B port	$V_{CCB} \geq V_{CCA}$		–0.5	+6.0	V
V_{CCA}	supply voltage A port	$V_{CCB} \geq V_{CCA}$		–0.5	+4.6	V
I_{IK}	input diode current	$V_I < 0$ V		-	–50	mA
V_I	input voltage		[2]	–0.5	+6.0	V
$V_{I/O}$	input voltage range for I/Os			–0.5	$V_{CC} + 0.5$	V
I_{OK}	output diode current	$V_O > V_{CC}$ or $V_O < 0$ V		-	±50	mA
V_O	output voltage	output HIGH or LOW state	[2]	–0.5	$V_{CC} + 0.5$	V
		output 3-state	[2]	–0.5	+6.0	V
I_O	output source or sink current	$V_O = 0$ V to V_{CC}		-	±50	mA
I_{CC}, I_{GND}	V_{CC} or GND current			-	±100	mA
T_{stg}	storage temperature			–65	+150	°C
P_{tot}	power dissipation					
	SSOP and TSSOP package	T_{amb} = –40 °C to +125 °C	[3]	-	500	mW

[1] The performance capability of a high-performance integrated circuit in conjunction with its thermal environment can create junction temperatures which are detrimental to reliability. The maximum junction temperature of this integrated circuit should not exceed 150 °C.

[2] The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

[3] For (T)SSOP48 packages: above 60 °C the value of P_{tot} derates linearly with 5.5 mW/K.

9. Recommended operating conditions

Table 6: Recommended operating conditions

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{CCB}	supply voltage B port	$V_{CCB} \geq V_{CCA}$				
		maximum speed performance	2.7	-	5.5	V
		low-voltage applications	1.5	-	5.5	V
V_{CCA}	supply voltage A port	$V_{CCB} \geq V_{CCA}$				
		maximum speed performance	2.7	-	3.6	V
		low-voltage applications	1.5	-	3.6	V
V_I	input voltage control inputs		0	-	5.5	V
$V_{I/O}$	input voltage					
	A port		0	-	V_{CCA}	V
	B port		0	-	V_{CCB}	V
V_O	output voltage					
	A port		0	-	V_{CCA}	V
	B port		0	-	V_{CCB}	V
T_{amb}	operating ambient temperature		–40	-	+125	°C
t_r, t_f	input rise and fall times	V_{CCA} = 2.7 V to 3.0 V	0	-	20	ns/V
		V_{CCA} = 3.0 V to 3.6 V	0	-	10	ns/V
		V_{CCB} = 3.0 V to 4.5 V	0	-	20	ns/V
		V_{CCB} = 4.5 V to 5.5 V	0	-	10	ns/V

10. Static characteristics

Table 7: Static characteristics

At recommended operating conditions; voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
T_{amb} = –40 °C to +85 °C [1]							
V_{IH}	HIGH-level input voltage						
	B port	V_{CCB} = 3.0 V to 5.5 V	[2]	2.0	-	-	V
	A port	V_{CCA} = 3.0 V to 3.6 V		2.0	-	-	V
		V_{CCA} = 2.3 V to 2.7 V	[2]	1.7	-	-	V
V_{IL}	LOW-level input voltage						
	B port	V_{CCB} = 4.5 V to 5.5 V	[2]	-	-	0.8	V
		V_{CCB} = 3.0 V to 3.6 V	[2]	-	-	0.7	V
	A port	V_{CCA} = 3.0 V to 3.6 V		-	-	0.8	V
		V_{CCA} = 2.3 V to 2.7 V	[2]	-	-	0.7	V

Table 7: Static characteristics *…continued*
At recommended operating conditions; voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
V_{OH}	HIGH-level output voltage						
	B port	$V_I = V_{IH}$ or V_{IL}					
		$I_O = -24$ mA; $V_{CCB} = 4.5$ V		$V_{CCB} - 0.8$	-	-	V
		$I_O = -12$ mA; $V_{CCB} = 4.5$ V		$V_{CCB} - 0.5$	-	-	V
		$I_O = -18$ mA; $V_{CCB} = 3.0$ V		$V_{CCB} - 0.8$	-	-	V
		$I_O = -100$ µA; $V_{CCB} = 3.0$ V		$V_{CCB} - 0.2$	V_{CCB}	-	V
	A port	$V_I = V_{IH}$ or V_{IL}					
		$I_O = -24$ mA; $V_{CCA} = 3.0$ V		$V_{CCA} - 0.7$	-	-	V
		$I_O = -100$ µA; $V_{CCA} = 3.0$ V		$V_{CCA} - 0.2$	-	-	V
		$I_O = -12$ mA; $V_{CCA} = 2.7$ V		$V_{CCA} - 0.5$	-	-	V
		$I_O = -8$ mA; $V_{CCA} = 2.3$ V		$V_{CCA} - 0.6$	-	-	V
		$I_O = -100$ µA; $V_{CCA} = 2.3$ V		$V_{CCA} - 0.2$	V_{CCA}	-	V
V_{OL}	LOW-level output voltage						
	B port	$V_I = V_{IH}$ or V_{IL}					
		$I_O = 24$ mA; $V_{CCB} = 4.5$ V		-	-	0.55	V
		$I_O = 12$ mA; $V_{CCB} = 4.5$ V		-	-	0.40	V
		$I_O = 100$ µA; $V_{CCB} = 4.5$ V		-	-	0.20	V
		$I_O = 18$ mA; $V_{CCB} = 3.0$ V		-	-	0.55	V
		$I_O = 100$ µA; $V_{CCB} = 3.0$ V		-	-	0.20	V
	A port	$V_I = V_{IH}$ or V_{IL}					
		$I_O = 24$ mA; $V_{CCA} = 3.0$ V		-	-	0.55	V
		$I_O = 100$ µA; $V_{CCA} = 3.0$ V		-	-	0.20	V
		$I_O = 12$ mA; $V_{CCA} = 2.7$ V		-	-	0.40	V
		$I_O = 12$ mA; $V_{CCA} = 2.3$ V		-	-	0.60	V
		$I_O = 100$ µA; $V_{CCA} = 2.3$ V		-	-	0.20	V
I_{LI}	input leakage current	$V_I = 5.5$ V or GND		-	±0.1	±5	µA
I_{OZ}	3-state output OFF-state current	$V_I = V_{IH}$ or V_{IL}; $V_O = V_{CC}$ or GND	[3]	-	±0.1	±10	µA
I_{CC}	quiescent supply current	$V_I = V_{CC}$ or GND; $I_O = 0$ A		-	0.1	40	µA
ΔI_{CC}	additional quiescent supply current per control pin	$V_I = V_{CC} - 0.6$ V; $I_O = 0$ A	[4]	-	5	500	µA
C_I	input capacitance			-	4.0	-	pF
$C_{I/O}$	input/output capacitance A and B port			-	5.0	-	pF
$T_{amb} = -40$ °C to +125 °C							
V_{IH}	HIGH-level input voltage						
	B port	$V_{CCB} = 3.0$ V to 5.5 V	[2]	2.0	-	-	V
	A port	$V_{CCA} = 3.0$ V to 3.6 V		2.0	-	-	V
		$V_{CCA} = 2.3$ V to 2.7 V	[2]	1.7	-	-	V

Table 7: Static characteristics *…continued*

At recommended operating conditions; voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{IL}	LOW-level input voltage					
	B port	V_{CCB} = 4.5 V to 5.5 V [2]	-	-	0.8	V
		V_{CCB} = 3.0 V to 3.6 V [2]	-	-	0.7	V
	A port	V_{CCA} = 3.0 V to 3.6 V	-	-	0.8	V
		V_{CCA} = 2.3 V to 2.7 V [2]	-	-	0.7	V
V_{OH}	HIGH-level output voltage					
	B port	$V_I = V_{IH}$ or V_{IL}				
		I_O = –24 mA; V_{CCB} = 4.5 V	V_{CCB} – 1.2	-	-	V
		I_O = –12 mA; V_{CCB} = 4.5 V	V_{CCB} – 0.8	-	-	V
		I_O = –18 mA; V_{CCB} = 3.0 V	V_{CCB} – 1.0	-	-	V
		I_O = –100 μA; V_{CCB} = 3.0 V	V_{CCB} – 0.3	V_{CCB}	-	V
	A port	$V_I = V_{IH}$ or V_{IL}				
		I_O = –24 mA; V_{CCA} = 3.0 V	V_{CCA} – 1.0	-	-	V
		I_O = –100 μA; V_{CCA} = 3.0 V	V_{CCA} – 0.3	-	-	V
		I_O = –12 mA; V_{CCA} = 2.7 V	V_{CCA} – 0.8	-	-	V
		I_O = –8 mA; V_{CCA} = 2.3 V	V_{CCA} – 0.6	-	-	V
		I_O = –100 μA; V_{CCA} = 2.3 V	V_{CCA} – 0.3	V_{CCA}	-	V
V_{OL}	LOW-level output voltage					
	B port	$V_I = V_{IH}$ or V_{IL}				
		I_O = 24 mA; V_{CCB} = 4.5 V	-	-	0.60	V
		I_O = 12 mA; V_{CCB} = 4.5 V	-	-	0.80	V
		I_O = 100 μA; V_{CCB} = 4.5 V	-	-	0.30	V
		I_O = 18 mA; V_{CCB} = 3.0 V	-	-	0.80	V
		I_O = 100 μA; V_{CCB} = 3.0 V	-	-	0.30	V
	A port	$V_I = V_{IH}$ or V_{IL}				
		I_O = 24 mA; V_{CCA} = 3.0 V	-	-	0.80	V
		I_O = 100 μA; V_{CCA} = 3.0 V	-	-	0.30	V
		I_O = 12 mA; V_{CCA} = 2.7 V	-	-	0.60	V
		I_O = 12 mA; V_{CCA} = 2.3 V	-	-	0.60	V
		I_O = 100 μA; V_{CCA} = 2.3 V	-	-	0.20	V
I_{LI}	input leakage current	V_I = 5.5 V or GND	-	±0.1	±10	μA
I_{OZ}	3-state output OFF-state current	$V_I = V_{IH}$ or V_{IL}; $V_O = V_{CC}$ or GND [3]	-	±0.1	±20	μA
I_{CC}	quiescent supply current	$V_I = V_{CC}$ or GND; I_O = 0 A	-	0.1	80	μA
ΔI_{CC}	additional quiescent supply current per control pin	$V_I = V_{CC}$ – 0.6 V; I_O = 0 A [4]	-	5	5000	μA

[1] All typical values are measured at V_{CCB} = 5.0 V, V_{CCA} = 3.3 V and T_{amb} = 25 °C.

[2] If V_{CCA} < 2.7 V, the switching levels at all inputs are not TTL compatible.

[3] For transceivers, the parameter I_{OZ} includes the input leakage current.

[4] V_{CCA} = 2.7 V to 3.6 V: other inputs at V_{CCA} or GND; V_{CCB} = 4.5 V to 5.5 V: other inputs at V_{CCB} or GND.

11. Dynamic characteristics

Table 8: Dynamic characteristics
$GND = 0$ V; $t_r = t_f \leq 2.5$ ns; $C_L = 50$ pF; see Figure 6.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
T_{amb} = −40 °C to +85 °C [1]						
t_{PHL}, t_{PLH}	propagation delay nAn to nBn	see Figure 4				
		V_{CCA} = 2.3 V to 2.7 V; V_{CCB} = 3.0 V tot 3.6 V	1.5	3.3	7.6	ns
		V_{CCA} = 2.7 V; V_{CCB} = 4.5 V to 5.5 V	1.0	3.0	5.9	ns
		V_{CCA} = 3.0 V to 3.6 V; V_{CCB} = 4.5 V to 5.5 V	1.0	2.9	5.8	ns
	propagation delay nBn to nAn	see Figure 4				
		V_{CCA} = 2.3 V to 2.7 V; V_{CCB} = 3.0 V tot 3.6 V	1.0	3.0	7.6	ns
		V_{CCA} = 2.7 V; V_{CCB} = 4.5 V to 5.5 V	1.0	4.3	6.7	ns
		V_{CCA} = 3.0 V to 3.6 V; V_{CCB} = 4.5 V to 5.5 V	1.2	2.5	5.8	ns
t_{PZH}, t_{PZL}	3-state output enable time $n\overline{OE}$ to nBn	see Figure 5				
		V_{CCA} = 2.3 V to 2.7 V; V_{CCB} = 3.0 V tot 3.6 V	1.5	4.1	11.5	ns
		V_{CCA} = 2.7 V; V_{CCB} = 4.5 V to 5.5 V	1.5	3.6	9.2	ns
		V_{CCA} = 3.0 V to 3.6 V; V_{CCB} = 4.5 V to 5.5 V	1.0	3.2	8.9	ns
	3-state output enable time $n\overline{OE}$ to nAn	see Figure 5				
		V_{CCA} = 2.3 V to 2.7 V; V_{CCB} = 3.0 V tot 3.6 V	1.5	4.6	12.3	ns
		V_{CCA} = 2.7 V; V_{CCB} = 4.5 V to 5.5 V	1.5	4.3	9.3	ns
		V_{CCA} = 3.0 V to 3.6 V; V_{CCB} = 4.5 V to 5.5 V	1.0	3.2	8.9	ns
t_{PHZ}, t_{PLZ}	3-state output disable time $n\overline{OE}$ to nBn	see Figure 5				
		V_{CCA} = 2.3 V to 2.7 V; V_{CCB} = 3.0 V tot 3.6 V	2.0	2.7	10.5	ns
		V_{CCA} = 2.7 V; V_{CCB} = 4.5 V to 5.5 V	2.5	4.6	9.0	ns
		V_{CCA} = 3.0 V to 3.6 V; V_{CCB} = 4.5 V to 5.5 V	2.1	4.9	8.6	ns
	3-state output disable time $n\overline{OE}$ to nAn	see Figure 5				
		V_{CCA} = 2.3 V to 2.7 V; V_{CCB} = 3.0 V tot 3.6 V	1.0	2.7	9.3	ns
		V_{CCA} = 2.7 V; V_{CCB} = 4.5 V to 5.5 V	1.5	3.5	9.0	ns
		V_{CCA} = 3.0 V to 3.6 V; V_{CCB} = 4.5 V to 5.5 V	2.0	3.2	8.6	ns
C_{PD}	power dissipation capacitance 5 V port: nAn to nBn	V_{CCB} = 5 V; V_{CCA} = 3.3 V [2] [3]				
		outputs enabled	-	30	-	pF
		outputs disabled	-	15	-	pF
	power dissipation capacitance 3 V port: nBn to nA	V_{CCB} = 5 V; V_{CCA} = 3.3 V [2] [3]				
		outputs enabled	-	40	-	pF
		outputs disabled	-	5	-	pF

Table 8: Dynamic characteristics *...continued*

GND = 0 V; $t_r = t_f \leq 2.5$ ns; C_L = 50 pF; see Figure 6.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
T_{amb} = −40 °C to +125 °C						
t_{PHL}, t_{PLH}	propagation delay nAn to nBn	see Figure 4				
		V_{CCA} = 2.3 V to 2.7 V; V_{CCB} = 3.0 V tot 3.6 V	1.5	-	9.5	ns
		V_{CCA} = 2.7 V; V_{CCB} = 4.5 V to 5.5 V	1.0	-	7.5	ns
		V_{CCA} = 3.0 V to 3.6 V; V_{CCB} = 4.5 V to 5.5 V	1.0	-	7.5	ns
	propagation delay nBn to nAn	see Figure 4				
		V_{CCA} = 2.3 V to 2.7 V; V_{CCB} = 3.0 V tot 3.6 V	1.0	-	9.5	ns
		V_{CCA} = 2.7 V; V_{CCB} = 4.5 V to 5.5 V	1.0	-	8.5	ns
		V_{CCA} = 3.0 V to 3.6 V; V_{CCB} = 4.5 V to 5.5 V	1.2	-	7.5	ns
t_{PZH}, t_{PZL}	3-state output enable time n$\overline{\text{OE}}$ to nBn	see Figure 5				
		V_{CCA} = 2.3 V to 2.7 V; V_{CCB} = 3.0 V tot 3.6 V	1.5	-	14.5	ns
		V_{CCA} = 2.7 V; V_{CCB} = 4.5 V to 5.5 V	1.5	-	11.5	ns
		V_{CCA} = 3.0 V to 3.6 V; V_{CCB} = 4.5 V to 5.5 V	1.0	-	12.0	ns
	3-state output enable time n$\overline{\text{OE}}$ to nAn	see Figure 5				
		V_{CCA} = 2.3 V to 2.7 V; V_{CCB} = 3.0 V tot 3.6 V	1.5	-	15.5	ns
		V_{CCA} = 2.7 V; V_{CCB} = 4.5 V to 5.5 V	1.5	-	12.0	ns
		V_{CCA} = 3.0 V to 3.6 V; V_{CCB} = 4.5 V to 5.5 V	1.0	-	11.5	ns
t_{PHZ}, t_{PLZ}	3-state output disable time n$\overline{\text{OE}}$ to nBn	see Figure 5				
		V_{CCA} = 2.3 V to 2.7 V; V_{CCB} = 3.0 V tot 3.6 V	2.0	-	13.5	ns
		V_{CCA} = 2.7 V; V_{CCB} = 4.5 V to 5.5 V	2.5	-	11.5	ns
		V_{CCA} = 3.0 V to 3.6 V; V_{CCB} = 4.5 V to 5.5 V	2.1	-	11.0	ns
	3-state output disable time n$\overline{\text{OE}}$ to nAn	see Figure 5				
		V_{CCA} = 2.3 V to 2.7 V; V_{CCB} = 3.0 V tot 3.6 V	1.0	-	12.0	ns
		V_{CCA} = 2.7 V; V_{CCB} = 4.5 V to 5.5 V	1.5	-	11.5	ns
		V_{CCA} = 3.0 V to 3.6 V; V_{CCB} = 4.5 V to 5.5 V	2.0	-	11.0	ns

[1] All typical values are measured at nominal voltage for V_{CCB} and V_{CCA} and at T_{amb} = 25 °C.

[2] C_{PD} is used to determine the dynamic power dissipation (P_D in μW).

$P_D = C_{PD} \times V_{CC}^2 \times f_i \times N + \Sigma(C_L \times V_{CC}^2 \times f_o)$ where:

f_i = input frequency in MHz;

f_o = output frequency in MHz;

C_L = output load capacitance in pF;

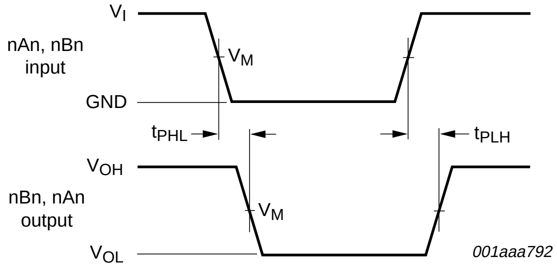
V_{CC} = supply voltage in Volts;

N = total load switching outputs;

$\Sigma(C_L \times V_{CC}^2 \times f_o)$ = sum of the outputs.

[3] The condition is V_I = GND to V_{CC}.

12. AC waveforms


V_I
nAn, nBn
input
V_M
GND
t_{PHL}
t_{PLH}
V_{OH}
nBn, nAn
output
V_M
V_{OL}
001aaa792

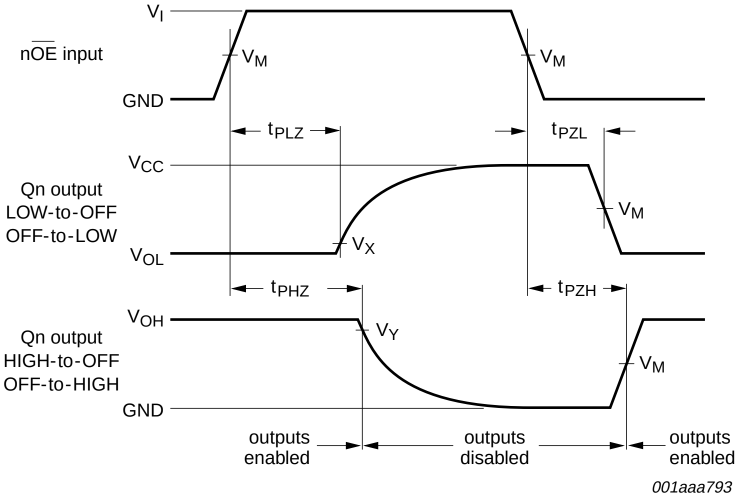
Measurement points are given in Table 9.

V_{OL} and V_{OH} are typical output voltage drop that occur with the output load.

Fig 4. **Input (nAn, nBn) to output (nBn, nAn) propagation delays.**

Table 9: Measurement points

Direction	**Supply voltage**		**Input**		**Output**
	V_{CCA}	V_{CCB}	V_I	V_M	V_M
A port to B port	2.3 V to 2.7 V	2.7 V to 3.6 V	V_{CCA}	$0.5 \times V_{CCA}$	1.5 V
B port to A port	2.3 V to 2.7 V	2.7 V to 3.6 V	2.7 V	1.5 V	$0.5 \times V_{CCA}$
A port to B port	2.7 V to 3.6 V	4.5 V to 5.5 V	2.7 V	1.5 V	$0.5 \times V_{CCB}$
B port to A port	2.7 V to 3.6 V	4.5 V to 5.5 V	3.0 V	1.5 V	1.5 V


V_I
$n\overline{OE}$ input
V_M
V_M
GND
t_{PLZ}
t_{PZL}
V_{CC}
Qn output
LOW-to-OFF
OFF-to-LOW
V_M
V_X
V_{OL}
t_{PHZ}
t_{PZH}
V_{OH}
V_Y
Qn output
HIGH-to-OFF
OFF-to-HIGH
V_M
GND
outputs
enabled
outputs
disabled
outputs
enabled
001aaa793

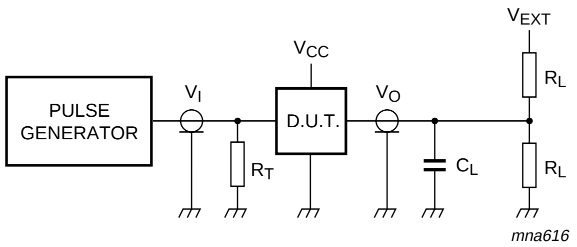
Measurement points are given in Table 10.

V_{OL} and V_{OH} are typical output voltage drop that occur with output load.

Fig 5. **3-state enable and disable times.**

Table 10: Measurement points

Direction	Supply voltage		Input		Output		
	V_{CCA}	V_{CCB}	V_I	V_M	V_M	V_X	V_Y
A port to B port	2.3 V to 2.7 V	2.7 V to 3.6 V	V_{CCA}	$0.5 \times V_{CCA}$	1.5 V	$V_{OL(B)} + 0.3$ V	$V_{OH(B)} - 0.3$ V
B port to A port	2.3 V to 2.7 V	2.7 V to 3.6 V	2.7 V	1.5 V	$0.5 \times V_{CCA}$	$V_{OL(A)} + 0.15$ V	$V_{OH(A)} - 0.15$ V
A port to B port	2.7 V to 3.6 V	4.5 V to 5.5 V	2.7 V	1.5 V	$0.5 \times V_{CCB}$	$0.2 \times V_{CCB}$	$0.8 \times V_{CCB}$
B port to A port	2.7 V to 3.6 V	4.5 V to 5.5 V	3.0 V	1.5 V	1.5 V	$V_{OL(A)} + 0.3$ V	$V_{OH(A)} - 0.3$ V



Test data is given in Table 11.

Definitions for test circuits:

R_L = Load resistor.

C_L = Load capacitance including jig and probe capacitance.

R_T = Termination resistance should be equal to the output impedance Z_o of the pulse generator.

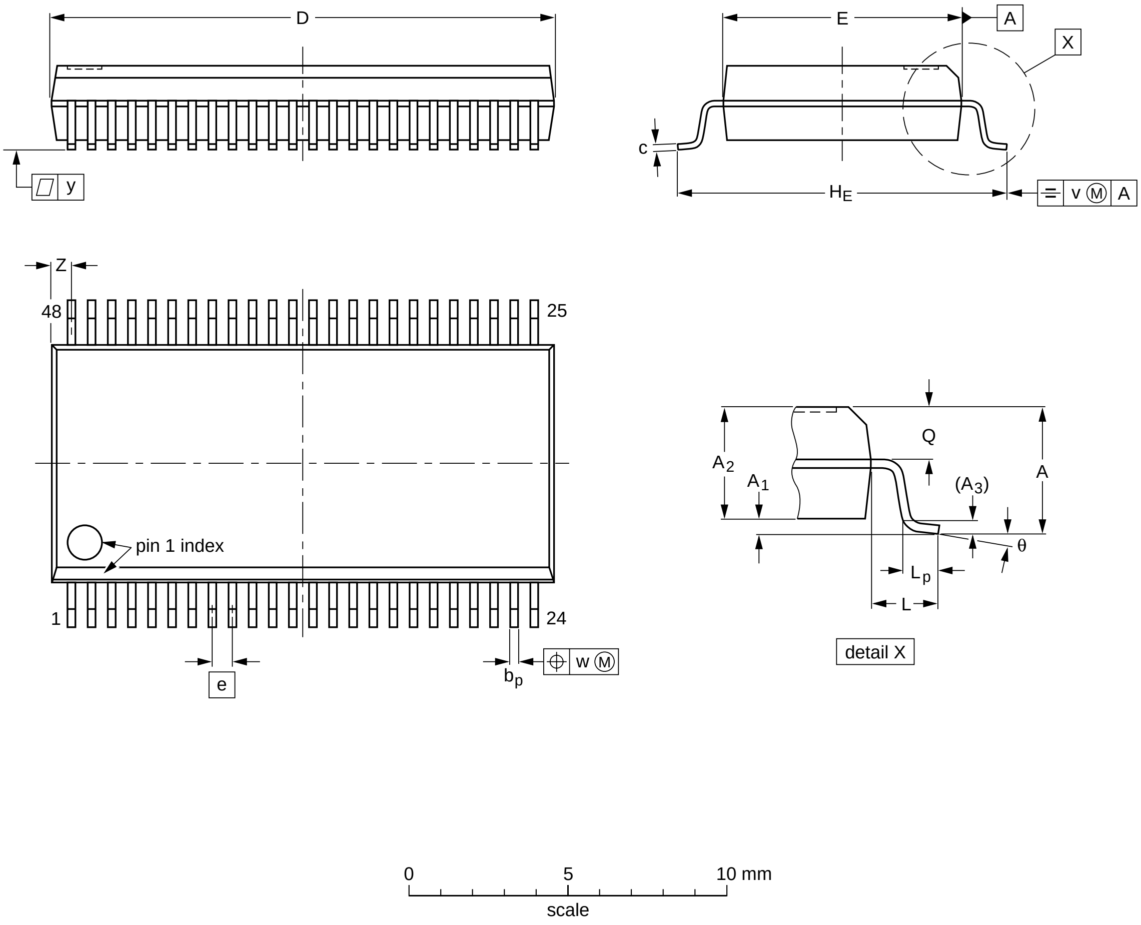
Fig 6. Load circuitry for switching times.

Table 11: Test data

Direction	Supply voltage		Load		V_{EXT}		
	V_{CCA}	V_{CCB}	C_L	R_L	t_{PLH}, t_{PHL}	t_{PZH}, t_{PHZ}	t_{PZL}, t_{PLZ}
A port to B port	2.3 V to 2.7 V	2.7 V to 3.6 V	50 pF	500 Ω	open	GND	$2 \times V_{CC}$
B port to A port	2.3 V to 2.7 V	2.7 V to 3.6 V	50 pF	500 Ω	open	GND	6.0 V
A port to B port	2.7 V to 3.6 V	4.5 V to 5.5 V	50 pF	500 Ω	open	GND	$2 \times V_{CC}$
B port to A port	2.7 V to 3.6 V	4.5 V to 5.5 V	50 pF	500 Ω	open	GND	6.0 V

13. Package outline

SSOP48: plastic shrink small outline package; 48 leads; body width 7.5 mm **SOT370-1**


D
y
E
A
X
c
H_E
v Ⓜ A
Z
48
25
pin 1 index
1
24
e
b_p
w Ⓜ
Q
A_2
A_1
(A_3)
A
θ
L_p
L
detail X
0
5
10 mm
scale

DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	D (1)	E (1)	e	H_E	L	L_p	Q	v	w	y	Z (1)	θ
mm	2.8	0.4 0.2	2.35 2.20	0.25	0.3 0.2	0.22 0.13	16.00 15.75	7.6 7.4	0.635	10.4 10.1	1.4	1.0 0.6	1.2 1.0	0.25	0.18	0.1	0.85 0.40	8° 0°

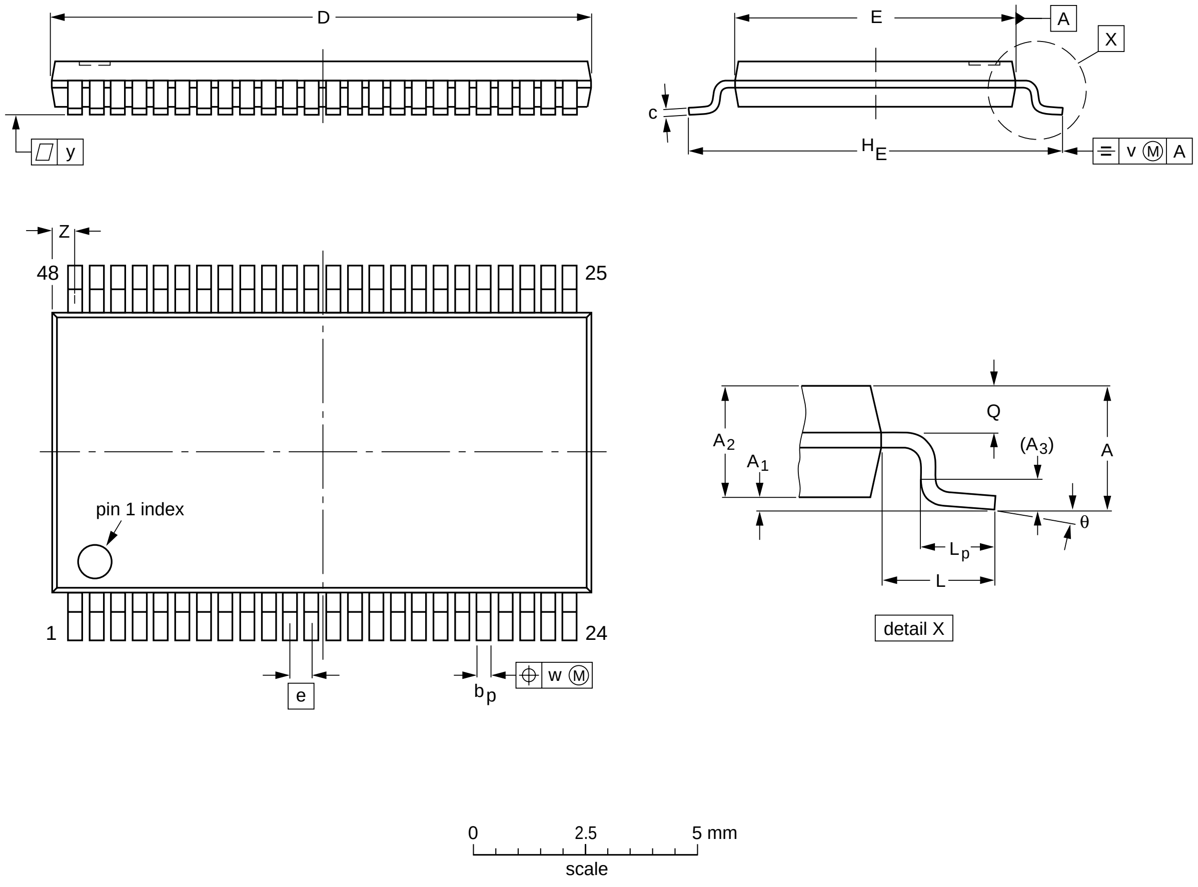
Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT370-1		MO-118				~~99-12-27~~ 03-02-19

Fig 7. Package outline SSOP48.

TSSOP48: plastic thin shrink small outline package; 48 leads; body width 6.1 mm **SOT362-1**



DIMENSIONS (mm are the original dimensions).

UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(2)}$	e	H_E	L	L_p	Q	v	w	y	Z	θ
mm	1.2	0.15 0.05	1.05 0.85	0.25	0.28 0.17	0.2 0.1	12.6 12.4	6.2 6.0	0.5	8.3 7.9	1	0.8 0.4	0.50 0.35	0.25	0.08	0.1	0.8 0.4	8° 0°

Notes

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.
2. Plastic interlead protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT362-1		MO-153				~~99-12-27~~ 03-02-19

Fig 8. Package outline TSSOP48.

14. Revision history

Table 12: Revision history

Document ID	Release date	Data sheet status	Change notice	Order number	Supersedes
74ALVC164245_2	20040601	Product data	-	9397 750 13248	74ALVC164245_1
Modifications:	• The format of this data sheet has been redesigned to comply with the current presentation and information standard of Philips Semiconductors. • Table 2: VFBGA56 type added • Table 7: Values for T_{amb} = –40 °C to +125 °C added • Table 8: Values for T_{amb} = –40 °C to +125 °C added				
74ALVC164245_1	19980826	Product specification	-	9397 750 04564	-

15. Data sheet status

Level	Data sheet status [1]	Product status [2] [3]	Definition
I	Objective data	Development	This data sheet contains data from the objective specification for product development. Philips Semiconductors reserves the right to change the specification in any manner without notice.
II	Preliminary data	Qualification	This data sheet contains data from the preliminary specification. Supplementary data will be published at a later date. Philips Semiconductors reserves the right to change the specification without notice, in order to improve the design and supply the best possible product.
III	Product data	Production	This data sheet contains data from the product specification. Philips Semiconductors reserves the right to make changes at any time in order to improve the design, manufacturing and supply. Relevant changes will be communicated via a Customer Product/Process Change Notification (CPCN).

[1] Please consult the most recently issued data sheet before initiating or completing a design.

[2] The product status of the device(s) described in this data sheet may have changed since this data sheet was published. The latest information is available on the Internet at URL http://www.semiconductors.philips.com.

[3] For data sheets describing multiple type numbers, the highest-level product status determines the data sheet status.

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Short-form specification — The data in a short-form specification is extracted from a full data sheet with the same type number and title. For detailed information see the relevant data sheet or data handbook.

Limiting values definition — Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 60134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.

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