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16-BIT 3.3-V TO 5-V LEVEL SHIFTING TRANSCEIVER WITH 3-STATE OUTPUTS

SCAS416F – MARCH 1994 – REVISED FEBRUARY 1999

- **Member of the Texas Instruments *Widebus*™ Family**
- ***EPIC*™ (Enhanced-Performance Implanted CMOS) Submicron Process**
- **Latch-Up Performance Exceeds 250 mA Per JESD 17**
- **Package Options Include Plastic 300-mil Shrink Small-Outline (DL) and Thin Shrink Small-Outline (DGG) Packages**

description

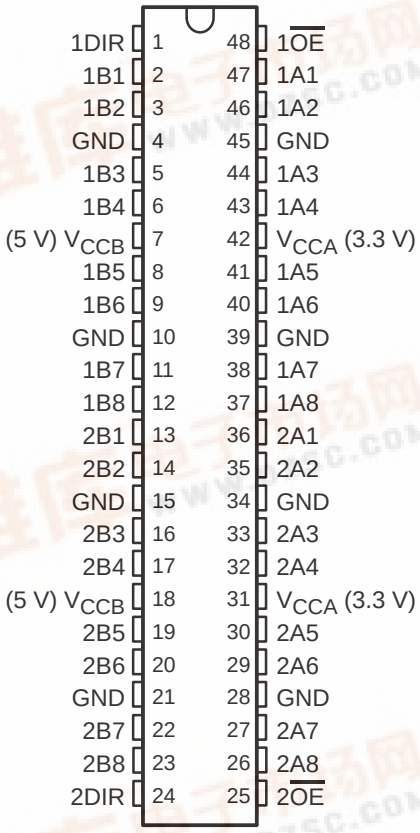
This 16-bit (dual-octal) noninverting bus transceiver contains two separate supply rails; B port has V_{CCB}, which is set at 5 V, and A port has V_{CCA}, which is set to operate at 3.3 V. This allows for translation from a 3.3-V to a 5-V environment and vice versa.

The SN74ALVC164245 is designed for asynchronous communication between data buses.

To ensure the high-impedance state during power up or power down, the output-enable ($\overline{OE}$) input should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

The SN74ALVC164245 is characterized for operation from –40°C to 85°C.

DGG OR DL PACKAGE
(TOP VIEW)



FUNCTION TABLE
(each 8-bit section)

INPUTS		OPERATION
$\overline{OE}$	DIR	
L	L	B data to A bus
L	H	A data to B bus
H	X	Isolation

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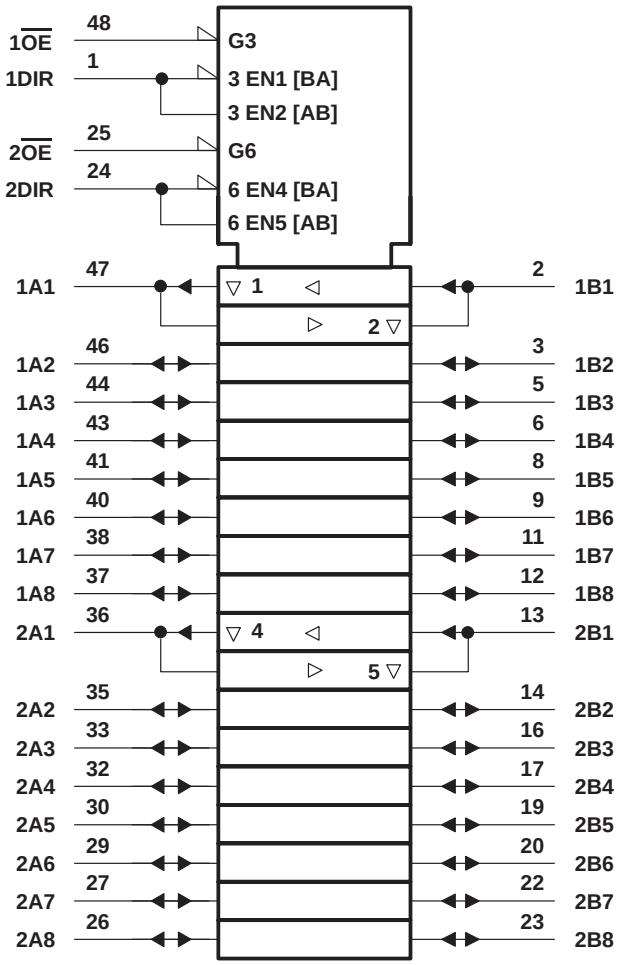
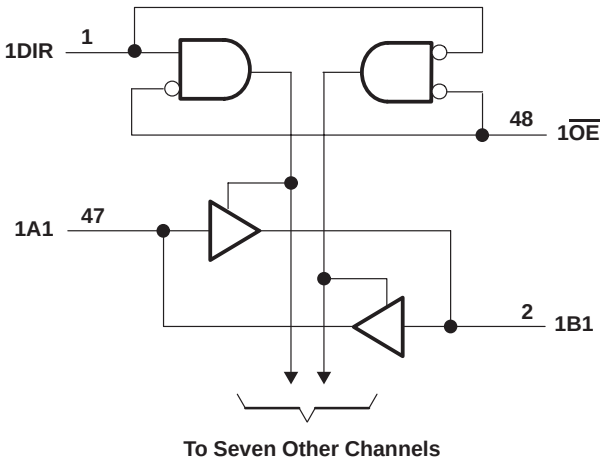
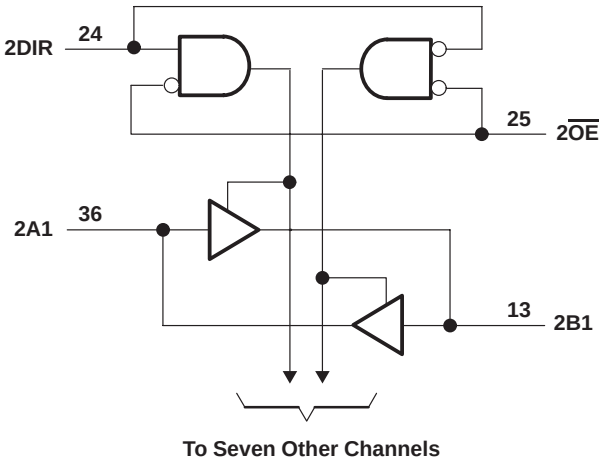
logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)





absolute maximum ratings over operating free-air temperature range for V_{CCB} at 5 V and V_{CCA} at 3.3 V (unless otherwise noted)†

Supply voltage range: V_{CCA} . . . . . –0.5 V to 4.6 V
V_{CCB} . . . . . –0.5 V to 6 V
Input voltage range, V_I: Except I/O ports (see Note 1) . . . . . –0.5 V to 6 V
I/O port A (see Note 2) . . . . . –0.5 V to V_{CCA} + 0.5 V
I/O port B (see Note 1) . . . . . –0.5 V to V_{CCB} + 0.5 V
Input clamp current, I_{IK} (V_I < 0) . . . . . –50 mA
Output clamp current, I_{OK} (V_O < 0) . . . . . –50 mA
Continuous output current, I_O . . . . . ±50 mA
Continuous current through each V_{CC} or GND . . . . . ±100 mA
Package thermal impedance, θ_{JA} (see Note 3): DGG package . . . . . 89°C/W
DL package . . . . . 94°C/W
Storage temperature range, T_{stg} . . . . . –65°C to 150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. This value is limited to 6 V maximum.
2. This value is limited to 4.6 V maximum.
3. The package thermal impedance is calculated in accordance with JESD 51.

recommended operating conditions for V_{CCB} at 5 V (see Note 4)

		MIN	MAX	UNIT
V_{CCB}	Supply voltage	4.5	5.5	V
V_{IH}	High-level input voltage	2		V
V_{IL}	Low-level input voltage		0.8	V
V_{IA}	Input voltage	0	V_{CCB}	V
V_{OB}	Output voltage	0	V_{CCB}	V
I_{OH}	High-level output current		–24	mA
I_{OL}	Low-level output current		24	mA
$\Delta t/\Delta v$	Input transition rise or fall rate		10	ns/V
T_A	Operating free-air temperature	–40	85	°C

NOTE 4: All unused inputs of the device must be held at the associated V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

recommended operating conditions for V_{CCA} at 3.3 V (see Note 4)

			MIN	MAX	UNIT
V_{CCA}	Supply voltage		2.7	3.6	V
V_{IH}	High-level input voltage	V_{CCA} = 2.7 V to 3.6 V	2		V
V_{IL}	Low-level input voltage	V_{CCA} = 2.7 V to 3.6 V		0.8	V
V_{IB}	Input voltage		0	V_{CCA}	V
V_{OA}	Output voltage		0	V_{CCA}	V
I_{OH}	High-level output current	V_{CCA} = 2.7 V		–12	mA
		V_{CCA} = 3 V		–24	
I_{OL}	Low-level output current	V_{CCA} = 2.7 V		12	mA
		V_{CCA} = 3 V		24	
$\Delta t/\Delta v$	Input transition rise or fall rate			10	ns/V
T_A	Operating free-air temperature		–40	85	°C

NOTE 4: All unused inputs of the device must be held at the associated V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

electrical characteristics over recommended operating free-air temperature range for V_{CCB} = 5 V (unless otherwise noted) (see Note 5)

PARAMETER		TEST CONDITIONS		V_{CCB}	MIN	TYP†	MAX	UNIT
V_{OH} (A to B)		I_{OH} = –100 µA		4.5 V	4.3			V
				5.5 V	5.3			
		I_{OH} = –24 mA		4.5 V	3.7			
				5.5 V	4.7			
V_{OL} (A to B)		I_{OL} = 100 µA		4.5 V			0.2	V
				5.5 V			0.2	
		I_{OL} = 24 mA		4.5 V			0.55	
				5.5 V			0.55	
I_I	Control inputs	V_I = V_{CCB} or GND		5.5 V			±5	µA
I_{OZ}‡	A or B ports	V_O = V_{CCB} or GND		5.5 V			±10	µA
I_{CC}		V_I = V_{CCB} or GND,	I_O = 0	5.5 V			40	µA
ΔI_{CC}§		One input at 3.4 V,	Other inputs at V_{CCB} or GND	4.5 V to 5.5 V			750	µA
C_i	Control inputs	V_I = V_{CCB} or GND		5 V		6.5		pF
C_{io}	A or B ports	V_O = V_{CCB} or GND		5 V		6.5		pF

† Typical values are measured at V_{CC} = 3.3 V, T_A = 25°C.
‡ For I/O ports, the parameter I_{OZ} includes the input leakage current.
§ This is the increase in supply current for each input that is at one of the specified TTL voltage levels rather than at 0 or the associated V_{CC}.
NOTE 5: V_{CCA} = 2.7 V to 3.6 V

electrical characteristics over recommended operating free-air temperature range for V_{CCA} = 3.3 V (unless otherwise noted) (see Note 6)

PARAMETER		TEST CONDITIONS		V_{CCA}	MIN	TYP†	MAX	UNIT
V_{OH} (B to A)		I_{OH} = –100 µA		2.7 V to 3.6 V	V_{CC}–0.2			V
		I_{OH} = –12 mA		2.7 V	2.2			
				3 V	2.4			
		I_{OH} = –24 mA		3 V	2			
V_{OL} (B to A)		I_{OL} = 100 µA		2.7 V to 3.6 V			0.2	V
		I_{OL} = 12 mA		2.7 V			0.4	
		I_{OL} = 24 mA		3 V			0.55	
I_I	Control inputs	$V_I = V_{CCA}$ or GND		3.6 V			±5	µA
I_{OZ}‡		$V_O = V_{CCA}$ or GND		3.6 V			±10	µA
I_{CC}		$V_I = V_{CCA}$ or GND,	I_O = 0	3.6 V			40	µA
ΔI_{CC}§		One input at V_{CCA} – 0.6 V,	Other inputs at V_{CCA} or GND	3 V to 3.6 V			750	µA
C_i	Control inputs	$V_I = V_{CCA}$ or GND		3.3 V		6.5		pF
C_{io}	A or B ports	$V_O = V_{CCA}$ or GND		3.3 V		8.5		pF

† Typical values are measured at V_{CC} = 3.3 V, T_A = 25°C.
‡ For I/O ports, the parameter I_{OZ} includes the input leakage current.
§ This is the increase in supply current for each input that is at one of the specified TTL voltage levels rather than at 0 or the associated V_{CC}.
NOTE 6: V_{CCB} = 5 V ± 0.5 V

switching characteristics over recommended operating free-air temperature range, C_L = 50 pF (unless otherwise noted) (see Figures 1 and 2)

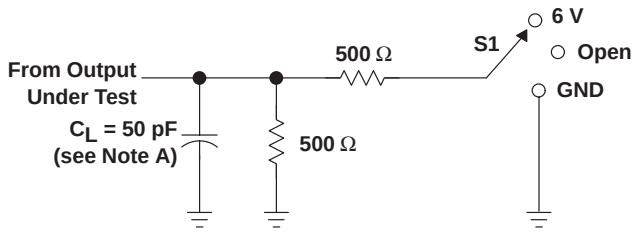
PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CCB} = 5 V ± 0.5 V				UNIT
			V_{CCA} = 2.7 V		V_{CCA} = 3.3 V ± 0.3 V		
			MIN	MAX¶	MIN¶	MAX¶	
t_{pd}	A	B		5.9	1	5.8	ns
	B	A		6.7	1.2	5.8	
t_{en}	$\overline{OE}$	B		9.3	1	8.9	ns
t_{dis}	$\overline{OE}$	B		9.2	2.1	9.5	ns
t_{en}	$\overline{OE}$	A		10.2	2	9.1	ns
t_{dis}	$\overline{OE}$	A		9	2.9	8.6	ns

¶ This limit can vary among suppliers.

operating characteristics, T_A = 25°C

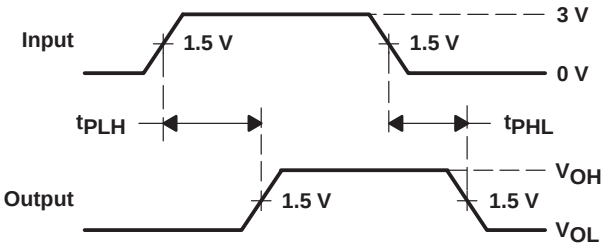
PARAMETER			TEST CONDITIONS	V_{CCA} = 3.3 V, V_{CCB} = 5 V	UNIT
				TYP	
C_{pd}	Power dissipation capacitance	Outputs enabled (A or B)	C_L = 50 pF, f = 10 MHz	56	pF
		Outputs disabled (A or B)		6	

PARAMETER MEASUREMENT INFORMATION
V_{CCA} = 2.7 V AND 3.3 V ± 0.3 V

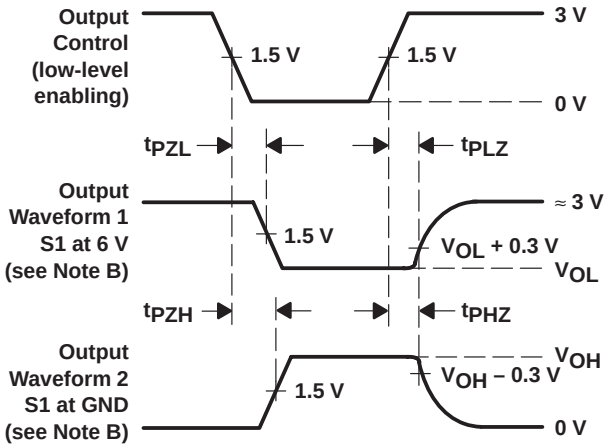


LOAD CIRCUIT

TEST	S1
t_{pd}	Open
t_{PLZ}/t_{PZL}	6 V
t_{PHZ}/t_{PZH}	GND



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES

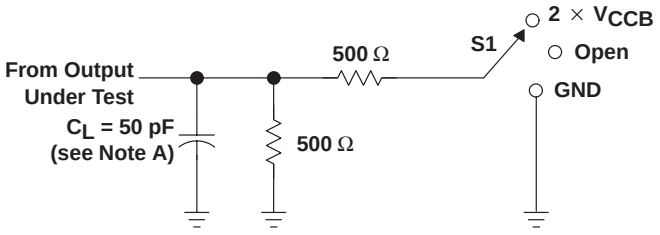


VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES

NOTES: A. C_L includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control.
Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r ≤ 2.5 ns, t_f ≤ 2.5 ns.
D. The outputs are measured one at a time with one transition per measurement.
E. t_{PLZ} and t_{PHZ} are the same as t_{dis}.
F. t_{PZL} and t_{PZH} are the same as t_{en}.
G. t_{PLH} and t_{PHL} are the same as t_{pd}.

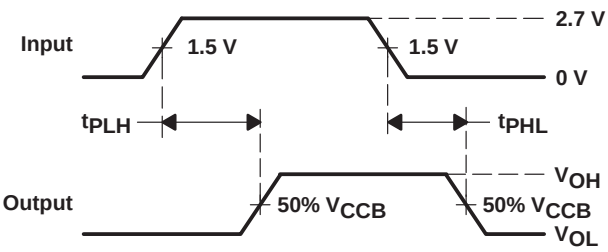
Figure 1. Load Circuit and Voltage Waveforms

PARAMETER MEASUREMENT INFORMATION
V_{CCB} = 5 V ± 0.5 V

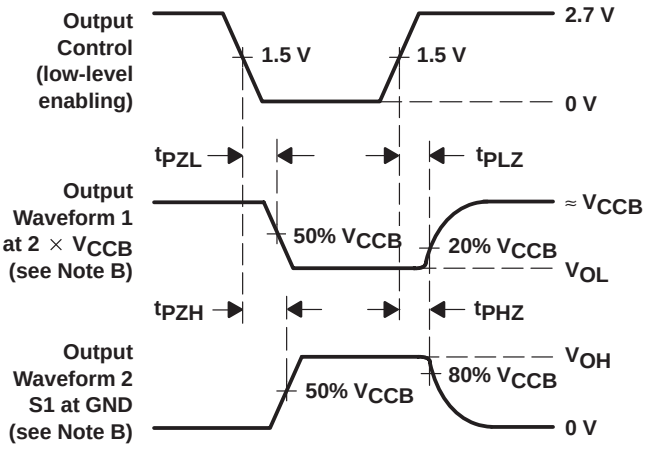


LOAD CIRCUIT

TEST	S1
t_{pd} t_{PLZ}/t_{PZL} t_{PHZ}/t_{PZH}	Open 2 × V_{CCB} GND



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES

NOTES: A. C_L includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r ≤ 2.5 ns, t_f ≤ 2.5 ns.
D. The outputs are measured one at a time with one transition per measurement.
E. t_{PLZ} and t_{PHZ} are the same as t_{dis}.
F. t_{PZL} and t_{PZH} are the same as t_{en}.
G. t_{PLH} and t_{PHL} are the same as t_{pd}.

Figure 2. Load Circuit and Voltage Waveforms

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