Integrated Device Technology, Inc.

# HIGH-SPEED 2K x 8 DUAL-PORT STATIC RAM

**IDT7132SA/LA**
**IDT7142SA/LA**

## FEATURES:

- High-speed access
  - — Military: 25/35/55/100ns (max.)
  - — Commercial: 25/35/55/100ns (max.)
  - — Commercial: 20ns only in PLCC for 7132
- Low-power operation
  - — IDT7132/42SA
    Active: 550mW (typ.)
    Standby: 5mW (typ.)
  - — IDT7132/42LA
    Active: 550mW (typ.)
    Standby: 1mW (typ.)
- Fully asynchronous operation from either port
- MASTER IDT7132 easily expands data bus width to 16-or-more bits using SLAVE IDT7142
- On-chip port arbitration logic (IDT7132 only)
- $\overline{BUSY}$ output flag on IDT7132; $\overline{BUSY}$ input on IDT7142
- Battery backup operation —2V data retention
- TTL-compatible, single 5V ±10% power supply
- Available in popular hermetic and plastic packages
- Military product compliant to MIL-STD, Class B
- Standard Military Drawing # 5962-87002
- Industrial temperature range (–40°C to +85°C) is available, tested to miliary electrical specifications

## DESCRIPTION:

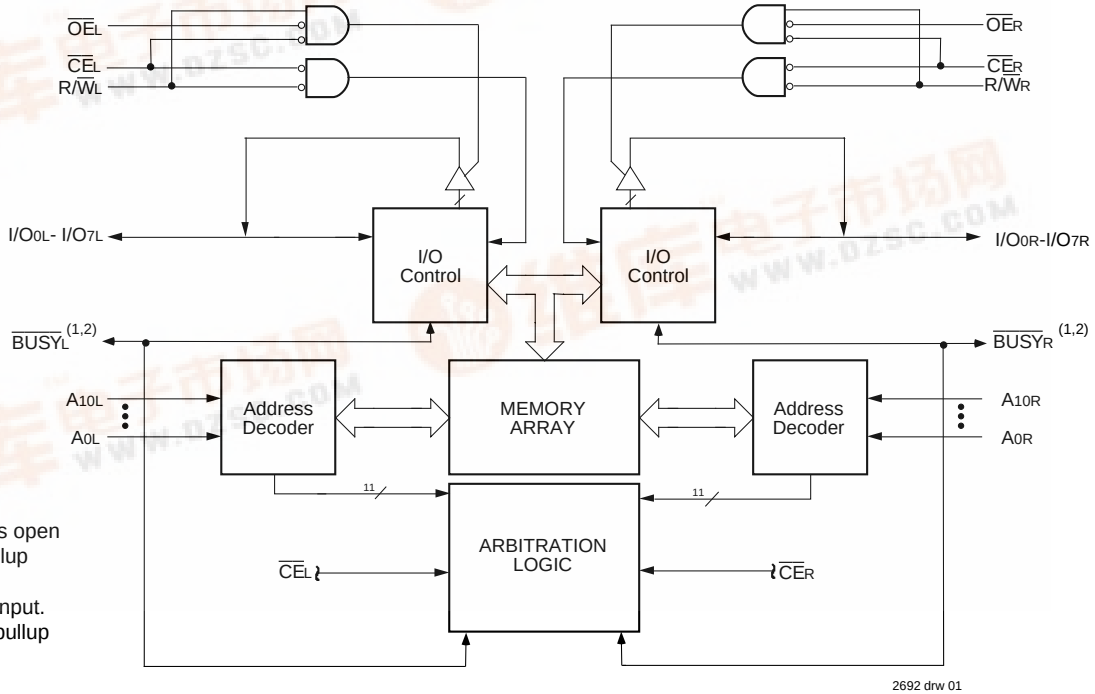
The IDT7132/IDT7142 are high-speed 2K x 8 Dual-Port Static RAMs. The IDT7132 is designed to be used as a stand-alone 8-bit Dual-Port RAM or as a "MASTER" Dual-Port RAM together with the IDT7142 "SLAVE" Dual-Port in 16-bit-or-more word width systems. Using the IDT MASTER/SLAVE Dual-Port RAM approach in 16-or-more-bit memory system applications results in full-speed, error-free operation without the need for additional discrete logic.

Both devices provide two independent ports with separate control, address, and I/O pins that permit independent, asynchronous access for reads or writes to any location in memory. An automatic power down feature, controlled by $\overline{CE}$ permits the on-chip circuitry of each port to enter a very low standby power mode.

Fabricated using IDT's CMOS high-performance technology, these devices typically operate on only 550mW of power. Low-power (LA) versions offer battery backup data retention capability, with each Dual-Port typically consuming 200µW from a 2V battery.

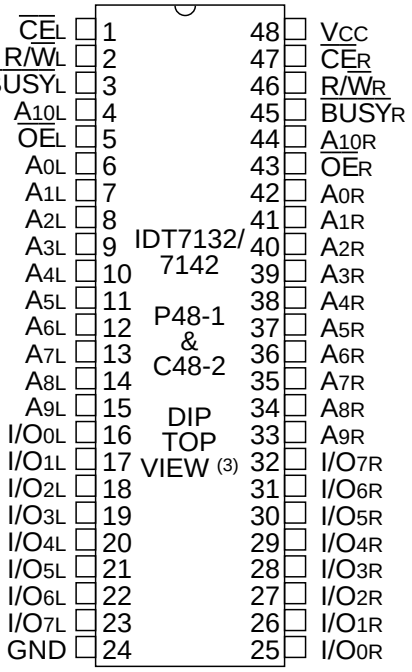
The IDT7132/7142 devices are packaged in a 48-pin sidebraze or plastic DIPs, 48-pin LCCs, 52-pin PLCCs, and 48-lead flatpacks. Military grade product is manufactured in compliance with the latest revision of MIL-STD-883, Class B, making it ideally suited to military temperature applications demanding the highest level of performance and reliability.

## FUNCTIONAL BLOCK DIAGRAM

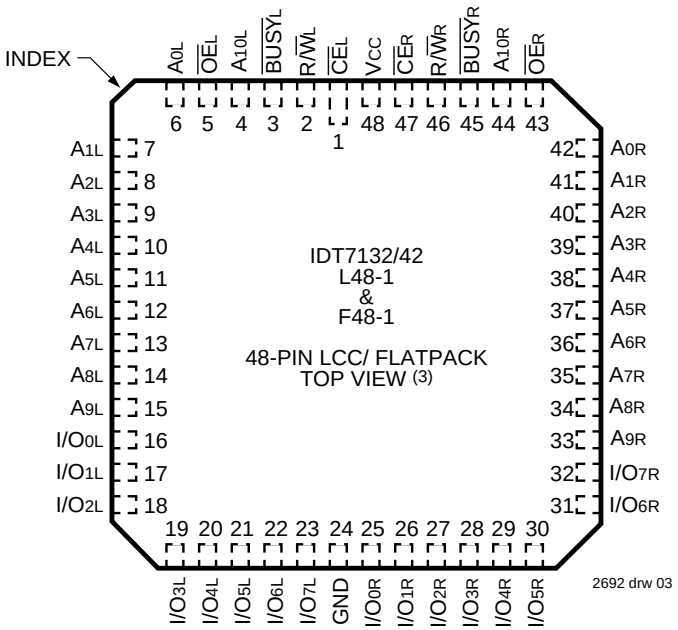



**NOTES:**
1. IDT7132 (MASTER): $\overline{BUSY}$ is open drain output and requires pullup resistor of 270Ω.
   IDT7142 (SLAVE): $\overline{BUSY}$ is input.
2. Open drain output: requires pullup resistor of 270Ω.

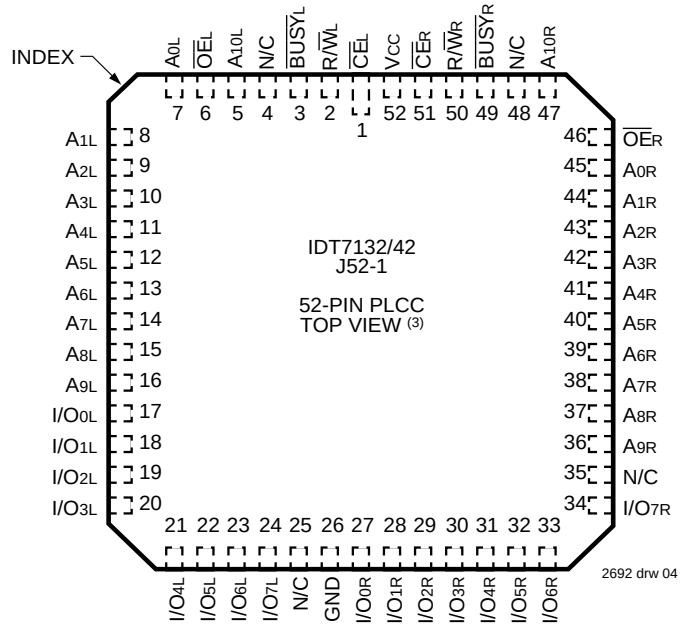
## PIN CONFIGURATIONS (1,2)




2692 drw 02




2692 drw 03




2692 drw 04

**NOTES:**
1. All Vcc pins must be connected to the power supply.
2. All GND pins must be connected to the ground supply.
3. This text does not indicate orientation of the actual part-marking.

## ABSOLUTE MAXIMUM RATINGS(1)

| Symbol | Rating | Commercial | Military | Unit |
|---|---|---|---|---|
| $V_{TERM}$(2) | Terminal Voltage with Respect to GND | -0.5 to +7.0 | -0.5 to +7.0 | V |
| $T_A$ | Operating Temperature | 0 to +70 | -55 to +125 | °C |
| $T_{BIAS}$ | Temperature Under Bias | -55 to +125 | -65 to +135 | °C |
| $T_{STG}$ | Storage Temperature | -55 to +125 | -65 to +150 | °C |
| $I_{OUT}$ | DC Output Current | 50 | 50 | mA |

2692 tbl 01

**NOTES:**
1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
2. $V_{TERM}$ must not exceed Vcc + 0.5V for more than 25% of the cycle time or 10ns maximum, and is limited to ≤ 20mA for the period of VTERM ≥ Vcc + 0.5V.

## RECOMMENDED OPERATING TEMPERATURE AND SUPPLY VOLTAGE

| Grade | Ambient Temperature | GND | Vcc |
|---|---|---|---|
| Military | -55°C to +125°C | 0V | 5.0V ± 10% |
| Commercial | 0°C to +70°C | 0V | 5.0V ± 10% |

2692 tbl 02

## RECOMMENDED DC OPERATING CONDITIONS

| Symbol | Parameter | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|
| Vcc | Supply Voltage | 4.5 | 5.0 | 5.5 | V |
| GND | Supply Voltage | 0 | 0 | 0 | V |
| $V_{IH}$ | Input High Voltage | 2.2 | — | 6.0(2) | V |
| $V_{IL}$ | Input Low Voltage | -0.5(1) | — | 0.8 | V |

2692 tbl 03

**NOTES:**
1. $V_{IL}$ (min.) = -1.5V for pulse width less than 10ns.
2. $V_{TERM}$ must not exceed Vcc + 0.5V.

## DC ELECTRICAL CHARACTERISTICS OVER THE OPERATING TEMPERATURE AND SUPPLY VOLTAGE RANGE[1,6] ($V_{CC}$ = 5.0V ± 10%)

| Symbol | Parameter | Test Conditions | Version | | 7132X20[2] Typ. | 7132X20[2] Max. | 7132X25[3] 7142X25[3] Typ. | 7132X25[3] 7142X25[3] Max. | 7132X35 7142X35 Typ. | 7132X35 7142X35 Max. | 7132X55 7142X55 Typ. | 7132X55 7142X55 Max. | 7132X100 7142X100 Typ. | 7132X100 7142X100 Max. | Unit |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| $I_{CC}$ | Dynamic Operating Current (Both Ports Active) | $\overline{CE}_L$ and $\overline{CE}_R$ = $V_{IL}$, Outputs open, f = $f_{MAX}$[4] | MIL. | SA | — | — | 110 | 280 | 80 | 230 | 65 | 190 | 65 | 190 | mA |
| | | | | LA | — | — | 110 | 220 | 80 | 170 | 65 | 140 | 65 | 140 | |
| | | | COM'L. | SA | 110 | 250 | 110 | 220 | 80 | 165 | 65 | 155 | 65 | 155 | |
| | | | | LA | 110 | 200 | 110 | 170 | 80 | 120 | 65 | 110 | 65 | 110 | |
| $I_{SB1}$ | Standby Current (Both Ports - TTL Level Inputs) | $\overline{CE}_L$ and $\overline{CE}_R$ = $V_{IH}$, f = $f_{MAX}$[4] | MIL. | SA | — | — | 30 | 80 | 25 | 80 | 20 | 65 | 20 | 65 | mA |
| | | | | LA | — | — | 30 | 60 | 25 | 60 | 20 | 45 | 20 | 45 | |
| | | | COM'L. | SA | 30 | 65 | 30 | 65 | 25 | 65 | 20 | 65 | 20 | 55 | |
| | | | | LA | 30 | 45 | 30 | 45 | 25 | 45 | 20 | 35 | 20 | 35 | |
| $I_{SB2}$ | Standby Current (One Port - TTL Level Inputs) | $\overline{CE}_{"A"}$ = $V_{IL}$ and $\overline{CE}_{"B"}$ = $V_{IH}$ [7] Active Port Outputs Open, f = $f_{MAX}$[4] | MIL. | SA | — | — | 65 | 160 | 50 | 150 | 40 | 125 | 40 | 125 | mA |
| | | | | LA | — | — | 65 | 125 | 50 | 115 | 40 | 90 | 40 | 90 | |
| | | | COM'L. | SA | 65 | 165 | 65 | 150 | 50 | 125 | 40 | 110 | 40 | 110 | |
| | | | | LA | 65 | 125 | 65 | 115 | 50 | 90 | 40 | 75 | 40 | 75 | |
| $I_{SB3}$ | Full Standby Current (Both Ports - All CMOS Level Inputs | $\overline{CE}_L$ and $\overline{CE}_R \geq V_{CC}$ -0.2V, $V_{IN} \geq V_{CC}$ -0.2V or $V_{IN} \leq$ 0.2V, f = 0[5] | MIL. | SA | — | — | 1.0 | 30 | 1.0 | 30 | 1.0 | 30 | 1.0 | 30 | mA |
| | | | | LA | — | — | 0.2 | 10 | 0.2 | 10 | 0.2 | 10 | 0.2 | 10 | |
| | | | COM'L. | SA | 1.0 | 15 | 1.0 | 15 | 1.0 | 15 | 1.0 | 15 | 1.0 | 15 | |
| | | | | LA | 0.2 | 5 | 0.2 | 5 | 0.2 | 4 | 0.2 | 4 | 0.2 | 4 | |
| $I_{SB4}$ | Full Standby Current (One Port - All CMOS Level Inputs) | $\overline{CE}_{"A"} \leq$ 0.2V and $\overline{CE}_{"B"} \geq V_{CC}$ -0.2V[7] $V_{IN} \geq V_{CC}$ -0.2V or $V_{IN} \leq$ 0.2V, Active Port Outputs Open, f = $f_{MAX}$[4] | MIL. | SA | — | — | 60 | 155 | 45 | 145 | 40 | 110 | 40 | 110 | mA |
| | | | | LA | — | — | 60 | 115 | 45 | 105 | 40 | 85 | 40 | 80 | |
| | | | COM'L. | SA | 60 | 155 | 60 | 145 | 45 | 110 | 40 | 100 | 40 | 95 | |
| | | | | LA | 60 | 115 | 60 | 105 | 45 | 85 | 40 | 70 | 40 | 70 | |

**NOTES:**

2689 tbl 04

1. 'X' in part numbers indicates power rating (SA or LA).
2. Com'l Only, 0°C to +70°C temperature range. PLCC package only.
3. Not available in DIP packages.
4. At f = $f_{Max}$, address and control lines (except Output Enable) are cycling at the maximum frequency read cycle of 1/$t_{RC}$, and using "AC TEST CONDITIONS" of input levels of GND to 3V.
5. f = 0 means no address or control lines change. Applies only to inputs at CMOS level standby.
6. Vcc = 5V, $T_A$=+25°C for Typ. and is not production tested. $V_{CC\,DC}$ = 100mA (Typ.)
7. Port "A" may be either left or right port. Port "B" is opposite from port "A".

## DC ELECTRICAL CHARACTERISTICS OVER THE OPERATING TEMPERATURE AND SUPPLY VOLTAGE RANGE ($V_{CC}$ = 5.0V ± 10%)

| Symbol | Parameter | Test Conditions | 7132SA 7142SA Min. | 7132SA 7142SA Max. | 7132LA 7142LA Max. | 7132LA 7142LA Max. | Unit |
|---|---|---|---|---|---|---|---|
| $\|I_{LI}\|$ | Input Leakage Current[1] | $V_{CC}$ = 5.5V, $V_{IN}$ = 0V to $V_{CC}$ | — | 10 | — | 5 | µA |
| $\|I_{LO}\|$ | Output Leakage Current[1] | $V_{CC}$ = 5.5V, $\overline{CE}$ = $V_{IH}$, $V_{OUT}$ = 0V to $V_{CC}$ | — | 10 | — | 5 | µA |
| $V_{OL}$ | Output Low Voltage (I/O0-I/O7) | $I_{OL}$ = 4mA | — | 0.4 | — | 0.4 | V |
| $V_{OL}$ | Open Drain Output Low Voltage ($\overline{BUSY}$, $\overline{INT}$) | $I_{OL}$ = 16mA | — | 0.5 | — | 0.5 | V |
| $V_{OH}$ | Output High Voltage | $I_{OH}$ = -4mA | 2.4 | — | 2.4 | — | V |

**NOTE:**

2689 tbl 05

1. At Vcc ≤ 2.0V leakages are undefined.

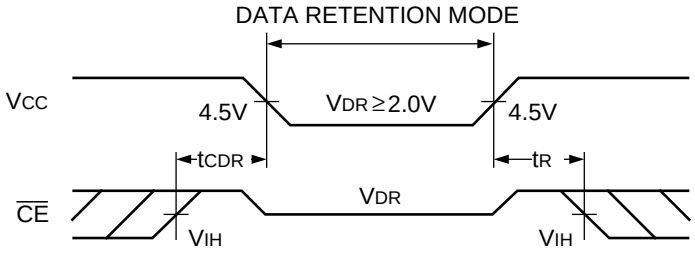
## DATA RETENTION CHARACTERISTICS (LA Version Only)

| Symbol | Parameter | Test Conditions | | IDT7132LA/IDT7142LA Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|---|
| $V_{DR}$ | $V_{CC}$ for Data Retention | | | 2.0 | — | — | V |
| $I_{CCDR}$ | Data Retention Current | $V_{CC}$ = 2.0V, $\overline{CE} \geq V_{CC}$ -0.2V | Mil. | — | 100 | 4000 | µA |
| | | $V_{IN} \geq V_{CC}$ -0.2V or $V_{IN} \leq 0.2V$ | Com'l. | — | 100 | 1500 | µA |
| $t_{CDR}$(3) | Chip Deselect to Data Retention Time | | | 0 | — | — | ns |
| $t_R$(3) | Operation Recovery Time | | | $t_{RC}$(2) | — | — | ns |

2692 tbl 06

**NOTES:**
1. $V_{CC}$ = 2V, $T_A$ = +25°C, and is not production tested.
2. $t_{RC}$ = Read Cycle Time
3. This parameter is guaranteed but not production tested.

## DATA RETENTION WAVEFORM




2692 drw 05

## AC TEST CONDITIONS

| | |
|---|---|
| Input Pulse Levels | GND TO 3.0V |
| Input Rise/Fall Times | 5ns |
| Input Timing Reference Levels | 1.5V |
| Output Reference Levels | 1.5V |
| Output Load | Figures 1, 2, and 3 |

2692 tbl 07

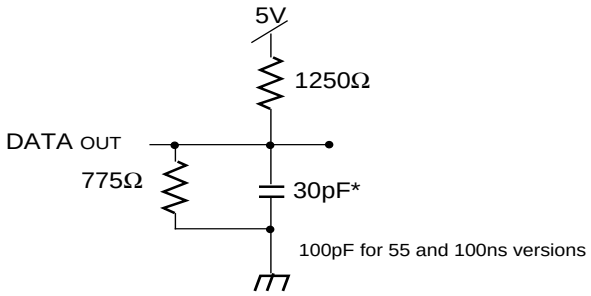
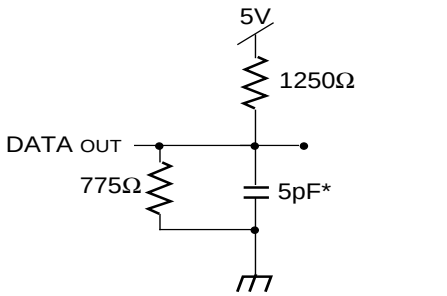



**Figure 1. AC Output Test Load**




2692 drw 06

**Figure 2. Output Test Load (for $t_{HZ}$, $t_{LZ}$, $t_{WZ}$, and $t_{OW}$)**
* Including scope and jig

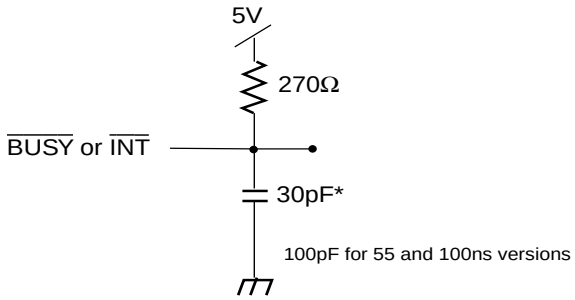



**Figure 3. $\overline{BUSY}$ and $\overline{INT}$ AC Output Test Load**

## AC ELECTRICAL CHARACTERISTICS OVER THE OPERATING TEMPERATURE AND SUPPLY VOLTAGE RANGE[3]

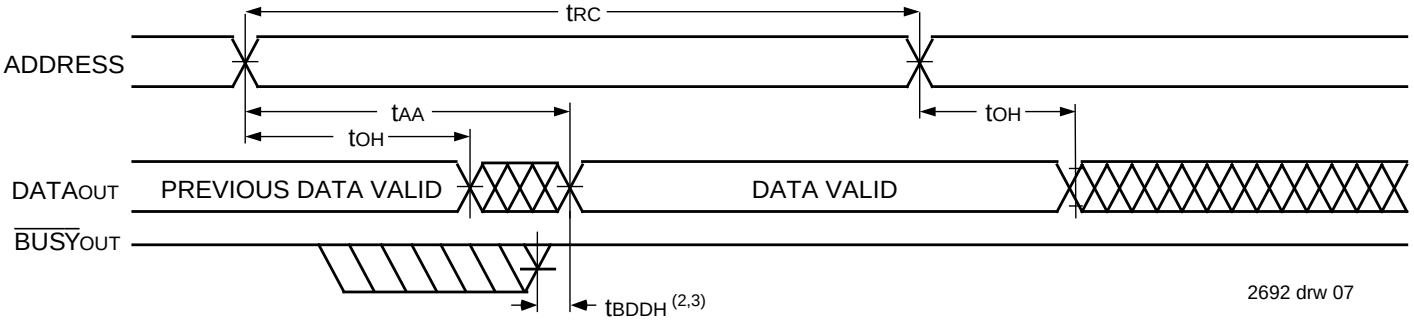
| Symbol | Parameter | 7132X20[2] Min. | 7132X20[2] Max. | 7132X25[5] 7142X25[5] Min. | 7132X25[5] 7142X25[5] Max. | 7132X35 7142X35 Min. | 7132X35 7142X35 Max. | 7132X55 7142X55 Min. | 7132X55 7142X55 Max. | 7132X100 7142X100 Min. | 7132X100 7142X100 Max. | Unit |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| **Read Cycle** | | | | | | | | | | | | |
| $t_{RC}$ | Read Cycle Time | 20 | — | 25 | — | 35 | — | 55 | — | 100 | — | ns |
| $t_{AA}$ | Address Access Time | — | 20 | — | 25 | — | 35 | — | 55 | — | 100 | ns |
| $t_{ACE}$ | Chip Enable Access Time | — | 20 | — | 25 | — | 35 | — | 55 | — | 100 | ns |
| $t_{AOE}$ | Output Enable Access Time | | 11 | — | 12 | — | 20 | — | 25 | — | 40 | ns |
| $t_{OH}$ | Output Hold From Address Change | 3 | — | 3 | — | 3 | — | 3 | — | 10 | — | ns |
| $t_{LZ}$ | Output Low-Z Time[1,4] | 0 | — | 0 | — | 0 | — | 5 | — | 5 | — | ns |
| $t_{HZ}$ | Output High-Z Time[1,4] | — | 10 | — | 10 | — | 15 | — | 25 | — | 40 | ns |
| $t_{PU}$ | Chip Enable to Power Up Time[4] | 0 | — | 0 | — | 0 | — | 0 | — | 0 | — | ns |
| $t_{PD}$ | Chip Disable to Power Down Time[4] | — | 20 | — | 25 | — | 35 | — | 50 | — | 50 | ns |

**NOTES:**

2689 tbl 08

1. Transition is measured ±500mV from Low or High-impedance voltage Output Test Load (Figure 2).
2. Com'l Only, 0°C to +70°C temperature range. PLCC package only.
3. "X" in part numbers indicates power rating (SA or LA).
4. This parameter is guaranteed by device characterization, but is not production tested.
5. Not available in DIP packages.

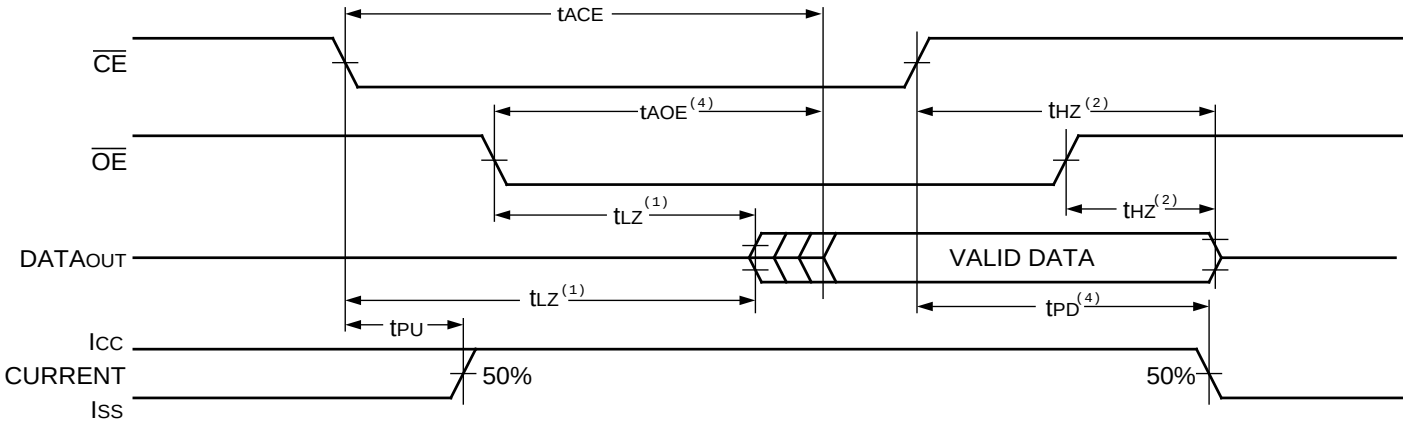
## TIMING WAVEFORM OF READ CYCLE NO. 1, EITHER SIDE[1]




**NOTES:**

1. R/$\overline{W}$ = $V_{IH}$, $\overline{CE}$ = $V_{IL}$, and is $\overline{OE}$ = $V_{IL}$. Address is valid prior to the coincidental with $\overline{CE}$ transition Low.
2. $t_{BDD}$ delay is required only in the case where the opposite port is completing a write operation to the same address location. For simultaneous read operations, $\overline{BUSY}$ has no relationship to valid output data.
3. Start of valid data depends on which timing becomes effective last $t_{AOE}$, $t_{ACE}$, $t_{AA}$, and $t_{BDD}$.

## TIMING WAVEFORM OF READ CYCLE NO. 2, EITHER SIDE (3)




2692 drw 08

**NOTES:**
1. Timing depends on which signal is asserted last, $\overline{OE}$ or $\overline{CE}$.
2. Timing depends on which signal is deasserted first, $\overline{OE}$ or $\overline{CE}$.
3. R/$\overline{W}$ = $V_{IH}$, and the address is valid prior to or coincidental with $\overline{CE}$ transition Low.
4. Start of valid data depends on which timing becomes effective last $t_{AOE}$, $t_{ACE}$, $t_{AA}$, and $t_{BDD}$.

## AC ELECTRICAL CHARACTERISTICS OVER THE OPERATING TEMPERATURE AND SUPPLY VOLTAGE RANGE(5)

| Symbol | Parameter | 7132X20(2) Min. | 7132X20(2) Max. | 7132X25(6) 7142X25(6) Min. | 7132X25(6) 7142X25(6) Max. | 7132X35 7142X35 Min. | 7132X35 7142X35 Max. | 7132X55 7142X55 Min. | 7132X55 7142X55 Max. | 7132X100 7142X100 Min. | 7132X100 7142X100 Max. | Unit |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| **Write Cycle** | | | | | | | | | | | | |
| $t_{WC}$ | Write Cycle Time(3) | 20 | — | 25 | — | 35 | — | 55 | — | 100 | — | ns |
| $t_{EW}$ | Chip Enable to End of Write | 15 | — | 20 | — | 30 | — | 40 | — | 90 | — | ns |
| $t_{AW}$ | Address Valid to End of Write | 15 | — | 20 | — | 30 | — | 40 | — | 90 | — | ns |
| $t_{AS}$ | Address Set-up Time | 0 | — | 0 | — | 0 | — | 0 | — | 0 | — | ns |
| $t_{WP}$ | Write Pulse Width(4) | 15 | — | 15 | — | 25 | — | 30 | — | 55 | — | ns |
| $t_{WR}$ | Write Recovery Time | 0 | — | 0 | — | 0 | — | 0 | — | 0 | — | ns |
| $t_{DW}$ | Data Valid to End of Write | 10 | — | 12 | — | 15 | — | 20 | — | 40 | — | ns |
| $t_{HZ}$ | Output High Z Time(1) | — | 10 | — | 10 | — | 15 | — | 25 | — | 40 | ns |
| $t_{DH}$ | Data Hold Time | 0 | — | 0 | — | 0 | — | 0 | — | 0 | — | ns |
| $t_{WZ}$ | Write Enabled to Output in High Z(1) | — | 10 | — | 10 | — | 15 | — | 30 | — | 40 | ns |
| $t_{OW}$ | Output Active From End of Write(1) | 0 | — | 0 | — | 0 | — | 0 | — | 0 | — | ns |

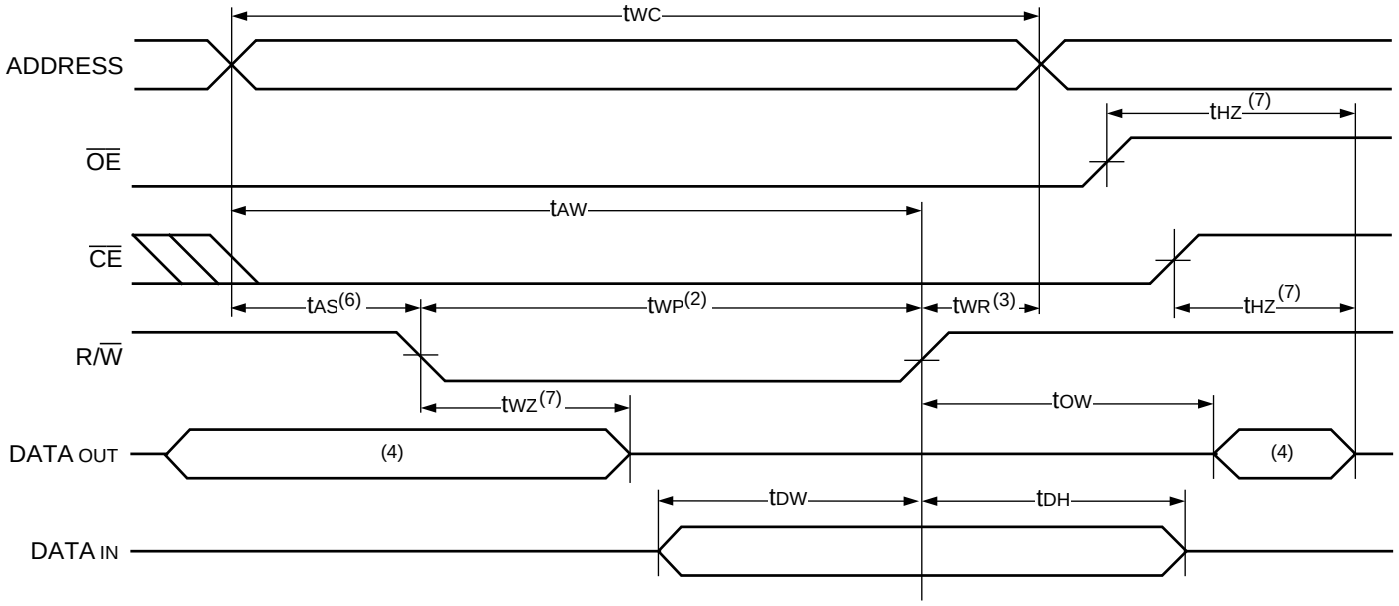
**NOTES:** 2692 tbl 09
1. Transition is measured ±500mV from Low or High-impedance voltage with Output Test Load (Figure 2). This parameter is guaranteed by device characterization but is not production tested.
2. 0°C to +70°C temperature range only, PLCC package only.
3. For Master/Slave combination, $t_{WC}$ = $t_{BAA}$ + $t_{WP}$, since R/$\overline{W}$ = $V_{IL}$ must occur after $t_{BAA}$.
4. If $\overline{OE}$ is low during a R/$\overline{W}$ controlled write cycle, the write pulse width must be the larger of $t_{WP}$ or ($t_{WZ}$ + $t_{DW}$) to allow the I/O drivers to turn off data to be placed on the bus for the required $t_{DW}$. If $\overline{OE}$ is High during a R/$\overline{W}$ controlled write cycle, this requirement does not apply and the write pulse can be as short as the specified $t_{WP}$.
5. "X" in part numbers indicates power rating (SA or LA).
6. Not available in DIP packages.

## CAPACITANCE(1) ($T_A$ = +25°C,f = 1.0MHz)

| Symbol | Parameter | Conditions(2) | Max. | Unit |
|---|---|---|---|---|
| $C_{IN}$ | Input Capacitance | $V_{IN}$ = 3dV | 11 | pF |
| $C_{OUT}$ | Output Capacitance | $V_{IN}$ = 3dV | 11 | pF |

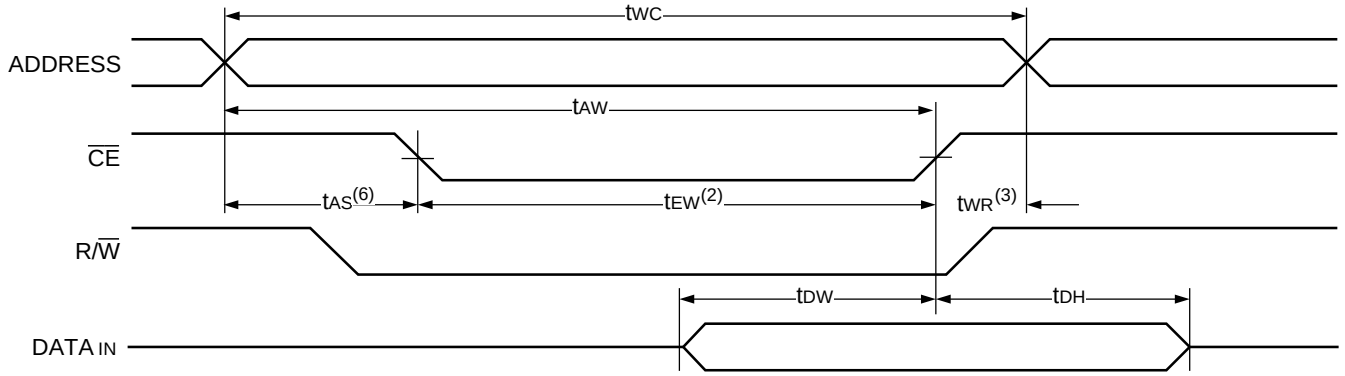
**NOTES:** 2692 tbl 10
1. This parameter is determined by device characterization but is not production tested.
2. 3dV represents the interpolated capacitance when the input and output r from 3V to 0V.

## TIMING WAVEFORM OF WRITE CYCLE NO. 1, (R/$\overline{W}$ CONTROLLED TIMING)(1,5,8)




2692 drw 09

## TIMING WAVEFORM OF WRITE CYCLE NO. 2, ($\overline{CE}$ CONTROLLED TIMING)(1,5)




2692 drw 10

**NOTES:**
1. R/$\overline{W}$ or $\overline{CE}$ must be High during all address transitions.
2. A write occurs during the overlap ($t_{EW}$ or $t_{WP}$) of $\overline{CE}$ = $V_{IL}$ and R/$\overline{W}$= $V_{IL}$.
3. $t_{WR}$ is measured from the earlier of $\overline{CE}$ or R/$\overline{W}$ going High to the end of the write cycle.
4. During this period, the I/O pins are in the output state and input signals must not be applied.
5. If the $\overline{CE}$ Low transition occurs simultaneously with or after the R/$\overline{W}$ Low transition, the outputs remain in the High-impedance state.
6. Timing depends on which enable signal ($\overline{CE}$ or R/$\overline{W}$) is asserted last.
7. This parameter is determined be device characterization, but is not production tested. Transition is measured +/- 500mV from steady state with the Output Test Load (Figure 2).
8. If $\overline{OE}$ is low during a R/$\overline{W}$ controlled write cycle, the write pulse width must be the larger of $t_{WP}$ or ($t_{WZ}$ + $t_{DW}$) to allow the I/O drivers to turn off data to be placed on the bus for the required $t_{DW}$. If $\overline{OE}$ is High during a R/$\overline{W}$ controlled write cycle, this requirement does not apply and the write pulse can be as short as the specified $t_{WP}$.

## AC ELECTRICAL CHARACTERISTICS OVER THE OPERATING TEMPERATURE AND SUPPLY VOLTAGE RANGE(7)

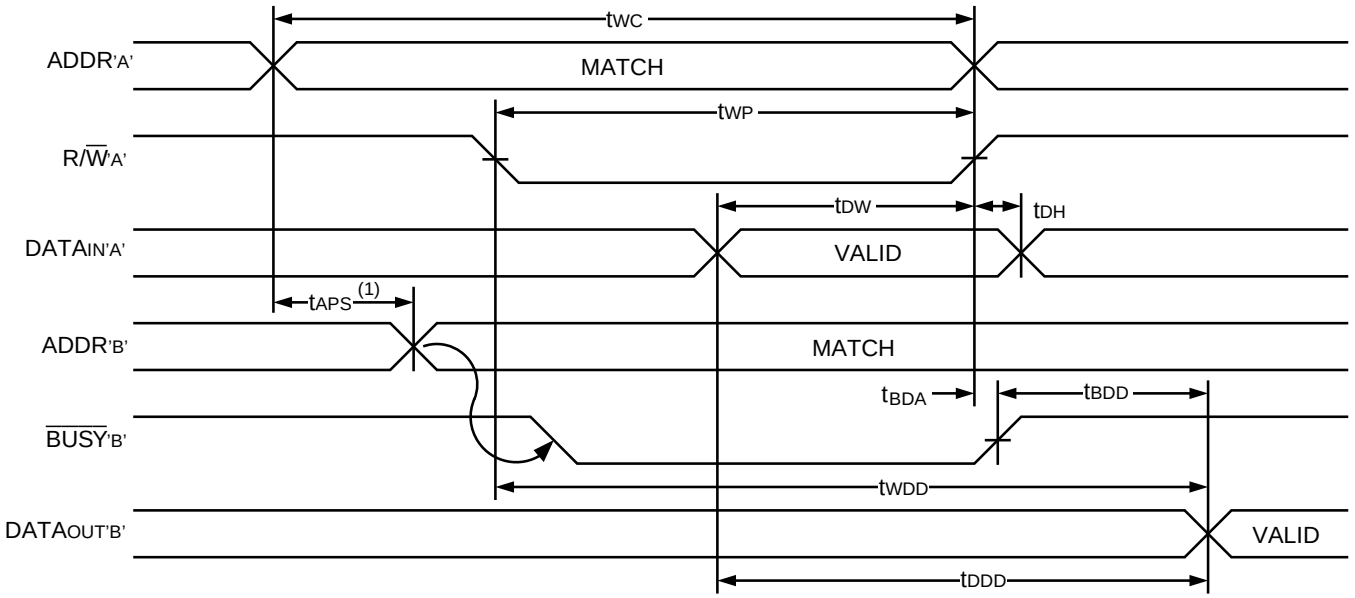
| Symbol | Parameter | 7132X20(1) Min. | 7132X20(1) Max. | 7132X25(8) 7142X25(8) Min. | 7132X25(8) 7142X25(8) Max. | 7132X35 7142X35 Min. | 7132X35 7142X35 Max. | 7132X55 7142X55 Min. | 7132X55 7142X55 Max. | 7132X100 7142X100 Min. | 7132X100 7142X100 Max. | Unit |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| **Busy Timing (For Master IDT7130 Only)** | | | | | | | | | | | | |
| $t_{BAA}$ | $\overline{BUSY}$ Access Time from Address | — | 20 | — | 20 | — | 20 | — | 30 | — | 50 | ns |
| $t_{BDA}$ | $\overline{BUSY}$ Disable Time from Address | — | 20 | — | 20 | — | 20 | — | 30 | — | 50 | ns |
| $t_{BAC}$ | $\overline{BUSY}$ Access Time from Chip Enable | — | 20 | — | 20 | — | 20 | — | 30 | — | 50 | ns |
| $t_{BDC}$ | $\overline{BUSY}$ Disable Time from Chip Enable | — | 20 | — | 20 | — | 20 | — | 30 | — | 50 | ns |
| $t_{WDD}$ | Write Pulse to Data Delay(2) | — | 50 | — | 50 | — | 60 | — | 80 | — | 120 | ns |
| $t_{WH}$ | Write Hold After $\overline{BUSY}$(6) | 12 | — | 15 | — | 20 | — | 20 | — | 20 | — | ns |
| $t_{DDD}$ | Write Data Valid to Read Data Delay(2) | — | 35 | — | 35 | — | 35 | — | 55 | — | 100 | ns |
| $t_{APS}$ | Arbitration Priority Set-up Time(3) | 5 | — | 5 | — | 5 | — | 5 | — | 5 | — | ns |
| $t_{BDD}$ | $\overline{BUSY}$ Disable to Valid Data(4) | — | 25 | — | 35 | — | 35 | — | 50 | — | 65 | ns |
| **Busy Timing (For Slave IDT7140 Only)** | | | | | | | | | | | | |
| $t_{WB}$ | Write to $\overline{BUSY}$ Input(5) | 0 | — | 0 | — | 0 | — | 0 | — | 0 | — | ns |
| $t_{WH}$ | Write Hold After $\overline{BUSY}$(6) | 12 | — | 15 | — | 20 | — | 20 | — | 20 | — | ns |
| $t_{WDD}$ | Write Pulse to Data Delay(2) | — | 40 | — | 50 | — | 60 | — | 80 | — | 120 | ns |
| $t_{DDD}$ | Write Data Valid to Read Data Delay(2) | — | 30 | — | 35 | — | 35 | — | 55 | — | 100 | ns |

**NOTES:**

2689 tbl 11

1. Com'l Only, 0°C to +70°C temperature range. PLCC package only.
2. Port-to-port delay through RAM cells from the writing port to the reading port, refer to "Timing Waveform of Write with Port -to-Port Read and $\overline{BUSY}$."
3. To ensure that the earlier of the two ports wins.
4. $t_{BDD}$ is a calculated parameter and is the greater of 0, $t_{WDD}$ – $t_{WP}$ (actual), or $t_{DDD}$ – $t_{DW}$ (actual).
5. To ensure that a write cycle is inhibited on port 'B' during contention on port 'A'..
6. To ensure that a write cycle is completed on port 'B' after contention on port 'A'.
7. "X" in part numbers indicates power rating (S or L).
8. Not available in DIP package

## TIMING WAVEFORM OF WRITE WITH PORT-TO-PORT READ AND $\overline{BUSY}$ (1,2,3)

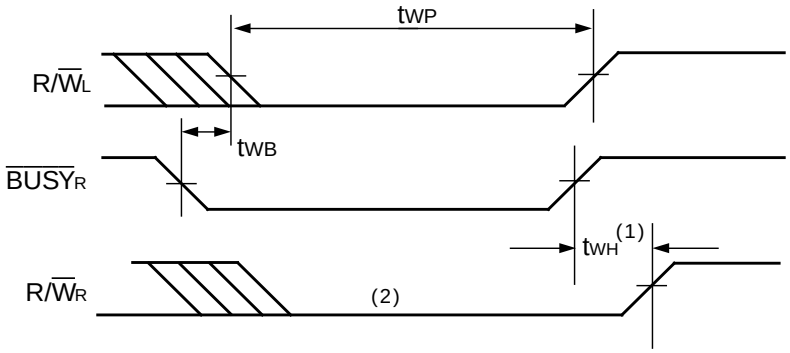



**NOTES:**

2692 drw 11

1. To ensure that the earlier of the two ports wins. $t_{APS}$ is ignored for Slave (IDT7142).
2. $\overline{CE}_L$ = $\overline{CE}_R$ = $V_{IL}$.
3. $\overline{OE}$ = $V_{IL}$ for the reading port.
4. All timing is the same for the left and right ports. Port 'A' may be either the left or right port. Port 'B' is opposite from port 'A'.

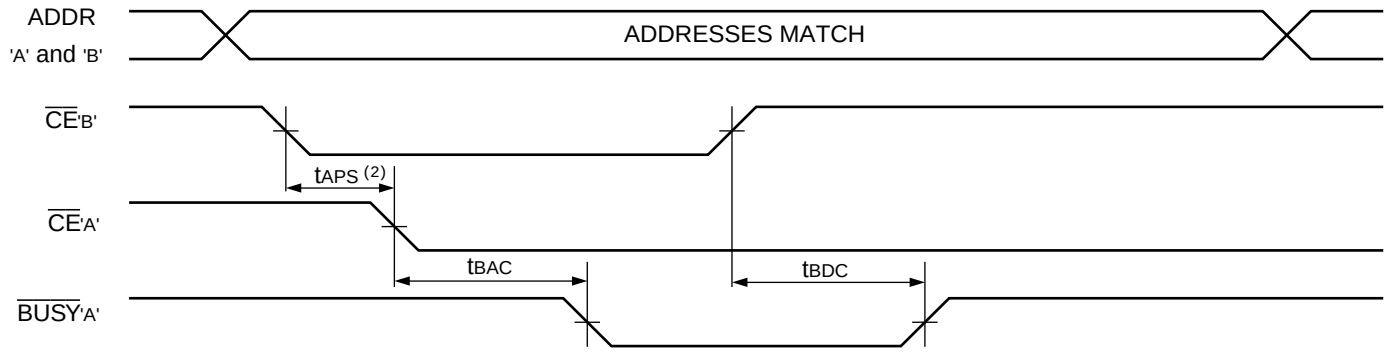
## TIMING WAVEFORM OF WRITE WITH $\overline{BUSY}$ (3)




2692 drw 12

**NOTES:**
1. $t_{WH}$ must be met for both $\overline{BUSY}$ Input (IDT7142, slave) or Output (IDT7132, master).
2. $\overline{BUSY}$ is asserted on port 'B' blocking R/$\overline{W}$'B', until $\overline{BUSY}$'B' goes High.
3. All timing is the same for the left and right ports. Port 'A' may be either the left or right port. Port 'B' is opposite from port 'A'.

## TIMING WAVEFORM OF BUSY ARBITRATION CONTROLLED BY $\overline{CE}$ TIMING (1)

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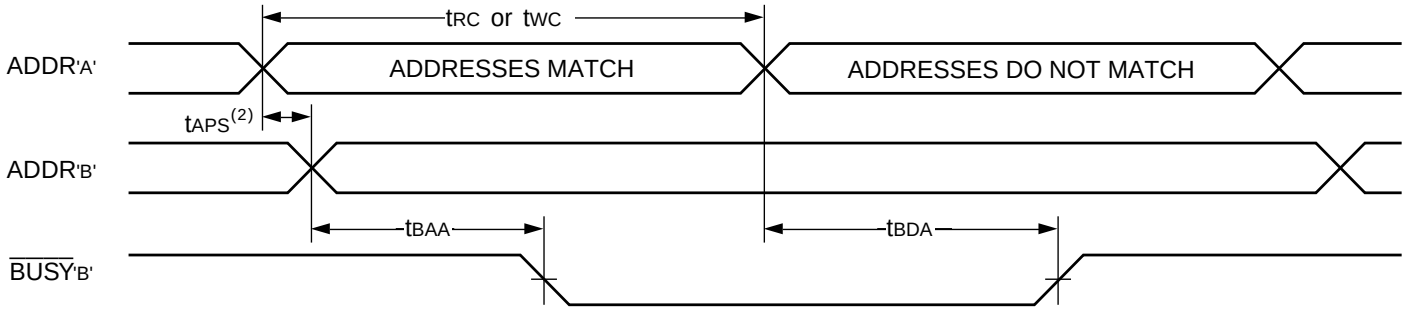
## TIMING WAVEFORM OF BUSY ARBITRATION CONTROLLED BY ADDRESS MATCH TIMING (1)




2692 drw 14

**NOTES:**
1. All timing is the same for left and right ports. Port 'A' may be either left or right port. Port 'B' is the opposite from port 'A'.
2. If $t_{APS}$ is not satisified, the $\overline{BUSY}$ will be asserted on one side or the other, but there is no guarantee on which side $\overline{BUSY}$ will be asserted (7132 only).

## TRUTH TABLES

### TABLE I — NON-CONTENTION READ/WRITE CONTROL(4)

| Left or Right Port(1) | | | | |
|---|---|---|---|---|
| R/$\overline{W}$ | $\overline{CE}$ | $\overline{OE}$ | $D_{0-7}$ | Function |
| X | H | X | Z | Port Disabled and in Power-Down Mode, $I_{SB2}$ or $I_{SB4}$ |
| X | H | X | Z | $\overline{CE}_R = \overline{CE}_L = V_{IH}$, Power-Down Mode, $I_{SB1}$ or $I_{SB3}$ |
| L | L | X | $DATA_{IN}$ | Data Written Into Memory(2) |
| H | L | L | $DATA_{OUT}$ | Data in Memory Output on Port(3) |
| H | L | H | Z | High Impedance Outputs |

2654 tbl 12

**NOTES:**
1. $A_{0L} - A_{10L} \neq A_{0R} - A_{10R}$.
2. If $\overline{BUSY}$ = L, data is not written.
3. If $\overline{BUSY}$ = L, data may not be valid, see $t_{WDD}$ and $t_{DDD}$ timing.
4. 'H' = $V_{IH}$, 'L' = $V_{IL}$, 'X' = DON'T CARE, 'Z' = High-impedance.

### TABLE II — ADDRESS BUSY ARBITRATION

| Inputs | | | Outputs | | |
|---|---|---|---|---|---|
| $\overline{CE}_L$ | $\overline{CE}_R$ | $A_{0L}$-$A_{10L}$ $A_{0R}$-$A_{10R}$ | $\overline{BUSY}_L$(1) | $\overline{BUSY}_R$(1) | Function |
| X | X | NO MATCH | H | H | Normal |
| H | X | MATCH | H | H | Normal |
| X | H | MATCH | H | H | Normal |
| L | L | MATCH | (2) | (2) | Write Inhibit(3) |

2654 tbl 13

**NOTES:**
1. Pins $\overline{BUSY}_L$ and $\overline{BUSY}_R$ are both outputs for IDT7130 (master). Both are inputs for IDT7140 (slave). $\overline{BUSY}_X$ outputs on the IDT7130 are open drain, not push-pull outputs. On slaves the $\overline{BUSY}_X$ input internally inhibits writes.
2. 'L' if the inputs to the opposite port were stable prior to the address and enable inputs of this port. 'H' if the inputs to the opposite port became stable after the address and enable inputs of this port. If tAPS is not met, either $\overline{BUSY}_L$ or $\overline{BUSY}_R$ = Low will result. $\overline{BUSY}_L$ and $\overline{BUSY}_R$ outputs can not be low simultaneously.
3. Writes to the left port are internally ignored when $\overline{BUSY}_L$ outputs are driving Low regardless of actual logic level on the pin. Writes to the right port are internally ignored when $\overline{BUSY}_R$ outputs are driving Low regardless of actual logic level on the pin.

## FUNCTIONAL DESCRIPTION

The IDT7132/IDT7142 provides two ports with separate control, address and I/O pins that permit independent access for reads or writes to any location in memory. The IDT7132/IDT7142 has an automatic power down feature controlled by $\overline{CE}$. The $\overline{CE}$ controls on-chip power down circuitry that permits the respective port to go into a standby mode when not selected ($\overline{CE}$ = $V_{IL}$). When a port is enabled, access to the entire memory array is permitted.

## BUSY LOGIC

Busy Logic provides a hardware indication that both ports of the RAM have accessed the same location at the same time. It also allows one of the two accesses to proceed and signals the other side that the RAM is "Busy". The busy pin can then be used to stall the access until the operation on the other side is completed. If a write operation has been attempted from the side that receives a busy indication, the write signal is gated internally to prevent the write from proceeding.

The use of busy logic is not required or desirable for all applications. In some cases it may be useful to logically OR the busy outputs together and use any busy indication as an interrupt source to flag the event of an illegal or illogical operation. If the write inhibit function of busy logic is not desirable, the busy logic can be disabled by placing the part in slave mode with the M/$\overline{S}$ pin. Once in slave mode the $\overline{BUSY}$ pin operates solely as a write inhibit input pin. Normal operation can be programmed by tying the $\overline{BUSY}$ pins High. If desired, unintended write operations can be prevented to a port by tying the busy pin for that port low.

The busy outputs on the IDT7132/IDT7142 RAM in master mode, are pull-up type outputs and do not require pull up resistors to operate. If these RAMs are being expanded in depth, then the busy indication for the resulting array requires the use of an external AND gate.

## WIDTH EXPANSION WITH BUSY LOGIC MASTER/SLAVE ARRAYS

When expanding an RAM array in width while using busy logic, one master part is used to decide which side of the RAM array will receive a busy indication, and to output that indication. Any number of slaves to be addressed in the same address range as the master, use the busy signal as a write inhibit signal. Thus on the IDT7130/IDT7140 RAM the busy pin is an output if the part is used as a master (M/$\overline{S}$ pin = $V_{IH}$), and the busy pin is an input if the part used as a slave (M/$\overline{S}$ pin = $V_{IL}$) as shown in Figure 4.

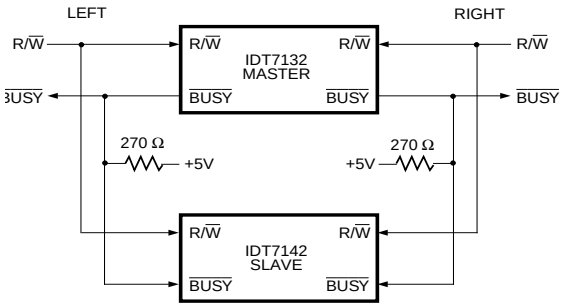
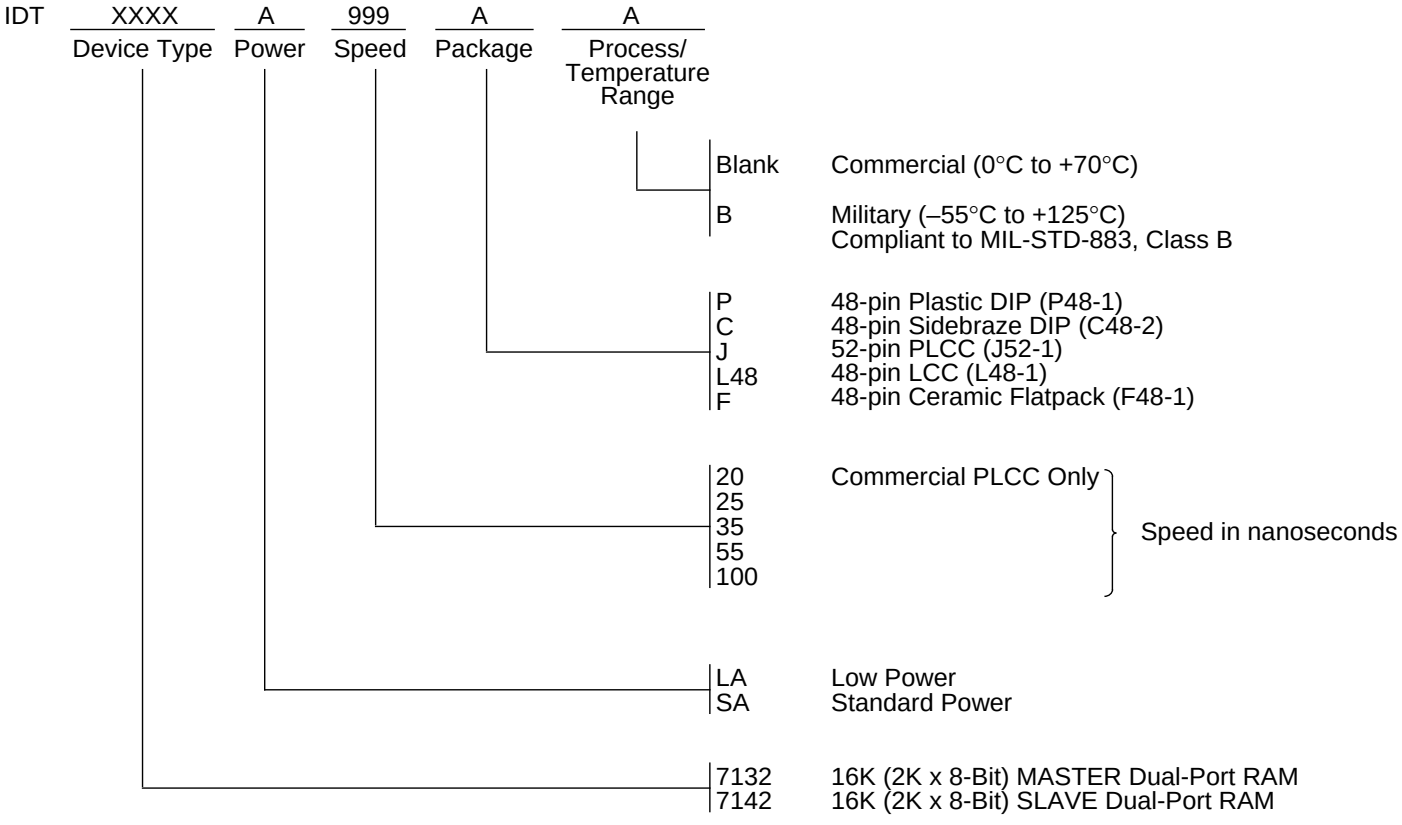



Figure 4. Busy and chip enable routing for both width and depth expansion with IDT7132 (Master) and IDT7142 (Slave) RAMs.

If two or more master parts were used when expanding in width, a split decision could result with one master indicating busy on one side of the array and another master indicating busy on one other side of the array. This would inhibit the write operations from one port for part of a word and inhibit the write operations from the other port for the other part of the word.

The busy arbitration, on a master, is based on the chip enable and address signals only. It ignores whether an access is a read or write. In a master/slave array, both address and chip enable must be valid long enough for a busy flag to be output from the master before the actual write pulse can be initiated with either the R/$\overline{W}$ signal or the byte enables. Failure to observe this timing can result in a glitched internal write inhibit signal and corrupted data in the slave.

## ORDERING INFORMATION

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