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CMOS LSI



Graphic Equalizer System

CCB

Overview

The LC7527E is a microprocessor controllable seven-band graphic equalizer LSI that does not require the use of external semiconductor inductors (simulated inductors).

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Functions

- Left and right channel seven-band graphic equalizers
- Each band operates in ±2 dB steps.
- Each band has a maximum boost of +12 dB and a maximum cut of -12 dB for a total of 13 settings.
- Independent left and right channel operation
- Serial data input supports CCB format communications with the system controller.
- CMOS LSI with a 12 V breakdown voltage

Features

- This LSI, in conjunction with a control microprocessor, can implement in two chips, an electronic graphic equalizer with the following features.
 - One touch gain control for each band
 - One touch memory setting recall allows users to select desired frequency characteristics for each track.
 - Since the LC7527E includes band filter amplifiers on chip, capacitors are the only external components required in application systems.
 - Minimal switching noise due to the use of a Silicon gate CMOS process.
 - CCB is a trademark of SANYO ELECTRIC CO., LTD.
 - CCB is SANYO's original bus format and all the bus addresses are controlled by SANYO.

Package Dimensions

unit: mm

3159-QFP64E





SANYO Electric Co., Ltd. Semiconductor Bussiness Headquarters

Specifications Absolute Maximum Ratings at Ta = 25° C, V_{SS} = 0 V

Parameter	Symbol	Conditions	Ratings	Unit
Maximum supply voltage	V _{DD} -V _{EE} max	AV_{DD} , AV_{EE} , DV_{DD} , DV_{EE}^*	12	V
	V _{IN} max1	CL, DI, CE	V_{SS} – 0.3 to V_{DD} + 0.3	V
Maximum input voltage	V _{IN} max2	LIN1, LIN2, RIN1, RIN2	V_{EE} – 0.3 to V_{DD} + 0.3	V
	V _{IN} max3	S1	V_{EE} – 0.3 to V_{DD} + 0.3	V
Allowable power dissipation	Pd max	Ta ≤ 85°C	280	mW
Operating temperature	Topr		-40 to +85	°C
Storage temperature	Tstg		-50 to +125	°C

Note: * –6 V \leq V_{EE} \leq V_{SS} \leq V_{DD}

Allowable Operating Ranges at Ta = 25°C, $V_{SS} = 0 V$

Deremeter	Symbol	Conditions	Ratings			Lloit
Falameter			min	typ	max	
	V _{DD}	AV _{DD} , DV _{DD}		5		V
Supply voltage	V _{EE}	AV _{EE} , DV _{EE}		-5		V
	V_{DD} - V_{EE}	AV_{DD} , AV_{EE} , DV_{DD} , DV_{EE}	8.0		11.0	V
Input high level voltage	VIH	CL, DI, CE	3.0		V _{DD}	V
Input low level voltage	VIL	CL, DI, CE	V _{SS}		1.0	V
Input amplitude voltage	V _{IN} 1	LIN1, LIN2, RIN1, RIN2	V _{EE}		V _{DD}	Vp-p
Input amplitude voltage	V _{IN} 2	S1	V_{EE}		V _{DD}	V
Clock pulse width	t _{øW}	CL	1			μs
Setup time	tsetup	CL, DI, CE	1			μs
Hold time	t _{HOLD}	CL, DI, CE	1			μs
Operating frequency	fopg	CL			500	kHz

Electrical Characteristics at Ta = 25°C, V_{DD} = 5 V, V_{EE} = –5 V, V_{SS} = 0 V

Deremeter	Cumhal	Conditions	Ratings			Linit
Parameter	Symbol Conditions		min	typ	max	Unit
	THD (1)	V _{OUT} = 1 Vrms, FLAT, f = 20 kHz		0.01	0.05	%
Total harmonic distortion	THD (2)	V _{OUT} = 1 Vrms, FLAT, f = 1 kHz		0.001	0.005	%
	THD (3)	V _{OUT} = 300 mVrms, FLAT, f = 20 kHz with all bands at full boost		0.042	0.2	%
	THD (4)	V_{OUT} = 300 mVrms, FLAT, f = 1 kHz with all bands at full boost		0.045	0.2	%
Crosstalk	СТ	V_{OUT} = 1 Vrms, f = 20 kHz, FLAT, Rg = 1 k Ω		58		dB
Setting error	ΔΒ	with other bands flat	-2		+2	dB
Current drain	I _{DD}	V_{DD} - V_{EE} = 11 V			30	mA
Analog switch off leakage current	I _{OFF}	LIN1, LIN2, RIN1, RIN2			10	μA



Electrical Characteristics Test Circuit



Pin Assignment





LC7527E

Pin Functions

Pin	Pin No.	Circuit type	Function
Lf1C1	62		
Lf1C2	63		Left channel f1 band control block
Lf1C3	64	AVDD	External capacitor connections
Rf1C1	51		
Rf1C2	50		Right channel f1 band control block
Rf1C3	49		External capacitor connections
Lf2C1	1	│	Left channel f2 band control block
Lf2C2	2		External capacitor connections
	3	AVEE	
Rf2C1	48	×01920	Disht shares I to have a series I black
Rf2C2	47		Right channel 12 band control block
Rf2C3	46		
1 f2C1	4	AVDD	
LISC1	5		Left channel f3 band control block
Lf3C3	6	│ ▲	External capacitor connections
		fnC2	
Rf3C1	45		Right channel f3 band control block
RI3C2 Rf3C3	44		External capacitor connections
	10		
Lf4C1	7	AVEE	Left channel f4 hand control block
Lf4C2	8		External capacitor connections
Lt4C3	9		
Rf4C1	42		
Rf4C2	41		Right channel 14 band control block
Rf4C3	40		
1.601	10		
LISC1	11		Left channel f5 band control block
Lf5C3	12	AVEE	External capacitor connections
DIFOL			
Rf5C1 Rf5C2	39	AVDD	Right channel f5 band control block
Rf5C3	37		External capacitor connections
		▲ ▲	
Lf6C1	13	Vref	Left channel f6 band control block
Lf6C2	14		External capacitor connections
LIDUS	15	₹	
Rf6C1	36		Dight sharped fC hand a set of black
Rf6C2	35	AVEE 401921	Right channel to band control block
Rf6C3	34		
L f7C1	17		
LI7C1	18		Left channel f7 band control block
Lf7C3	19		External capacitor connections
DIZO1			
Rf7C2	32		Right channel f7 band control block
Rf7C3	30		External capacitor connections
			Power supply: +5 V typ. Audio signal power supply
AVDD	23		Power supply: -5 V typ. Audio signal power supply
	56 22		Power supply: +5 V typ. Logic signal power supply Power supply: -5 V typ. Logic signal power supply
DVEE	57		Power supply: 0 V
V _{SS}	28		AV_{DD} must be equal to $\text{DV}_{\text{DD}},$ and AV_{EE} must be equal to
			DV _{EE} .





Continued from preceding page.

Pin	Pin No.	Circuit type	Function		
LVref RVref	58 55		Power supply: Analog ground The impedance of the pattern connected to these pins should be kept as low as possible. LVref and RVref are not connected to the V _{SS} pin.		
LIN1 LIN2	59 60		Left channel audio signal input IN1 is normally connected to an operational amplifier inverting input. IN2 is normally connected to an operational amplifier non- inverting input.		
RIN1 RIN2	54 53		Right channel audio signal input IN1 is normally connected to an operational amplifier inverting input. IN2 is normally connected to an operational amplifier non- inverting input.		
CE	27		Chip enable input. Internal data is latched when this pin goes from high to low and the analog switches operate. Data transfers are enabled when this pin is high.		
CL	25		Clock input. Schmitt inverter input circuit		
DI	26	VSS 401924	Data input. Schmitt inverter input circuit		
S1	24		Dual chip system chip select input. By connecting S1 (this pin) to either V _{DD} or V _{EE} , data input is enabled when the address matches the corresponding address listed below. S1 = V _{DD} \rightarrow Address: 8C S1 = V _{EE} \rightarrow Address: 8D		
NC NC NC NC NC NC NC	16 20 21 29 33 52 61		No connection. Do not connect signals to these pins.		



LC7527E







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Data Input

ma Pa

The LC7527E is controlled by inputting stipulated data using the CE, CL, and DI pins. The data has a total of 20 bits, of which eight are address and 12 are data.



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10# -Ach INPUT LCh INPUT *1ún≢) ŏŏ 1 VEE R11C3 R11C3 ġ NC 52 51 50 49 Lf2Cs A12C1 Rch fi bend Lch fi bend -11-- 1 48 -11-47 Rf2C2 L12C2 2 Lch 12 band Ach 12 han L + 2C3 L + 2C3 L + 3C1 L + 3C1 47 46 8f2C3 46 8f3C1 -13C1 -11-45 L f 3C2 5 8130 Lch f3 band Ach f3 bend 44 L 1 3C3 Rf3C3 43 -11 . 42 L14C2 L14C2 B L14C3 L14C3 L15C1 f4 band Lch f4 band Rch 41 LC7527E Rf4C 40 41 C 1 -11-10 39 -II L15C2 RfSC f5 ben 38 f5 band Lch Acl 11 L12C3 L16C1 L16C1 38 815C3 37 816C1 36 L16C2 14 35 81602 f6 bend Ach 16 band Lch 36 R/6C3 L+6C3 33 NC NC 15 Rch f7 band Lch f7 bend 17 18 19 20 21 22 23 24 25 26 27 28 29 30 31 32 1761 R17C3 L 1703 A 00 ÿ Ŷ 00,00 10 5 1 5 ۲<u>8</u>8 R17C1 **,** VDD DI CE *C0

Unit (resistance: Ω, capacitance: F)

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Note: If at all possible, use bipolar capacitors for all capacitors that do not have a polarity specified. *1. A resistor of about 100 k Ω is recommended if impulse noise (popping sounds) is a problem.



Sample Application Circuit

External Component Value Calculations

The external capacitors required for each band in the LC7527E are the structural elements in semiconductor inductors (simulated inductors). The remainder of this section presents the equivalent circuits and the formulas used to determine the center frequencies.

1. Semiconductor Inductor Equivalent Circuit

The LC7527E provides circuits with differing constants for the low and high bands.



2. Calculation Example

Specifications: 1) Center frequency: Fo = 63 Hz 2) Q at maximum boost: $Q_{+12 \text{ dB}} = 1.05$

- Derive the sharpness Qo of the semiconductor inductor itself. $Qo = \frac{(R1 + R4)}{R1} \times Q_{+12 \text{ dB}} \approx 4.064 \quad \text{See the internal equivalent circuit figure for R4.}$
- Derive C1. C1 = $1/2\pi$ FoR1Qo $\neq 0.953$ (µF)
- Derive C2. C2 = Qo/2πFoR2 ≠ 0.034 (μF)
- 3. Sample Values for C1 and C2

Center frequency Fo (Hz)	C1 (F)	C2 (F)
63	0.953 µ	0.034 µ
160	0.377 µ	0.014 µ
400	0.151 µ	5390 p
1000	0.060 µ	2156 p
2500	0.024 µ	862 p
6300	9563 p	3422 p
16000	3765 p	1348 p







Usage Notes

- 1. The states of the internal analog switches are undefined when power is first applied. System output should be muted until control data has been sent to the LC7527E.
- 2. To prevent the high frequency digital signals associated with data transfers over the CL, CI, and DI pins from generating interference in the analog signals, either guard those lines with a ground pattern or use shielded cables.

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