M5M5256BP,FP,KP-70,-85,-10,-12,-15,-70L,-85L, -10L,-12L,-15L,-70LL,-85LL,-10LL,-12LL,-15LL

262144-BIT (32768-WORD BY 8-BIT) CMOS STATIC RAM

DESCRIPTION

This M5M5256BP, FP, KP is a 262144-bit CMOS static RAM organized as 32768-words by 8-bits which is fabricated using high-performance double polysilicon CMOS technology. The use of resistive load NMOS cells and CMOS periphery result in a high-density and low-power static RAM. It is ideal for the memory systems which require simple interface.

The stand-by current is low enough for a battery back-up application. It is mounted in a standard 28pin package and configured in an industrial standard 32K × 8-bit pinout.

FEATURES

Type name	Access time (max)	Power supply current	
		Active (max)	Stand-by (max)
M5M5256BP, FP, KP-70	70ns		
M5M5256BP, FP, KP-85	85ns		
M5M5256BP, FP, KP-10	100ns		2mA
M5M5256BP, FP, KP-12	120ns		
M5M5256BP, FP, KP-15	150ns		
M5M5256BP, FP, KP-70L	70ns		100μA (Vcc = 5.5V) 50μA (Vcc = 3.0V)
M5M5256BP, FP, KP-85L	85ns	70mA	
M5M5256BP, FP, KP-10L	100ns		
M5M5256BP, FP, KP-12L	120ns		
M5M5256BP, FP, KP-15L	150ns		
M5M5256BP, FP, KP-70LL	70ns		20μA (Vcc = 5.5V) 10μA (Vcc = 3.0V)
M5M5256BP, FP, KP-85LL	85ns		
M5M5256BP, FP, KP-10LL	100ns		
M5M5256BP, FP, KP-12LL	120ns		
M5M5256BP, FP, KP-15LL	150ns		

● Single +5V power supply
● No clocks, no refresh
● Data-hold on +2V power supply

PIN CONFIGURATION (TOP VIEW)
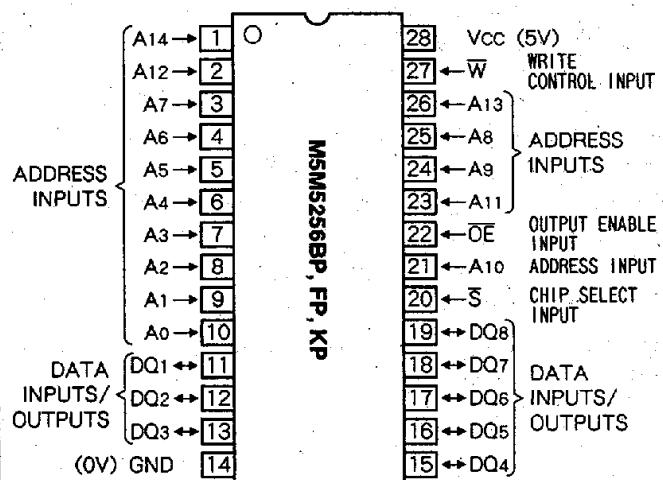
Outline 28P4(P)
28P2W-C(FP)
28P4Y(KP)

● Directly TTL compatible : All inputs and outputs
● Three-state outputs : OR-tie capability
● Simple memory expansion by $\overline{S}$
● $\overline{OE}$ prevents data contention in the I/O bus
● Common data I/O
● Package

M5M5256BP ··············28pin 600mil DIP
M5M5256BKP ··············28pin 300mil DIP
M5M5256BFP ·····28pin small outline package(SOP)

APPLICATION

Small capacity memory units

BLOCK DIAGRAM
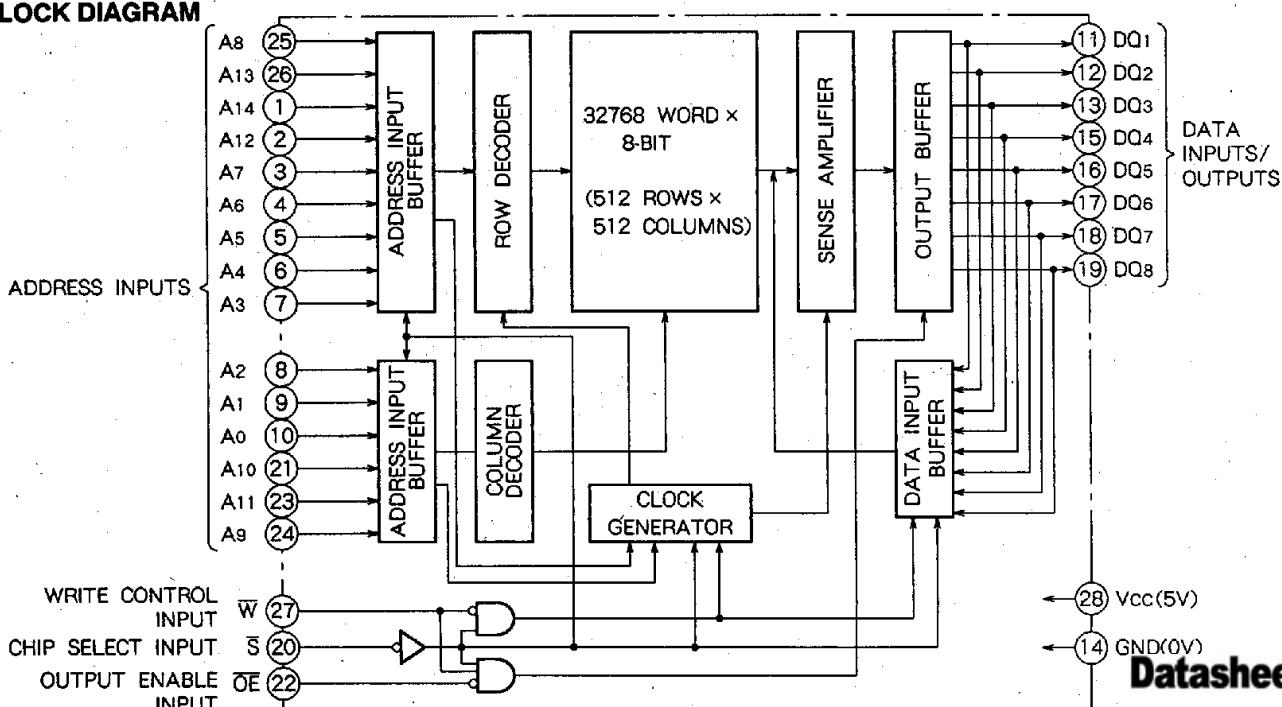
M5M5256BP,FP,KP-70,-85,-10,-12,-15,-70L,-85L, -10L,-12L,-15L,-70LL,-85LL,-10LL,-12LL,-15LL

262144-BIT (32768-WORD BY 8-BIT) CMOS STATIC RAM

FUNCTION

The operation mode of the M5M5256BP, FP, KP is determined by a combination of the device control inputs $\overline{S}$, $\overline{W}$ and $\overline{OE}$. Each mode is summarized in the function table.

A write cycle is executed whenever the low level $\overline{W}$ overlaps with the low level $\overline{S}$. The address must be set up before the write cycle and must be stable during the entire cycle. The data is latched into a cell on the trailing edge of $\overline{W}$, $\overline{S}$, whichever occurs first, requiring the set-up and hold time relative to these edge to be maintained. The output enable $\overline{OE}$ directly controls the output stage. Setting the $\overline{OE}$ at a high level, the output stage is in a high-impedance state, and the data bus contention problem in the write cycle is eliminated.

A read cycle is executed by setting $\overline{W}$ at a high level and $\overline{OE}$ at a low level while $\overline{S}$ are in an active state.

When setting $\overline{S}$ at a high level, the chip is in a non-selectable mode in which both reading and writing are disabled. In this mode, the output stage is in a high-impedance state, allowing OR-tie with other chips and memory expansion by $\overline{S}$. The power supply current is reduced as low as the stand-by current which is specified as Icc3 or Icc4, and the memory data can be held + 2V power supply, enabling battery back-up operation during power failure or power-down operation in the non-selected mode.

FUNCTION TABLE

$\overline{S}$	$\overline{W}$	$\overline{OE}$	Mode	DQ	Icc
H	X	X	Non selection	High-impedance	Stand-by
L	L	X	Write	Din	Active
L	H	L	Read	Dout	Active
L	H	H		High-impedance	Active

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Conditions	Ratings	Unit
Vcc	Supply voltage	With respect to GND	− 0.3 ∼7	V
VI	Input voltage		− 0.3 ∼Vcc + 0.3	V
Vo	Output voltage		0 ∼Vcc	V
Pd	Power dissipation	Ta = 25℃	700	mW
Topr	Operating temperature		0∼70	℃
Tstg	Storage temperature		− 65∼150	℃

ELECTRICAL CHARACTERISTICS (Ta = 0∼70℃, Vcc = 5V ± 10%, unless otherwise noted)

Symbol	Parameter	Test conditions		Limits			Unit
				Min	Typ	Max	
VIH	High input voltage			2.2		Vcc+0.3	V
VIL	Low input voltage			− 0.3		0.8	V
VOH	High output voltage	IOH = − 1mA		2.4			V
VOL	Low output voltage	IOL = 2mA				0.4	V
Ii	Input leakage current	VI = 0∼Vcc				± 1	µA
Io	Output leakage current	$\overline{S}$ = VIH or $\overline{OE}$ = VIH, VI/o = 0∼Vcc				± 1	µA
Icc1	Active supply current(AC MOS level)	$\overline{S}$ < 0.2, $\overline{W}$ > Vcc−0.2 output open Other inputs < 0.2 or > Vcc − 0.3 Min cycle			30	65	mA
Icc2	Active supply current(AC TTL level)	$\overline{S}$ = VIL, $\overline{W}$ = VIH output open Other inputs = VIL or VIH Min cycle			35	70	mA
Icc3	Stand by supply current	$\overline{S}$ ≧ Vcc − 0.2V Other inputs = 0∼Vcc	BP, FP, KP			2	mA
			BP, FP, KP-L			100	µA
			BP, FP, KP-LL			20	µA
Icc4	Stand by supply current	$\overline{S}$ = VIH, other inputs = 0∼Vcc				3	mA
Ci	Input capacitance (Ta = 25℃)	VI = GND, VI = 25mVrms, f = 1MHz				6	pF
Co	Output capacitance (Ta = 25℃)	Vo = GND, Vo = 25mVrms, f =1MHz				8	pF

Note 1. Direction for current flowing into IC is indicated as positive (no mark)
2. Typical value is Vcc = 5V, Ta = 25℃

M5M5256BP,FP,KP-70,-85,-10,-12,-15,-70L,-85L, -10L,-12L,-15L,-70LL,-85LL,-10LL,-12LL,-15LL

262144-BIT (32768-WORD BY 8-BIT) CMOS STATIC RAM

SWITCHING CHARACTERISTICS (Ta = 0~70°C, Vcc = 5V ± 10%, unless otherwise noted)
Read cycle

Symbol	Parameter	Limits										Unit
		M5M5256-70 M5M5256-70L M5M5256-70LL		M5M5256-85 M5M5256-85L M5M5256-85LL		M5M5256-10 M5M5256-10L M5M5256-10LL		M5M5256-12 M5M5256-12L M5M5256-12LL		M5M5256-15 M5M5256-15L M5M5256-15LL		
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
tCR	Read cycle time	70		85		100		120		150		ns
ta(A)	Address access time		70		85		100		120		150	ns
ta(S)	Chip select access time		70		85		100		120		150	ns
ta(OE)	Output enable access time		35		45		50		60		75	ns
tdis(S)	Output disable time after $\overline{S}$ high		30		30		35		40		45	ns
tdis(OE)	Output disable time after $\overline{OE}$ high		25		30		35		40		45	ns
ten(S)	Output enable time after $\overline{S}$ low	5		5		10		10		10		ns
ten(OE)	Output enable time after $\overline{OE}$ low	5		5		10		10		10		ns
tv(A)	Data valid time after address change	20		20		20		20		20		ns

TIMING REQUIREMENTS (Ta = 0~70°C, Vcc = 5V ± 10%, unless otherwise noted)
Write cycle

Symbol	Parameter	Limits										Unit
		M5M5256-70 M5M5256-70L M5M5256-70LL		M5M5256-85 M5M5256-85L M5M5256-85LL		M5M5256-10 M5M5256-10L M5M5256-10LL		M5M5256-12 M5M5256-12L M5M5256-12LL		M5M5256-15 M5M5256-15L M5M5256-15LL		
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
tCW	Write cycle time	70		85		100		120		150		ns
tw(W)	Write pulse width	55		60		60		70		80		ns
tsu(A)	Address set up time	0		0		0		0		0		ns
tsu(A-WH)	Address set up time with respect to $\overline{W}$ high	65		75		80		85		90		ns
tsu(S)	Chip select set up time	65		75		80		85		90		ns
tsu(D)	Data set up time	30		35		35		40		50		ns
th(D)	Data hold time	0		0		0		0		0		ns
trec(W)	Write recovery time	0		0		0		0		0		ns
tdis(W)	Output disable time after $\overline{W}$ low		25		30		35		40		45	ns
tdis(OE)	Output disable time after $\overline{OE}$ high		25		30		35		40		45	ns
ten(W)	Output enable time after $\overline{W}$ high	5		5		10		10		10		ns
ten(OE)	Output enable time after $\overline{OE}$ low	5		5		10		10		10		ns

TIMING DIAGRAM
Read cycle
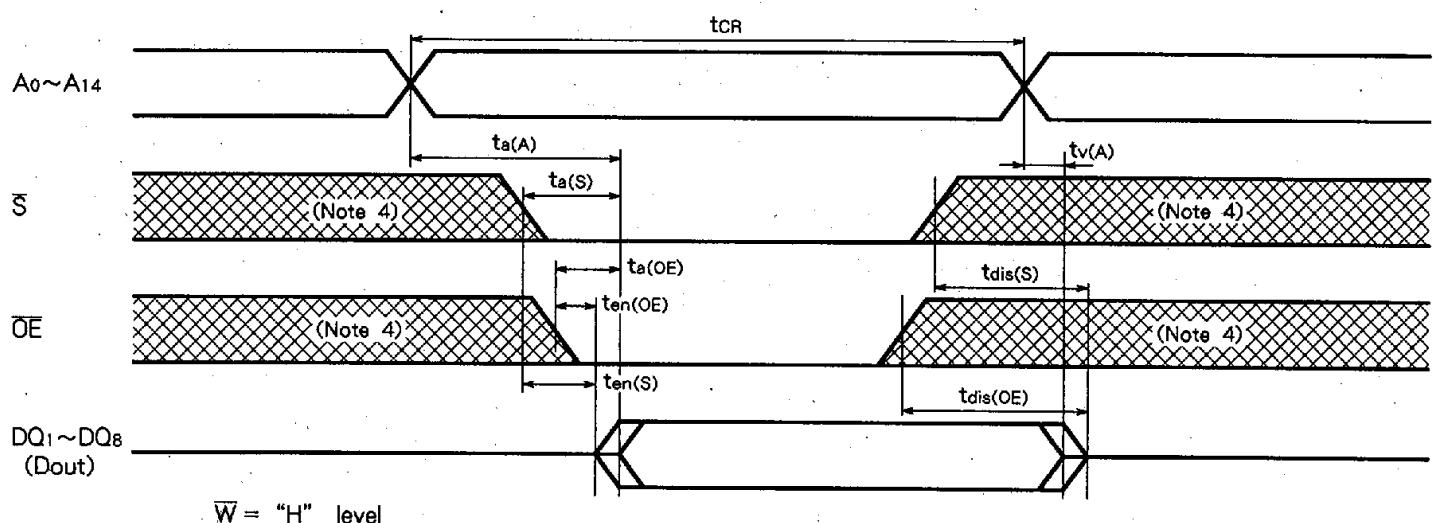
$\overline{W}$ = "H" level

Write cycle ($\overline{W}$ control)
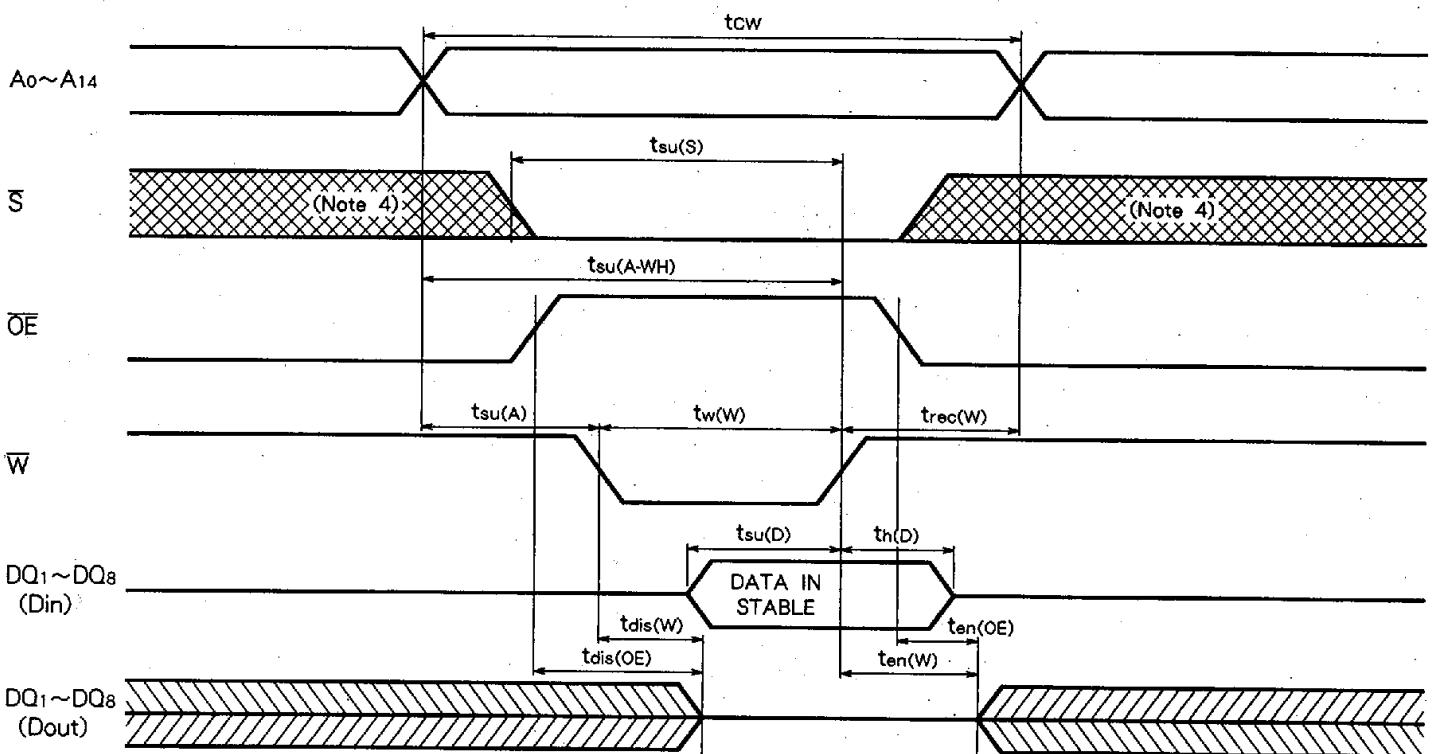
M5M5256BP,FP,KP-70,-85,-10,-12,-15,-70L,-85L, -10L,-12L,-15L,-70LL,-85LL,-10LL,-12LL,-15LL

262144-BIT (32768-WORD BY 8-BIT) CMOS STATIC RAM

Write cycle ($\overline{S}$ control)
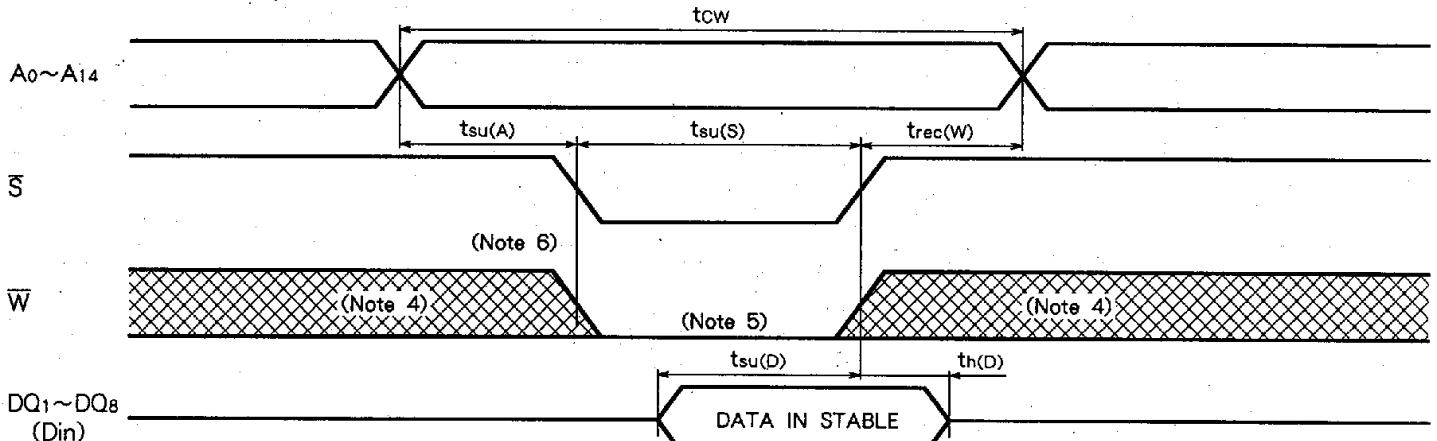
Note 3 : Test condition

Input pulse levels ·· $V_{IH} = 2.4V$, $V_{IL} = 0.6V$

Input rise and fall time ·································· 10ns

Reference levels ·· $V_{OH} = V_{OL} = 1.5V$

Transition is measured $\pm 500mV$ from steady state voltage.(for t_{en}, t_{dis})

Output loads ·················· Fig. 1, $C_L = 100pF$ (BP, FP, KP-85, -10, -12, -15, -85L, -10L, -12L, -15L, -85LL, -10LL, -12LL, -15LL)

$C_L = 30pF$ (BP, FP, KP-70, -70L, -70LL)

$C_L = 5pF$ (for t_{en}, t_{dis})
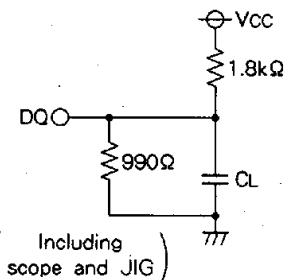
Note 4. Hatching indicates the state is don't care.
 5. Writing is executed in overlap of $\overline{S}$ and $\overline{W}$ low.
 6. If $\overline{W}$ goes low simultaneously with or prior to $\overline{S}$, the output remains in the high-impedance state.
 7. Don't apply inverted phase signal externally when DQ pin is in output mode.

Fig. 1 Output load

POWER DOWN CHARACTERISTICS
ELECTRICAL CHARACTERISTICS (Ta = 0~70℃, unless otherwise noted)

Symbol	Parameter	Test conditions		Limits			Unit
				Min	Typ	Max	
$V_{CC(PD)}$	Power down supply voltage			2			V
$V_{I(\overline{S})}$	Chip select input $\overline{S}$	$2.2V \leqq V_{CC(PD)}$		2.2			V
		$2V \leqq V_{CC(PD)} \leqq 2.2V$			$V_{CC(PD)}$		
$I_{CC(PD)}$	Power down supply current	$V_{CC} = 3V$, Other inputs=3V	BP,FP,KP			2	mA
			BP,FP,KP-L			50	μA
			BP,FP,KP-LL			10*	μA

* Ta = 25℃, $I_{CC(PD)}$ = 1μA

TIMING REQUIREMENTS (Ta = 0~70℃, unless otherwise noted)

Symbol	Parameter	Test conditions		Limits			Unit
				Min	Typ	Max	
$t_{su(PD)}$	Power down setup time			0			ns
$t_{rec(PD)}$	Power down recovery time			tCR			ns

POWER DOWN CHARACTERISTICS