

K6F1616U6A Family

CMOS SRAM

Document Title

1M x16 bit Super Low Power and Low Voltage Full CMOS Static RAM

Revision History

<u>Revision No.</u>	<u>History</u>	<u>Draft Date</u>	<u>Remark</u>
0.0	Initial draft	September 11, 2001	Preliminary
1.0	Finalize - added 45ns product - changed ICC1 : 3mA to 2mA - changed ICC2 : 38mA to 30mA for 55ns product 30mA to 25mA for 70ns product	January 4, 2002	Final
1.1	Revise - Deleted 45ns product	September 11, 2002	Final

1M x 16 bit Super Low Power and Low Voltage Full CMOS Static RAM

FEATURES

- Process Technology: Full CMOS
- Organization: 1M x16
- Power Supply Voltage: 2.7~3.3V
- Low Data Retention Voltage: 1.5V(Min)
- Three State Outputs
- Package Type: 48-TBGA-7.50x9.50

GENERAL DESCRIPTION

The K6F1616U6A families are fabricated by SAMSUNG's advanced full CMOS process technology. The families support industrial operating temperature ranges and have chip scale package for user flexibility of system design. The families also support low data retention voltage for battery back-up operation with low data retention current.

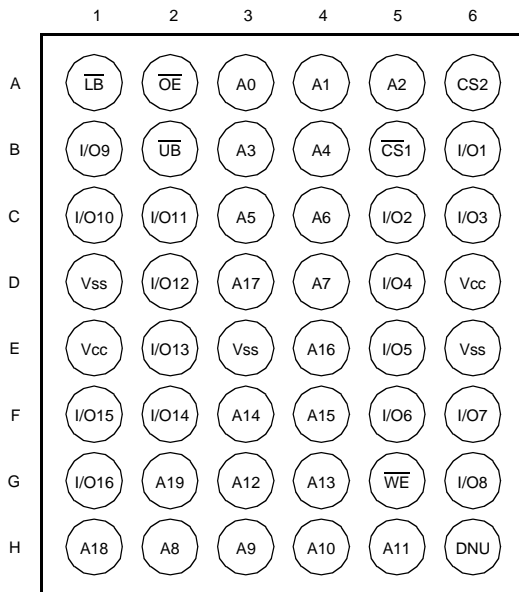
PRODUCT FAMILY

Product Family	Operating Temperature	Vcc Range	Speed	Power Dissipation		PKG Type
				Standby (I _{SB1} , Typ.)	Operating (I _{CC1} , Max)	
K6F1616U6A-F	Industrial(-40~85°C)	2.7~3.3V	55 ¹ /70ns	1μA ²)	2mA	48-TBGA-7.50x9.50

1. The parameter is measured with 30pF test load.

2. Typical values are measured at V_{CC}=3.0V, T_A=25°C and not 100% tested.

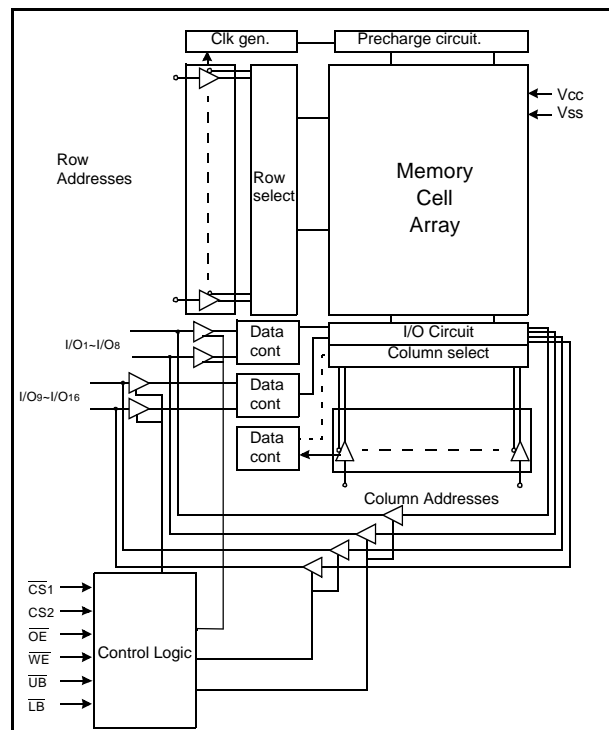
PIN DESCRIPTION



48-TBGA: Top View (Ball Down)

Name	Function	Name	Function
$\overline{CS1}$, $CS2$	Chip Select Inputs	Vcc	Power
\overline{OE}	Output Enable Input	Vss	Ground
\overline{WE}	Write Enable Input	\overline{UB}	Upper Byte(I/O _{9~16})
A _{0~A19}	Address Inputs	\overline{LB}	Lower Byte(I/O _{1~8})
I/O _{1~I/O16}	Data Inputs/Outputs	DNU	Do Not Use

FUNCTIONAL BLOCK DIAGRAM



PRODUCT LIST

Industrial Temperature Products(-40~85°C)	
Part Name	Function
K6F1616U6A-EF55	48-TBGA, 55ns, 3.0V
K6F1616U6A-EF70	48-TBGA, 70ns, 3.0V

FUNCTIONAL DESCRIPTION

\overline{CS}_1	CS_2	\overline{OE}	\overline{WE}	\overline{LB}	\overline{UB}	I/O ₁₋₈	I/O ₉₋₁₆	Mode	Power
H	X ¹⁾	X ¹⁾	X ¹⁾	X ¹⁾	X ¹⁾	High-Z	High-Z	Deselected	Standby
X ¹⁾	L	X ¹⁾	X ¹⁾	X ¹⁾	X ¹⁾	High-Z	High-Z	Deselected	Standby
X ¹⁾	X ¹⁾	X ¹⁾	X ¹⁾	H	H	High-Z	High-Z	Deselected	Standby
L	H	H	H	L	X ¹⁾	High-Z	High-Z	Output Disabled	Active
L	H	H	H	X ¹⁾	L	High-Z	High-Z	Output Disabled	Active
L	H	L	H	L	H	Dout	High-Z	Lower Byte Read	Active
L	H	L	H	H	L	High-Z	Dout	Upper Byte Read	Active
L	H	L	H	L	L	Dout	Dout	Word Read	Active
L	H	X ¹⁾	L	L	H	Din	High-Z	Lower Byte Write	Active
L	H	X ¹⁾	L	H	L	High-Z	Din	Upper Byte Write	Active
L	H	X ¹⁾	L	L	L	Din	Din	Word Write	Active

1. X means don't care. (Must be low or high state)

ABSOLUTE MAXIMUM RATINGS¹⁾

Item	Symbol	Ratings	Unit
Voltage on any pin relative to Vss	V _{IN} , V _{OUT}	-0.2 to V _{CC} +0.3V(Max. 3.6V)	V
Voltage on Vcc supply relative to Vss	V _{CC}	-0.2 to 3.6	V
Power Dissipation	P _d	1.0	W
Storage temperature	T _{STG}	-65 to 150	°C
Operating Temperature	T _A	-40 to 85	°C

1. Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. Functional operation should be restricted to recommended operating condition. Exposure to absolute maximum rating conditions for extended period may affect reliability.



RECOMMENDED DC OPERATING CONDITIONS¹⁾

Item	Symbol	Min	Typ	Max	Unit
Supply voltage	V _{CC}	2.7	3.0	3.3	V
Ground	V _{SS}	0	0	0	V
Input high voltage	V _{IH}	2.2	-	V _{CC} +0.3 ²⁾	V
Input low voltage	V _{IL}	-0.3 ³⁾	-	0.6	V

Note:

1. T_A=-40 to 85°C, otherwise specified
2. Overshoot: V_{CC}+2.0V in case of pulse width ≤20ns.
3. Undershoot: -2.0V in case of pulse width ≤20ns.
4. Overshoot and Undershoot are sampled, not 100% tested.

CAPACITANCE¹⁾ (f=1MHz, T_A=25°C)

Item	Symbol	Test Condition	Min	Max	Unit
Input capacitance	C _{IN}	V _{IN} =0V	-	8	pF
Input/Output capacitance	C _{IO}	V _{IO} =0V	-	10	pF

1. Capacitance is sampled, not 100% tested

DC AND OPERATING CHARACTERISTICS

Item	Symbol	Test Conditions	Min	Typ ¹⁾	Max	Unit
Input leakage current	I _{LI}	V _{IN} =V _{SS} to V _{CC}	-1	-	1	μA
Output leakage current	I _{LO}	$\overline{CS}_1=V_{IH}$ or $CS_2=V_{IL}$ or $\overline{OE}=V_{IH}$ or $\overline{WE}=V_{IL}$ or $\overline{LB}=\overline{UB}=V_{IH}$, V _{IO} =V _{SS} to V _{CC}	-1	-	1	μA
Average operating current	I _{CC1}	Cycle time=1μs, 100%duty, I _{IO} =0mA, $\overline{CS}_1 \leq 0.2V$, $\overline{LB} \leq 0.2V$ or/and $\overline{UB} \leq 0.2V$, $CS_2 \geq V_{CC}-0.2V$, V _{IN} ≤0.2V or V _{IN} ≥V _{CC} -0.2V	-	-	2	mA
	I _{CC2}	Cycle time=Min, I _{IO} =0mA, 100% duty, $\overline{CS}_1=V_{IL}$, CS ₂ =V _{IH} , $\overline{LB}=V_{IL}$ or/and $\overline{UB}=V_{IL}$, V _{IN} =V _{IL} or V _{IH}	70ns 55ns	- -	25 30	mA
Output low voltage	V _{OL}	I _{OL} = 2.1mA	-	-	0.4	V
Output high voltage	V _{OH}	I _{OH} = -1.0mA	2.4	-	-	V
Standby Current (CMOS)	I _{SB1}	Other input =0-V _{CC} 1) $\overline{CS}_1 \geq V_{CC}-0.2V$, $CS_2 \geq V_{CC}-0.2V$ (\overline{CS}_1 controlled) or 2) $0V \leq CS_2 \leq 0.2V$ (CS_2 controlled)	-	1.0	20	μA

1. Typical values are measured at V_{CC}=3.0V, T_A=25°C and not 100% tested.

AC OPERATING CONDITIONS

TEST CONDITIONS (Test Load and Input/Output Reference)

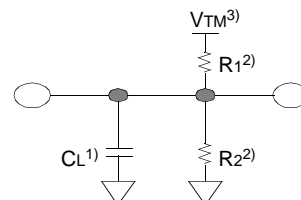
Input pulse level: 0.4 to 2.2V

Input rising and falling time: 5ns

Input and output reference voltage: 1.5V

Output load(see right): $C_L=100\text{pF}+1\text{TTL}$

$C_L=30\text{pF}+1\text{TTL}$



1. Including scope and jig capacitance
2. $R_1=3070\Omega$, $R_2=3150\Omega$
3. $V_{TM}=2.8\text{V}$

AC CHARACTERISTICS ($V_{CC}=2.7\sim 3.3\text{V}$, Industrial product: $T_A=-40$ to 85°C)

Parameter List	Symbol	Speed				Units	
		55ns		70ns			
		Min	Max	Min	Max		
Read	Read cycle time	t _{RC}	55	-	70	-	ns
	Address access time	t _{AA}	-	55	-	70	ns
	Chip select to output	t _{CO1} , t _{CO2}	-	55	-	70	ns
	Output enable to valid output	t _{OE}	-	25	-	35	ns
	$\overline{\text{UB}}$, $\overline{\text{LB}}$ valid to data output	t _{BA}	-	55	-	70	ns
	Chip select to low-Z output	t _{LZ1} , t _{LZ2}	10	-	10	-	ns
	$\overline{\text{UB}}$, $\overline{\text{LB}}$ enable to low-Z output	t _{BLZ}	10	-	10	-	ns
	Output enable to low-Z output	t _{OLZ}	5	-	5	-	ns
	Chip disable to high-Z output	t _{HZ1} , t _{HZ2}	0	20	0	25	ns
	$\overline{\text{UB}}$, $\overline{\text{LB}}$ disable to high-Z output	t _{BHZ}	0	20	0	25	ns
	Output disable to high-Z output	t _{OHZ}	0	20	0	25	ns
Output hold from address change	t _{OH}	10	-	10	-	ns	
Write	Write cycle time	t _{WC}	55	-	70	-	ns
	Chip select to end of write	t _{CW1} , t _{CW2}	45	-	60	-	ns
	Address set-up time	t _{AS}	0	-	0	-	ns
	Address valid to end of write	t _{AW}	45	-	60	-	ns
	$\overline{\text{UB}}$, $\overline{\text{LB}}$ Valid to End of Write	t _{BW}	45	-	60	-	ns
	Write pulse width	t _{WP}	40	-	50	-	ns
	Write recovery time	t _{WR}	0	-	0	-	ns
	Write to output high-Z	t _{WHZ}	0	20	0	20	ns
	Data to write time overlap	t _{DW}	25	-	30	-	ns
	Data hold from write time	t _{DH}	0	-	0	-	ns
End write to output low-Z	t _{OW}	5	-	5	-	ns	

DATA RETENTION CHARACTERISTICS

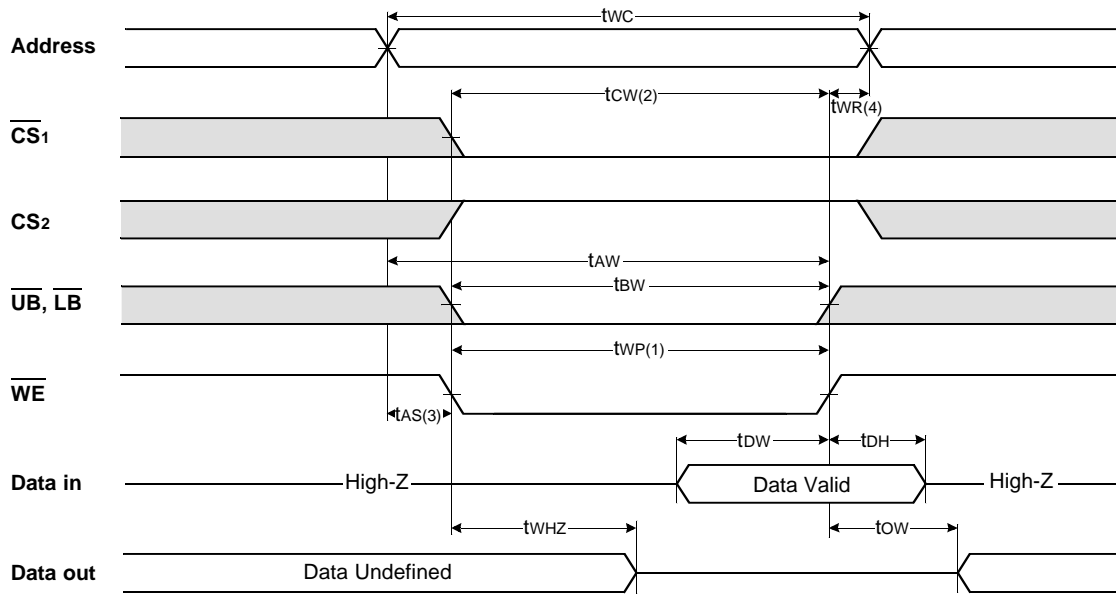
Item	Symbol	Test Condition	Min	Typ	Max	Unit
V _{CC} for data retention	V _{DR}	$\overline{\text{CS}}_1 \geq V_{CC}-0.2\text{V}^{(1)}$, $V_{IN} \geq 0\text{V}$	1.5	-	3.3	V
Data retention current	I _{DR}	$V_{CC}=1.5\text{V}$, $\overline{\text{CS}}_1 \geq V_{CC}-0.2\text{V}^{(1)}$, $V_{IN} \geq 0\text{V}$	-	1.0 ⁽²⁾	8	μA
Data retention set-up time	t _{SDR}	See data retention waveform	0	-	-	ns
Recovery time	t _{RDR}		t _{RC}	-	-	

1. 1) $\overline{\text{CS}}_1 \geq V_{CC}-0.2\text{V}$, $\text{CS}_2 \geq V_{CC}-0.2\text{V}$ ($\overline{\text{CS}}_1$ controlled) or

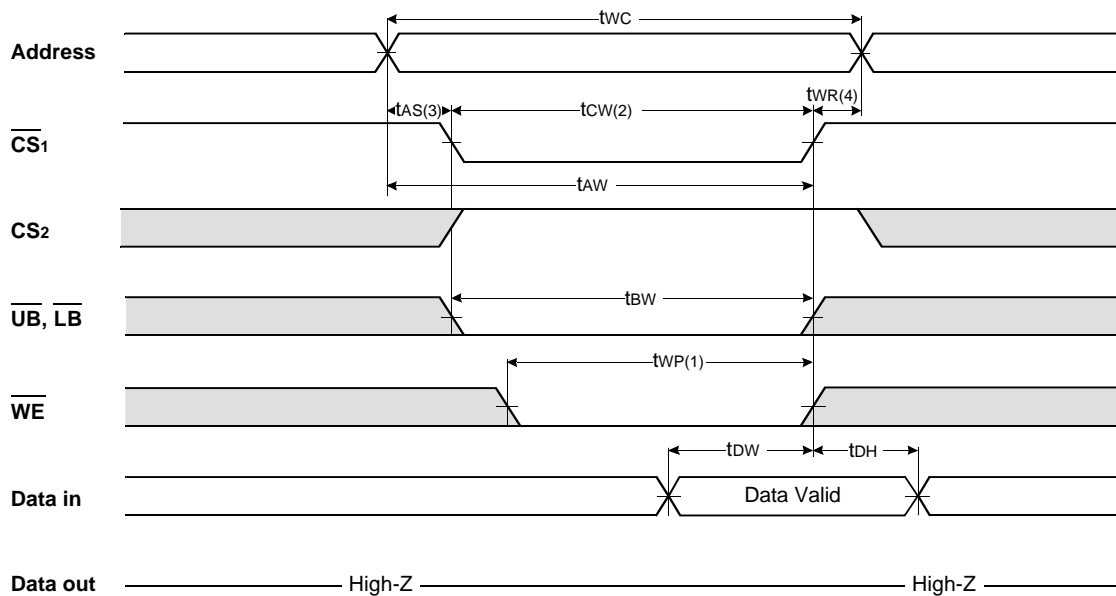
2) $0 \leq \text{CS}_2 \leq 0.2\text{V}$ (CS_2 controlled)

2. Typical value is measured at $T_A=25^\circ\text{C}$ and not 100% tested.

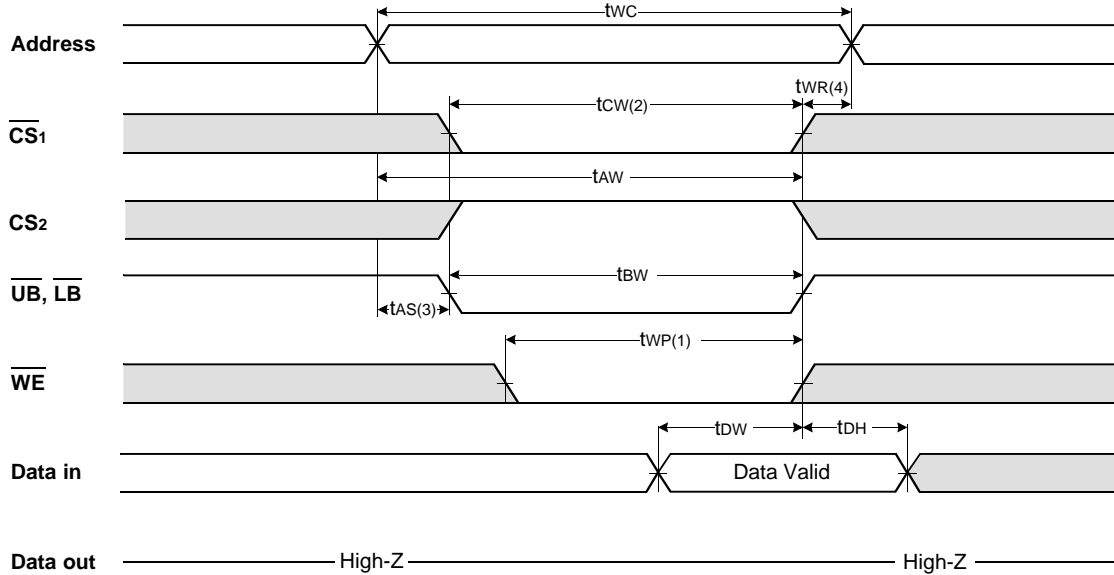
TIMING WAVEFORM OF WRITE CYCLE(1) (\overline{WE} Controlled)



TIMING WAVEFORM OF WRITE CYCLE(2) (\overline{CS}_1 Controlled)



TIMING WAVEFORM OF WRITE CYCLE(3) (\overline{UB} , \overline{LB} Controlled)

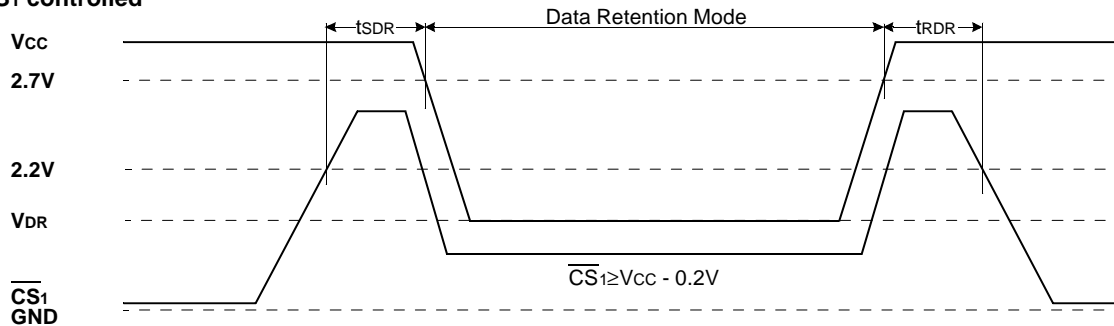


NOTES (WRITE CYCLE)

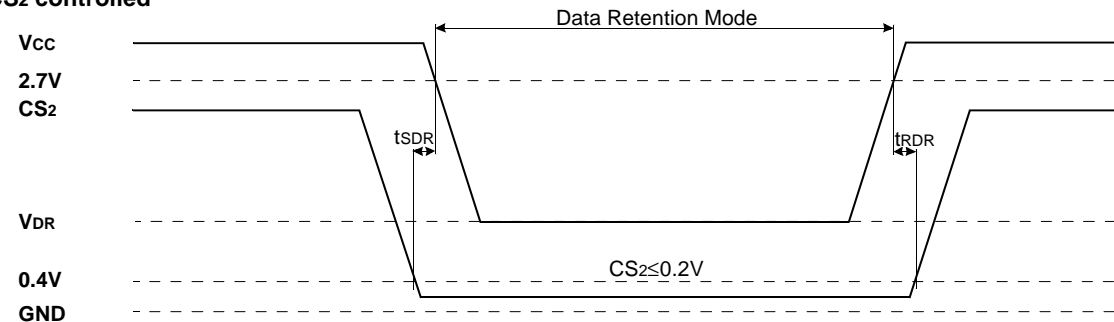
1. A write occurs during the overlap (t_{WP}) of low $\overline{CS1}$ and low \overline{WE} . A write begins when $\overline{CS1}$ goes low and \overline{WE} goes low with asserting \overline{UB} or \overline{LB} for single byte operation or simultaneously asserting \overline{UB} and \overline{LB} for double byte operation. A write ends at the earliest transition when $\overline{CS1}$ goes high and \overline{WE} goes high. The t_{WP} is measured from the beginning of write to the end of write.
2. t_{CW} is measured from the $\overline{CS1}$ going low to the end of write.
3. t_{AS} is measured from the address valid to the beginning of write.
4. t_{WR} is measured from the end of write to the address change. t_{WR} is applied in case a write ends with $\overline{CS1}$ or \overline{WE} going high.

DATA RETENTION WAVE FORM

$\overline{CS1}$ controlled



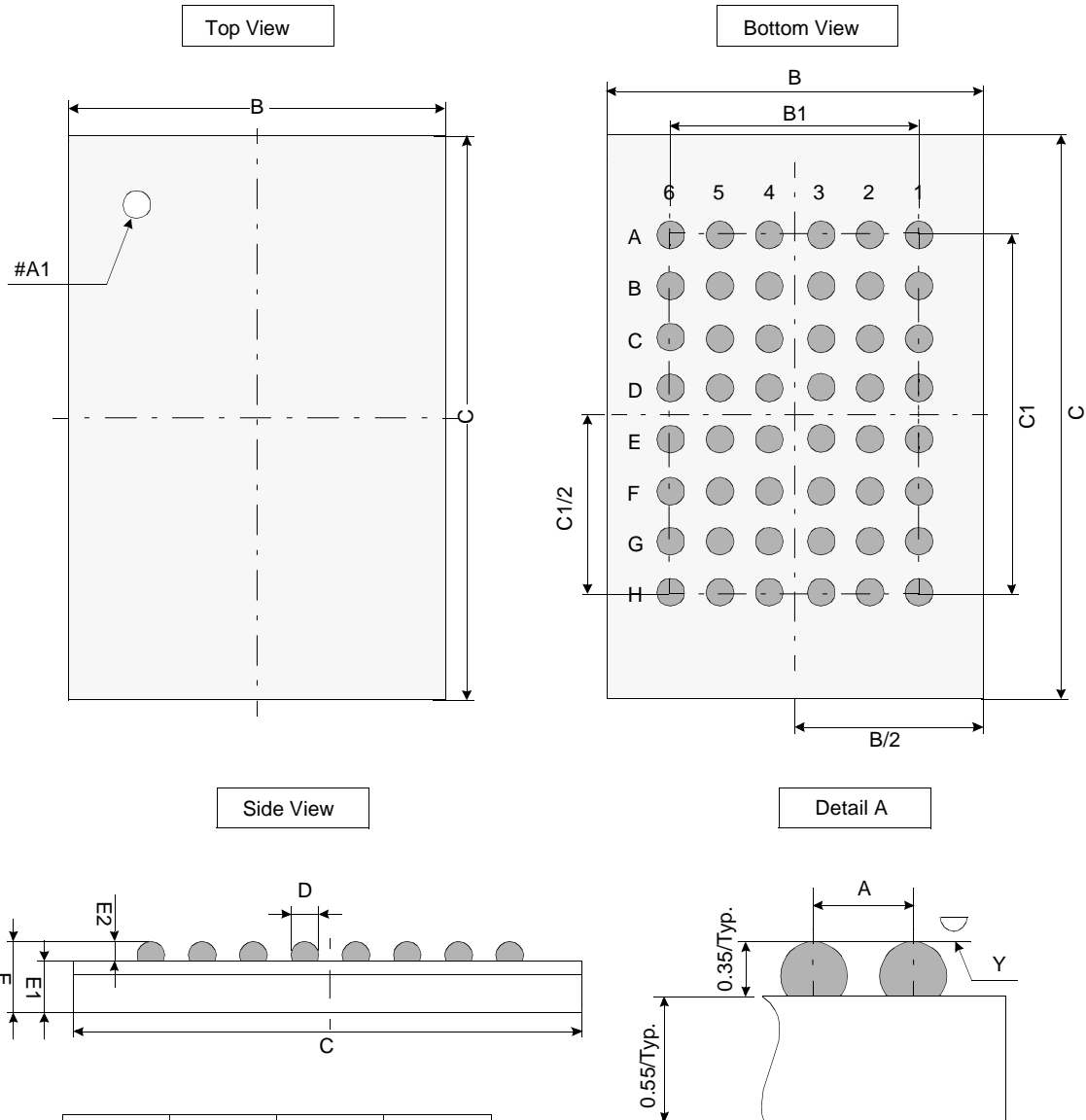
$CS2$ controlled



PACKAGE DIMENSION

Unit: millimeters

48 BALL TAPE BALL GRID ARRAY(0.75mm ball pitch)



	Min	Typ	Max
A	-	0.75	-
B	7.40	7.50	7.60
B1	-	3.75	-
C	9.40	9.50	9.60
C1	-	5.25	-
D	0.40	0.45	0.50
E	0.80	0.90	1.00
E1	-	0.55	-
E2	0.30	0.35	0.40
Y	-	-	0.08

Notes.

1. Bump counts: 48(8 row x 6 column)
2. Bump pitch: (x,y)=(0.75 x 0.75)(typ.)
3. All tolerance are ± 0.050 unless otherwise specified.
4. Typ: Typical
5. Y is coplanarity: 0.08(Max)