REALTEK SINGLE CHIP 16-PORT 10/100 ETHERNET SWITCH CONTROLLER WITH EMBEDDED MEMORY RTL8316

The Realtek RTL8316 is a highly cost-effective 16-port 10/100M Fast Ethernet switch controller which integrates a 4M-bit DRAM packet buffer, an 8K-entry look up table and a 128-entry CAM. Packaged in a 128-pin PQFP, the new chip features ultra-low power consumption as well as port-based Home VLAN, trunking, and 2-level QoS functions. With its high integration, enhanced features and micro-size, the RTL8316 provides an economic and optimal solution for design of stand-alone switches. The RTL8316 supports a Reduced MII (RMII) interface and requires only one 50MHz oscillator, saving BOM cost.

1. Features

- **Supports up to 16 10/100Mbps Full/Half duplex Ethernet ports with RMII interface**
- **All ports support Speed, Duplex and Flow-control auto-negotiation**
- **Two ports support Speed, Duplex and Flow-control by force-mode setting for fiber applications**
- **Provides non-blocking and non-head-of-line-blocking forwarding**
- **4M bit DRAM built in as packet storage buffer uses page-based buffer management to efficiently utilize the internal packet buffer**
- **Embedded 8K entry look-up table with direct mapping and 128 entries of CAM to eliminate hash collision problems**
- **Only one 50MHz OSC input for both system clock and RMII reference clock**
- **Supports tri-state design on MDC and MDIO during reset period**
- **Flow control fully supported:**
  - **Half-duplex: Back pressure**
  - **Full-duplex: IEEE 802.3x**
- **Broadcast storm filtering control**
- **Aging function supported**
- **Supports Store-and-forward operation**
- **Port Trunking supported. Four trunk groups are provided, each consisting of 4 physical ports. Trunk load balance is controlled by DA/SA hash algorithm. Trunk Port LEDs supported.**
- **Port based HOME VLAN function**
- **Supports QoS function on each port**
  - **QoS based on: (1) Port-based (2)VLAN tag (3) TCP/IP header's TOS/DS**
  - **Supports two level priority queues**
  - **Weighted round robin service**
- **128-pin PQFP, 3.3V single power technology**

2. General Description

The RTL8316 provides 16 10/100 Mbps RMII Ethernet ports. Each port can operate in a 10 Mbps or 100 Mbps data rate, and in full or half duplex mode. Speed, duplex, link status and flow control can be acquired by periodically polling the status of the PHY devices via MDIO.

Two ports can support Speed, Duplex and Flow-control abilities through force setting mode for fiber applications. The address look-up table consists of 8K entries of hash table and a 128 entries of CAM. The RTL8316 uses 13 bit MAC address direct mapping method to search the destination MAC address and record source MAC address from and to the hash table.

The RTL8316 supports IEEE 802.3x full duplex flow control and half duplex back pressure control. The ability of IEEE 802.3x flow control is auto-negotiated by writing the flow control ability via MDIO. For half duplex, the RTL8316 adopts a special back pressure design to allow forwarding of one packet successfully after 48 force collisions. This back pressure algorithm can prevent the connected repeater from being partitioned due to excessive collisions. The full/half duplex flow control ability can be enabled or disabled via a hardware strap upon reset.

The RTL8316 provides a Broadcast storm filtering function which is provided to compensate for unusual broadcast storm interference.

The RTL8316 port trunking function supports the ability to aggregate four 10/100 ports into a single logical link to increase the bandwidth between the RTL8316 and another device (switch or server) with trunking function enabled. Four Trunk Groups are supported. The trunk load balance is controlled by the DA/SA hash algorithm. The load balancing algorithm will make sure that frame distribution does not become mis-ordered , and that there is no frame duplication in the port trunk.

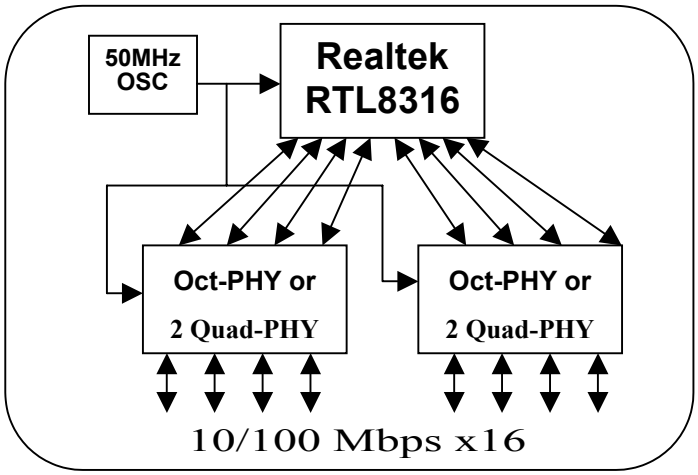
The RTL8316 supports 3 types of QoS functions to improve multi-medium or real-time networking applications. They are based on: (1) Port based priority (2) 802.1p/Q VLAN priority tag (3) TCP/IP's TOS/DS (DiffServ) field. The QoS function can be easily enabled or disabled and configured by hardware pins without any EEPROM or CPU configuration required.

There are two output queues on each output port when QoS is enabled: one is for high priority frames, the other is for low priority frames. The RTL8316 supports an intelligent adaptive flow control for high priority frames in order to avoid the flow control function, which can affect the quality of high priority frames such as real-time multi-media application traffic. By setting EnFCAutoOff high upon reset, the RTL8316 will automatically turn off the 802.3x flow control and back pressure flow control for 1~2 sec whenever the port receives high priority frames. Flow control will be re-enabled when no high priority frames are received during this 1~2 sec duration.

All system configuration and control hardware pins have a default value, implemented through internal pull-high/low resisters.

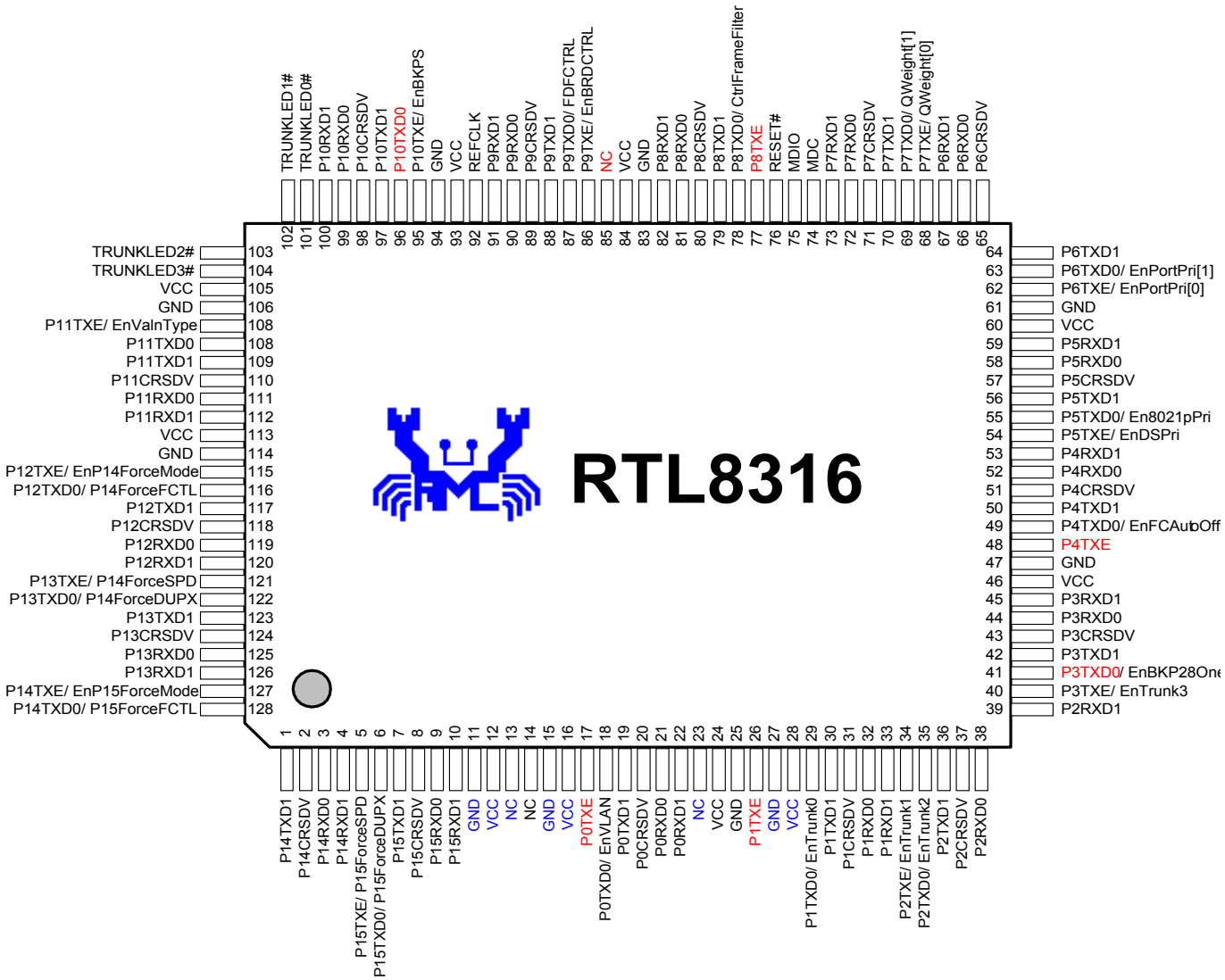
The RTL8316 supports a port based HOME Virtual Local Area Network (VLAN) function for network topology security configuration. When the port based security function is enabled, the 16 ports of the RTL8316 can be configured as 14 individual VLANs that share the same two overlapping ports. Or, the 16 ports can be configured as 15 individual VLANs that share the same one overlapping port. This 14 VLANs or 15 VLANs topology is useful to allow home networks to share a common server or router, but be configured as different VLANs for security reasons.

The RTL8316 supports non-blocking 148800 packets/second wire speed forwarding rate and includes a special design to resolve head-of-line-blocking problems. Finally, only one 50MHz OSC is needed for system design.



Example of a 16-port switch system

3. Pin Assignments



4. Pin Description

4.1 RMII Interface (Port #0 ~ Port #15)

Symbol	Type	Pin No	Description
P0TXE, P1TXE, P2TXE, P3TXE, P4TXE, P5TXE, P6TXE, P7TXE, P8TXE, P9TXE, P10TXE, P11TXE, P12TXE, P13TXE, P14TXE, P15TXE,	O	17, 26, 34, 40, 48, 54, 62, 77, 68, 86, 95, 107, 115, 121, 127, 5	**RMII Transmit Enable:** The RTL8316 asserts high to indicate that valid data for transmission is presented on the TXD[1:0]. It is synchronous with REFCLK.
P0TXD[1:0], P1TXD[1:0], P2TXD[1:0], P3TXD[1:0], P4TXD[1:0], P5TXD[1:0], P6TXD[1:0], P7TXD[1:0], P8TXD[1:0], P9TXD[1:0], P10TXD[1:0], P11TXD[1:0], P12TXD[1:0], P13TXD[1:0], P14TXD[1:0], P15TXD[1:0],	O	19,18, 30,29, 36,35, 42,41, 50,49, 56,55, 64,63, 70,69, 79,78, 88,87, 97,96, 109,108, 117,116, 123,122, 1,128, 7, 6	**RMII Transmit Data [1:0]:** The RTL8316 transmit data TXD[1:0] is clocked out by the rising edge of REFCLK.
P0CRSDV, P1CRSDV, P2CRSDV, P3CRSDV, P4CRSDV, P5CRSDV, P6CRSDV, P7CRSDV, P8CRSDV, P9CRSDV, P10CRSDV, P11CRSDV, P12CRSDV, P13CRSDV, P14CRSDV, P15CRSDV,	I	20, 31, 37, 43, 51, 57, 65, 71, 80, 89, 98, 110, 118, 124, 2, 8	**RMII CRSDV signals:** CRSDV from PHY device is asserted high when media is non-idle.

P0RXD[1:0], P1RXD[1:0], P2RXD[1:0], P3RXD[1:0], P4RXD[1:0], P5RXD[1:0], P6RXD[1:0], P7RXD[1:0], P8RXD[1:0], P9RXD[1:0], P10RXD[1:0], P11RXD[1:0], P12RXD[1:0], P13RXD[1:0], P14RXD[1:0], P15RXD[1:0],	I	22,21, 33,32, 39,38, 45,44, 53,52, 59,58, 67,66, 73,72, 82,81, 91,90, 100,99, 112,111, 120,119, 126,125, 4,3, 10,9	**RMII Receive Data [1:0]:** The RTL8316 samples the receive data RXD[1:0] on the rising edge of REFCLK when CRSDV is high.
REFCLK	I	92	**RMII Reference Clock input:** A 50 MHz signal is used for the RMII clock reference and is used to generate an internal 66 MHz system clock.

4.2 Serial Management Interface

Symbol	Type	Pin No	Description
MDC	O (P-up)	74	**Serial Management Data Clock:** Tri-state when RST# is active low.
MDIO	I/O (P-up)	75	**Serial Management Data Input/Output:** Tri-state when RST# is active low.

4.3 System Pins

Symbol	Type	Pin No	Description
RST#	I (P-up)	76	**System Reset:** Active low to reset the system to a known state. After power-on reset (low to high), the configuration modes from Mode Pins are sampled and determined, then RTL8316 will start to access the management register of PHY devices and restart the Auto-negation.

4.4 Mode Control Pins

Symbol	Type	Pin No	Description
EnP14ForceMode	I (P-down)	P12TXE	**Port 14 Force Mode Setup Enable:** Pulled high upon reset will enable port 14 to set flow control, duplex mode and speed by P14FCTRL, P14DUPLEX and P14SPEED pins separately. Otherwise, these setups will depend on port 14 auto-negotiation results. 1: Enable force mode setting 0: Disable force mode setting (Default)
P14ForceFCTRL	I (P-up)	P12TXD0	**Port 14 Flow Control Force Mode Setup:** During RST# rising edge, if EnP14ForceMode = High, this pin acts as port 14s flow control force mode setup pin, set as below: 1: Force enable flow control. (Default) 0: Force disable flow control.
P14ForceDUPLEX	I (P-up)	P13TXD0	**Port 14 Duplex Force Mode Setup:** During RST# rising edge, if EnP14ForceMode = High, this pin acts as port 14s duplex force mode setup pin set as below: 1: Force full duplex mode. (default) 0: Force half duplex mode

P14ForceSPEED	I (P-up)	P13TXE	**Port 14 Speed Force Mode Setup:** During RST# rising edge, if EnP14ForceMode = High, this pin acts as port 14s speed force mode setup pin set as below: 1: Force 100 Mbps speed. (default) 0: Force 10 Mbps speed.
EnP15ForceMode	I (P-down)	P14TXE	**Port 15 Force Mode Setup Enable:** Pulled high upon reset will enable port 15 to set flow control, duplex mode and speed by P15FCTRL, P15DUPLEX and P15SPEED pins separately. Otherwise, the setup will depends on port 15s auto-negotiation results. 1: Enable force mode setting 0: Disable force mode setting (default)
P15ForceFCTRL	I (P-up)	P14TXD0	**Port 15 Flow Control Force Mode Setup:** During RST# rising edge, if EnP15ForceMode = High, this pin acts as port 15s flow control force mode setup pin set as below: 1: Force enable flow control (default) 0: Force disable flow control
P15ForceDUPLEX	I (P-up)	P15TXD0	**Port 15 Duplex Force Mode Setup:** During RST# rising edge, if EnP15ForceMode = High, this pin acts as port 15s duplex force mode setup pin set as below: 1: Force full duplex mode (default) 0: Force half duplex mode
P15ForceSPEED	I (P-up)	P15TXE	**Port 15 Speed Force Mode Setup:** During RST# rising edge, if EnP15ForceMode = High, this pin acts as port 15s speed force mode setup pin set as below: 1: Force 100 Mbps speed (default) 0: Force 10 Mbps speed
ENBRDCTRL	I (P-down)	P9TXE	**Enable Broadcast Storm Filtering Control:** Pulled high upon reset will enable the broadcast storm control function. Pulled low upon reset will disable the broadcast storm control function.
EnCtrlFrameFilter	I (P-down)	P8TXD0	**Enable 802.1D specified reserved group MAC addresses frame filtering:** When network control frames are received with the destination MAC address as a group MAC address: (01-80-C2-00-00-03 ~ 01-80-C2-00-00-0F), the RTL8316 will drop the frames if the EnCtrlFrameFilter is set. Otherswise , it will be flooded. The value of EnCtrlFrameFilter is trapped on the power on reset. 1: Enable drop 0: Disable drop (default)
EnBKPRS	I (P-up)	P10TXE	**Enable Back pressure flow control function** During hardware reset, the pull-high/low value will control the Back pressure flow control function. 1: Enable back pressure (default) 0: Disable back pressure
ENFDFCTRL	I (P-up)	P9TXD0	**Enable Full Duplex 802.3x Flow Control:** Pulled high upon reset will enable the full duplex IEEE802.3x flow control function. The flow control ability will be written to management register 4 of the PHY device once (and only once) after power-on reset, for advertising. Pulled low upon reset will disable the full duplex flow control function.
ENTRUNK0	I/O (P-down)	P1TXD0	**Enable Port Trunk 0:** Pulled high upon reset will enable port trunk 0 which consists of ports 0,1,2,3.
ENTRUNK1	I/O (P-down)	P2TXE	**Enable Port Trunk 1:** Pulled high upon reset will enable port trunk 1 which consists of ports 4,5,6,7.
ENTRUNK2	I/O (P-down)	P2TXD0	**Enable Port Trunk 2:** Pulled high upon reset will enable port trunk 2 which consists of ports 8,9,10,11.
ENTRUNK3	I/O (P-down)	P3TXE	**Enable Port Trunk 3:** Pulled high upon reset will enable port trunk 3 which consists of ports 12,13,14,15.

ENVLAN	I (P-down)	P0TXD0	**Enable Port Based VLAN configuration function:** Latched during hardware reset. The VLAN topology is control by VlanType pin, but will be disabled if the trunking function is enabled. 1: Enable the VLAN function on each port. 0: Disable the VLAN function on each 16 ports. (default)
VlanType	I (P-down)	P11TXE	**VLAN topology type selection:** Used to select 14 VLANs or 15 VLANs topology. During hardware reset, the pull-high/low value will control the HOME VLAN topology type : 1: Select 15 VALNs (port#0~14) with 1 overlapping port (port #15) topology. 0: Select 14 VLANs (port#0~13) with 2 overlapping ports (port #14,15) topology. **(default)**
EnPortPri[1:0]	I (P-down, P-down)	[P6TXD0, P6TXE]	**Enable Port based priority QoS function:** Latched during hardware reset. Setting as follows: 00: Disable port based priority. (default) 01: Set port#0~1 as high priority ports. (2 ports) 10: Set port#0~3 as high priority ports. (4 ports) 11: Set port#0~7 as high priority ports. (8 ports)
En8021pPri	I (P-down)	P5TXD0	**Enable 802.1p VLAN Tag priority based QoS function:** Latched during hardware reset. 1: Enabled 0: Disabled (default)
EnDSPri	I (P-down)	P5TXE	**Enable TCP/IP TOS/DS (DiffServ) based QoS function:** Latched during hardware reset. 1: Enabled **High Priority**: if TOS/DS[0:5] = (EF) "101110"; (AF) "001010", "010010", "011010", "100010"; (Network Control) "11x000"; **Low Priority**: if TOS/DS = other codepoint values. 0: Disabled (default) (DS = Differentiated Service)
QWEIGHT[1:0]	I (P-up, P-up)	[P7TXD0, P7TXE]	**Weighted round robin ration of priority queue:** Latched during hardware reset. The frame service rate is High-pri queue: Low-pri queue 11 = always high priority queue first (default) 10 = 8:1 01 = 4:1 00 = 2:1
EnFCAutoOff	I (P-down)	P4TXD0	**Enable Flow Control Ability Auto Turn Off:** Latched during hardware reset. Enable Auto turn off low priority queue's flow control ability 1~2 seconds whenever the port received a high priority frame. The flow control ability will be re-enabled when no high priority frames are received for the 1~2 second period. 1: Enabled 0: Disabled

4.5 LED Pins

Symbol	Type	Pin No	Description
TRUNKLED0#	I/O (P-down)	101	**Port Trunk 0 Status LED:** After reset, this pin acts as the port trunk 0 status LED. The LED will be active low when port trunk 0 is enabled. It will blink for 250ms ON and 250ms OFF when any physical port link failures occur within the enabled port trunk. It is dark when port trunk 0 is disabled.
TRUNKLED1#	I/O (P-down)	102	**Port Trunk 1 Status LED:** After reset, this pin acts as the port trunk 1 status LED. The LED will be active low when port trunk 1 is enabled. It will blink for 250ms ON and 250ms OFF when any physical port link failures occur within the enabled port trunk. It is dark when port trunk 1 is disabled.
TRUNKLED2#	I/O (P-down)	103	**Port Trunk 2 Status LED:** After reset, this pin acts as the port trunk 2 status LED. The LED will be active low when port trunk 2 is enabled. It will blink for 250ms ON and 250ms OFF when any physical port link failures occur within the enabled port trunk. It is dark when port trunk 2 is disabled.
TRUNKLED3#	I/O (P-down)	104	**Port Trunk 3 Status LED:** After reset, this pin acts as the port trunk 3 status LED. The LED will be active low when port trunk 3 is enabled. It will blink for 250ms ON and 250ms OFF when any physical port link failures occur within the enabled port trunk. It is dark when port trunk 3 is disabled.

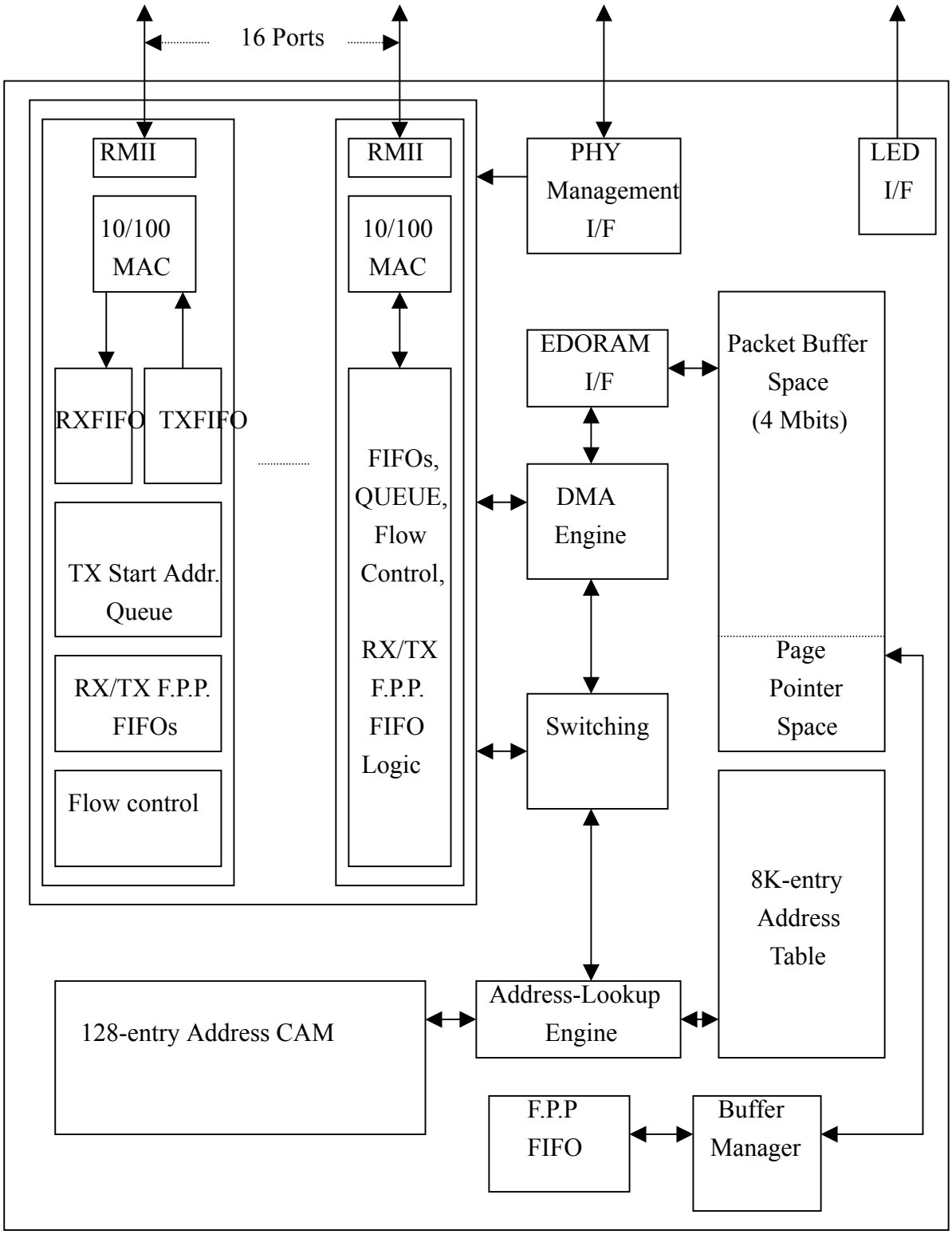
4.6 Power / Ground Pins

Symbol	Type	Pin No	Description
VCC for I/O & Core	I	24,46,60, 84,93, 105,113,	**Digital Power Supply** (7 pins)
GND for I/O & Core	I	25,47,61, 83,94, 106,114,	**Digital Ground** (7 pins)
VCC for embedded DRAM	I	12,16,28	**Embedded DRAM Power Supply** (3 pins)
GND for embedded DRAM	I	11,15,27	**Embedded DRAM Ground** (3 pins)

4.7 Test Pins

Symbol	Type	Pin No	Description
EnAcceptErr	I (P-down)	P4TXE	**Enable Accept Error Packets:** Enables the RTL8316 to accept error packets and forward them to the destination port. But the acceptable error packet is only limited to 64 ~ 1536 bytes. Note: Used for testing only. Do Not pull-up this pin.
ENBKP28ONE	I (P-up)	P3TXD0	**Realtek Internal Test Pin:** Please back up an external 10K pull low resister for advanced configuration and testing.
DscThrTest	I (P-down)	P0TXE	**Realtek Internal Test Pin:** Please back up an external 10K pull up resister for advanced configuration and testing.
NC (IpgCompTest)	I (P-up)	P10TXD0	**Realtek Internal Test Pin:** Please back up an external 10K pull low resister for advanced configuration and testing.
NC (DRAMPWTest)	I/O	13, 23	**Realtek Internal Test Pin:** Please keep these pins floating.
NC (ExtCKITest)	I	85	**Realtek Internal Test Pin:** Please keep this pin floating.
NC (ExtCKSTest)	I (P-down)	P1TXE	**Realtek Internal Test Pin:** Please keep this pin floating.
NC	-	14	**Reserved:** Please keep this pin floating.

5. Block Diagram



6. Functional Description

6.1 Reset

After hardware reset, the RTL8316 will determine some default settings through the hardware strap pins and then write abilities to connected PHY management registers via MDC/MDIO. It is most important that the RTL8316 and connected PHYs use the same reset signal source. Otherwise, if the reset action of PHY is finished after the RTL8316, there is no guarantee of proper operation on the expected port speed, duplex and flow control ability.

6.2 RMII interface

The RTL8316 provides a 10/100 Mbps low pin count RMII interface to connect with PHYs. The RMII is capable of supporting 10Mbps and 100Mbps data rates. A single clock reference, 50MHz, sourced from an external clock input, is used for receive and transmit. It also provides independent 2 bit wide (di-bit) transmit and receive data paths. As the REFCLK is 10 times the data rate in 10Mbps mode each data di-bit must be output on TXD[1:0] and input on RXD[1:0] for ten consecutive REFCLK cycles. The RTL8316 can regenerate the COL signal of the MII internally by ANDing TXEN and CRS as recovered from CRSDV. Note that TXEN cannot be ANDed directly with CRSDV since CRSDV may toggle at the end of the frame to provide separation of RXDV and CRS.

RMII Specification Signals are as below,

Signal Name	Direction (with respect to the PHY)	Direction (with respect to the RTL8316)	Description
REFCLK	Input	Input	Synchronous clock reference for receive, transmit and control interface.
CRSDV	Output	Input	Carrier Sense/Receive Data Valid
RXD[1:0]	Output	Input	Receive Date
TXEN	Input	Output	Transmit Enable
TXD[1:0]	Input	Output	Transmit Data

6.3 Serial Management Interface MDC/MDIO

The RTL8316 supports PHY management through the serial MDIO and MDC signal lines (SMI). After power on reset, the RTL8316 write abilities to the advertisement register 4 of connected PHY and restarts the auto-negotiation process through MDIO using PHY, addressed incrementally from 10000b (16) to 11111b (31). After restarting auto-negotiation, the RTL8316 will continuously read the link status and link partner's ability which includes speed, duplex and flow control of the PHY devices via MDIO.

When the RST# pin is asserted low, the MDC and MDIO pins are both in a tri-state. This feature provides the ability for an external controller to access PHY's internal registers easily by using the same serial management interface during the period of RST# active low. When RST# is active high, the MDC changes to be an output pin and MDIO becomes an I/O pin.

Following is the SMI management frame format:

	Management frame fields							
	PRE	ST	OP	PHYAD	REGAD	TA	DATA	IDLE
READ	1…1	01	10	AAAAA	RRRRR	Z0	DDDDDDDDDDDDDDDD	Z
WRITE	1…1	01	01	AAAAA	RRRRR	10	DDDDDDDDDDDDDDDD	Z

6.4 Address Search and Learning

The address look-up table consists of 8K entries of hash table and 128 entries of CAM. The RTL8316 uses the last 13 bits of MAC address Direct Mapping method to index the 8K-entry look-up table for address searching and learning. If the mapped location in the 8K entries is occupied, then the RTL8316 will compare the destination MAC address with the contents of the CAM for address searching and store source MAC address to CAM for address learning. The 128 entry CAM can avoid the address hash collision and will improve the switch network performance.

6.5 Address Aging

The address aging function supports the ability to keep the contents of the address table to be the most recent and correct in a dynamic network topology. A learned source address entry will be cleared (aging out) if it is not updated by the address learning process during an aging time period. The default aging timer of the MAC address look-up table is about 300 sec.

6.6 Illegal Frames

Illegal frames such as a bad CRC packet, runt packet (less than 64 bytes) or oversized packet (greater than 1536) will be discarded.

6.7 802.1D Reserved Group Addresses Filtering

The RTL8316 supports the ability to enable or disable the drop frames function of the 802.1D specified reserved group MAC addresses: 01-80-C2-00-00-03 to 01-80-C2-00-00-0F. The RTL8316 default setting will disable dropping of these reserved group MAC address control frames. The frames with group MAC address 01-80-C2-00-00-01~2 will always be filtered.

6.8 Back off Algorithm

The RTL8316 implements the truncated exponential back off algorithm compliant to the IEEE 802.3 standard. The collision counter will be restarted after 16 consecutive collisions.

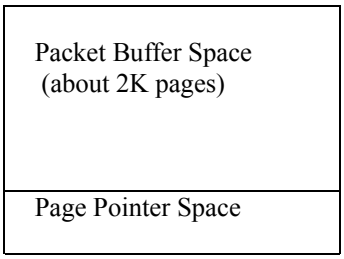
6.9 Inter-Frame Gap

The Inter-Frame Gap is 9.6us for 10Mbps Ethernet and 960ns for 100Mbps fast Ethernet.

6.10 Buffer Management

An embedded 4M bit (512K Bytes) DRAM is built-in as a packet storage buffer. To efficiently utilize the packet buffer, the RTL8316 divides the 4Mbit (512 Kbytes) DRAM into 2K pages of storage spaces, i.e., per page contains 256 bytes. For Ethernet packets, a maximum of seven pages can be used and the minimum is one.

The embedded DRAM is divided into two parts. The first is the Packet Buffer Space, used for storing received packet data. The second is Page Pointer Space for buffer management. The Packet Buffer Space consists of about 2k storage units in a page. Each page consists of 16-byte Header information, including next page pointer and received byte count, and 240 bytes of data. The page pointers are contained in Page Pointer Space.



4M bit DRAM

6.11 Buffer Manager

The Buffer Manager of the RTL8316 contains a Free Page Pointer FIFO pool to store and provide available free page pointers to all ports. After power up reset, the Buffer Manager will initiate the *Descriptor Read* command to get some available free page pointers from Page Pointer Space. When the contents of the Free Page Pointer FIFO is almost empty due to continuous data receptions, the Descriptor Read command will be reinitiated to get more available free page pointers. However, when the FIFO contents is almost full due to continuous successful data transmissions, the RTL8316 initiates the *Descriptor Write* command to write the additional available free page pointers back to Page Pointer Space.

6.12 Data Reception

Each port contains a Receive Data FIFO and a Receive Free Page Pointer FIFO. Initially the Free Page Pointer FIFO is filled with free page pointers received from the Buffer Manager. On reception of a packet, the received data flows into the Receive Data FIFO first and then is moved into the Packet Buffer by the Receive DMA Engine, using the free page pointers in the Receive Free Page Pointer FIFO via the *Get Free Page* command. The RTL8316 always attempts to fill the Receive Free Page Pointer FIFO with free page pointers.

6.13 Data Forwarding

Each port also contains a Transmit Data FIFO, a Transmit Free Page Pointer FIFO and a Transmit Start Address Queue. Once a forwarding condition is met (for store-and-forward mode a packet is completely received) the receiving port will pass the beginning page pointer using the Send TX Descriptor command to the transmit port and start the Transmit DMA. The transmission port stores the beginning page pointer in the Transmit Start address Queue. The Transmit DMA moves data from the Packet Buffer through the Transmit Data FIFO and to the RMII interface using the free page pointer in the Transmit Free Page Pointer FIFO. Once the packet has been forwarded successfully, the RTL8316 uses the Put Free Page command to put related free page pointers back to buffer manager's Free Page Pointer FIFO.

6.14 Flow Control

The RTL8316 supports IEEE 802.3x full duplex flow control and half duplex back pressure congestion control.

The ability of full duplex flow control is enabled by the ENFDFCTRL pin setting during H/W reset. The IEEE 802.3x flow control's ability is auto-negotiated between the remote device and the RTL8316 by writing the flow control ability via MDIO to external connected PHY.

If ENFDFCTRL is set and the 802.3x pause ability from the auto-negotiation result is enabled, the full duplex 802.3x flow control function is enabled. Otherwise, the full duplex 802.3x flow control function is disabled. When 802.3x flow control is enabled, the RTL8316 will only recognize the 802.3x flow control PAUSE ON/OFF frames with DA="0180C2000001", type="8808", OP-code="01",PAUSE Time = maximum or zero, and with good CRC.

If a PAUSE frame is received from any PAUSE flow control enabled port with DA=0180C2000001, the corresponding port of the RTL8316 will stop its packet transmission until a PAUSE timer timeout or another PAUSE frame with zero PAUSE time is received. No 802.3x PAUSE frames received from any port will be forwarded by the RTL8316.

The RTL8316 adopts a special half duplex back pressure design, forwarding one packet successfully after 48 force collisions to prevent the connected repeater from being partitioned due to excessive collisions. The half duplex back pressure flow control is controlled by EnBKPRS pin strap upon hardware reset.

6.15 Broadcast Storm Filtering Control

The RTL8316 can enable broadcast storm filtering control by hardware setting of pin ENBRDCTRL. Each port will drop broadcast packets (Destination MAC ID is ff ff ff ff ff ff) after receiving continuous 64 broadcast packets. The counter will be reset to 0 every 800ms or when receiving any non-broadcast packets (Destination MAC ID is not ff ff ff ff ff ff).

6.16 Head-Of-Line Blocking Prevention

The RTL8316 incorporates a simple mechanism to prevent Head-Of-Line blocking problems when flow control is disabled. When the flow control function is disabled, the RTL8316 will first check the destination address of the incoming packet. If the destined port is congested, then the RTL8316 will discard this packet to avoid blocking the next packet which is going to a non-congested port.

6.17 Port Trunking and Load Balance

Port Trunking is the ability to aggregate several 10/100 Mbps ports into a single logical link. There are 4 trunk groups supported by the RTL8316. Each trunk group comprises 4 fixed physical ports. They are simply identified as: Trunk0 = port{0,1,2,3}, Trunk1 = port{4,5,6,7}, Trunk2 = port{8,9,10,11}, Trunk3 = port{12,13,14,15} and are individually enabled by pins ENTRUNK[3:0] during hardware reset. Each trunk supports a trunking port status LED. The LED will be active low when the trunking function is enabled. If any physical port of a trunk group has a link down, then all of the physical ports of the trunk group will be treated as having a link down and the Trunk LED will blink for 250ms ON and 250ms OFF to indicate that a fault condition has happened on this trunk group.

The RTL8316 trunking port always sends packets over the same link path in the trunk with a given source and destination MAC address to prevent frames from becoming out of order, but the reverse path may follow a different link. The scheme of load balance between links in a trunk group is simply determined by an Index[1:0] value that is calculated by the DA and SA hash algorithm defined as follows.

The DA[0:47] SA[0:47] (order based on serial stream) hashed value Index[1:0] is calculate as below:

Index bit0 = XOR ((bits 47, 45, 43, 41, 39, 37, 35, 33 of DA),
(bits 46, 44, 42, 40, 38, 36, 34, 32 of SA))

Index bit1 = XOR ((bits 47, 45, 43, 41, 39, 37, 35, 33 of SA),
(bits 46, 44, 42, 40, 38, 36, 34, 32 of DA))

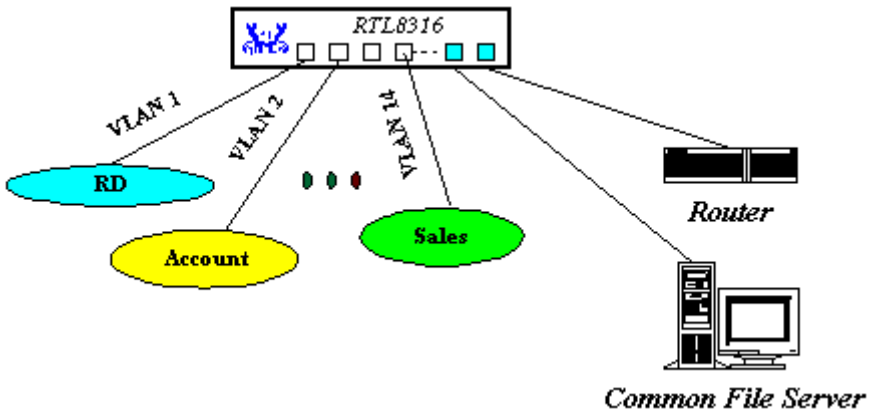
6.18 Force Mode Setting of Port ability

The RTL8316 supports Duplex/Speed/Flow Control ability force mode setup on two ports. The two ports are Port[14] and Port[15]. Each port has 4 force setting pins EnForceMode, ForceDUPLEX, ForceSPEED and ForceFCTRL. For each port, EnForceMode = 1 indicates the force mode has been enabled on the corresponding port. The corresponding port of the RTL8316 will use the duplex, speed and flow control ability as these pins are set. Furthermore, the RTL8316 will write the DUPLEX and SPEED to bit 13 and bit 8 of PHY's register 0, and bit 12 of register 0 will be written to be '0' to enable the corresponding PHY port to act at force mode. It will then continue to poll the port link status from the SMI.

6.19 Port Based HOME VLAN Function

Port based HOME VLAN function is supported by the RTL8316. The VLAN function is controlled by pin "ENVLAN" during h/w reset. When ENVLAN ='1', the VLAN function is enabled and the system is configured as 14 VLANs +2 overlapping ports or 15 VLANs +1 overlapping port topology. That is, for 14 VLANs + 2 overlapping ports topology, each port of port#0~13 is configured as an independent VLAN, and all these 14 VLANs share the same overlapping ports: port#14,15. For 15 VLANs + 1 overlapping port topology, each port of port#0~14 is configured as an independent VLAN, and all of these 15 VLANs share the same overlapping port: port#15.

For VLAN packet forwarding (ex. 14VLANs +2 overlapping ports): Any unicast/broadcast packet received from ports #0~13 can only be forward to the overlapping ports, if the destination port belongs to another VLAN, the packet will be discarded. If the source port is an overlapping port (port #14,or #15), then the frame can be forward to any destination port. This 14 VLANs or 15 VLANs topology is useful to allow home networks to share a common server or router, but be configured as different VLANs for security reasons.



Security HOME VLAN application diagram

6.20 QoS Function

The RTL8316 can recognize QoS priority information for the incoming packets for assignment of egress service priority. The RTL8316 identifies the packets as high priority based on 3 type of QoS priority information: 1) Port based priority; 2)802.1p/Q VLAN priority tag; 3)The TCP/IP TOS/DiffServ (DS) priority field. These 3 types of QoS are selected by hardware pins EnProtPri[1:0], En8021pPri and EnDSPri respectively and can be used together.

There are 2 priority queues, high and low, supported by the RTL8316 to buffer high and low priority frames. The queue service rate is based on the Weighted Round Robin algorithm. The packet based service weight ratio of high-priority and low-priority queuing can be set as 2:1, 4:1, 8:1 or "Always high priority first" by hardware pins QWeight[1:0].

When Port based priority is applied, any packet received from the high priority port, which is set by EnPortPri[1:0], will be treated as a high priority frame.

When 802.1p VLAN tag priority is applied, the RTL8316 can recognize the 802.1Q VLAN tag frames and extract the 3-bit User_Priority information from the VLAN tag. The RTL8316 will then set the threshold of User_Priority to 3. Therefore, VLAN tagged frames with User_Priority value = 4~7 will be treated as high priority frames, an other User_Priority values (0~3) as low priority frames (following 802.1p standard).

When TCP/IP's TOS/DiffServ(DS) based priority is applied, the RTL8316 can recognize TCP/IP Differentiated Services Codepoint (DSCP) priority information from the DS-field defined on RFC2474. The DS field byte for IPv4 is the Type-of-Service (TOS) octet, and for IPv6, it is the Traffic-Class octet. The recommended DiffServ Codepoints is defined in RFC2597 to classify the traffic into different service classes. The RTL8316 can extract the codepoint value of the DS-field from IPv4 and IPv6 packets, and identify the priority of the incoming IP packet following the definitions listed bellow:

High priority: whose DS-field = (EF,expected forwarding:) 101110;
(AF, Assured Forwarding:) 001010; 010010; 011010; 100010
(Network Control:) 11x000.

Low priority: whose DS-field = others values.

The VLAN tagged frame and 6-bit DS-filed in IPv4 and IPv6 frame format are shown below:

802.1Q VLAN tag frame format:

6 bytes	6 bytes	2 bytes	3 bits	
DA	SA	**81-00**	**User-Priority (0~3:Low-pri; 4~7: High-pri)**	----

IPv4/6 frame format:

6 bytes	6 bytes	4 bytes	2 bytes	4 bits	4 bits	6 bits	
DA	SA	**802.1Q Tag (optional)**	**08-00**	**Version IPv4= 0100**	IHL	**TOS[0:5] = DS-field**	----

6 bytes	6 bytes	4 bytes	2 bytes	4 bits	6 bits	
DA	SA	**802.1Q Tag (optional)**	**08-00**	**Version IPv6= 0110**	**Traffic Class [0:5] =DS-field**	----

Note: IPv6 refer to rcf2460;

The RTL8316 can automatically turn off 802.3x flow control and Back pressure flow control for 1~2 seconds whenever the port receives a high priority frames. The flow control is re-enabled when no priority frames are received for 1~2 seconds. This auto-turn off function is enabled by hardware pin EnFCAutoOff.

7. Electrical Characteristics

7.1 Temperature Limit Ratings:

Parameter	Minimum	Maximum	Units
Storage temperature	-55	+125	℃
Operating temperature	0	70	℃

7.2 DC Characteristics

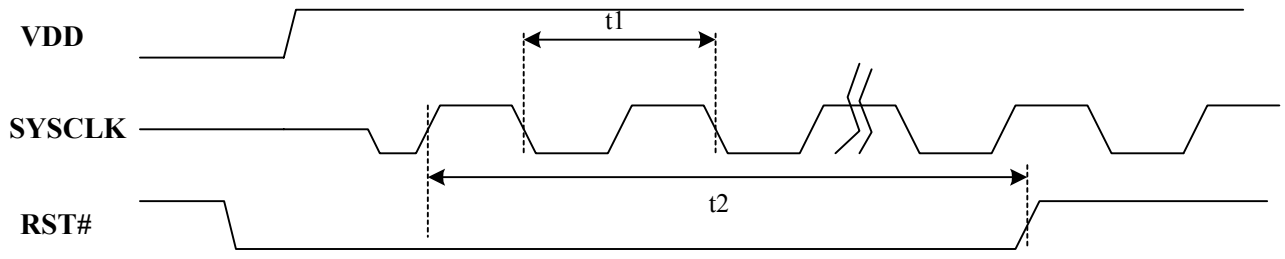
Supply voltage Vcc = 3.3V ± 5%

Symbol	Parameter	Conditions	Minimum	Typical	Maximum	Units
V_{OH}	Minimum High Level Output Voltage	I_{OH}= -8mA	0.9 * Vcc		Vcc	V
V_{OL}	Maximum Low Level Output Voltage	I_{OL}= 8mA			0.1 * Vcc	V
V_{IH}	Minimum High Level Input Voltage		0.5 * Vcc		Vcc+0.5	V
V_{IL}	Maximum Low Level Input Voltage		-0.5		0.3 * Vcc	V
I_{IN}	Input Current	V_{IN}=V_{CC} or GND	-1.0		1.0	μA
I_{OZ}	Tri-State Output Leakage Current	V_{OUT}=V_{CC} or GND	-10		10	μA
I_{CC}	Average Operating Supply Current	I_{OUT}=0mA,			370	mA

7.3 AC Characteristics

7.3.1 Reset and Clock Timing

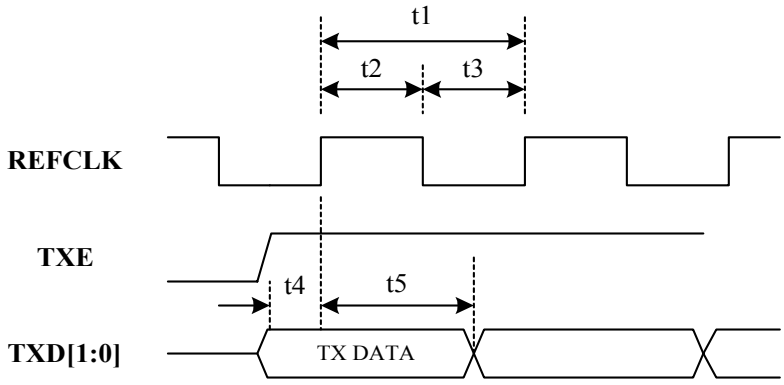
Symbol	Description	Minimum	Typical	Maximum	Units
$f_{clock\ (SYSCK)}$	SYSCLK clock frequency (= REFCLK)	--	50	--	MHZ
t1	SYSCLK clock period	--	20	--	ns
t2	RST# low pulse duration	1000	-	-	ns



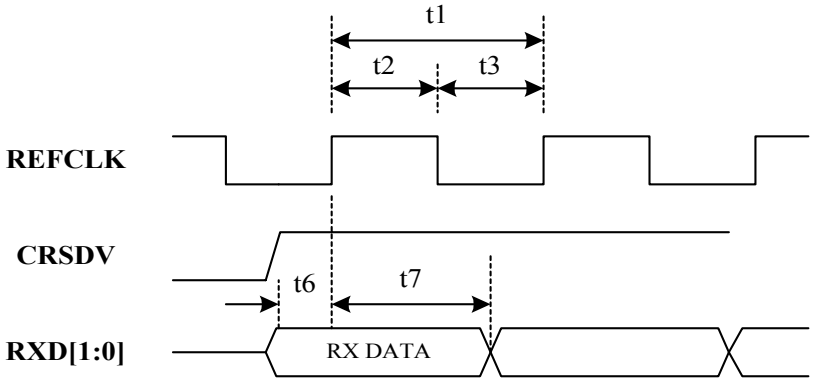
Reset and Clock Timing

7.3.2 RMII Timing

Symbol	Description	Minimum	Typical	Maximum	Units
t1	REFCLK clock period (frequency =50Mhz 50ppm)	-	20	-	ns
t2	REFCLK high level width	-	10	-	ns
t3	REFCLK low level width	-	10	-	ns
t4	TXE,TXD to REFCLK rising setup time	4	-	-	ns
t5	TXE,TXD to REFCLK rising hold time	2	-	-	ns
t6	CSRDV,RXD to REFCLK rising setup time	4	-	-	ns
t7	CRSDV,RXD to REFCLK rising hold time	2	-	-	ns



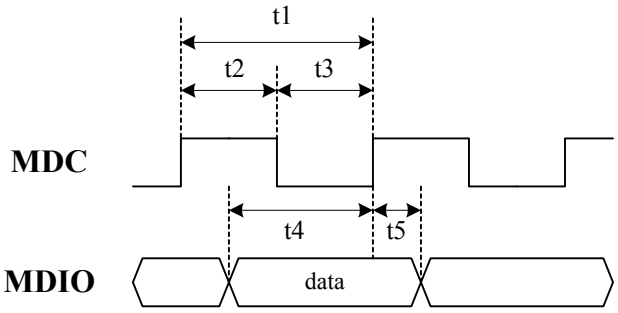
RMII Transmit Timing



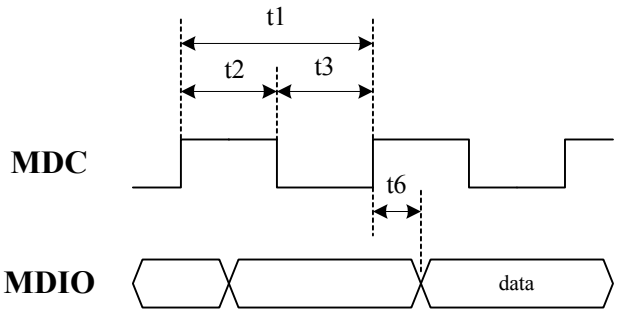
RMII Receive Timing

7.3.3 PHY Management (SMI) Timing

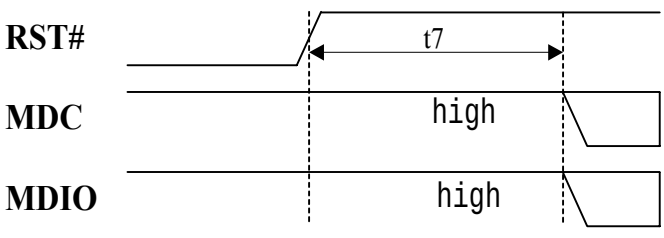
Symbol	Description	Minimum	Typical	Maximum	Units
t1	MDC clock period	-	SYSCK * 32	-	ns
t2	MDC high level width	-	SYSCK * 16	-	ns
t3	MDC low level width	-	SYSCK * 16	-	ns
t4	MDIO to MDC rising setup time (Write Bits)	10	-	-	ns
t5	MDIO to MDC rising hold time (Write Bits)	10	-	-	ns
t6	MDC to MDIO delay (Read Bits)	-	-	20	ns
t7	MDC/MDIO actives from RST# deasserted	-	500	-	us



MDIO Write Timing

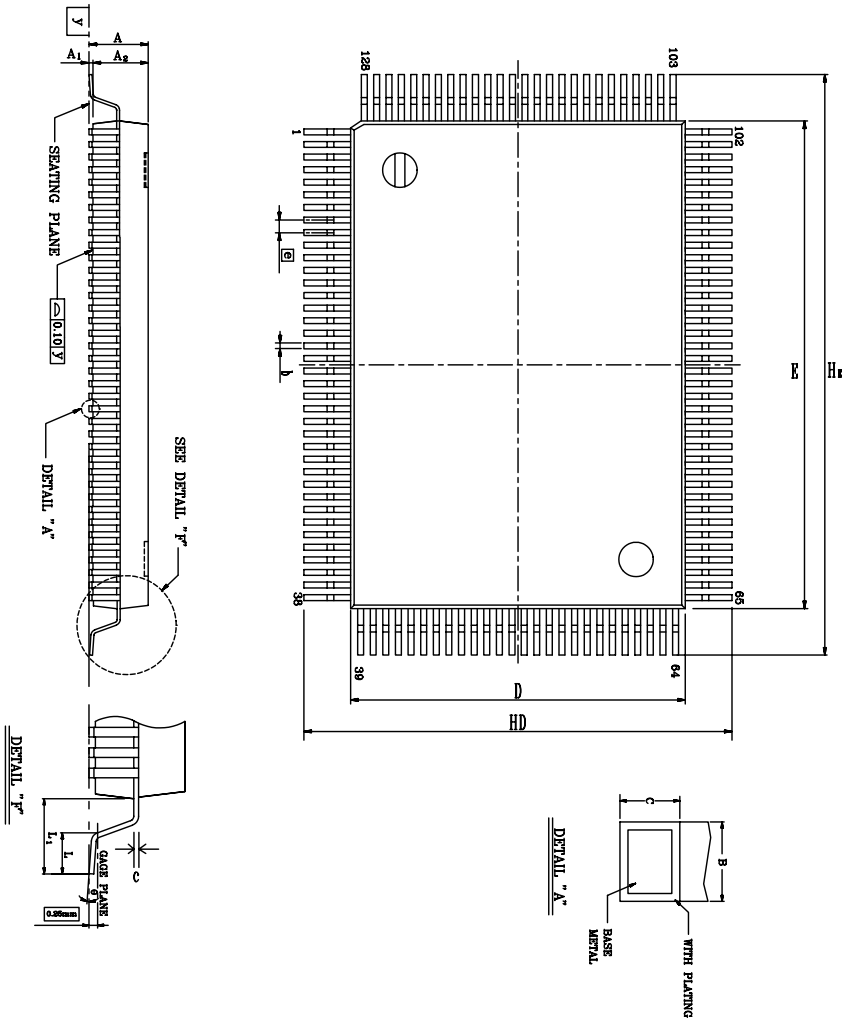


MDIO Read Timing



MDC/MDIO Reset Timing

8. Mechanical Information



Symbol	Dimension in inch			Dimension in mm		
	Min	Typical	Max	Min	Typical	Max
A	-	-	0.134	-	-	3.40
A1	0.004	0.010	0.036	0.10	**0.25**	0.91
A2	0.102	0.112	0.122	2.60	**2.85**	3.10
b	0.005	0.009	0.013	0.12	**0.22**	0.32
c	0.002	0.006	0.010	0.05	**0.15**	0.25
D	0.541	0.551	0.561	13.75	**14.00**	14.25
E	0.778	0.787	0.797	19.75	**20.00**	20.25
e	0.010	0.020	0.030	0.25	**0.5**	0.75
HD	0.665	0.677	0.689	16.90	**17.20**	17.50
HE	0.902	0.913	0.925	22.90	**23.20**	23.50
L	0.027	0.035	0.043	0.68	**0.88**	1.08
L1	0.053	0.063	0.073	1.35	**1.60**	1.85
y	-	-	0.004	-	-	0.10
θ	0°	-	12°	0°	-	12°

1. Dimensions D & E do not include interlead flash.
2. Dimension b does not include dambar protrusion/intrusion.
3. Controlling dimension: Millimeter
4. General appearance spec. should be based on final visual inspection spec.

9. Revision History

Revision	Version State	Date	Description of Change
1.0	Draft	02/16/2001	Original document.
1.1	Draft	02/27/2001	1. Update Broadcast Storm Filtering Control setting method
1.2	Draft	06/15/2001	1. Update the pin assignment definition. 2. Add 802.1D reserved group MAC addresses filtering 3. Add more VALN topology mode selection:(14VLANs; 15VLANs) 4. Disable Cut-through mode. 5. modify QWeight[1:0] definition 6. Change EnBKP[1:0] as EnBKP and BKPMode two definition 7. disable SpdAge function
1.3	Draft	07/06/2001	1. Change pin name FDFCTRL as ENFDFCTRL 2. Change pin name ENBKP as ENBKPRS 3. Change pin name AcceptErr as EnAcceptErr 4. Correct some key in error. 5. Update Pin Assignment diagram.
1.4	Draft	07/27/2001	1. Change the 802.1d reserved group MAC address filtering spec 2. Modify the back pressure function 3.delete the SpdAge function
1.5	Draft	08/13/2001	1. change pin name of 8021DFilter as CtrlFrameFilter. 2. modift the Pin assignment diagram
1.6	Draft	08/15/2001	1. English grammatical check and general polish.
1.7	Draft	11/09/2001	1. SD review and check 2. add an test pin "IpgCompTest" 3. update some test pin definition. 4. Change 6.16 H-O-L Blocking to H-O-L Blocking Prevention
1.72	Final	12/12/2001	1. update mistakes of the Pin description

Realtek Semiconductor Corp.

Headquarters

1F, No. 2, Industry East Road IX, Science-based

Industrial Park, Hsinchu, 300, Taiwan, R.O.C.

Tel : 886-3-5780211 Fax : 886-3-5776047

WWW: www.realtek.com.tw