

# HD74LS374

● Octal D-type Edge-triggered Flip-Flops (with three-state outputs)

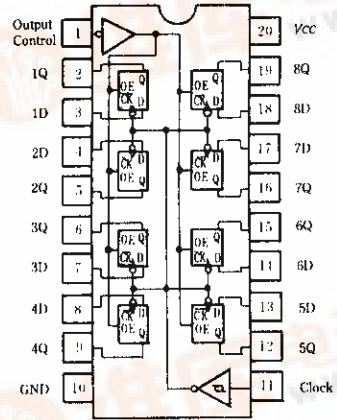
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The HD74LS374, 8-bit registers features totem-pole three-state outputs designed specifically for driving highly-capacitive or relatively low-impedance loads. The high-impedance third state and increased high-logic-level drive provide this register with the capability of being connected directly to and driving the bus lines in a bus-organized system without need for interface or pull-up components. They are particularly attractive for implementing buffer registers, I/O ports, bidirectional bus drivers, and working registers. The eight flip-flops are edge-triggered D-type flip-flops. On the positive transition the clock, the Q outputs will be set to the logic states that were setup at the D inputs.

## ■ PIN ARRANGEMENT



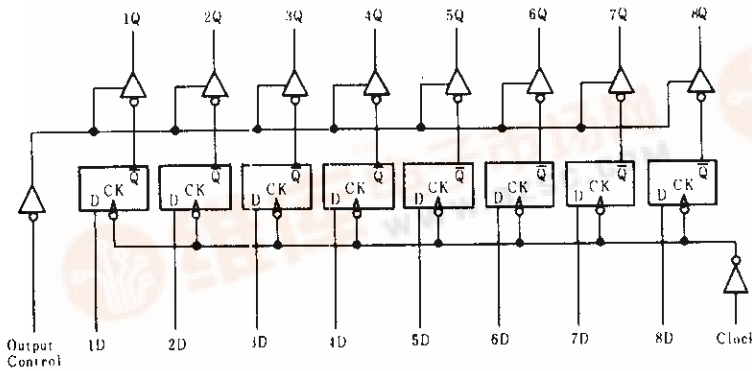
(Top View)

## ■ FUNCTION TABLE

Inputs			Output
Output control	Clock	D	Q
L	↑	H	H
L	↑	L	L
L	L	X	Q <sub>0</sub>
H	X	X	Z

Notes: H = high level, L = low level, X = irrelevant  
 ↑ = transition from low to high level  
 Q<sub>0</sub> = level of Q before the indicated steady-state input conditions were established  
 Z = off (high-impedance) state of a three-state output

## ■ BLOCK DIAGRAM



## ■ RECOMMENDED OPERATING CONDITION

Item	Symbol	min	typ	max	Unit
Supply voltage	V <sub>CC</sub>	4.75	5.00	5.25	V
Output voltage	V <sub>OH</sub>	—	—	5.5	V
Output current	I <sub>OH</sub>	—	—	-2.6	mA
	I <sub>OL</sub>	—	—	24	mA
Clock pulse width	"H" level	t <sub>w</sub>	15	—	ns
	"L" level	t <sub>w</sub>	15	—	ns
Data setup time	t <sub>su</sub>	20	↑	—	ns
Data hold time	t <sub>h</sub>	3	↑	—	ns

Note) ↑ : The arrow indicates the rising edge of clock pulse.



# HD74LS374

## ■ELECTRICAL CHARACTERISTICS ( $T_a = -20 \sim +75^\circ\text{C}$ )

Item	Symbol	Test Conditions	min	typ*	max	Unit	
Input voltage	$V_{IH}$		2.0	—	—	V	
	$V_{IL}$		—	—	0.8	V	
Output voltage	$V_{OH}$	$V_{CC} = 4.75\text{V}, V_{IH} = 2\text{V}, V_{IL} = 0.8\text{V}, I_{OH} = -2.6\text{mA}$	2.4	—	—	V	
	$V_{OL}$	$V_{CC} = 4.75\text{V}, V_{IH} = 2\text{V}, V_{IL} = 0.8\text{V}$	—	—	0.4	V	
Off-state output current	$I_{OZH}$	$V_{CC} = 5.25\text{V}, V_{IH} = 2\text{V}$	$V_O = 2.7\text{V}$	—	—	20	$\mu\text{A}$
	$I_{OZL}$		$V_O = 0.4\text{V}$	—	—	-20	
Input current	$I_{IH}$	$V_{CC} = 5.25\text{V}, V_I = 2.7\text{V}$	—	—	20	$\mu\text{A}$	
	$I_{IL}$	$V_{CC} = 5.25\text{V}, V_I = 0.4\text{V}$	—	—	-0.4	mA	
	$I_I$	$V_{CC} = 5.25\text{V}, V_I = 7\text{V}$	—	—	0.1	mA	
Short-circuit output current	$I_{OS}$	$V_{CC} = 5.25\text{V}$	-30	—	-130	mA	
Supply current	$I_{CC}$	$V_{CC} = 5.25\text{V}, V_I = 4.5\text{V}$ (Output control)	—	27	40	mA	
Input clamp voltage	$V_{IK}$	$V_{CC} = 4.75\text{V}, I_{IK} = -18\text{mA}$	—	—	-1.5	V	

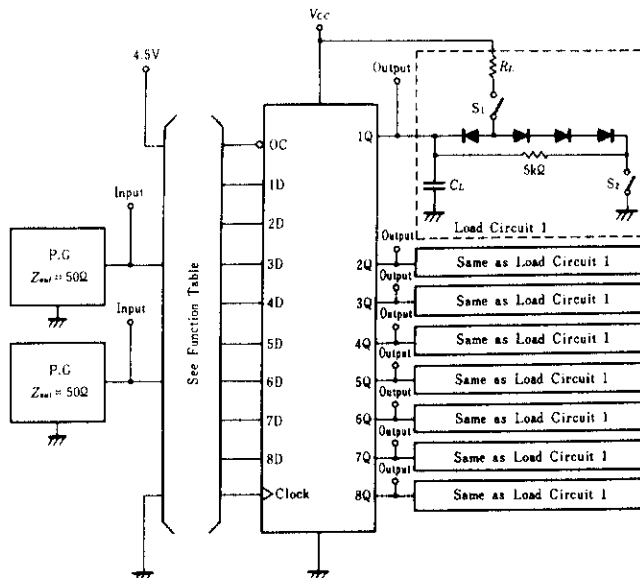
\*  $V_{CC} = 5\text{V}, T_a = 25^\circ\text{C}$

## ■SWITCHING CHARACTERISTICS ( $V_{CC} = 5\text{V}, T_a = 25^\circ\text{C}$ )

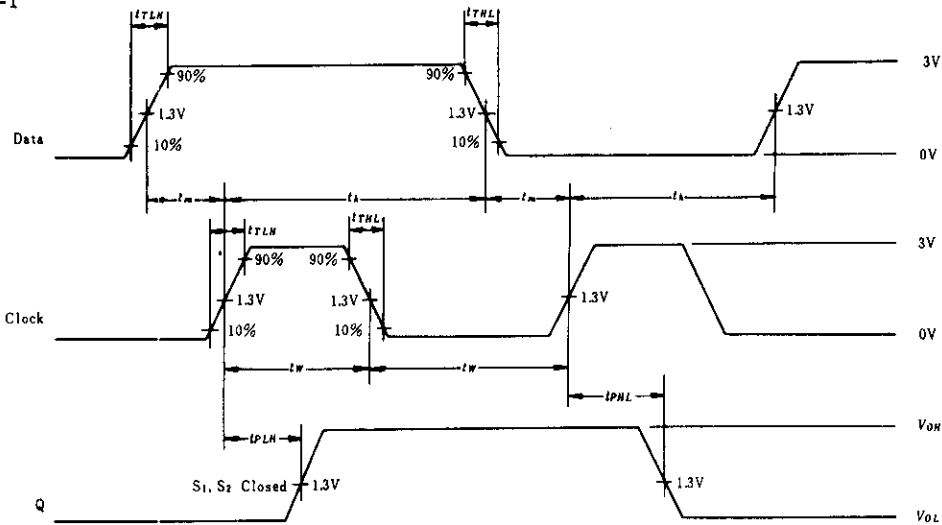
Item	Symbol	Inputs	Outputs	Test Conditions	min	typ	max	Unit
Maximum clock frequency	$f_{max}$	Clock	Q	$C_L = 45\text{pF}$ $R_L = 667\Omega$	35	50	—	MHz
Propagation delay time	$t_{PLH}$	Clock	Q		—	15	28	
	$t_{PHL}$				—	19	28	
Output enable time	$t_{ZH}$	OC	Q	$C_L = 5\text{pF}$ $R_L = 667\Omega$	—	20	28	ns
	$t_{ZL}$				—	21	28	
Output disable time	$t_{H2}$	OC	Q		—	12	20	
	$t_{L2}$				—	14	25	

## ■TESTING METHOD

### Test Circuit

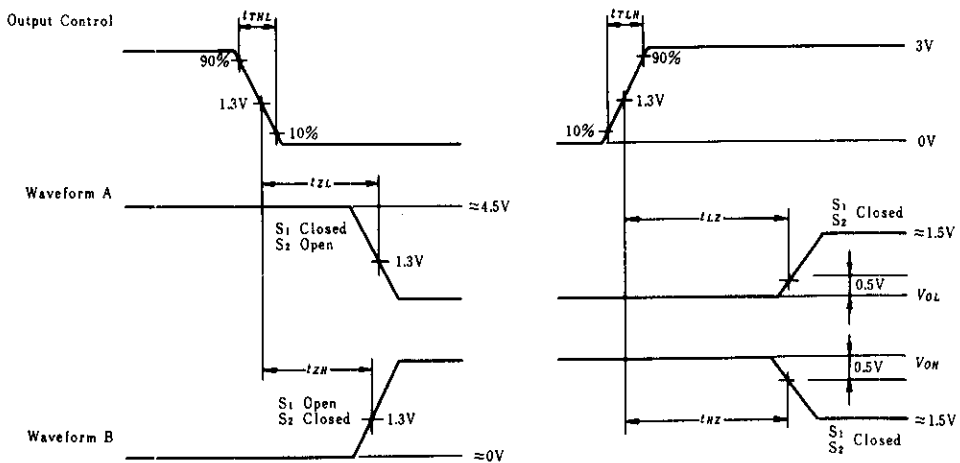


Waveform-1



- Notes:
1. Input pulse;  $t_{TLH} = 15\text{ns}$ ,  $t_{THL} = 6\text{ns}$   
 Clock input;  $PRR = 1\text{MHz}$ , duty cycle 50%  
 Data input;  $PRR = 500\text{kHz}$ , duty cycle 50%
  2.  $f_{max}$ ;  $t_{TLH} = 2.5\text{ns}$ ,  $t_{THL} = 2.5\text{ns}$

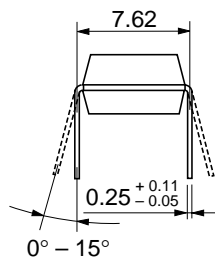
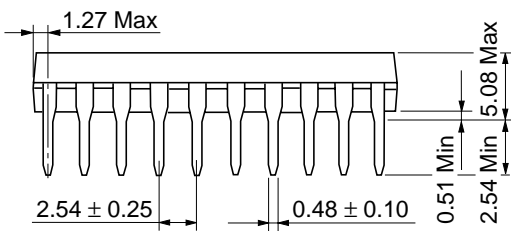
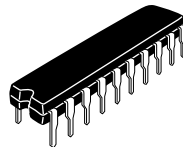
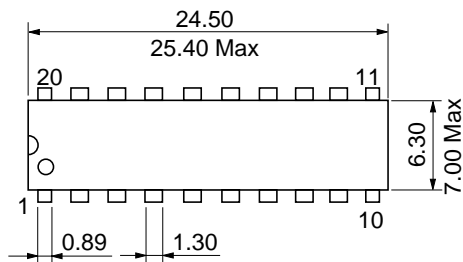
Waveform-2



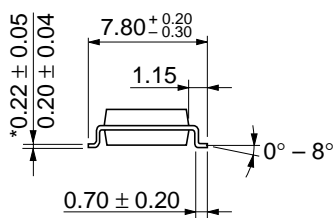
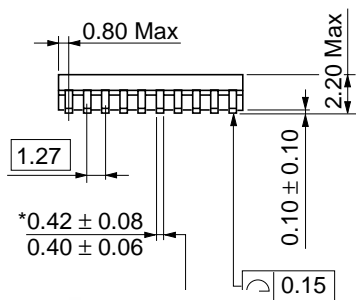
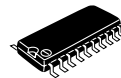
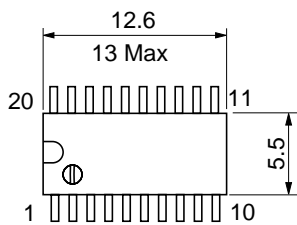
- Notes:
1. Input pulse;  $t_{TLH} = 15\text{ns}$ ,  $t_{THL} = 6\text{ns}$ ,  $PRR = 1\text{MHz}$ , duty cycle 50%
  2. Waveform A is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform B is for an output with internal conditions such that the output is high except when disabled by the output control.



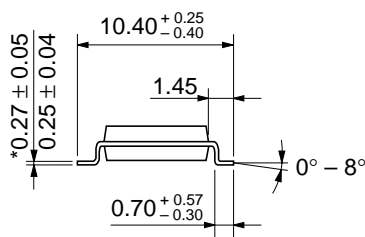
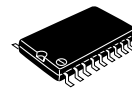
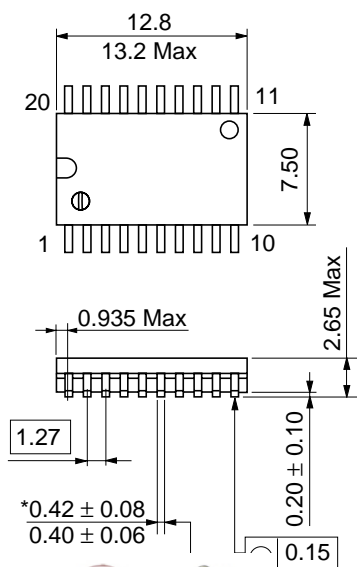
Unit: mm



Unit: mm



Unit: mm



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# HITACHI

## Hitachi, Ltd.

Semiconductor & Integrated Circuits.  
Nippon Bldg., 2-6-2, Ohte-machi, Chiyoda-ku, Tokyo 100-0004, Japan  
Tel: Tokyo (03) 3270-2111 Fax: (03) 3270-5109

URL      NorthAmerica      : <http://semiconductor.hitachi.com/>  
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### For further information write to:

Hitachi Semiconductor  
(America) Inc.  
179 East Tasman Drive,  
San Jose, CA 95134  
Tel: <1> (408) 433-1990  
Fax: <1>(408) 433-0223

Hitachi Europe GmbH  
Electronic components Group  
Dornacher StraÙe 3  
D-85622 Feldkirchen, Munich  
Germany  
Tel: <49> (89) 9 9180-0  
Fax: <49> (89) 9 29 30 00

Hitachi Europe Ltd.  
Electronic Components Group.  
Whitebrook Park  
Lower Cookham Road  
Maidenhead  
Berkshire SL6 8YA, United Kingdom  
Tel: <44> (1628) 585000  
Fax: <44> (1628) 778322

Hitachi Asia Pte. Ltd.  
16 Collyer Quay #20-00  
Hitachi Tower  
Singapore 049318  
Tel: 535-2100  
Fax: 535-1533

Hitachi Asia Ltd.  
Taipei Branch Office  
3F, Hung Kuo Building, No.167,  
Tun-Hwa North Road, Taipei (105)  
Tel: <886> (2) 2718-3666  
Fax: <886> (2) 2718-8180

Hitachi Asia (Hong Kong) Ltd.  
Group III (Electronic Components)  
7/F., North Tower, World Finance Centre,  
Harbour City, Canton Road, Tsim Sha Tsui  
Kowloon, Hong Kong  
Tel: <852> (2) 735 9218  
Fax: <852> (2) 730 0281  
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