DATA SHEET

For a complete data sheet, please also download:

- The IC06 74HC/HCT/HCU/HCMOS Logic Family Specifications
- The IC06 74HC/HCT/HCU/HCMOS Logic Package Information
- The IC06 74HC/HCT/HCU/HCMOS Logic Package Outlines

74HC/HCT4520
Dual 4-bit synchronous binary counter

Product specification
File under Integrated Circuits, IC06

December 1990

PHILIPS

FEATURES

- Output capability: standard
- I_{CC} category: MSI

GENERAL DESCRIPTION

The 74HC/HCT4520 are high-speed Si-gate CMOS devices and are pin compatible with the “4520” of the “4000B” series. They are specified in compliance with JEDEC standard no. 7A.

The 74HC/HCT4520 are dual 4-bit internally synchronous binary counters with an active HIGH clock input (nCP_0) and an active LOW clock input ($n\overline{CP}_1$), buffered outputs from all four bit positions (nQ_0 to nQ_3) and an active HIGH overriding asynchronous master reset input (nMR).

The counter advances on either the LOW-to-HIGH transition of nCP_0 if $n\overline{CP}_1$ is HIGH or the HIGH-to-LOW transition of $n\overline{CP}_1$ if nCP_0 is LOW. Either nCP_0 or $n\overline{CP}_1$ may be used as the clock input to the counter and the other clock input may be used as a clock enable input. A HIGH on nMR resets the counter (nQ_0 to nQ_3 = LOW) independent of nCP_0 and $n\overline{CP}_1$.

APPLICATIONS

- Multistage synchronous counting
- Multistage asynchronous counting
- Frequency dividers

QUICK REFERENCE DATA

GND = 0 V; T_{amb} = 25 °C; $t_r = t_f$ = 6 ns

SYMBOL	PARAMETER	CONDITIONS	TYPICAL		UNIT
			HC	HCT	
t_{PHL}/ t_{PLH}	propagation delay nCP_0, $n\overline{CP}_1$ to nQ_n	C_L = 15 pF; V_{CC} = 5 V	24	24	ns
t_{PHL}	propagation delay nMR to nQ_n		13	13	ns
f_{max}	maximum clock frequency		68	64	MHz
C_I	input capacitance		3.5	3.5	pF
C_{PD}	power dissipation capacitance per counter	notes 1 and 2	29	24	pF

Notes

1. C_{PD} is used to determine the dynamic power dissipation (P_D in μW):

   $P_D = C_{PD} \times V_{CC}^2 \times f_i + \sum (C_L \times V_{CC}^2 \times f_o)$ where:

   f_i = input frequency in MHz

   f_o = output frequency in MHz

   $\sum (C_L \times V_{CC}^2 \times f_o)$ = sum of outputs

   C_L = output load capacitance in pF

   V_{CC} = supply voltage in V

2. For HC the condition is V_I = GND to V_{CC}
   For HCT the condition is V_I = GND to V_{CC} – 1.5 V

ORDERING INFORMATION

See *“74HC/HCT/HCU/HCMOS Logic Package Information”*.

PIN DESCRIPTION

PIN NO.	SYMBOL	NAME AND FUNCTION
1, 9	$1CP_0$, $2CP_0$	clock inputs (LOW-to-HIGH, edge-triggered)
2, 10	$1\overline{CP}_1$, $2\overline{CP}_1$	clock inputs (HIGH-to-LOW, edge-triggered)
3, 4, 5, 6	$1Q_0$ to $1Q_3$	data outputs
7, 15	1MR, 2MR	asynchronous master reset inputs (active HIGH)
8	GND	ground (0 V)
11, 12, 13, 14	$2Q_0$ to $2Q_3$	data outputs
16	V_{CC}	positive supply voltage

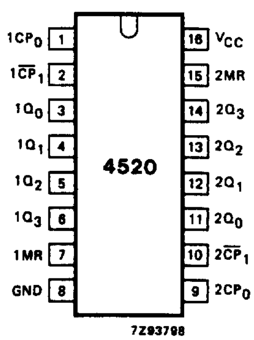

Fig.1 Pin configuration.

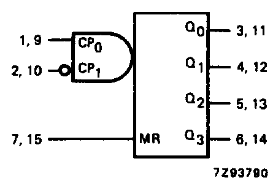

Fig.2 Logic symbol.

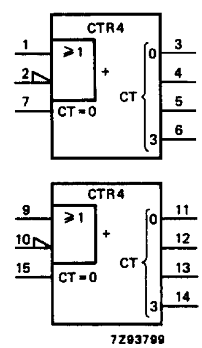

Fig.3 IEC logic symbol.

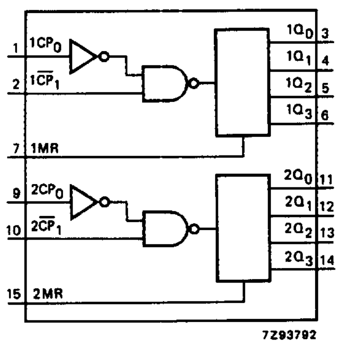

Fig.4 Functional diagram.

FUNCTION TABLE

nCP_0	$n\overline{CP}_1$	MR	MODE
↑	H	L	counter advances
L	↓	L	counter advances
↓	X	L	no change
X	↑	L	no change
↑	L	L	no change
H	↓	L	no change
X	X	H	Q_0 to Q_3 = LOW

Notes

1. H = HIGH voltage level
   L = LOW voltage level
   X = don't care
   ↑ = LOW-to-HIGH clock transition
   ↓ = HIGH-to-LOW clock transition

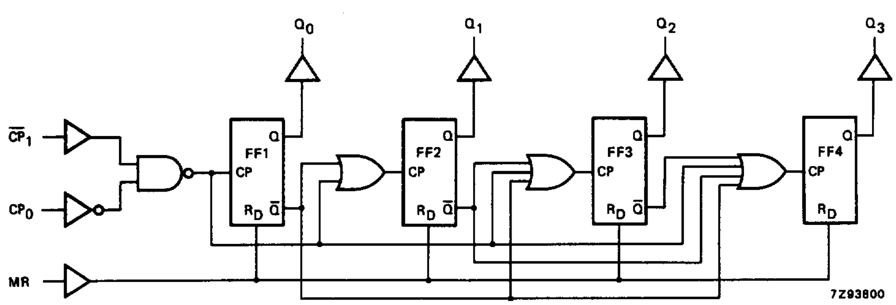

Fig.5 Logic diagram (one counter).

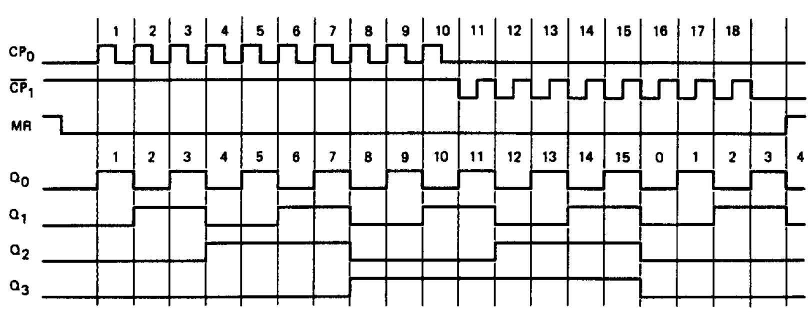

Fig.6 Timing diagram.

DC CHARACTERISTICS FOR 74HC

For the DC characteristics see *“74HC/HCT/HCU/HCMOS Logic Family Specifications”*.

Output capability: standard
I_{CC} category: MSI

AC CHARACTERISTICS FOR 74HC

GND = 0 V; $t_r = t_f = 6$ ns; $C_L = 50$ pF

SYMBOL	PARAMETER	T_{amb} (°C)							UNIT	TEST CONDITIONS	
		74HC								V_{CC} (V)	WAVEFORMS
		+25			−40 to +85		−40 to +125				
		min.	typ.	max.	min.	max.	min.	max.			
t_{PHL}/ t_{PLH}	propagation delay nCP_0 to nQ_n		77 28 22	240 48 41		300 60 51		360 72 61	ns	2.0 4.5 6.0	Fig.8
t_{PHL}/ t_{PLH}	propagation delay $n\overline{CP}_1$ to nQ_n		77 28 22	240 48 41		300 60 51		360 72 61	ns	2.0 4.5 6.0	Fig.8
t_{PHL}	propagation delay nMR to nQ_n		44 16 13	150 30 26		190 38 33		225 45 38	ns	2.0 4.5 6.0	Fig.9
t_{THL}/ t_{TLH}	output transition time		19 7 6	75 15 13		95 19 16		110 22 19	ns	2.0 4.5 6.0	Fig.8
t_W	clock pulse width HIGH or LOW	80 16 14	22 8 6		100 20 17		120 24 20		ns	2.0 4.5 6.0	Fig.7
t_W	master reset pulse width HIGH	120 24 20	39 14 11		150 30 26		180 36 31		ns	2.0 4.5 6.0	Fig.7
t_{rem}	removal time nMR to nCP_0; $n\overline{CP}_1$	0 0 0	−28 −10 −8		0 0 0		0 0 0		ns	2.0 4.5 6.0	Fig.7
t_{su}	set-up time $n\overline{CP}_1$ to nCP_0; nCP_0 to $n\overline{CP}_1$	80 16 14	14 5 4		100 20 17		120 24 20		ns	2.0 4.5 6.0	Fig.8
f_{max}	maximum clock pulse frequency	6.0 30 35	19 58 69		4.8 24 28		4.0 20 24		MHz	2.0 4.5 6.0	Fig.7

DC CHARACTERISTICS FOR 74HCT

For the DC characteristics see *"74HC/HCT/HCU/HCMOS Logic Family Specifications"*.

Output capability: standard
I_{CC} category: MSI

Note to HCT types

The value of additional quiescent supply current (ΔI_{CC}) for a unit load of 1 is given in the family specifications. To determine ΔI_{CC} per input, multiply this value by the unit load coefficient shown in the table below.

INPUT	UNIT LOAD COEFFICIENT
nCP_0, $n\overline{CP}_1$	0.80
nMR	1.50

AC CHARACTERISTICS FOR 74HCT

GND = 0 V; $t_r = t_f = 6$ ns; $C_L = 50$ pF

SYMBOL	PARAMETER	T_{amb} (°C) 74HCT +25 min.	typ.	max.	−40 to +85 min.	max.	−40 to +125 min.	max.	UNIT	TEST CONDITIONS V_{CC} (V)	WAVEFORMS
t_{PHL}/ t_{PLH}	propagation delay nCP_0 to nQ_n		28	53		66		80	ns	4.5	Fig.8
t_{PHL}/ t_{PLH}	propagation delay $n\overline{CP}_1$ to nQ_n		25	53		66		80	ns	4.5	Fig.8
t_{PHL}	propagation delay nMR to nQ_n		16	35		44		53	ns	4.5	Fig.9
t_{THL}/ t_{TLH}	output transition time		7	15		19		22	ns	4.5	Fig.8
t_W	clock pulse width HIGH or LOW	20	10		25		30		ns	4.5	Fig.7
t_W	master reset pulse width HIGH	20	12		25		30		ns	4.5	Fig.7
t_{rem}	removal time nMR to nCP_0; $n\overline{CP}_1$	0	−8		0		0		ns	4.5	Fig.7
t_{su}	set-up time $n\overline{CP}_1$ to nCP_0; nCP_0 to $n\overline{CP}_1$	16	6		20		24		ns	4.5	Fig.8
f_{max}	maximum clock pulse frequency	30	58		24		20		MHz	4.5	Fig.7

AC WAVEFORMS

Conditions:
$n\overline{CP}_1$ = HIGH while nCP_0 is triggered on a LOW-to-HIGH transition; t_W and t_{rem} also apply when nCP_0 = LOW and $n\overline{CP}_1$ is triggered on a HIGH-to-LOW transition.

(1) HC : V_M = 50%; V_I = GND to V_{CC}.
HCT: V_M = 1.3 V; V_I = GND to 3 V.

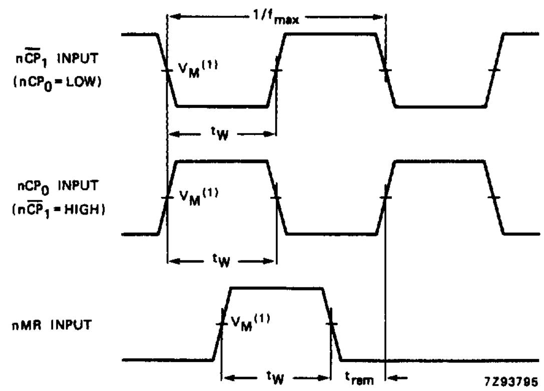

Fig.7 Waveforms showing removal time for nMR; minimum nCP_0, $n\overline{CP}_1$, nMR pulse widths and maximum clock pulse frequency.

(1) HC : V_M = 50%; V_I = GND to V_{CC}.
HCT: V_M = 1.3 V; V_I = GND to 3 V.

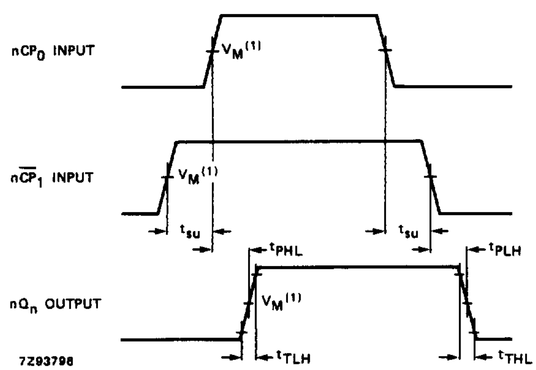

Fig.8 Waveforms showing set-up times for nCP_0 to $n\overline{CP}_1$ and $n\overline{CP}_1$ to nCP_0, propagation delays and output transition times.

(1) HC : V_M = 50%; V_I = GND to V_{CC}.
HCT: V_M = 1.3 V; V_I = GND to 3 V.

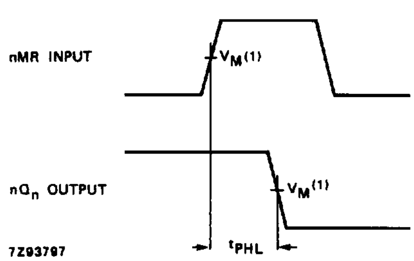

Fig.9 Waveforms showing propagation delay from nMR to nQ_n output.

PACKAGE OUTLINES

See *"74HC/HCT/HCU/HCMOS Logic Package Outlines"*.