



Data Book

AU6333

USB2.0 SD/MMC/MS

Single-LUN

Card Reader Controller

Technical Reference Manual

Product Specification

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Objective specification	This data sheet contains target or goal specifications for product development.
Preliminary specification	This data sheet contains preliminary data; supplementary data may be published later.
Product specification	This data sheet contains final product specifications.

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Jul 2005	1.01W	To modify "4.1 Pin Descriptions – pin 37"



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1.0 Introduction

1.1 Description

AU6333 is an USB2.0 high-speed transmission controller, which is designed as a bridge between USB and SD/MS compatible flash card interface, such as SD, HS-SD, MMC, HS-MMC, RS-MMC, MMCmicro, MS, MS Pro and MS Duo...etc. AU6333 can read digital contents stored on memory card designed to cover a wide area of applications such as digital cameras, PDAs, MP3 players and smart phones...etc. With the AU6333, users can transfer digital data between flash memory card and PC or other electronic devices.

AU6333 inherits the high-performance and cost-efficiency character from Alcor's products, included power switch integration, dynamic icon utility support, and speed-up engine integration. With these unique characters, AU6333 will let the manufacturers easily come into the market.

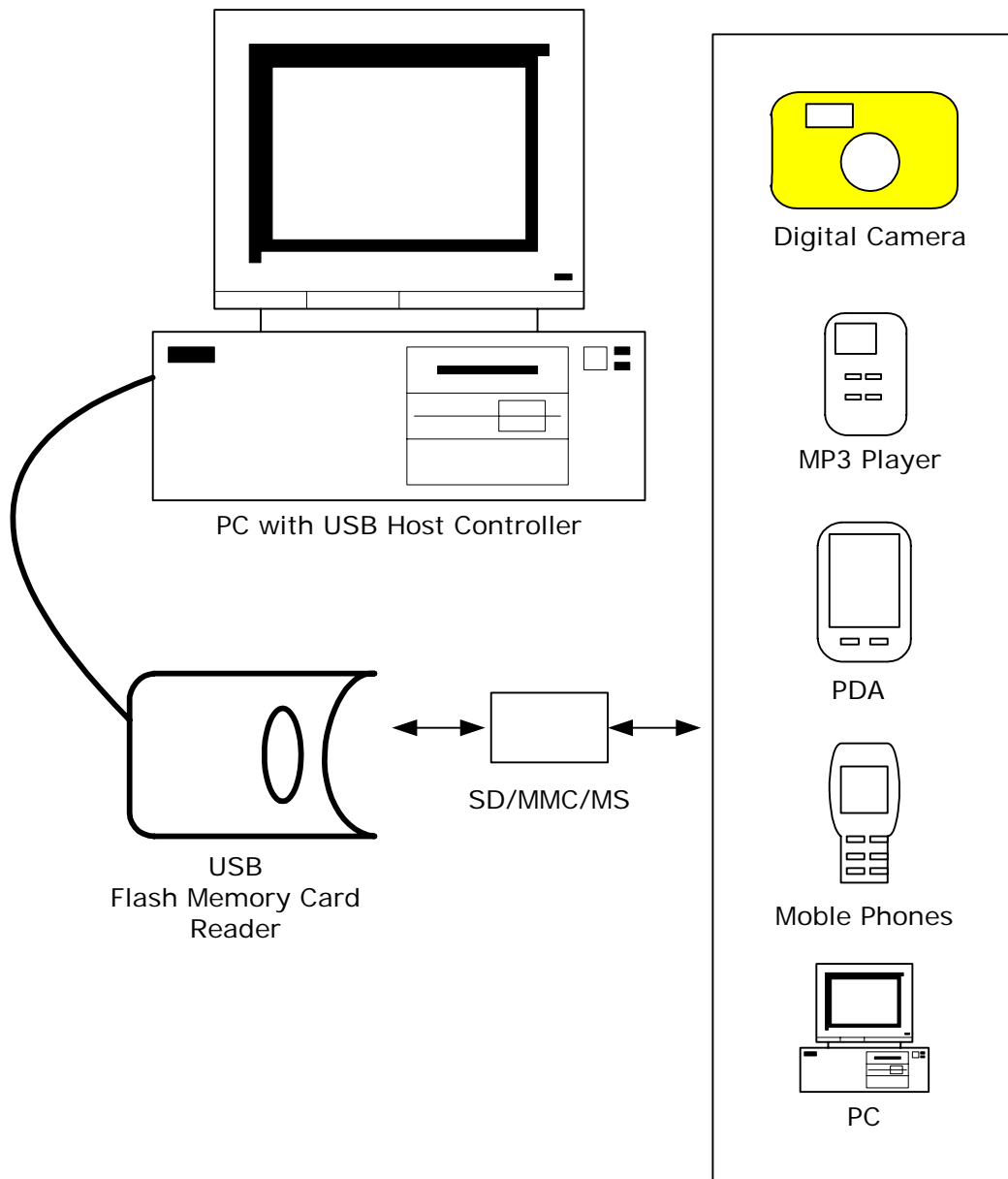
1.2 Features

- Support USB V2.0 specification and USB Device Class Definition for Mass Storage, Bulk-Transport V1.0
- Support SD/MMC/MS compatible flash card
- Support the latest flash card specification: SD1.1 (HS-SD), MMC4.0 (8-bit), MSPro parallel mode (4-bit)
- Alcor speed-up engine integrated for data transmission performance enhancement
- Work with default driver from Windows ME/2000/XP and Mac OS X; Windows 98/2000(SP1/SP2) and Mac OS 9 are supported by vendor driver from Alcor.
- Ping-pong FIFO implementation for concurrent bus operation
- Support multiple sectors transfer optimize performance
- Support slot-to-slot read/write operation (Dual LUN)
- Support Dynamic Icon Utility
- Support LED for bus operating indication
- Power switch integrated to reduce production BOM cost
- 30MHz 8051 CPU
- Built in 3.3V to 2.5V regulator

2.0 Application Block Diagram

Following is the application diagram of a typical card reader product with AU6333. By connecting the card reader to a desktop or notebook PC through USB bus, AU6333 is implemented as a bus-powered, full speed USB card reader, which can be used as a bridge for data transfer between Desktop PC and Notebook PC.

2.1 Block Diagram





3.0 Power Switch Feature

AU6333 integrates a 3.3V to 2.5V voltage regulator and power switch to replace all MOS chips for flash card power supply.

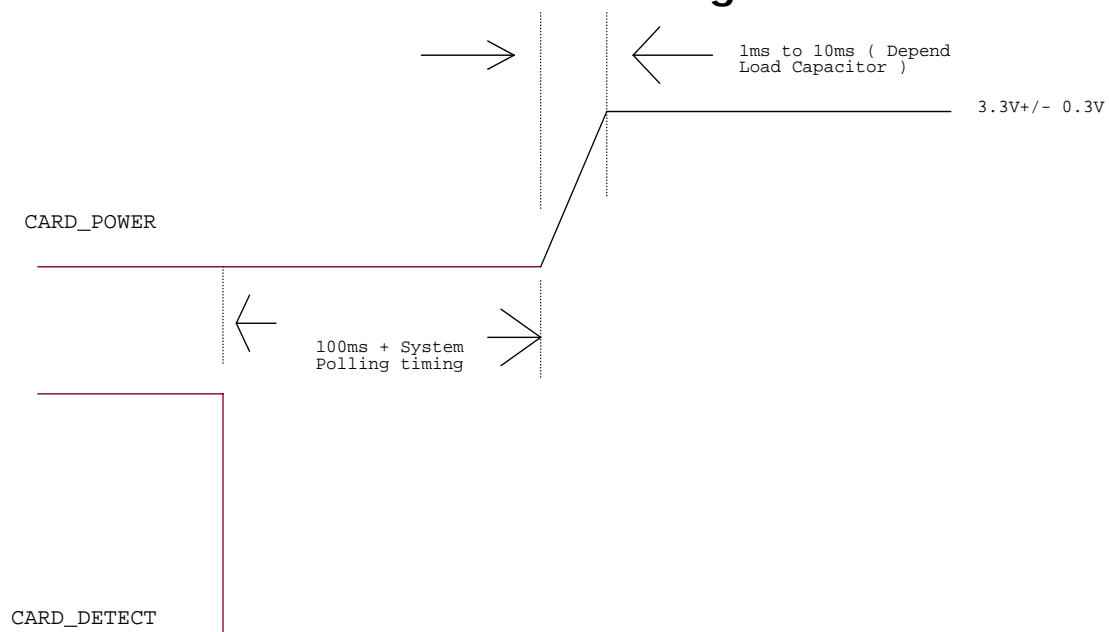
3.1 Card Power Output Current Range

- For SD/MMC/MS
 - ◆ MAX: 100mA

- Card power output voltage range
 - ◆ SD/MMC/MS: $3.3V \pm 0.3V$

- AU6333 will turn off all of Card Power in suspend mode

3.2 Card Detect Power-on Timing



4.0 Pin Assignment

The AU6333 is packed in 48pin-LQFP-form factor. The following figure shows signal name for each pin and the table in the following page describes each pin in detail.

Figure 4.1 Pin Assignment Diagram

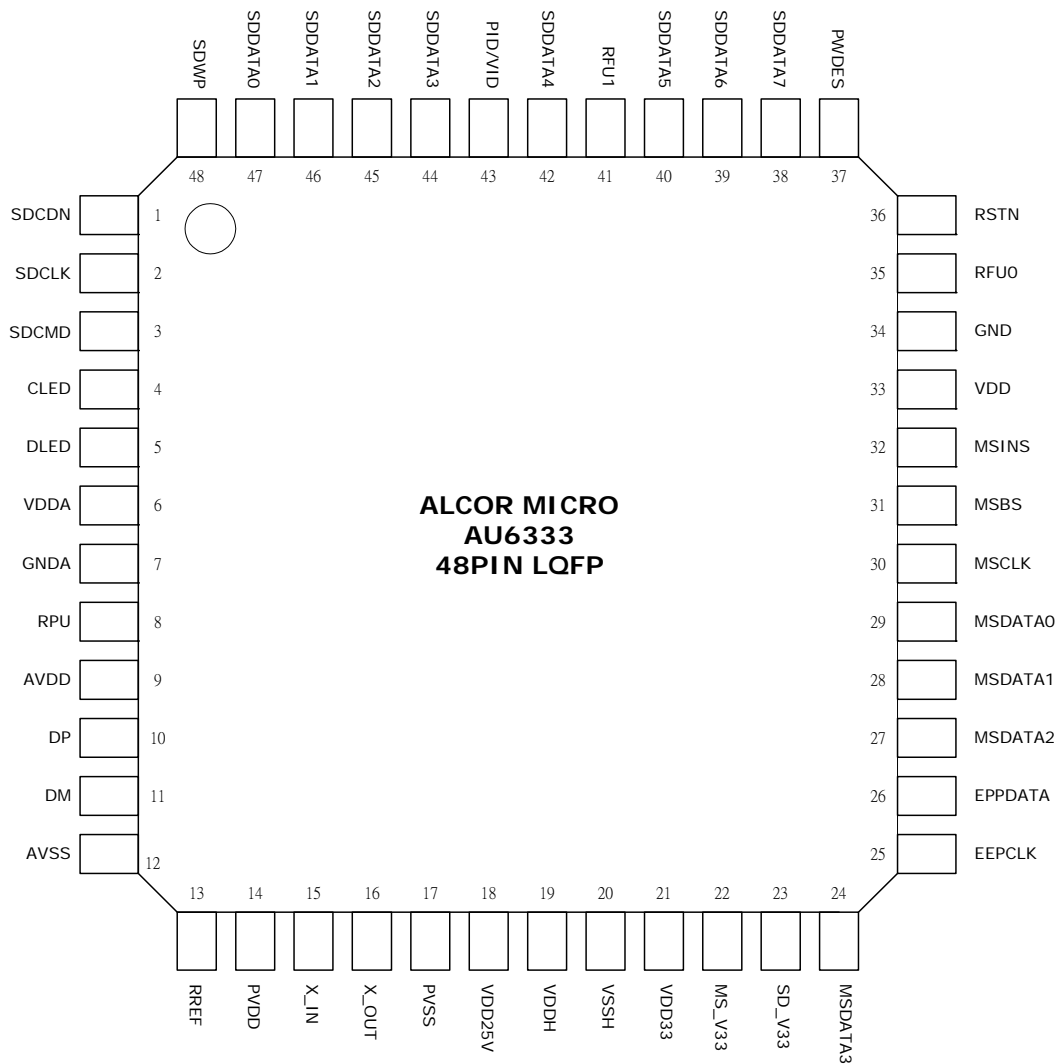




Table 4.1 Pin Descriptions

Pin #	Pin Name	I/O	Description
1	SDCDN	I	SD card detect; ("0":Detected; "1":unDetected[Default])
2	SDCLK	O	SD CLK
3	SDCMD	I/O	SD CMD
4	CLED	O	Card operating LED
5	DLED	O	Device LED
6	VDDA	I	2.5V Analog power for PLL
7	GNDA	I	Analog GND for PLL
8	RPU	I	Connect 1.5K pull up resistor to 3.3V VDD
9	AVDD	I	3.3V Analog power
10	DP	I/O	DP
11	DM	I/O	DM
12	AVSS	I	Analog GND
13	RREF	I	Connect 1K resistor to AVSS for impedance match
14	PVDD	I	OSC power 3.3V
15	X_IN	I	12MHz crystal input
16	X_OUT	O	12MHz crystal output
17	PVSS	I	OSC GND
18	VDD25V	O	2.5V output connect to core power VDD
19	VDDH	I	I/O power 3.3V
20	VSSH	I	I/O GND
21	VDD33	I	3.3V for card power
22	MS_V33	O	3.3V for MS card
23	SD_V33	O	3.3V for SD card
24	MSDATA3	I/O	MS data3
25	EEPCLK	O	EEPROM CLK
26	EPPDATA	I/O	EEPROM Data
27	MSDATA2	I/O	MS data2
28	MSDATA1	I/O	MS data1
29	MSDATA0	I/O	MS data0
30	MSCLK	O	MS CLK
31	MSBS	O	MS BS
32	MSINS	I	MS INS
33	VDD	I	Core power 2.5V
34	GND	I	Core GND
35	RFU0	I	Always pull low
36	RSTN	I	Chip reset, pull up with RC.
37	PWDES	I	Operating power description; ("0": 100mA[Default]; "1": 250mA)

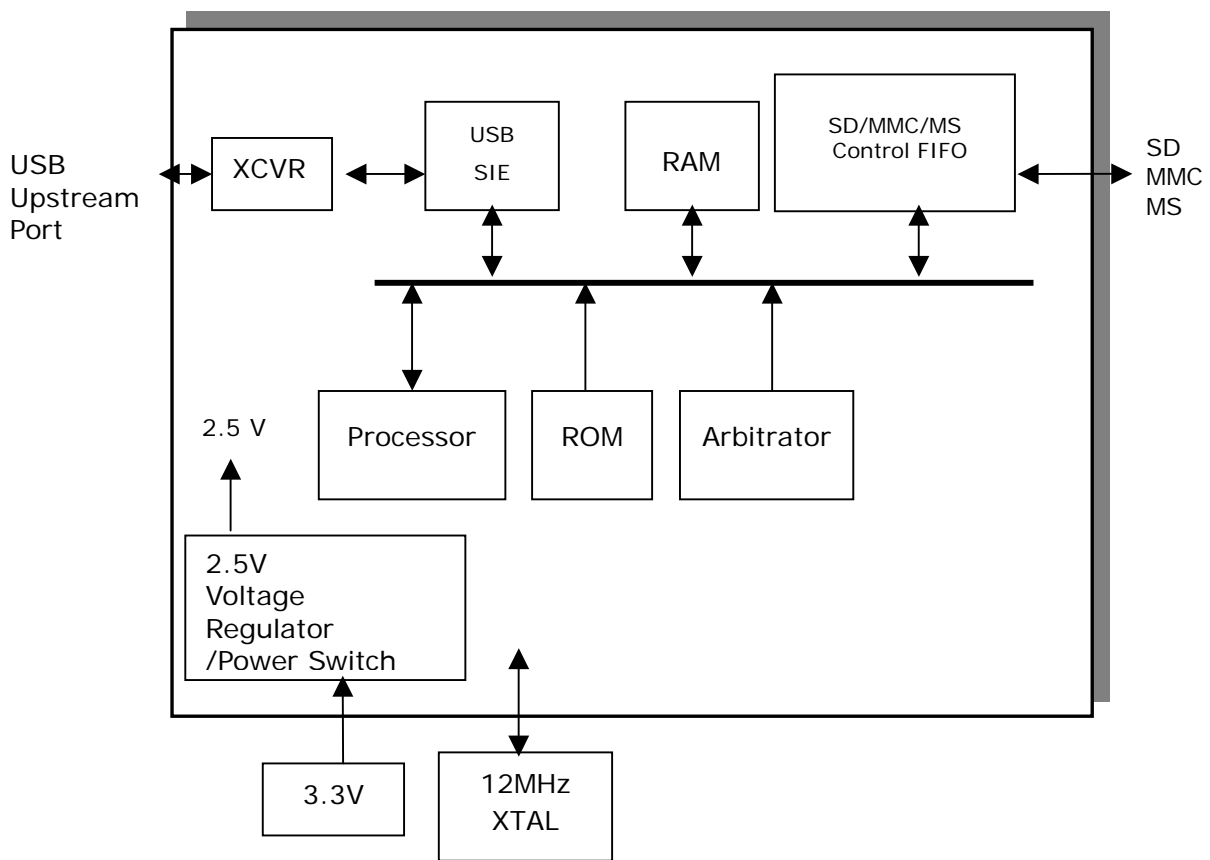


38	SDDATA7	I/O	SD data7
39	SDDATA6	I/O	SD data6
40	SDDATA5	I	SD data5
41	RFU1	I	Always pull low
42	SDDATA4	I/O	SD data4
43	PID/VID	I	LUN Mode Selection ("0": 2-LUN; "1": 1-LUN)
44	SDDATA3	I/O	SD data3
45	SDDATA2	I/O	SD data2
46	SDDATA1	I/O	SD data1
47	SDDATA0	I/O	SD data0
48	SDWP	I	SD write protect

5.0 System Architecture and Reference Design

5.1 AU6333 Block Diagram

Figure 5.1 AU6333 Block Diagram





6.0 Electrical Characteristics

6.1 Absolute Maximum Ratings

Table 6.1 Absolute Maximum Ratings

SYMBOL	PARAMETER	RATING	UNITS
V _{CC}	Power Supply	-0.3 to V _{CC} +0.3	V
V _{IN}	Input Voltage	-0.3 to 3.3	V
V _{OUT}	Output Voltage	-0.3 to V _{CC} +0.3	V
T _{STG}	Storage Temperature	-40 to 150	°C

6.2 Recommended Operating Conditions

Table 6.2 Recommended Operating Conditions

SYMBOL	PARAMETER	MIN	TYP	MAX	UNITS
V _{CC}	Power Supply	3.0	3.3	3.6	V
V _{IN}	Input Voltage	0	3.3	5.2	V
T _{OPR}	Operating Temperature	-40		115	°C

6.3 Leakage Current and Capacitance

Table 6.3 General DC Characteristics

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
I _{IN}	Input current	no pull-up or pull-down	-10	±1	10	μA
I _{OZ}	Tri-state leakage current		-10	±1	10	μA
C _{IN}	Input capacitance	Pad Limit		2.8		ρF
C _{OUT}	Output capacitance	Pad Limit		2.8		ρF
C _{BID}	Bi-directional buffer capacitance	Pad Limit		2.8		ρF



6.4 DC Electrical Characteristics of 3.3V I/O Cells

Table 6.4 DC Electrical Characteristics of 3.3V I/O Cells

SYMBOL	PARAMETER	CONDITIONS	Limits			UNIT
			MIN	TYP	MAX	
V _{CC}	Power supply	3.3V I/O	3.0	3.3	3.6	V
V _{il}	Input low voltage	LVTTTL			0.8	V
V _{ih}	Input high voltage		2.0			V
V _{ol}	Output low voltage	I _{ol} = 2~16mA			0.4	V
V _{oh}	Output high voltage	I _{oh} = 2~16mA	2.4			V
R _{pu}	Input pull-up resistance	PU=high, PD=low	40	75	190	KΩ
R _{pd}	Input pull-down resistance	PU=low, PD=high	40	75	190	KΩ
I _{in}	Input leakage current	V _{in} = V _{CC} or 0	-10	±1	10	μA
I _{oz}	Tri-state output leakage current		-10	±1	10	μA



6.5 USB Transceiver Characteristics

Table 6.5 Electrical characteristics

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
AVCC	Analog supply current		3.0	3.3	3.6	V
VCC	Digital supply current		2.25	2.5	2.75	V
I _{CC}	Operating supply current	High speed operating at 480 MHz			73	mA
I _{CC(susp)}	Suspend supply current	In suspend mode, current with 1.5kΩ pull-up resistor on pin RPU disconnected			120	μA

Table 6.6 Static characteristic : Digital pin

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
Input levels						
V _{IL}	Low-level input voltage				0.8	V
V _{IH}	High-level input voltage		2.0			V
Output levels						
V _{OL}	Low-level output voltage				0.2	V
V _{OH}	High-level output voltage		VCC-0.2			V

AVCC=3.0V~3.6V ; VCC=2.25V~2.75V ; Temp=0°C ~ 115°C



Table 6.7 Static characteristic : Analog I/O pins (DP/DM)

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
USB2.0 Transceiver (HS)						
Input Levels (differential receiver)						
V_{HSDIFF}	High speed differential input sensitivity	$ V_{I(DP)} - V_{I(DM)} $ measured at the connection as application circuit	300			mV
V_{HSCM}	High speed data signaling common mode voltage range		-50		500	mV
V_{HSSQ}	High speed squelch detection threshold	Squelch detected			100	mV
		No squelch detected	150			mV
V_{HSDSC}	High speed disconnection detection threshold	Disconnection detected	625			mV
		Disconnection not detected			525	mV
Output Levels						
V_{HSOI}	High speed idle level output voltage(differential)		-10		10	mV
V_{HSOL}	High speed low level output voltage(differential)		-10		10	mV
V_{HSOH}	High speed high level output voltage(differential)		-360		400	mV
V_{CHIRPJ}	Chirp-J output voltage (differential)		700		1100	mV
V_{CHIRPK}	Chirp-K output voltage (differential)		-900		-500	mV
Resistance						
R_{DRV}	Driver output impedance	Equivalent resistance used as internal chip only	3	6	9	Ω
		Overall resistance including external resistor	40.5	45	49.5	
Termination						
V_{TERM}	Termination voltage for pull-up resistor on pin RPU		3.0		3.6	V
USB1.1 Transceiver (FS/LS)						
Input Levels (differential receiver)						
V_{DI}	Differential input sensitivity	$ V_{I(DP)} - V_{I(DM)} $	0.2			V
V_{CM}	Differential common mode voltage		0.8		2.5	V
Input Levels (single-ended receivers)						



V_{SE}	Single ended receiver threshold		0.8		2.0	V
Output levels						
V_{OL}	Low-level output voltage		0		0.3	V
V_{OH}	High-level output voltage		2.8		3.6	V

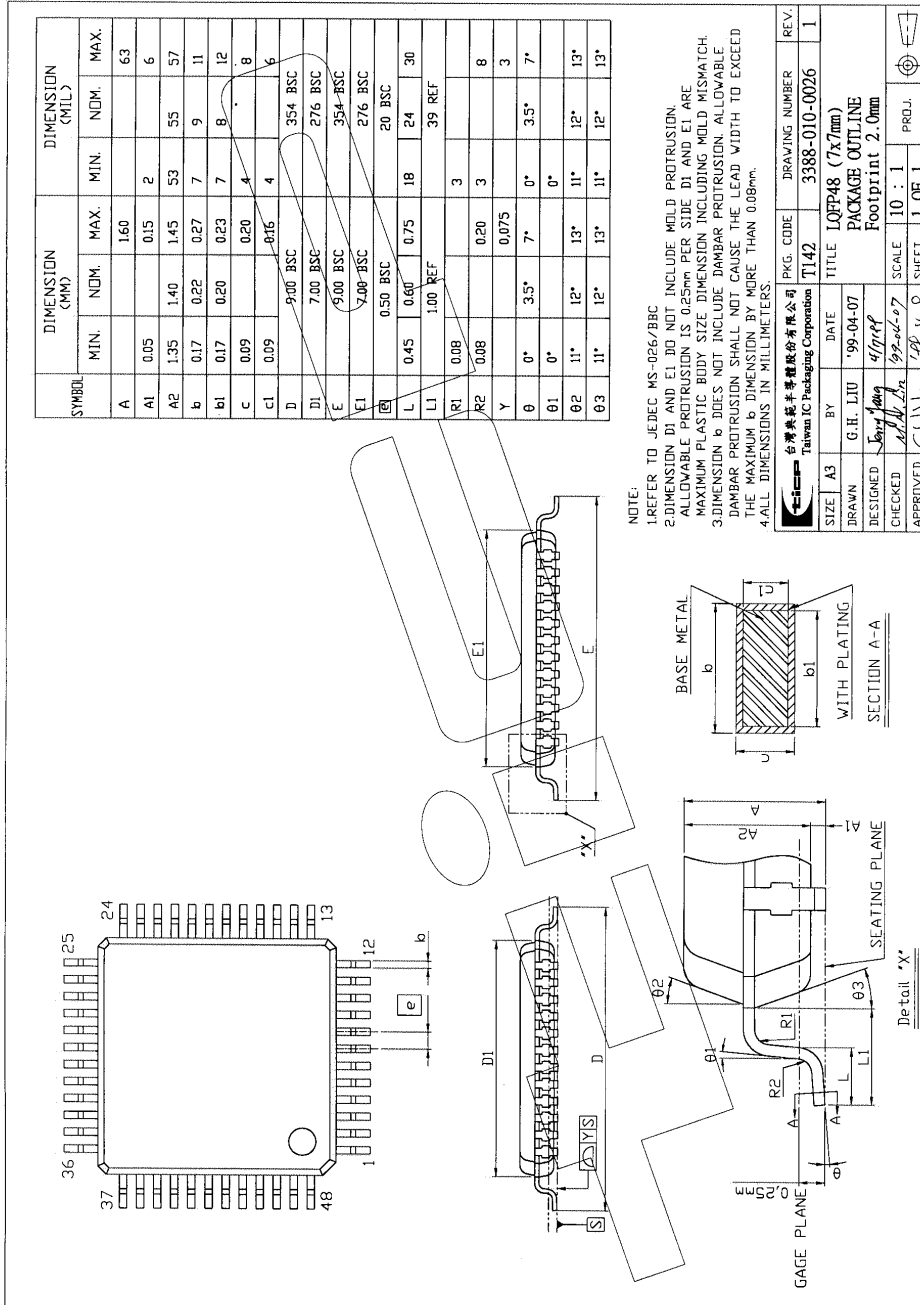
AVCC=3.0V~3.6V ; VCC=2.25V~2.75V ; Temp=0°C~115°C

Table 6.8 Dynamic characteristic : Analog I/O pins (DP/DM)

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
Driver Characteristics						
High-Speed Mode						
t_{HSR}	High-speed differential rise time		500			ps
t_{HSF}	High-speed differential fall time		500			ps
Full-Speed Mode						
t_{FR}	Rise time	CL=50pF ; 10 to 90% of $ V_{OH}-V_{OL} $;	4		20	ns
t_{FF}	Fall time	CL=50pF ; 90 to 10% of $ V_{OH}-V_{OL} $;	4		20	ns
t_{FRMA}	Differential rise/fall time matching (t_{FR} / t_{FF})	Excluding the first transition from idle mode	90		110	%
V_{CRS}	Output signal crossover voltage	Excluding the first transition from idle mode	1.3		2.0	V
Low-Speed Mode						
t_{LR}	Rise time	CL=200pF-600pF ; 10 to 90% of $ V_{OH}-V_{OL} $;	75		300	ns
t_{LF}	Fall time	CL=200pF-600pF ; 90 to 10% of $ V_{OH}-V_{OL} $;	75		300	ns
t_{LRMA}	Differential rise/fall time matching (t_{LR} / t_{LF})	Excluding the first transition from idle mode	80		125	%
V_{CRS}	Output signal crossover voltage	Excluding the first transition from idle mode	1.3		2.0	V
V_{OH}	High-level output voltage		2.8		3.6	V

7.0 Mechanical Information

Figure 7.1 Mechanical Information Diagram



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8.0 Abbreviations

This chapter lists and defines terms and abbreviations used throughout this specification.

SIE	Serial Interface Engine
SD	Secure Digital
MMC	Multimedia Card
MS	Memory Stick Card
UTMI	USB Transceiver Macrocell Interface



【MEMO】

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