AVERLOGIC

QUAD Video Processor
AL700/701/710 Data Sheets

Preliminary

Amendments (Since November 30, 2001)

01.11.30	Preliminary version A1.0
01.12.07	Preliminary version A1.1: (1) Adds features in paragraph 2 (2) Modifies the function block diagram in paragraph 4 (3) Modifies the pin-out diagrams in paragraph 5 (4) Modifies the pin number assignment in page 11 (5) Modifies Figure 7 (6) Modifies the register description of 15h, 17h, and 58h registers (7) Updates the mechanical drawing in page 81
02.01.11	Preliminary version B1.0: (1) Adds AL701 type that does not support analog video outputs, and modifies the related articles (2) Modifies the features in paragraph 2 (3) Modifies the function block diagram in paragraph 4 (4) Modifies the pin-out diagrams in paragraph 5 (5) Modifies the pin definition and description in paragraph 6 (6) Modifies contact information in the last page
02.04.09	Preliminary version C1.0: (1) Removes the Underscan feature (2) Modifies the pin-out diagrams in paragraph 5 (3) Modifies the blinking bit definition of Font index for one byte mode in figure 15 (4) Modifies the definitions of the BLINKCTRL (#21h) register
02.05.16	Preliminary version C1.1: (1) Updates the AC timing characteristics

THE INFORMATION CONTAINED HEREIN IS SUBJECT TO CHANGE WIHOUT NOTICE.

Contents:

1 General Description

AL700/701/710 is a 4 channel QUAD-screen video controller that can accept digital video input sources, provides 2 analog output ports (not for AL701), 2 digital output ports, and memory direct access mode allowing images to be uploaded onto a PC. AL700/701/710 not only supports 4 channel 8-bit ITU-R-656 4:2:2 interface inputs, dual 8/16-bit digital outputs for successive process and dual analog (TV encoder embedded, not for AL701) video outputs for TV, Camcorder, VCR, etc. SDRAM memory is supported via a direct video frame buffer interface. Through I^2C serial or proprietary parallel bus, fully programmable register set allows flexibility of control of video window overlay, OSD display, input channel select or output source select.
OSD (On Screen Display) windows provide overlay of various graphics images such as Pop-up menu, logo bitmap or message text, etc. Other functions provided by AL700/701/710, such as PIP (Picture In Picture), 2X zoom with vertical and horizontal interpolation, anti-rolling and motion detection, can increase the value and power of a security system design. Averlogic's proprietary digital and analog signal processing technologies create a high quality tear free, flicker free and anti-aliasing display. The AL700/701/710 provides a cost-effective solution for all applications of security related system.

All parts are available in 208-pin PQFP packages.

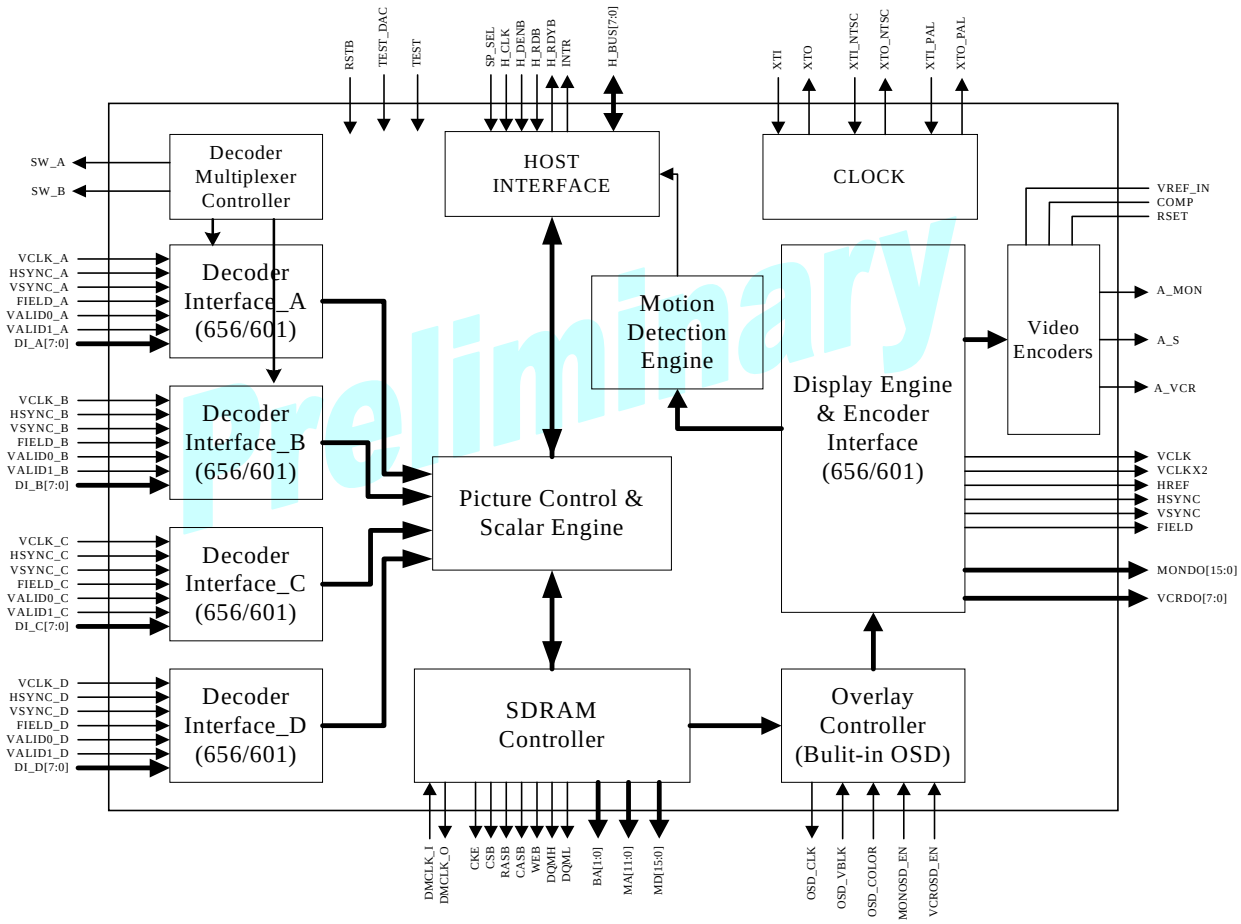
2 Features

- Accepts NTSC, PAL and SECAM video formats
- Supports 4 independent 656/601 8-bit video inputs
- Supports multiplexing function for 2 channels using one decoder
- Provides 2 independent 656/601 8/16-bit digital outputs
- Provides 2 independent S-video/Composite analog video outputs (no need external encoders, not for AL701)
- Picture location selectable
- Supports PIP (Picture-In-Picture) function
- Supports programmable picture overlay and layer priority
- Displays picture at arbitrary channels of 1,2,3 and 4
- Provides channel switching without rolling
- Freeze individual channel
- Provides video loss detection and motion detection
- 2X zoom with vertical and horizontal interpolation
- Provides embedded OSD (On Screen Display) and supports external OSD function
- Supports BMP image overlay and Non-fixed font display
- Provides fading effects for OSD overlay
- Supports various types of video decoder and 1Mx16 or 4Mx16 SDRAM
- Supports registers programming via I^2C serial or proprietary parallel interface
- Supports uploading image data onto PC
- Provides horizontal image mirroring
- Available in 208-pin 28*28mm PQFP
- Note: AL710 only supports Black & White video mode

3 Applications

- Security System: Video Surveillance System
  Video Splitting Processor
- Car Rear Vision System

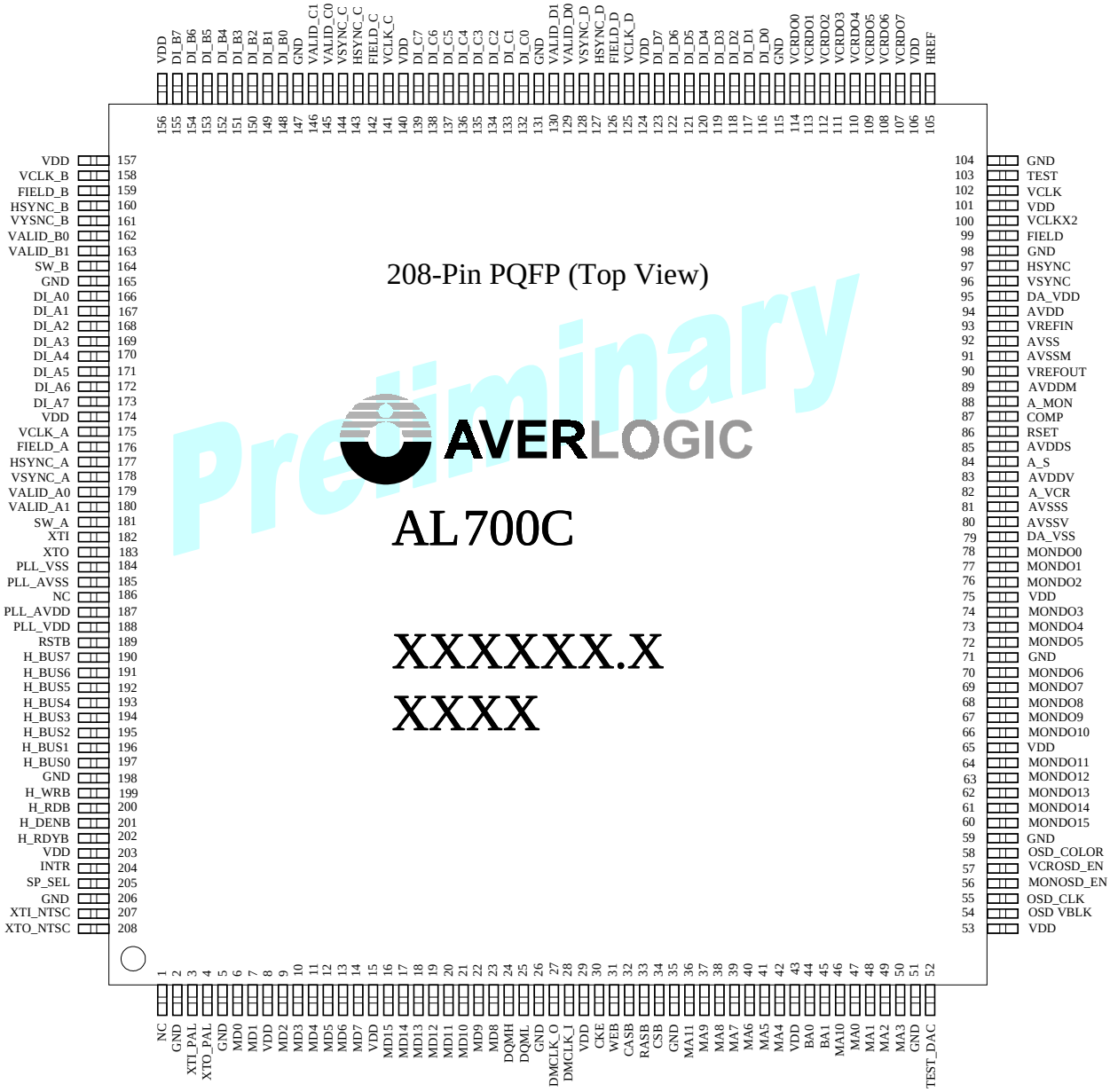
4 Function Block Diagram

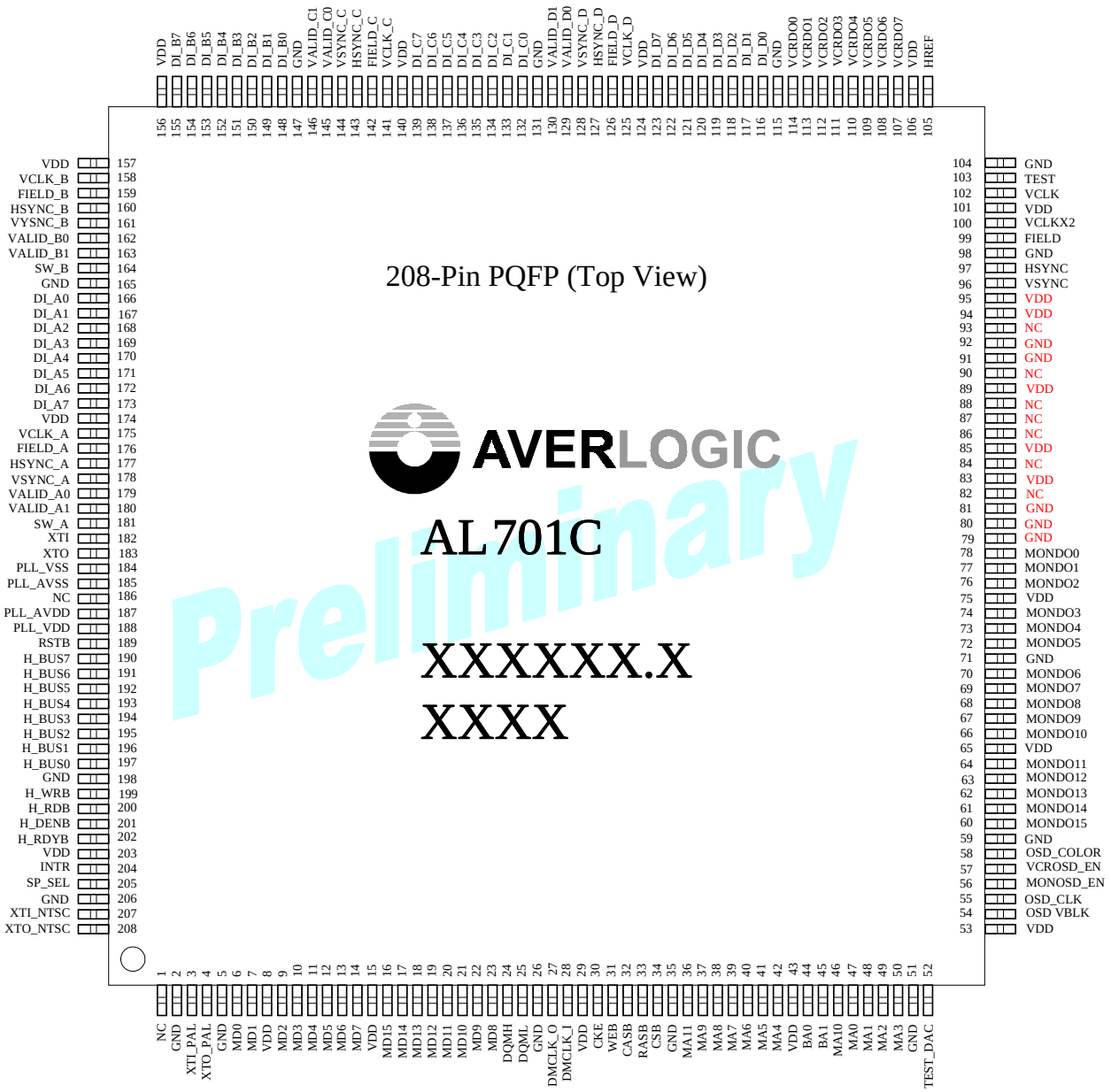


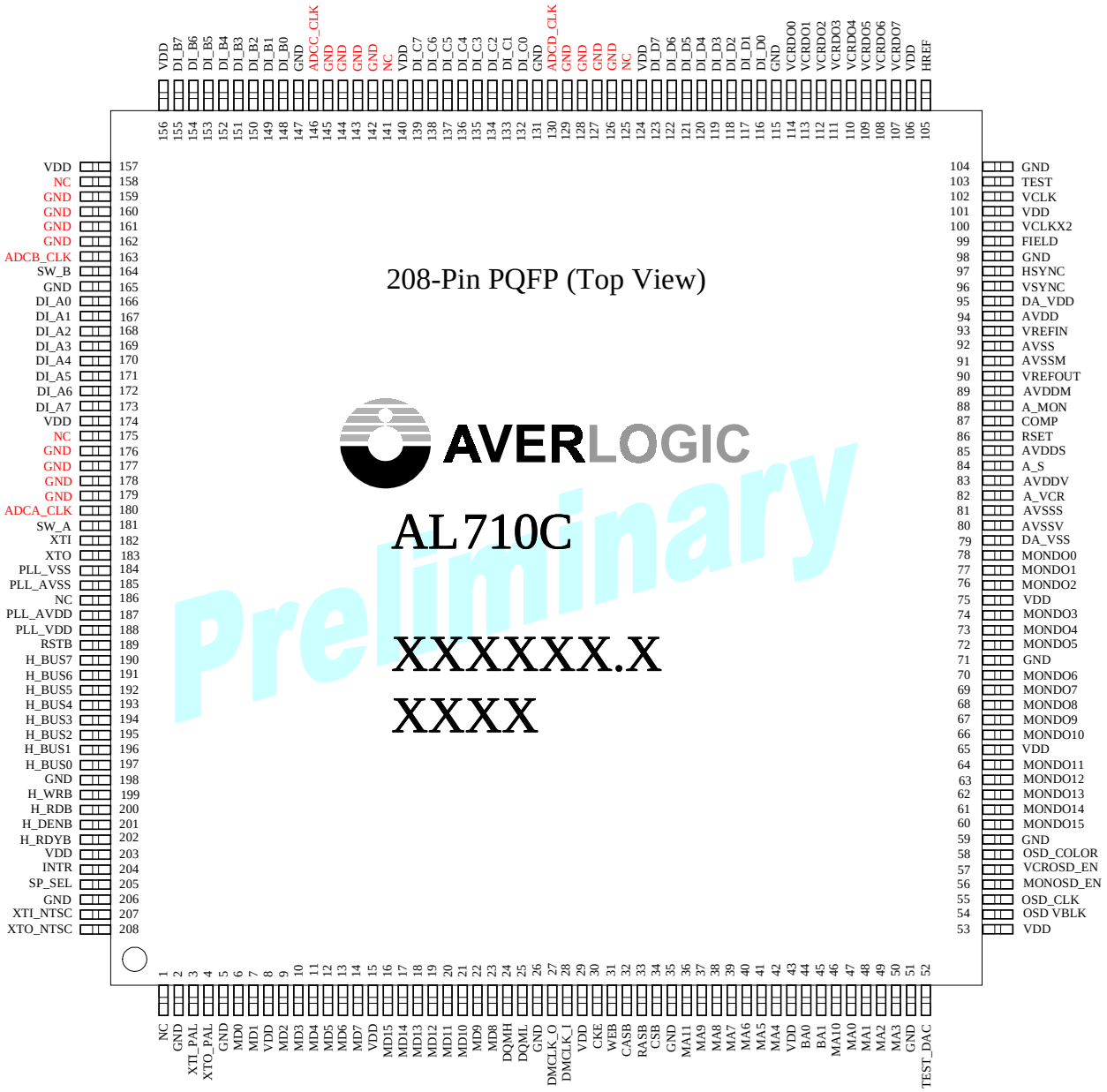
Note: Some signals are not available for AL701/710. For detailed information refer to Pin-out Diagram.

5 Pin-out Diagram

208 pin 28*28mm PQFP package:




208-Pin PQFP (Top View)
AVERLOGIC
AL701C
XXXXXX.X
XXXX
Preliminary
1 NC
2 GND
3 XTI_PAL
4 XTO_PAL
5 GND
6 MD0
7 MD1
8 VDD
9 MD2
10 MD3
11 MD4
12 MD5
13 MD6
14 MD7
15 VDD
16 MD15
17 MD14
18 MD13
19 MD12
20 MD11
21 MD10
22 MD9
23 MD8
24 DQMH
25 DQML
26 GND
27 DMCLK_O
28 DMCLK_I
29 VDD
30 CKE
31 WEB
32 CASB
33 RASB
34 CSB
35 GND
36 MA11
37 MA9
38 MA8
39 MA7
40 MA6
41 MA5
42 MA4
43 VDD
44 BA0
45 BA1
46 MA10
47 MA0
48 MA1
49 MA2
50 MA3
51 GND
52 TEST_DAC
53 VDD
54 OSD VBLK
55 OSD_CLK
56 MONOSD_EN
57 VCROSD_EN
58 OSD_COLOR
59 GND
60 MONDO15
61 MONDO14
62 MONDO13
63 MONDO12
64 MONDO11
65 VDD
66 MONDO10
67 MONDO9
68 MONDO8
69 MONDO7
70 MONDO6
71 GND
72 MONDO5
73 MONDO4
74 MONDO3
75 VDD
76 MONDO2
77 MONDO1
78 MONDO0
79 GND
80 GND
81 GND
82 NC
83 VDD
84 NC
85 VDD
86 NC
87 NC
88 NC
89 VDD
90 NC
91 GND
92 GND
93 NC
94 VDD
95 VDD
96 VSYNC
97 HSYNC
98 GND
99 FIELD
100 VCLKX2
101 VDD
102 VCLK
103 TEST
104 GND
105 HREF
106 VDD
107 VCRDO7
108 VCRDO6
109 VCRDO5
110 VCRDO4
111 VCRDO3
112 VCRDO2
113 VCRDO1
114 VCRDO0
115 GND
116 DI_D0
117 DI_D1
118 DI_D2
119 DI_D3
120 DI_D4
121 DI_D5
122 DI_D6
123 DI_D7
124 VDD
125 VCLK_D
126 FIELD_D
127 HSYNC_D
128 VSYNC_D
129 VALID_D0
130 VALID_D1
131 GND
132 DI_C0
133 DI_C1
134 DI_C2
135 DI_C3
136 DI_C4
137 DI_C5
138 DI_C6
139 DI_C7
140 VDD
141 VCLK_C
142 FIELD_C
143 HSYNC_C
144 VSYNC_C
145 VALID_C0
146 VALID_C1
147 GND
148 DI_B0
149 DI_B1
150 DI_B2
151 DI_B3
152 DI_B4
153 DI_B5
154 DI_B6
155 DI_B7
156 VDD
157 VDD
158 VCLK_B
159 FIELD_B
160 HSYNC_B
161 VYSNC_B
162 VALID_B0
163 VALID_B1
164 SW_B
165 GND
166 DI_A0
167 DI_A1
168 DI_A2
169 DI_A3
170 DI_A4
171 DI_A5
172 DI_A6
173 DI_A7
174 VDD
175 VCLK_A
176 FIELD_A
177 HSYNC_A
178 VSYNC_A
179 VALID_A0
180 VALID_A1
181 SW_A
182 XTI
183 XTO
184 PLL_VSS
185 PLL_AVSS
186 NC
187 PLL_AVDD
188 PLL_VDD
189 RSTB
190 H_BUS7
191 H_BUS6
192 H_BUS5
193 H_BUS4
194 H_BUS3
195 H_BUS2
196 H_BUS1
197 H_BUS0
198 GND
199 H_WRB
200 H_RDB
201 H_DENB
202 H_RDYB
203 VDD
204 INTR
205 SP_SEL
206 GND
207 XTI_NTSC
208 XTO_NTSC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13 MD6
14 MD7
15 VDD
16 MD15
17 MD14
18 MD13
19 MD12
20 MD11
21 MD10
22 MD9
23 MD8
24 DQMH
25 DQML
26 GND
27 DMCLK_O
28 DMCLK_I
29 VDD
30 CKE
31 WEB
32 CASB
33 RASB
34 CSB
35 GND
36 MA11
37 MA9
38 MA8
39 MA7
40 MA6
41 MA5
42 MA4
43 VDD
44 BA0
45 BA1
46 MA10
47 MA0
48 MA1
49 MA2
50 MA3
51 GND
52 TEST_DAC
53 VDD
54 OSD VBLK
55 OSD_CLK
56 MONOSD_EN
57 VCROSD_EN
58 OSD_COLOR
59 GND
60 MONDO15
61 MONDO14
62 MONDO13
63 MONDO12
64 MONDO11
65 VDD
66 MONDO10
67 MONDO9
68 MONDO8
69 MONDO7
70 MONDO6
71 GND
72 MONDO5
73 MONDO4
74 MONDO3
75 VDD
76 MONDO2
77 MONDO1
78 MONDO0
79 DA_VSS
80 AVSSV
81 AVSSS
82 A_VCR
83 AVDDV
84 A_S
85 AVDDS
86 RSET
87 COMP
88 A_MON
89 AVDDM
90 VREFOUT
91 AVSSM
92 AVSS
93 VREFIN
94 AVDD
95 DA_VDD
96 VSYNC
97 HSYNC
98 GND
99 FIELD
100 VCLKX2
101 VDD
102 VCLK
103 TEST
104 GND
105 HREF
106 VDD
107 VCRDO7
108 VCRDO6
109 VCRDO5
110 VCRDO4
111 VCRDO3
112 VCRDO2
113 VCRDO1
114 VCRDO0
115 GND
116 DI_D0
117 DI_D1
118 DI_D2
119 DI_D3
120 DI_D4
121 DI_D5
122 DI_D6
123 DI_D7
124 VDD
125 NC
126 GND
127 GND
128 GND
129 GND
130 ADCD_CLK
131 GND
132 DI_C0
133 DI_C1
134 DI_C2
135 DI_C3
136 DI_C4
137 DI_C5
138 DI_C6
139 DI_C7
140 VDD
141 NC
142 GND
143 GND
144 GND
145 GND
146 ADCC_CLK
147 GND
148 DI_B0
149 DI_B1
150 DI_B2
151 DI_B3
152 DI_B4
153 DI_B5
154 DI_B6
155 DI_B7
156 VDD
157 VDD
158 NC
159 GND
160 GND
161 GND
162 GND
163 ADCB_CLK
164 SW_B
165 GND
166 DI_A0
167 DI_A1
168 DI_A2
169 DI_A3
170 DI_A4
171 DI_A5
172 DI_A6
173 DI_A7
174 VDD
175 NC
176 GND
177 GND
178 GND
179 GND
180 ADCA_CLK
181 SW_A
182 XTI
183 XTO
184 PLL_VSS
185 PLL_AVSS
186 NC
187 PLL_AVDD
188 PLL_VDD
189 RSTB
190 H_BUS7
191 H_BUS6
192 H_BUS5
193 H_BUS4
194 H_BUS3
195 H_BUS2
196 H_BUS1
197 H_BUS0
198 GND
199 H_WRB
200 H_RDB
201 H_DENB
202 H_RDYB
203 VDD
204 INTR
205 SP_SEL
206 GND
207 XTI_NTSC
208 XTO_NTSC

6 Pin Definition and Description

The I/O pins of AL700/701/710 can be grouped into decoder interface (data, clock, flag and control pins), OSD interface (data, clock and control pins), encoder interface (data, clock, flag and control pins), SDRAM interface (data, clock and control pins), Host interface (data, clock and control pins) and general-purpose pins (clock, reset, power and ground.)

The pin-out definitions are described as follows:

Pin Name	Pin Number	I/O type	Description
Decoder Interface			
VCLK_A, B, C, D	175, 158, 141, 125	I	For AL700/701, Video clock signal for channel A, B, C, and D, respectively
NC	175, 158, 141, 125	I	For AL710, they are NC pins
HSYNC_A, B, C, D	177, 160, 143, 127	I	For AL700/701, Video horizontal Sync signal (new line indicator) for channel A, B, C, and D, respectively (used in ITU-R-601 input)
VSYNC_A, B, C, D	178, 161, 144, 128	I	For AL700/701, Video vertical Sync signal (new field indicator) for channel A, B, C, and D, respectively (used in ITU-R-601 input)
FIELD_A, B, C, D	176, 159, 142, 126	I	For AL700/701, Video field flag signal for channel A, B, C, and D, respectively (used in ITU-R-601 input)
VALID_A0, B0, C0, D0	179, 162, 145, 129	I	For AL700/701, Valid data indicator 0 for channel A, B, C, and D, respectively (used in ITU-R-601 input)
GND	176, 159, 142, 126 177, 160, 143, 127 178, 161, 144, 128 179, 162, 145, 129	DP	For AL710, these pins should be tired to Digital Ground
VALID_A1, B1, C1, D1	180, 163, 146, 130	I/O	For AL700/701, Valid data indicator1 for channel A, B, C, and D, respectively (used in ITU-R-601 input)
ADCA_CLK, ADCB_CLK, ADCC_CLK, ADCD_CLK	180, 163, 146, 130	I/O	For AL710, ADC clock for channel A, B, C, and D, respectively
DI_A[7:0], B[7:0], C[7:0], D[7:0]	173-166, 155-148, 139-132, 123-116	I	Video stream data for channel A, B, C, and D, respectively
SW_A	181	O	Channel switch control for channel A and C
SW_B	164	O	Channel switch control for channel B and D
OSD Interface			
OSD_VBLK	54	I	Blank the video output and show OSD when active (High)
OSD_CLK	55	O	Clock to external OSD

Pin Name	Pin Number	I/O type	Description
MONOSD_EN	56	I	Monitor OSD Enable
VCROSD_EN	57	I	VCR OSD Enable
OSD_COLOR	58	I	OSD color selection
Encoder Interface			
VCLK	102	O	Video clock output of monitor/VCR
VCLKX2	100	O	2 times video clock output of monitor/VCR
VSYNC	96	I/O	Video vertical Sync signal of monitor/VCR
HSYNC	97	I/O	Video horizontal Sync signal of monitor/VCR
FIELD	99	O	Video field flag signal of monitor/VCR
HREF	105	O	Horizontal reference signal of monitor/VCR
MONDO[15:0]	60-64, 66-70, 72-74, 76-78	O	Monitor video stream data output that can be programmed to be various data formats through host interface
VCRDO[7:0]	107-114	O	VCR video stream data output
Analog Output			
AVDDM, AVDDS, AVDDV	89, 85, 83	AP/DP	Analog power for monitor, S-video, and VCR output, respectively (VDD for AL701)
AVSSM, AVSSS, AVSSV	91, 81, 80	AP/DP	Analog ground for monitor, S-video, and VCR output, respectively (GND for AL701)
AVDD	94	AP/DP	Analog power (VDD for AL701)
AVSS	92	AP/DP	Analog ground (GND for AL701)
DA_VDD	95	DP	Digital power
DA_VSS	79	DP	Digital ground
VREFIN	93	AI	Voltage reference input (NC for AL701)
VREFOUT	90	AO	Voltage reference output (NC for AL701)
RSET	86	AI/O	Full-scale current adjust (NC for AL701)
COMP	87	AO	Compensation pin (NC for AL701)
A_MON	88	AO	Monitor Composite output or Y output for S-video (NC for AL701)
A_S	84	AO	C output for S-video (NC for AL701)
A_VCR	82	AO	VCR Composite output or Y output for S-video (NC for AL701)
NC	82, 84, 86, 87, 88 90, 93	AI/O	For AL701, they are NC pins
SDRAM Interface			
CSB	34	O	Chip select for SDRAM, active Low
RASB	33	O	Row address strobe for SDRAM, active Low
CASB	32	O	Column address strobe for SDRAM, active Low
WEB	31	O	Write enable for SDRAM, active Low
BA[1:0]	45, 44	O	Bank select for SDRAM
MA[11:0]	36, 46, 37-42, 50-47	O	Address bus for SDRAM

Pin Name	Pin Number	I/O type	Description
MD[15:0]	16-23, 14-9, 7, 6	I/O	Data bus for SDRAM
DQMH	24	O	High byte data mask for SDRAM
DQML	25	O	Low byte data mask for SDRAM
CKE	30	O	Clock enable for SDRAM
DMCLK_I	28	I	Clock input for SDRAM controller
DMCLK_O	27	O	Clock output for SDRAM
Host Interface			
SP_SEL	205	I	Serial/parallel host interface selection, High for serial mode and Low for parallel mode
H_WRB	199	I	1. Host write signal for parallel mode, active Low to High trigger 2. Equivalent to SCL (serial clock) for I^2C serial mode
H_DENB	201	I	1. Host data enable signal for parallel mode, Low for address and High for data 2. Slave address selection for I^2C serial mode, Low for 70h/71h and High for 72h/73h
H_RDB	200	I	Host read enable signal, Low for read operation and High for write operation
H_BUS[7:0]	190-197	I/O	Host stream data or address bus in parallel mode. H_BUS7 is I^2C data line (SDA) in serial mode
INTR	204	O	Interrupt output for motion detection, video loss or other events
Clock			
XTI	182	I	27MHz OSC input
XTO	183	O	27MHz OSC output
XTI_NTSC	207	I	28.6364MHz OSC input
XTO_NTSC	208	O	28.6364MHz OSC output
XTI_PAL	3	I	35.4690MHz OSC input
XTO_PAL	4	O	35.4690MHz OSC output
PLL_AVDD	187	AP	Analog power for PLL
PLL_AVSS	185	AP	Analog ground for PLL
PLL_VDD	188	DP	Digital power for PLL
PLL_VSS	184	DP	Digital ground for PLL
System			
RSTB	189	I	System reset, active Low
Others			
TEST	103	I	Factory test pin
TEST_DAC	52	I	Factory test pin
H_RDYB	202	O	Reserved
NC	1, 186	-	No connection

Pin Name	Pin Number	I/O type	Description
Digital Power			
VDD	8, 15, 29, 43, 53, 65, 75, 101, 106, 124, 140, 156, 157, 174, 203	DP	Digital power
GND	2, 5, 26, 35, 51, 59, 71, 98, 104, 115, 131, 147, 165, 198, 206	DP	Digital ground

Note: For I/O type, I, O, AP, and DP indicate input, output, analog power, and digital power respectively.

7 Function Description

7.1 Decoder/ADC Video Input Interface

AL700/701/710 has four video input interfaces that can directly connect to external video decoders (or video ADC outputs for AL710) and support 4 channels of 8-bit ITU-R-601/656 4:2:2 data stream. To support various video decoders, AL700/701/710 accepts different types of sync, flags, data formats, and data sequence by adjusting data in the internal control register #04h. The polarity of the input/output video signals can also be adjusted through register #05h. Because all the 4 external video inputs are controlled by the same internal control registers, using the same type of video decoders or ADC devices in the design is recommended.

When SoftRef (register #08h<2>) is set to 0, the input active region is defined by HACTIVE code in ITU-R-656 mode or by hardware valid pins in ITU-R-601 8-bit mode. The input active region is defined by register CAPHSTART (#09h and #0Ah) and register CAPVSTART (#0Bh) if SoftRef is set to 1. All the parameters are relative to the leading edges of the input horizontal and vertical sync signals. The following diagram shows the input active window timing and the related registers. The internal control signals are assumed to be active High. Therefore, register POLARITY (#05h) should be adjusted to match the required format if the input control signals are active Low.

Many video decoders support channel-multiplexing functions. AL700/701/710 supports a channel multiplexing mode using1 decoder for 2 channels by the SW_A and SW_B output control signals. When mux_mode (register #08h<4>) is set to 1, AL700/701/710 will control the SW_A and SW_B output signals and automatically swap the internal decoder interface to reflect the respective channel data. The SW_A controls the channels A and C data and SW_B controls the channels B and D. Therefore, you should only connect the external decoders to channels A and B interface of AL700/701/710.

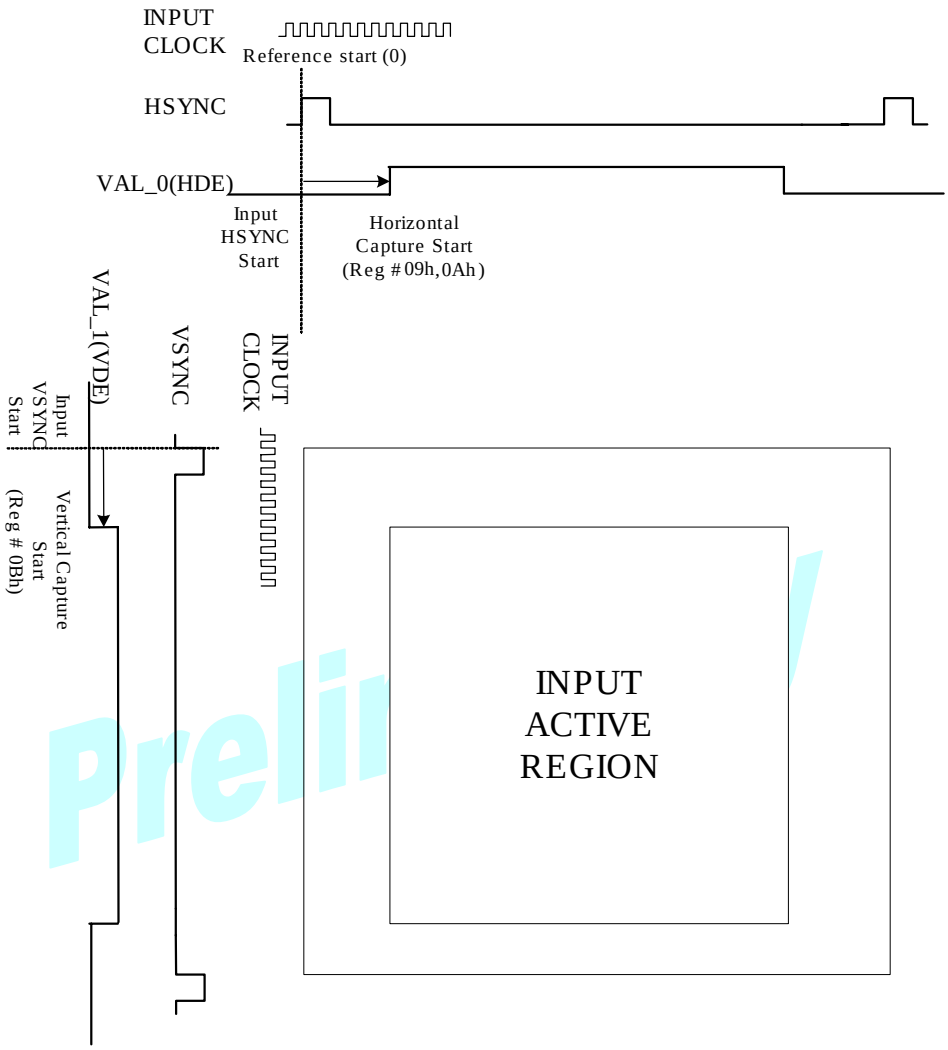


Figure 1: Input Video Timing

7.2 Encoder Video Output Interface

All the AL700, AL701 and AL710 provide two digital video output interfaces that can be directly connected external TV encoders for composite output or AL250/251 devices for RGB analog/digital output. But only AL700 and AL710 provide internal encoders to support two analog composite outputs that can be simultaneously connected to TV and VCR. Both 8-bit ITU-R-601 4:2:2 and ITU-R-656 4:2:2 interface are supported when external encoder mode is selected. The monitor output interface also supports 16-bit ITU-R-601 4:2:2 data stream.

For AL700/710, the digital output data is still available when internal encoder mode is selected, but the horizontal size of picture is non-standard because the internal operating clock for the output is 14.318 MHz in NTSC or 17.734 MHz in PAL, not the CCIR standard of 13.5 MHz.

AL700/701/710 uses internal control registers #03h and #04h to adjust output timing with different sync, flags, data formats and data sequence, and select 8-bit or 16-bit data bus width. To support various TV encoders, AL700/701/710 uses internal control register #04h to adjust output timing with different sync, flags, data formats, and data sequence. The encoder interface can be set to Master or Slave mode by register #18h while using external encoders. The following table shows the output formats supported by AL700/701/710.

Video System		Total Resolution	Active Resolution
External encoder	NTSC	858 * 525	720 * 480
	PAL	864 * 625	720 * 576
Internal encoder	NTSC	910 * 525	737 * 480
	PAL	1135 * 625	929 * 576

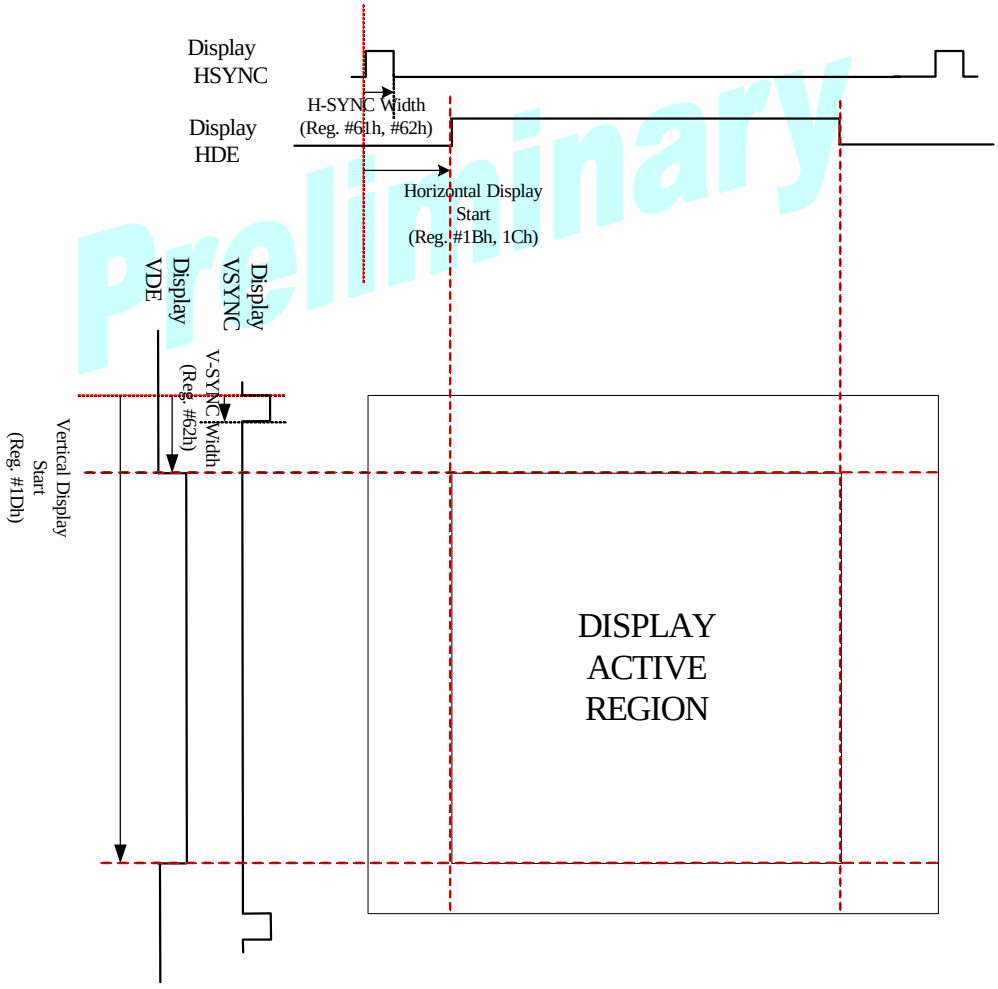


Figure 2: Output Video Timing

The output display system, sync signal pulse width, and active display window are fully programmable. They are defined by HSYNCWIDTH (#60h, #61h), DISPHSTART (#1Bh,

#1Ch), VSYNCWIDTH (#62h), and DISPVSTART (#1Dh) registers. Figure 2 shows the output active window timing and the related registers.

For AL701, EncoderSel (#18h <0>) should be set to "1" in the initialization stage of AL701 because it does not support internal encoder mode.

7.3 Host Interface

AL700/701/710 supports I^2C serial and proprietary parallel programming interfaces that can be selected through SP_SEL pin. I^2C serial interface requires two wires to access while the proprietary parallel interface needs 11 wires. The communication speed of proprietary parallel interface is much faster than I^2C serial interface.

7.3.1 I^2C Serial Interface

The I^2C serial interface consists of SCL (serial clock) and SDA (serial data) signals. There are internal pull-up circuits in AL700/701/710 for both SCL (equivalent to H_WRB) and SDA (equivalent to H_BUS7) pins. When SP_SEL is pulled low, the I^2C serial interface is disabled and both SCL and SDA pins are pulled high. For both read and write cycles, each byte is transferred from MSB bit to LSB bit. The Master/Slave device samples and holds the SDA data at the rising edge of the SCL signal.

The read/write command format is as follows:

Write: <S> <Write SA> <A> <Register Index> <A> <Data> <A> <P>

Read: <S> <Write SA> <A> <Register Index> <A> <S> <Read SA> <A> <Data> <NA> <P>

Following are the details:

<**S**>: Start signal

SCL	SDA
High	High to Low

The Start signal appears at High to Low transition on the SDA line when SCL is High.

<**Write SA**>: Write Slave Address

The Write Slave Address is 70h or 72h.

<**Read SA**>: Read Slave Address

The Read Slave Address is 71h or 73h.

<**Register Index**>: Value of the AL700/710 register index.

<**A**>: Acknowledge stage

The host (master) generates acknowledge-related clock pulse. During the acknowledge clock pulse, the host must release the SDA line (to High) in order that AL700/701/710 (slave) can pull down the SDA.

<**NA**>: Non-Acknowledged stage

The host (master) generates acknowledge-related clock pulse. The host also releases the SDA line (to High) during the acknowledge clock pulse, but the AL700/701/710 does not pull it down during this stage.

<**Data**>: Data byte written to or read from the register index

In read operation, the host must release the SDA line (to High) before the first clock pulse is transmitted to the AL700/701/710.

<**P**>: Stop signal

SCL	SDA
High	Low to High

The Stop signal appears at Low to High transition on the SDA line when SCL is High.

Suppose data F0h is to be written to register 0Fh using write slave address 70h, the timing is as follows:

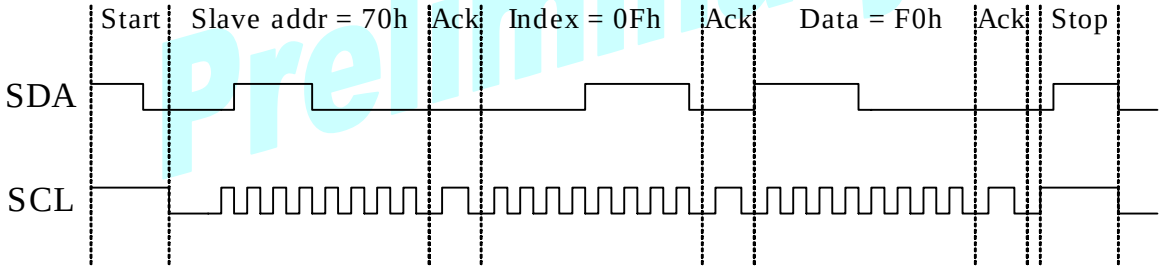


Figure 3: I²C Serial Bus Write Timing

Suppose data is to be read from register 55h using read slave address 71h, the timing is as follows:

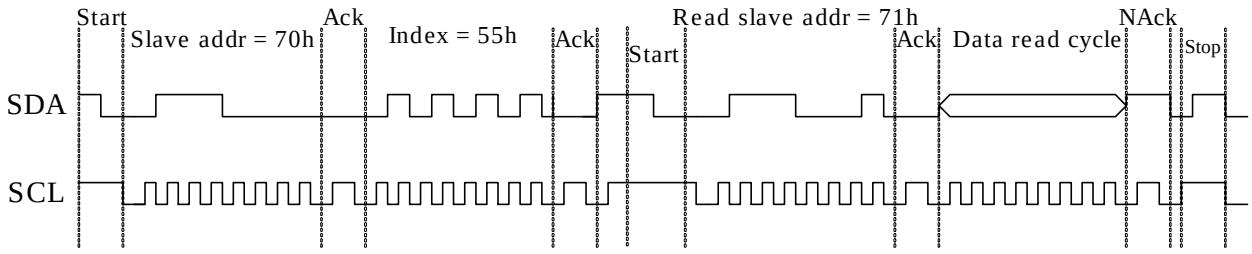


Figure 4: I²C Serial Bus Read Timing

7.3.2 Proprietary Parallel Interface

The parallel bus interface consists of the H_WRB (latch clock), H_BUS[7:0], H_DENB and H_RDB signals. There are internal pull-up circuits for all pins. When SP_SEL is high, the parallel bus interface is disabled and all parallel interface pins are pulled high. The parallel interface transfers base register address or read/write data in one H_WRB cycle. H_WRB is a latch clock signal. H_BUS[7:0] represents an 8-bit data bus. H_DENB defines the data bus as register address bus or data bus. The H_BUS[7:0] appears a register address at the rising edge of H_WRB when H_DENB is High. H_RDB defines Read/Write mode. The High H_RDB represents the host operates in the Write mode. At the rising edge of H_WRB, read/write data is latched or read-out data is read. The following figures show read/write timing chart of host parallel interface.

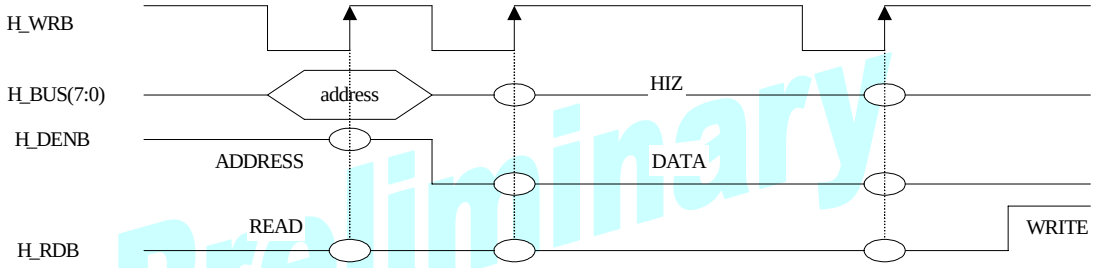


Figure 5: Host Read Cycle

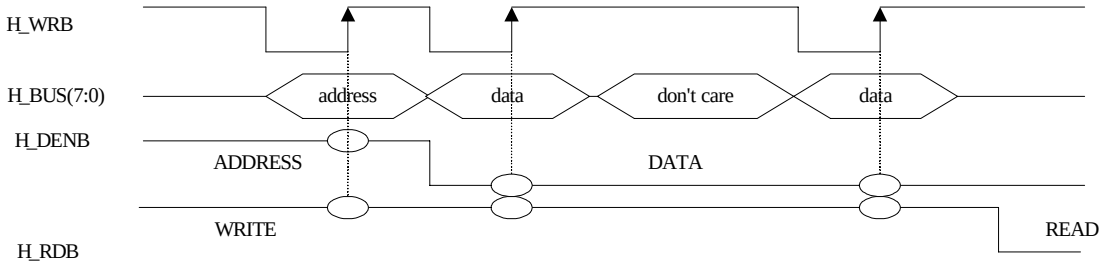


Figure 6: Host Write Cycle

7.4 Picture Control

AL700/701/710 provides various functions that can be controlled by inside registers. Picture control takes effect on the fly. Display attributes apply to all channels but channel attributes apply to each channel.

7.4.1 Picture Attributes

AL700/701/710 provides QUAD or FULL screen picture display. In addition, picture location, layer priority and channel attributes can be programmed via host interface.

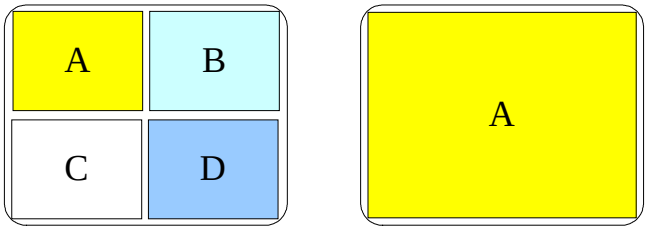


Figure 7: QUAD and Full Screen Display

Each channel can be located in any one position of left-top, left-bottom, right-top, and right-bottom screen in PIP (Picture In Picture) display mode. AL700/701/710 provides two-layer effect on picture layer priority. The bottom layer is always chosen as base video and the top layer shows the sub video window in PIP mode. These effects are defined by MTROUTSEL (#19h) and PIPCTRL (#1Ah) registers.

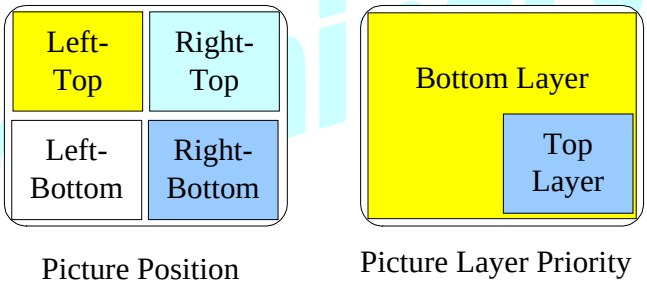


Figure 8: Picture Position and Picture Layer

By setting up data in MTROUTSEL (#19h) and PIPCTRL (#1Ah) registers, you can get various useful features like PIP, channel overlay, sequential scan picture, anti-rolling switching channel, 1 to 4 picture display, and so on.

7.4.2 Display Attributes

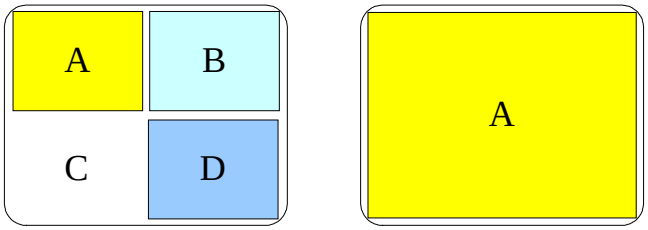
Display control will affect all channels at the same time. These controls include NTSC or PAL/SECAM system selection, background and full screen borderline color selection, and full screen borderline display/blink enable or disable.

AL700/701/710 supports 525-line system in NTSC and 625-line system in PAL/SECAM. The Vsystem in SYSCONFIG register (#03h <0>) defines the video system.

The background area is defined as outside of all active picture region. The background color is defined in BGColor (#20h <1:0>) and has four 24-bit color choices. The selected colors are defined in color Look Up Table (LUT).

The full screen borderline color is defined in Border5_color (#14h <3:2>) and can be one of color 0, color 1, color 2, and color 3 defined in color LUT. No matter what channel is displayed in full screen, the full screen borderline color and blink attribute are the same. For the full screen display, it has its own control attributes to enable/disable or blink the

borderline. The register Border5_enx (#14h <1:0>) is used to enable/disable full screen borderline in monitor output, VCR output, or both monitor and VCR outputs. The register Border5_blink (#15h <4>) controls the disable or enable of full screen borderline blink function.



QUAD Screen Full Screen

Figure 9: Borderline and Background Attributes

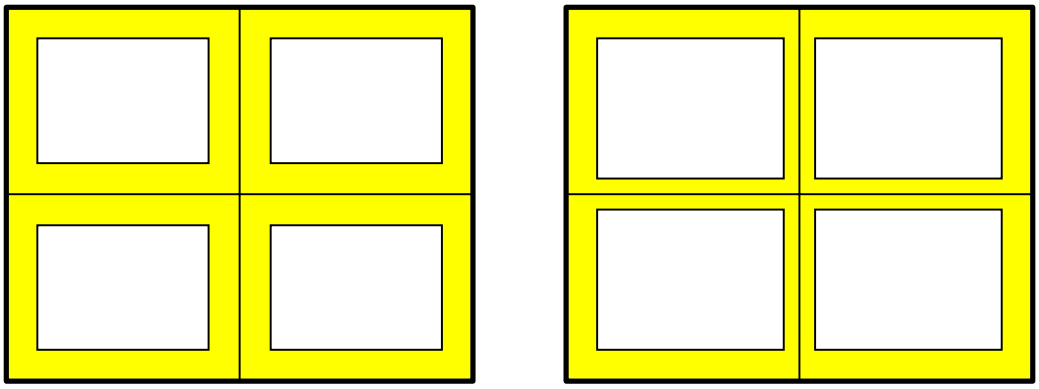
7.4.3 Channel Attributes

There are independent channel configuration registers for each channel that can do various display control. The attribute controls include channel borderline enable or disable, channel borderline color, channel borderline blinking enable or disable, channel layer priority, channel location, channel image mirror enable or disable, and channel freeze control.

The input channels are assigned to fixed locations of the four windows in QUAD screen display mode. In PIP mode, PIPCTRL (#1Ah) register controls each channel location. AL700/701/710 supports top and bottom layer priority that is only available in PIP mode. Base video channel defined by ChSel (#19h <1:0>) is always on the bottom layer. The sub video channel defined by PIPCTRL (#1Ah) is always on the top layer and enabled by LTPIP_en (#19h <4>), RTPIP_en (#19h <5>), LBPIP_en (#19h <6>), or RBPIP_en (#19h <7>).

Each channel has its own borderline color and is defined in Border1_color (#10h <5:4>) for channel A, Border2_color (#11h <5:4>) for channel B, Border3_color (#12h <5:4>) for channel C, or Border4_color (#13h <5:4>) for channel D. The borderline color can be one of color 0, color 1, color 2, and color 3 defined in color LUT. Each channel also has its own enable or disable borderline display or blink controls. Border1_enx (#10h <3:2>), Border2_enx (#11h <3:2>), Border3_enx (#12h <3:2>), and Border4_enx (#13h <3:2>) are used to disable channel borderline display, or enable channel borderline display in monitor output, VCR output, or both monitor and VCR outputs for channel A, B, C, and D, respectively. Border1_blink (#15h <0>), Border2_blink (#15h <1>), Border3_blink (#15h <2>), and Border4_blink (#15h <3>) control the disable or enable of channel A, B, C, and D borderline blink function, respectively.

Borderline is at a fixed position for each channel except Border1 (the left-top channel borderline) and the effect of BorderCenter (#18h <3>). HZOOMSTART (#1Eh) and VZOOMSTART (#1Fh) registers can shift the Border1 to mark the zoomed area. BorderCenter can overlay the borderline in the center of screen and its effect is shown in Figure 10.



BorderCenter = 0 BorderCenter = 1

Figure 10: The Effect of BorderCenter Setting

The picture can be frozen independently through controlling v1FreezeSel (#10h <1:0>), v2FreezeSel (#11h <1:0>), v3FreezeSel (#12h <1:0>), or v4FreezeSel (#13h <1:0>). Freeze function supports to capture a frame image, an odd field image, or an even field image.

The image mirroring is supported in each channel at X-axis (horizontal axis) direction. Setting v1_flipx (#10h <6>), v2_flipx (#11h <6>), v3_flipx (#12h <6>), and v4_flipx (#13h <6>) to 1 can enable the mirror function of channel A, B, C, and D, respectively.

7.5 Video Loss

AL700/701/710 supports video loss detection in both QUAD and FULL screen display modes. This is a very useful function in monitoring emergency situations. If there is an interrupt event due to video loss condition and the corresponding mask is not set to 1, the INTR pin will be active.

The video loss condition refers to the following input signals: VALID 0, VALID 1, HSYNC, VSYNC, VCLK, DI [7:0] and Htotal_range (#0Fh <7:4>). Each signal can be enabled to reflect the video loss condition. VLOSSSIG (#0Ch) register controls the signal enable or disable attribute and applies the controls to all the channels. When one or more of the status bits are set during the operation that indicates the corresponding channels lose the input video signals.

7.6 Motion Detection

AL700/701/710 supports hardware and software motion detection function. The motion detection function is always applied in the QUAD screen image of VCR output. The QUAD screen image is divided into 16 equal-size windows. Each video channel is assigned 4 windows. For hardware motion detection, each window in the same channel shares the same threshold of mean and variance defined in registers #70h~#7Fh. The motion detection algorithm built in AL700/701/710 uses the threshold of mean and variance to automatically

detect an object motion. Once AL700/701/710 detects motion from any channel, the corresponding interrupt status (MotionA~D, #06h <7:4>) will reflect the incident. If the corresponding mask bit (Mask_MA~D, #07h<7:4>) is not set to 1, then the INTR pin will be active.

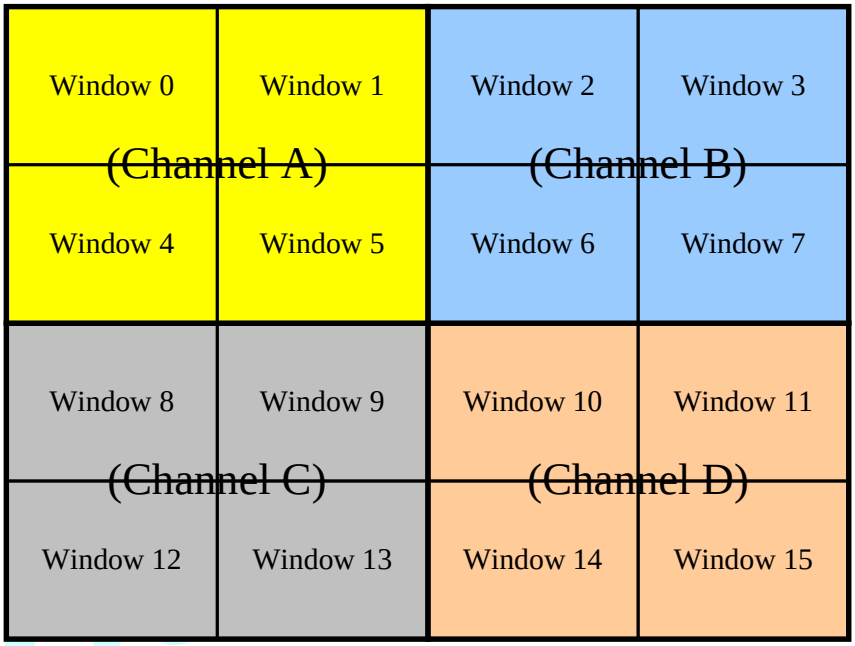


Figure 11: Motion-Detection Windows

AL700/701/710 offers the calculating results, such as mean and variance, for each window, and system designers can implement their own motion detection algorithm based on these values. Through setting the window address of mean and variance (MOTIONADDR, #6Bh), one can read the mean data from MEANDATA registers (#6Ch and #6Dh), and the variance data from VARIANCEDATA registers (#6Eh and #6Fh).

7.7 2X Zoom

AL700/701/710 provides 2X Zoom with interpolation function that allows you to watch a larger image twice the size of the original size in either real-time or frozen. This function applies an AverLogic proprietary interpolation algorithm to display a high quality image on the screen.

When DisplayMode (#19h <3:2>) is set to ZOOM in mode, an area in each field defined by HzoomStart (#1Eh <6:0>) and VzoomStart (#01Fh <6:0>) will be zoomed in 2 times. The area size is 360x240 pixel-line in NTSC mode or 360x288 pixel-line in PAL mode. The unit of HzoomStart is 4 pixels and the unit of VzoomStart is 2 lines. Therefore, the horizontal left boundary (HLB) address equals to 4 times of HzoomStart and the vertical top boundary (VTB) address equals to 2 times of VzoomStart. (HLB, VTB) defines the original point of the zoomed in area. You can zoom in any 1/4 screen of base video image to full screen image as shown in figure 12.

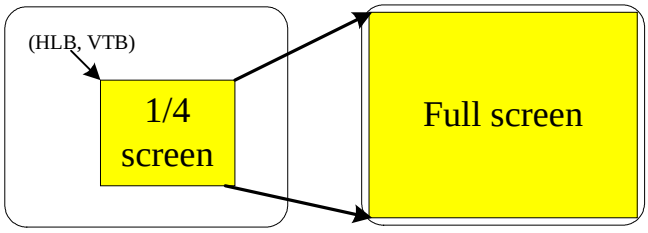


Figure 12: 2X Zoom In Function

In application, Borderline 1 can be turned on first to preview the zooming area on QUAD or FULL display screen. The previewing window can be moved around by programming registers (HZOOMSTART, VZOOMSTART), and then change display to ZOOM in mode.

7.8 Overlay Control

AL700/701/710 supports internal and external OSD (On-Screen Display) overlay control. By embedding SRAM, AL700/701/710 can overlay internal OSD text on top of the video for the applications like pop-up menu, message text or captions. Also AL700/701/710 can interface with external OSD chip.

7.8.1 Internal OSD mode

There are 1K-byte Context RAM and 4K-byte Font RAM embedded to support internal OSD function. Two independent OSD (OSD1 and OSD2) windows are provided and can be enabled on monitor and/or VCR output respectively. If there is an overlap between OSD1 and OSD2, the OSD1 will be on the top display layer. The internal OSDs are very flexible in the way that the font, size, and display location are fully programmable.

There are two kinds of OSD modes supported in the internal OSDs, they are 1-byte mode and 2-byte mode. The internal Context RAM storages the OSD character codes. The character codes in the Context RAM would be decoded as the index of the font table in Font RAM. Also included in the Context RAM is the blinking bit that can enable or disable the blinking function for the corresponding character. In 2-byte mode, additional attributes define the foreground and background color information related to the corresponding character.

The OSD controller will generate OSD key after it reads out the font data. The OSD key selects the colors to be overlaid on the screen based on the data stored in Context RAM (in 2-byte mode) or the control registers (in 1-byte mode, #32h<3:0> and #42h<3:0>) that decide when and where these colors are displayed on the screen. The OSD key is used to select four out of 16 million (24 bits) OSD colors.

The selected OSD characters and their color data are then passed through the internal blink control circuits. The blinking frequency is controlled by the BLINKCTRL (register #21h) with VYSNC as the reference counting clock. The blinking information is stored as data embedded with character codes stored in Context RAM.

After the processed blinking data is passed to the Boolean logic operation section, the Boolean logic operation section performs special OSD effects such as translucent, opaque, negative, and posterization. The Boolean logic operation feature, which provides a vivid and unique way of implementing display menu and status, is controlled by the FOREOP (#23h) register.

The fading operation block creates the effect of smoothly fading in and fading out the OSD titles or menu. Fading is controlled by register ALPHA (#22h).

Following is the block diagram of the AL700/701/710 OSD.

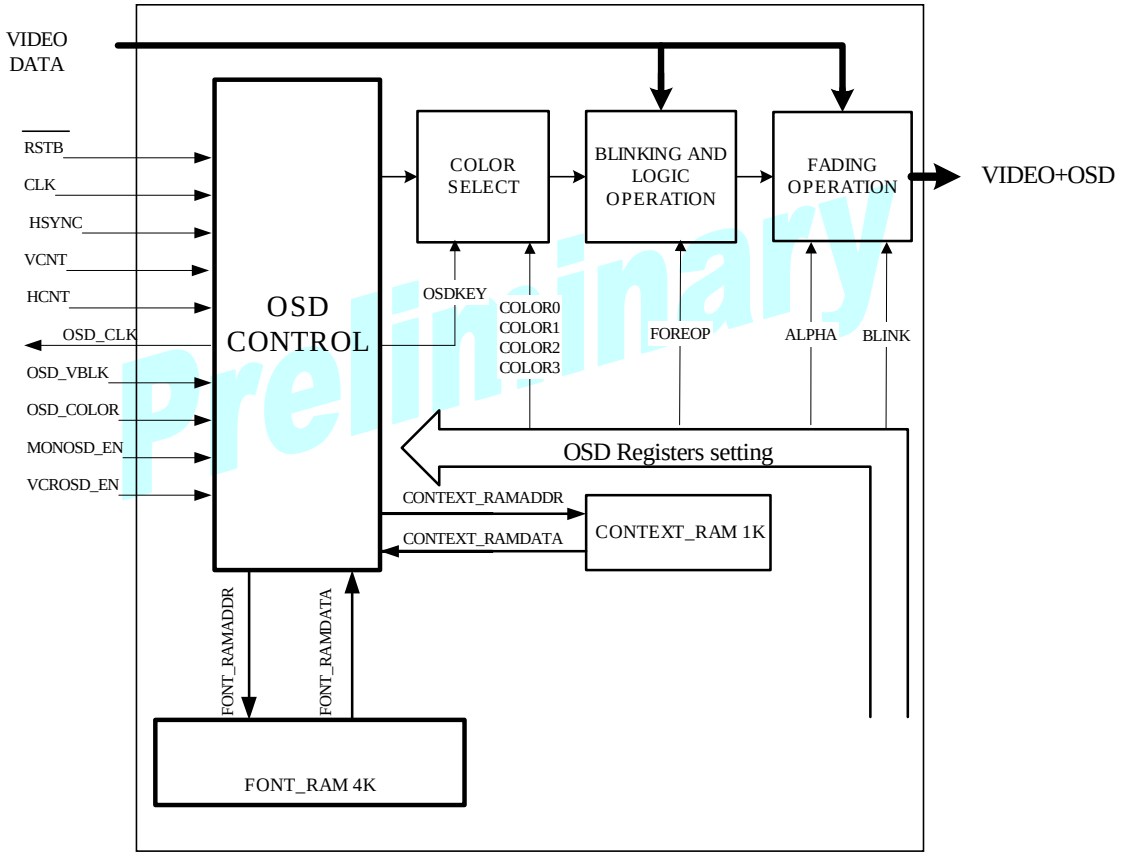


Figure 13: AL700/701/710 OSD Block Diagram

The Context RAM is used to store the Character code or index for accessing a specific font (a font can be viewed as a pre-defined bitmap) stored in Font RAM. The address of the Character code is generated first to retrieve the index address to a specific font or bitmap. The following Font RAM address generators then calculate the address of the font stored in Font RAM based on the Character code read from Context RAM. The 8-bit data read from Font RAM is then unpacked into 1-bit or 2-bit data depending if 2-color mode or 4-color mode is selected. MSB bits are read out as OSD data before the LSB bits. This is illustrated as follows:

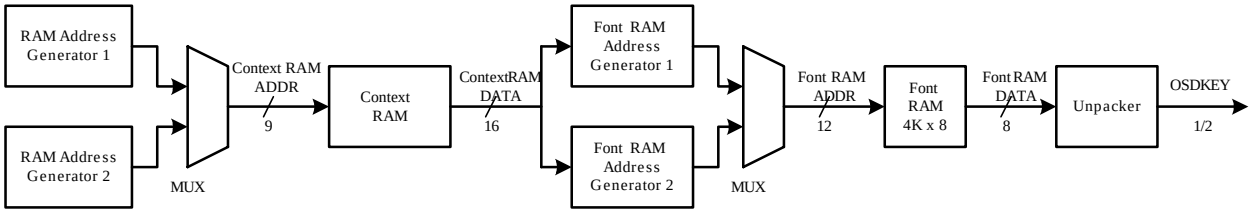


Figure 14: The Addressing of Context and Font RAMs

The font addressing code can be in 1-byte or 2-byte formats. CONTEXTSTADDR1 (#36h) and CONTEXTSTADDR2 (#46h) are the starting addresses of the Character codes of OSD1 and OSD2 stored in Context RAM. The starting address should be an even number in the 2-byte data mode. The Character code is used to address the font data stored in Font RAM. The address of a data of a specific font is calculated as:

Address = Font RAM Start Address + (Character code * Font Address Unit) + (OSD line count * FONTLINESIZE)

The data format stored in Context RAM for addressing of OSD bitmap data is illustrated in the following diagram.

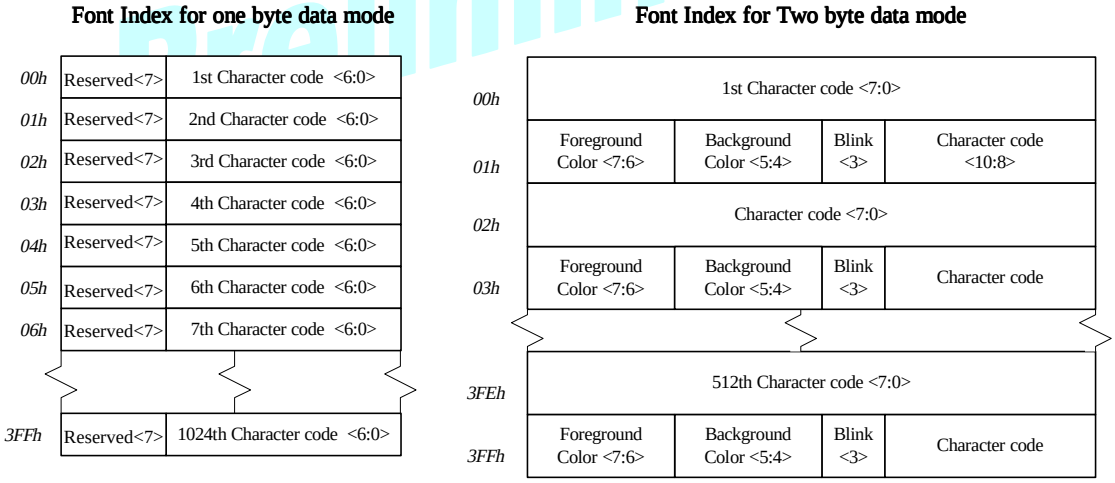


Figure 15: OSD Data Addressing in Context RAM

7.8.2 Internal OSD Timing

The register OSDHSTART (#34h or #44h) refers to the horizontal starting position of the OSD window relative to the leading edge of HSYNC. OSDVSTART (#35h or #45h) refers to the vertical starting position of the OSD window relative to the leading edge of VSYNC. The BMAPHSIZE (#38h or #48h) defines the horizontal visible portion of the font (it can be smaller or equal to the actual horizontal font size). BMAPHTOTAL (#39h or #49h) is BMAPHSIZE plus the horizontal size of the border or gap in between fonts. The BMAPVSIZE (#3Ah or #4Ah) defines the vertical visible portion of the font (it can be smaller or equal to the actual vertical font size). BMAPVTOTAL (#3Bh or #4Bh) is

BMAPVSIZE plus the vertical size of border or gap in between fonts. The total numbers of fonts in the horizontal and vertical directions are defined by ICONHTOTAL (#3Ch or #4Ch) and ICONVTOTAL (#3Dh or #4Dh).

The screen-timing diagram of the OSD window is as follows:

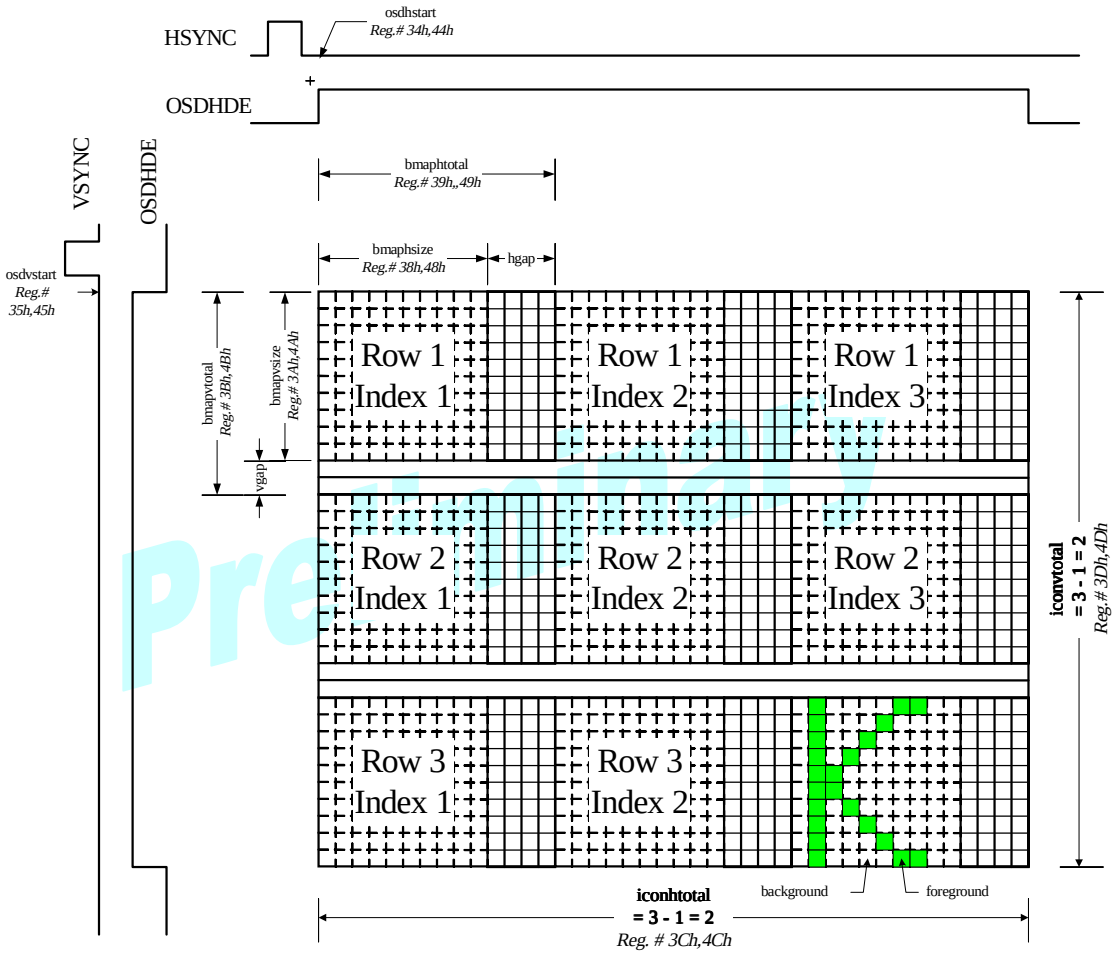


Figure 16: OSD Screen Timing Diagram

7.8.3 OSD Bitmap/Font Formatting

The following two examples show how the bitmaps or fonts should be formatted for internal OSD operation. The first example uses 2-bit per pixel formatting:

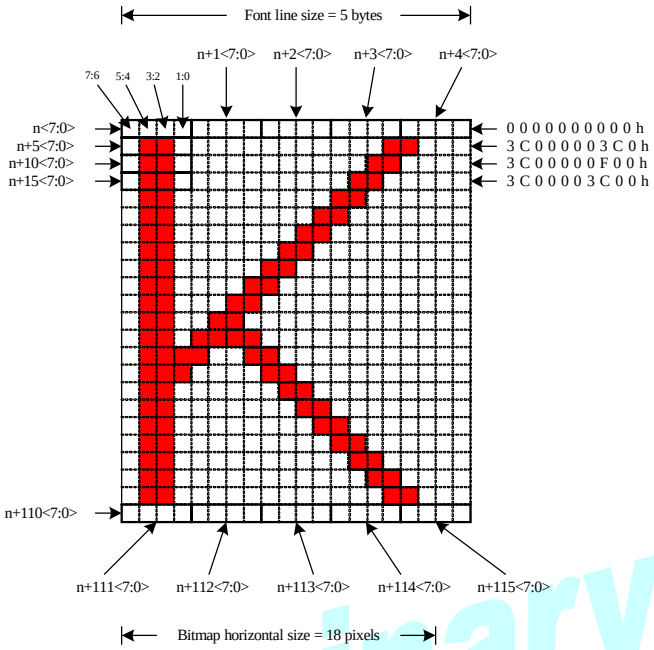


Figure 17: OSD Bitmap_Font Formating (2-bit per pixel)

The next example uses 1-bit per pixel formatting:

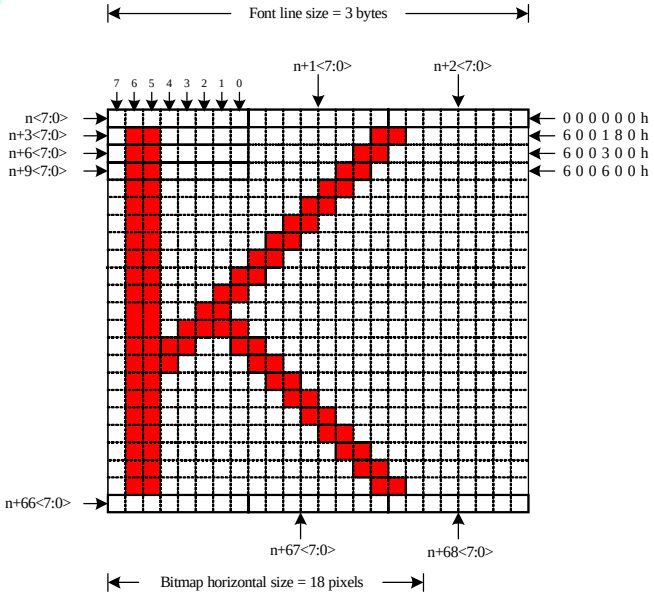
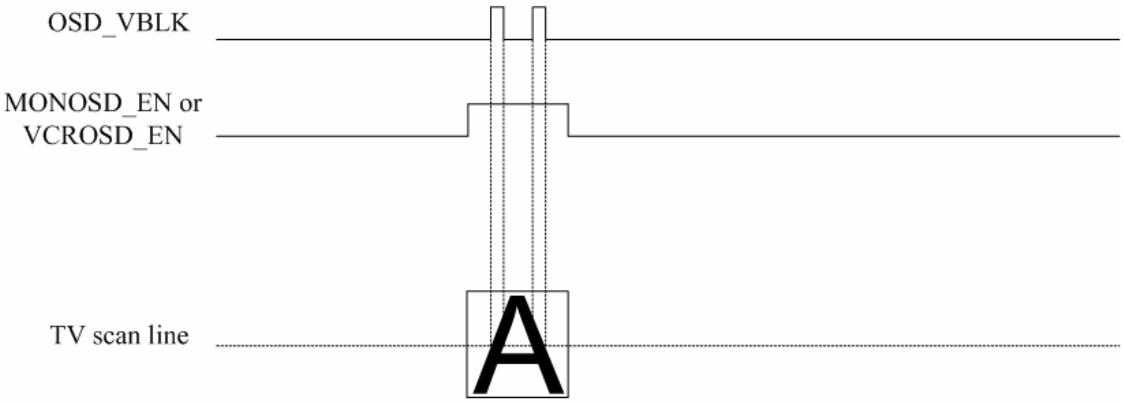


Figure 18: OSD Bitmap_Font Formating (1-bit per pixel)

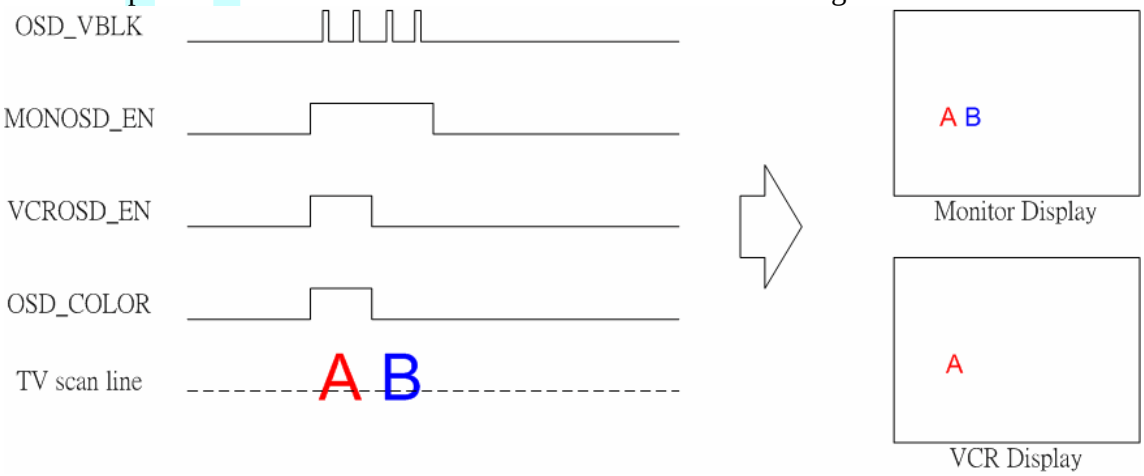
7.8.4 External OSD Mode

AL700/701/710 also supports external OSD mode. Most of the OSD devices use OSD_VBLK to define the OSD active region. AL700/701/710 uses MONOSD_EN and VCROSD_EN to decide whether the OSD Icons are shown on monitor and/or VCR display output. The OSD_COLOR selects the color from color 0 or color 1 defined in color LUT.

The following diagram shows how the OSD_VBLK signal defines the OSD active region:



The example bellow describes the function of each OSD control signal.



7.9 Memory Interface

AL700/701/710 supports various SDRAM configurations, such as 1Mx16 and 4Mx16 bit SDRAM, which can be selected by register #81h. AL700/701/710 uses sequential Burst mode to control SDRAM memory that operates at minimum 108MHz (9ns cycle time) of clock frequency. Also you can use DRAMCTL0 and DRAMCTL1 registers (#80h and #81h) to adjust the read/write performance of SDRAM. For detail operation of SDRAM, please reference memory maker specifications.

7.10 Image Data Upload

AL700/701/710 supports 8-bit host bus that allows the microprocessor to directly read the digital image data from the SDRAM video memory. UPIMGCTR (#58h) register controls the image data uploading attributes. UPIMGYDP (#59h) and UPIMGCDP (#5Ah) registers store the Luminance and Chrominance data of a pixel, respectively.

Internal image read counter will automatically increase when read UpImgYDP or UPImagCDP. To ensure image uploading correctly, the monitor output must be set to freeze mode and the internal image read counter must be reset before uploading an image.

The pixel number of an image depends on the monitor display output mode. The first pixel is the upper most, top left point of a picture image. The image data is sequentially stored in the memory. The first pixel data of the following horizontal line is next to the last pixel data of the previous horizontal line. The microprocessor should calculate the image resolution, such as vertical and horizontal total pixels, to the read-out data so that it can re-build the picture image properly.

7.11 Interrupt

AL700/701/710 interrupt function is supported by INTR pin, INTRSTATUS (#06h) and INTRMASK (#07h) registers. The Intr_pol (#03h <4>) controls the polarity of INTR pin. The INTR pin is active High if Intr_pol is set to 1 and vice versa. INTRSTATUS reflects the interrupt status of video loss or motion detection. Each bit of INTRSTATUS indicates one interrupt event and is active High. Set '1' to the corresponding bit in the INTRSTATUS register will clear the interrupt status.

Each interrupt status bit has its mask bit to disable the hardware INTR signal. Set '1' to the corresponding bit in the INTRMASK register will prohibit that channel to activate the interrupt. The mask bit affects only the action of INTR and will not change the interrupt status in INTRSTATUS register. AL700/701/710 will issue an "INTR" request to an external micro-controller if there is at least one non-zero bit in the INTRSTATUS register and its corresponding mask bit is 0.

06h	INTRSTATUS						R/W
[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
MotionD	MotionC	MotionB	MotionA	VdoLossD	VdoLossC	VdoLossB	VdoLossA
07h	INTRMASK						R/W
[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
Mask_MD	Mask_MC	Mask_MB	Mask_MA	Mask_VLD	Mask_VLC	Mask_VLB	Mask_VLA

If INTR is active High, then using Boolean logic equation to express INTR is as follows:

INTR = (MotionD AND Mask_MD) OR (MotionC AND Mask_MC) OR (MotionB AND Mask_MC) OR (MotionA AND Mask_MA) OR (VdoLossD AND Mask_VLD) OR (VdoLossC AND Mask_VLC) OR (VdoLossB AND Mask_VLB) OR (VdoLossA AND Mask_VLA)

8 Register Definition

Registers are provided to setup AL700/701/710. These registers can be programmed via host interface. The host interface protocol is illustrated in "Host Interface" paragraph. The application notes will describe more detailed settings about these registers. Upon request, AverLogic will provide the sample code or tool of host interface control software.

8.1 Register Set

Register Name	Address	R/W	Default	Function
System Configuration				
COMPANYID	00h	R	46h	Company ID
REVISION	01h	R		Revision number
FAMILY	02h	R	70/71h	Chip family
SYSCONFIG	03h	R/W	00h	System configuration
DATAFORMAT	04h	R/W	00h	Input/Output data format
POLARITY	05h	R/W	00h	Signal polarity
Interruption Status and Mask				
INTRSTATUS	06h	R/W	00h	Interruption status
INTRMASK	07h	R/W	00h	Interruption mask
Capture Control				
CAPTURECTRL	08h	R/W	00h	Capture control
CAPHSTART	09h, 0Ah	R/W	00h	Horizontal capture start position
CAPVSTART	0Bh	R/W	00h	Vertical capture start position
VLOSSSIG	0Ch	R/W	00h	Video loss referred Signal
ADCTHRESHOLD	0Dh, 0Eh	R/W	00h	ADC threshold
DECSWCTR	0Fh	R/W	00h	Decoder switch control
Channel Configuration				
CHACTRL	10h	R/W	00h	Channel A control
CHBCTRL	11h	R/W	00h	Channel B control
CHCCTRL	12h	R/W	00h	Channel C control
CHDCTRL	13h	R/W	00h	Channel D control
FULLBDRCTR	14h	R/W	00h	Full border line control
BDRBLINKCTR	15h	R/W	00h	Border line blink control
	16h			Reserved
Display Control				
INTENCOUTSEL	17h	R/W	00h	Internal encoder output selection
DISPLAYCTRL	18h	R/W	00h	Display control
MTROUTSEL	19h	R/W	00h	Monitor output configuration
PIPCTRL	1Ah	R/W	00h	Picture in picture control
DISPHSTART	1Bh, 1Ch	R/W	00h	Horizontal display start position
DISPVSTART	1Dh	R/W	00h	Vertical display start position
HZOOMSTART	1Eh	R/W	00h	The left boundary of zoom-in area
VZOOMSTART	1Fh	R/W	00h	The top boundary of zoom-in area

Register Name	Address	R/W	Default	Function
Overlay Control				
OVERLAYCTRL	20h	R/W	00h	Overlay control
BLINKCTRL	21h	R/W	00h	Blinking control
ALPHA	22h	R/W	00h	Alpha register
FOREOP	23h	R/W	00h	Overlay Boolean operation
LUT0Y	24h	R/W	00h	Look-up table (LUT) color 0 – Luminance Y
LUT0U	25h	R/W	00h	LUT color 0 – Chrominance U
LUT0V	26h	R/W	00h	LUT color 0 – Chrominance V
LUT1Y	27h	R/W	00h	LUT color 1 – Luminance Y
LUT1U	28h	R/W	00h	LUT color 1 – Chrominance U
LUT1V	29h	R/W	00h	LUT color 1 – Chrominance V
LUT2Y	2Ah	R/W	00h	LUT color 2 – Luminance Y
LUT2U	2Bh	R/W	00h	LUT color 2 – Chrominance U
LUT2V	2Ch	R/W	00h	LUT color 2 – Chrominance V
LUT3Y	2Dh	R/W	00h	LUT color 3 – Luminance Y
LUT3U	2Eh	R/W	00h	LUT color 3 – Chrominance U
LUT3V	2Fh	R/W	00h	LUT color 3 – Chrominance V
OSD 1 Control				
OSDCONTROL1	30h	R/W	00h	OSD1 control
FONTSTADDR1	31h	R/W	00h	OSD1 Font RAM start address
FONTADDRUNIT1	32h	R/W	00h	OSD1 font address unit
FONTLINESIZE1	33h	R/W	00h	OSD1 font line size
OSDHSTART1	34h	R/W	00h	OSD1 horizontal start point
OSDVSTART1	35h	R/W	00h	OSD1 vertical start point
CONTEXTSTADDR1	36h	R/W	00h	OSD1 context RAM start address
RAMSTRIDE1	37h	R/W	00h	OSD1 RAM line stride
BMAPHSIZE1	38h	R/W	00h	OSD1 bitmap horizontal size
BMAPHTOTAL1	39h	R/W	00h	OSD1 bitmap total horizontal size
BMAPVSIZE1	3Ah	R/W	00h	OSD1 bitmap vertical size
BMAPVTOTAL1	3Bh	R/W	00h	OSD1 bitmap total vertical size
ICONHTOTAL1	3Ch	R/W	00h	OSD1 total horizontal icons
ICONVTOTAL1	3Dh	R/W	00h	OSD1 total vertical icons
	3Eh, 3Fh			Reserved
OSD 2 Control				
OSDCONTROL2	40h	R/W	00h	OSD2 control
FONTSTADDR2	41h	R/W	00h	OSD2 Font RAM start address
FONTADDRUNIT2	42h	R/W	00h	OSD2 font address unit
FONTLINESIZE2	43h	R/W	00h	OSD2 font line size
OSDHSTART2	44h	R/W	00h	OSD2 horizontal start point
OSDVSTART2	45h	R/W	00h	OSD2 vertical start point
CONTEXTSTADDR2	46h	R/W	00h	OSD2 context RAM start address
RAMSTRIDE2	47h	R/W	00h	OSD2 RAM line stride

Register Name	Address	R/W	Default	Function
BMAPHSIZE2	48h	R/W	00h	OSD2 bitmap horizontal size
BMAPHTOTAL2	49h	R/W	00h	OSD2 bitmap total horizontal size
BMAPVSIZE2	4Ah	R/W	00h	OSD2 bitmap vertical size
BMAPVTOTAL2	4Bh	R/W	00h	OSD2 bitmap total vertical size
ICONHTOTAL2	4Ch	R/W	00h	OSD2 total horizontal icons
ICONVTOTAL2	4Dh	R/W	00h	OSD2 total vertical icons
	4Eh, 4Fh			Reserved
RAM Access				
ADDRL	50h	W	00h	Address [7:0]
ADDRM	51h	W	00h	Address [15:8]
ADDRH	52h	W	00h	Target selection & Address [17:16]
DATAPORT	53h	W	00h	Data port
	54~57h			Reserved
Image Upload Setting				
UPIMGCTR	58h	R/W	00h	Upload image control
UPIMGYDP	59h	R	00h	Upload image Y read port
UPIMGCDP	5Ah	R	00h	Upload image C read port
	5B~5Fh			Reserved
External Encoder Interface Setting				
HSYNCWIDTH	60h, 61h	R/W	00h	Output HSYNC width
VSYNCWIDTH	62h	R/W	00h	Output VSYNC width
	63~6Ah			Reserved
Motion Detection				
MOTIONADDR	6Bh	W	00h	Mean and Variance address
MEANDATAL, H	6Ch, 6Dh	R	00h	Data of mean
VARIANCEDATAL, H	6Eh, 6Fh	R	00h	Data of variance
MEANTH0L, H	70h, 71h	W	00h	Threshold of mean 0
MEANTH1L, H	72h, 73h	W	00h	Threshold of mean 1
MEANTH2L, H	74h, 75h	W	00h	Threshold of mean 2
MEANTH3L, H	76h, 77h	W	00h	Threshold of mean 3
VARIANCETH0L, H	78h, 79h	W	00h	Threshold of variance 0
VARIANCETH1L, H	7Ah, 7Bh	W	00h	Threshold of variance 1
VARIANCETH2L, H	7Ch, 7Dh	W	00h	Threshold of variance 2
VARIANCETH3L, H	7Eh, 7Fh	W	00h	Threshold of variance 3
SDRAM Interface				
DRAMCTRL0, 1	80h, 81h	R/W	00h	SDRAM timing parameters
ENABLE_CTRL	82h	R/W	00h	SDRAM enable control
MIN_REFRESH	83h	R/W	00h	SDRAM minimum refresh control
CAW_LEVEL	84h	R/W	08h	Channel A quad capture FIFO control
CBW_LEVEL	85h	R/W	08h	Channel B quad capture FIFO control
CCW_LEVEL	86h	R/W	08h	Channel C quad capture FIFO control
CDW_LEVEL	87h	R/W	08h	Channel D quad capture FIFO control

Register Name	Address	R/W	Default	Function
CFW_LEVEL	88h	R/W	10h	Full video capture FIFO control
QDR_LEVEL	89h	R/W	10h	VCR output display FIFO control
FDR_LEVEL	8Ah	R/W	10h	Monitor output display FIFO control
	8B~8Fh			Reserved
Test Registers				
	90~9Fh		00h	Reserved for factory test only

8.2 Register Description

8.2.1 System Configuration

00h	COMPANYID						R
[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
CompanyId							

COMPANYID: Defines the company ID.

CompanyId <7:0> Company ID (default value is 46h)

01h	REVISION						R
[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
Revision							

REVISION: Defines the IC revision number.

Revision <7:0> Revision number

02h	FAMILY						R
[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
Family							

FAMILY: Defines the chip family.

Family <7:0> 0x70 AL700 series
0x71 AL710 series

03h	SYSCONFIG						R/W
[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
disp_tstb	cap_tstb	dram_rstb	Intr_pol	Reserved	OSDsource	ITU-R-601-16bit	Vsystem

SYSCONFIG: Defines the system configurations.

Vsystem	<0>	Video system (default value is 0)
	0	525 line system (like as NTSC)
	1	625 line system (like as PAL/SECAM)
ITU-R-601_16bit	<1>	Bus width of ITU-R-601 output data (default value is 0)
	0	8 bits
	1	16 bits (suitable for AL250/251)
OSDsource	<2>	Select OSD source (default value is 0)
	0	Use internal OSD controller
	1	Use external OSD IC
Intr_pol	<4>	Defines interrupt active level (default value is 0)
	0	Interrupt active Low
	1	Interrupt active High
dram_rstb	<5>	Used to reset the SDRAM interface (default value is 0)
	0	Normal
	1	Reset SDRAM interface
cap_rstb	<6>	Used to rest capture interface (default value is 0)
	0	Normal
	1	Reset capture interface
disp_rstb	<7>	Used to reset display interface (default value is 0)
	0	Normal
	1	Reset display interface

04h	DATAFORMAT						R/W
[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
Reserved	OutSeq		Out656	Rev_Vclk_en	InSeq		In656

DATAFORMAT: Defines the input/output data formats.

In656	<0>	Enable ITU-R-656 format for input data (default value is 0)
	0	ITU-R-601 compatible 4:2:2 YCrCb video format with independent sync and flag signals. AL710 only supports ITU-R-601 format.
	1	ITU-R-656 compatible video format with embedded sync signal
InSeq	<2:1>	Select YCrCb sequence for input data (default value is 00)
	00	Cb, Y, Cr, Y
	01	Cr, Y, Cb, Y
	10	Y, Cb, Y, Cr
	11	Y, Cr, Y, Cb
Rev_Vclk_en	<3>	Select video clock output pattern (default value is 0)
	0	Normal
	1	Reverse video clock output (VCLK)
Out656	<4>	Enable ITU-R-656 format for output data (default value is 0)
	0	ITU-R-601 compatible 4:2:2 YCrCb video format with independent sync and flag signals. AL710 only supports ITU-R-601 format.
	1	ITU-R-656 compatible video format with embedded sync signal
OutSeq	<6:5>	Select YCrCb sequence for output data (default value is 00)
	00	Cb, Y, Cr, Y
	01	Cr, Y, Cb, Y
	10	Y, Cb, Y, Cr
	11	Y, Cr, Y, Cb

05h	POLARITY						R/W
[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
Reserved	field_det	OutFldPol	OutHsPol	OutVspol	InFldPol	InHsPol	InVsPol

POLARITY: Defines the signal polarity.

InVsPol	<0>	Choose input vertical sync polarity (default value is 0)
	0	Positive polarity
	1	Negative polarity
InHsPol	<1>	Choose input horizontal sync polarity (default value is 0)
	0	Positive polarity
	1	Negative polarity
InFldPol	<2>	Choose input field polarity (default value is 0)
	0	Positive polarity
	1	Negative polarity
OutVsPol	<3>	Choose output vertical sync polarity (default value is 0)
	0	Positive polarity
	1	Negative polarity
OutHsPol	<4>	Choose output horizontal sync polarity (default value is 0)
	0	Positive polarity
	1	Negative polarity
OutFldPol	<5>	Choose output field polarity (default value is 0)
	0	Positive polarity
	1	Negative polarity
field_det	<6>	Choose field detection mode (default value is 0)
	0	Use external signal
	1	Detected by Horizontal sync and Vertical sync

8.2.2 Interruption Status and Mask

06h	INTRSTATUS							R/W
[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
MotionD	MotionC	MotionB	MotionA	VdoLossD	VdoLossC	VdoLossB	VdoLossA

INTRSTATUS: Defines the interrupt status. There indicates a corresponding interrupt while reading '1' at a bit. Write '1' to a bit will clear the corresponding interrupt status. There is no effect while writing '0' to any bit. Default value is 0.

VdoLossA	<0>	Status of video loss from channel A
VdoLossB	<1>	Status of video loss from channel B
VdoLossC	<2>	Status of video loss from channel C
VdoLossD	<3>	Status of video loss from channel D
MotionA	<4>	Status of motion detection from channel A
MotionB	<5>	Status of motion detection from channel B
MotionC	<6>	Status of motion detection from channel C
MotionD	<7>	Status of motion detection from channel D

07h	INTRMASK							R/W
[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
Mask_MD	Mask_MC	Mask_MB	Mask_MA	Mask_VLD	Mask_VLC	Mask_VLB	Mask_VLA

INTRMASK: Defines the interrupt masks. There represents that a corresponding interrupt is masked while writing '1' to a bit. AL700/701/710 will issue an "INTR" request to an external micro-controller if there is at least one non-zero bit in the INTRSTATUS register and its corresponding mask bit is 0. Default value is 0.

Mask_VLA	<0>	Mask of video loss from channel A
Mask_VLB	<1>	Mask of video loss from channel B
Mask_VLC	<2>	Mask of video loss from channel C
Mask_VLD	<3>	Mask of video loss from channel D
Mask_MA	<4>	Mask of motion detection from channel A
Mask_MB	<5>	Mask of motion detection from channel B
Mask_MC	<6>	Mask of motion detection from channel C
Mask_MD	<7>	Mask of motion detection from channel D

8.2.3 Capture Control

08h	CAPTURECTRL						R/W
[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
ext_syncsep	Field_Cap	Samplerate_sel	mux_mode	Reserved	SoftRef	Qualify1	Qualify0

CAPTURECTRL: Defines the capture control features.

Qualify0	<0>	Select operation for qualified data (default value is 0)
	0	Choose valid 0 for each channel
	1	Choose the reverse of valid 0 for each channel (~valid 0)
Qualify1	<1>	Select operation for qualified data (default value is 0)
	0	Choose valid 1 for each channel
	1	Choose reverse of valid 1 for each channel (~valid 1)
SoftRef	<2>	Select data-valid modes. Default value is 0. For AL710, this bit should be set to '1' and the registers 09h, 0Ah, and 0Bh should be set appropriate values.
	0	Valid data is qualified by the hardware valid pins in ITU-R-601 mode or HACTIVE code in ITU-R-656 mode
	1	Capture start is defined by registers 09h, 0Ah, and 0Bh
mux_mode	<4>	Choose the number of decoders (default value is 0)
	0	normal (connect 4 external decoders)
	1	1 decoder for 2 channels (connect 2 external decoders)
Samplerate_sel	<5>	Select ADC sample rate (only for AL710, default value is 0)
	0	27 MHz
	1	54 MHz
Field_Cap	<6>	Choose field capture mode (default value is 0)
	0	Capture odd field only
	1	Capture maybe either odd or even field
ext_syncsep	<7>	Defines sync separator source (only for AL710, default value is 1)

	0	Use internal sync separator for AL710. Not only the Samplerate_sel bit but also the registers 0Dh and 0Eh should be set appropriate values. The decoder input pins used in this mode are DI_A[7:0], DI_B[7:0], DI_C[7:0], DI_D[7:0], VCLK_A, VCLK_B, VCLK_C, and VCLK_D.
	1	Use external sync separator for AL710

09h	CAPHSTART						R/W
[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
CapHStart[7:0]							
0Ah	CAPHSTART						R/W
[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
Reserved						CapHStart[9:8]	

CAPHSTART: Defines the horizontal capture start position. Default value is 0. The unit is one pixel.

CapHStart[7:0]	<7:0>	Bits<7:0> of horizontal capture start position
CapHStart[9:8]	<1:0>	Bits<9:8> of horizontal capture start position

0Bh	CAPVSTART						R/W
[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
CapVStart[7:0]							

CAPVSTART: Defines the vertical capture start position. Default value is 0. The unit is one line.

CapVStart	<7:0>	Vertical capture start position

0Ch	VLOSSSIG						R/W
[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
DATA_Loss	CLK_Loss	Htotal_Loss	VS_Loss	HS_Loss	Reserved	Val1_Loss	Val0_Loss

VLOSSSIG: Enables the video loss referred signals. Default value is 0. There represents that the signal is enabled if the corresponding bit is set to '1'. The Vloss will be enabled if there is any one bit enabled.

Val0_Loss	<0>	Enable the Valid 0 loss signal
	0	Disable
	1	Enable
Val1_Loss	<1>	Enable the Valid 1 loss signal

	0	Disable
	1	Enable
Reserved	<2>	Reserved
HS_Loss	<3>	Enable the horizontal sync loss signal
	0	Disable
	1	Enable
VS_Loss	<4>	Enable the vertical sync loss signal
	0	Disable
	1	Enable
Htotal_Loss	<5>	Enable the horizontal total pixel loss signal
	0	Disable
	1	Enable
CLK_Loss	<6>	Enable the clock loss signal
	0	Disable
	1	Enable
DATA_Loss	<7>	Enable the data loss signal
	0	Disable
	1	Enable

Vloss = Val0_Loss or Val1_Loss or HS_Loss or VS_Loss or Htotal_Loss or CLK_Loss or DATA_Loss

0Dh	ADCTHRESHOLD						R/W
[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
ADC2_Threshold				ADC1_Threshold			
0Eh	ADCTHRESHOLD						R/W
[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
ADC4_Threshold				ADC3_Threshold			

ADCTHRESHOLD: Defines the threshold of ADC. Default values are 0. These registers are only available for AL710. The unit is the same as the external ADC resolution.

ADC1_Threshold	<3:0>	ADC threshold of channel A
ADC2_Threshold	<7:4>	ADC threshold of channel B
ADC3_Threshold	<3:0>	ADC threshold of channel C

ADC4_Threshold <7:4> ADC threshold of channel D

0Fh	DECSWCTR						R/W
[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
Htotal_range				Swithc_Dly			

DECSWCTR: Defines the delayed field numbers while switching channel and the horizontal total lost pixels during two Hsync signals for video loss detection.

Switch_Dly <3:0> Field numbers delayed while switching channel (default value is 0)

Htotal_range <7:4> Horizontal total pixel range for video loss detection (default value is 0)

8.2.4 Channel Configuration

10h	CHACTRL						R/W
[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
Reserved	V1_flipx	Border1_color		Border1_enx		v1FreezeSel	
11h	CHBCTRL						R/W
[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
Reserved	V2_flipx	Border2_color		Border2_enx		v2FreezeSel	
12h	CHCCTRL						R/W
[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
Reserved	V3_flipx	Border3_color		Border3_enx		v3FreezeSel	
13h	CHDCTRL						R/W
[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
Reserved	V4_flipx	Border4_color		Border4_enx		v4FreezeSel	

CHACTRL, CHBCTRL, CHCCTRL, CHDCTRL: Defines the control configurations of channel A, B, C, and D repectively.

v1FreezeSel <1:0> Select freeze mode (default value is 0)

v2FreezeSel 00 Normal (live video)

v3FreezeSel 01 Freeze a frame image

v4FreezeSel 10 Freeze an odd field image

11 Freeze an even field image

Border1_enx <3:2> Control borderline display (default value is 0)

Border2_enx	00	Disable
Border3_enx	01	Enable monitor
Border4_enx	10	Enable VCR
	11	Enable both monitor and VCR
Border1_color	<5:4>	Select borderline color (default value is 0)
Border2_color	00	LUT 0
Border3_color	01	LUT 1
Border4_color	10	LUT 2
	11	LUT 3
v1_flipx	<6>	Mirror the channel video image at X-axis (default
v2_flipx		value is 0)
v3_flipx	0	Normal (no mirror)
v4_flipx	1	Enable mirror function

14h	FULLBDCTRL						R/W
[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
Reserved				Border5_color		Border5_enx	

FULLBDRCTR: Defines the control configurations of full borderline.

Border5_enx	<1:0>	Control borderline display (default value is 0)
	00	Disable
	01	Enable monitor
	10	Enable VCR
	11	Enable both monitor and VCR
Border5_color	<3:2>	Select borderline color (default value is 0)
	00	LUT 0
	01	LUT 1
	10	LUT 2
	11	LUT 3

15h	BDRBLINKCTR						R/W
[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
Reserved			Border5_ blink	Border4_ blink	Border3_ blink	Border2_ blink	Border1_ blink

BDRBLINKCTR: Defines the borderline blink controls.

Border1_blink	<0>	Enable Border1 blink function (default value is 0)
	0	Normal (on blink)
	1	Blink
Border2_blink	<1>	Enable Border2 blink function (default value is 0)
	0	Normal (on blink)
	1	Blink
Border3_blink	<2>	Enable Border3 blink function (default value is 0)
	0	Normal (on blink)
	1	Blink
Border4_blink	<3>	Enable Border4 blink function (default value is 0)
	0	Normal (on blink)
	1	Blink
Border5_blink	<4>	Enable Border5 blink function (default value is 0)
	0	Normal (on blink)
	1	Blink

8.2.5 Display Control

17h	INTENCOUTSEL						R/W
[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
Reserved				RevVCRField	RevMonField	Ienc_Out_Sel	

INTENCOUTSEL: Selects internal encoder outputs and field polarity.

Ienc_Out_Sel	<1:0>	Choose the output formats for monitor and VCR (default value is 0)
	00	Composite output for both monitor and VCR
	01	S-video output for monitor and Composite output for VCR
	10	Composite output for monitor and S-video output for VCR

	11	Reserved
RevMonField	<2>	Reverse the field polarity of monitor output (default value is 0)
	0	Normal
	1	Reverse
RevVCRField	<3>	Reverse the field polarity of VCR output (default value is 0)
	0	Normal
	1	Reverse

18h	DISPLAYCTRL						R/W
[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
Genlock	Reserved	ColorBar	BW	BorderCenter	BorderWidth	Enc_clksel	EncoderSel

DISPLAYCTRL: Defines the control configurations of display.

EncoderSel	<0>	Select encoder source (default value is 0)
	0	Use internal encoders
	1	Use external encoders
	Note: For AL701, this bit should be set to “1”.	
Enc_clksel	<1>	Select internal encoder clock (default value is 0)
	0	4 times of video clock frequency (14.3182MHz for NTSC, 17.7345MHz for PAL)
	1	27 MHz
BorderWidth	<2>	Select borderline width (default value is 0)
	0	4 pixels
	1	8 pixels
BorderCenter	<3>	Choose the overlay width of borderline (default value is 0)
	0	Normal (no overlay)
	1	overlay the borderlines in the center of screen
BW	<4>	Enable black and white mode of video output (only for AL700/701, default value is 0)
	0	Normal
	1	Video output is black and white
ColorBar	<5>	Generate Color-Bar pattern (default value is 0)

	0	Display normal picture
	1	Display Color-Bar Pattern
Genlock	<7>	Select the source of Sync timing for external encoder (default value is 0 and only valid when EncorderSel is set to 1)
	0	Use internally generated sync timing
	1	Sync timing generated by external encoder

19h	MTROUTSEL						R/W
[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
RBPIP_en	LBPIP_en	RTPIP_en	LTPIP_en	DisplayMode		ChSel	

MTROUTSEL: Defines the configurations of monitor output.

ChSel	<1:0>	Choose a channel as base video in FULL, PIP, or ZOOM mode (default value is 0)
	00	Choose channel A
	01	Choose channel B
	10	Choose channel C
	11	Choose channel D
DisplayMode	<3:2>	Select display mode (default value is 0)
	00	QUAD mode
	01	FULL mode
	10	PIP mode (Picture In Picture)
	11	ZOOM in mode
LTPIP_en	<4>	Enable the Left-Top window to show sub video in PIP mode (default value is 0)
	0	Disable
	1	Enable
RTPIP_en	<5>	Enable the Right-Top window to show sub video in PIP mode (default value is 0)
	0	Disable
	1	Enable
LBPIP_en	<6>	Enable the Left-Bottom window to show sub video in PIP mode (default value is 0)
	0	Disable

	1	Enable
RBPIP_en	<7>	Enable the Right-Bottom window to show sub video in PIP mode (default value is 0)
	0	Disable
	1	Enable

1Ah	PIPCTRL						R/W
[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
RB_ChSel		LB_ChSel		RT_ChSel		LT_ChSel	

PIPCTRL: Defines video channel source for each display window in PIP display mode.

LT_ChSel	<1:0>	Choose video channel for Left-Top window in PIP display mode (default value is 0)
	00	Choose channel A
	01	Choose channel B
	10	Choose channel C
	11	Choose channel D
RT_ChSel	<3:2>	Choose video channel for Right-Top window in PIP display mode (default value is 0)
	00	Choose channel A
	01	Choose channel B
	10	Choose channel C
	11	Choose channel D
LB_ChSel	<5:4>	Choose video channel for Left-Bottom window in PIP display mode (default value is 0)
	00	Choose channel A
	01	Choose channel B
	10	Choose channel C
	11	Choose channel D
RB_ChSel	<7:6>	Choose video channel for Right-Bottom window in PIP display mode (default value is 0)
	00	Choose channel A
	01	Choose channel B
	10	Choose channel C
	11	Choose channel D

1Bh	DISPHSTART						R/W
[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
DispHStart[7:0]							
1Ch	DISPHSTART						R/W
[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
Reserved						DispHStart[9:8]	

DISPHSTART: Defines the horizontal display start position. Default value is 0. The unit is 2 pixels.

DispHStart[7:0] <7:0> Bits<7:0> of horizontal display start position

DispHStart[9:8] <1:0> Bits<9:8> of horizontal display start position

1Dh	DISPVSTART						R/W
[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
DispVStart[7:0]							

DISPVSTART: Defines the vertical display start position. Default value is 0. The unit is 2 lines.

DispVStart <7:0> Bits<7:0> of vertical display start position

1Eh	HZOOMSTART						R/W
[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
Reserved	HZoomStart[6:0]						

HZOOMSTART: Defines the left boundary of ZOOM in area. Default value is 0. The unit is 4 pixels.

HZoomStart <6:0> Define the position of left boundary

Horizontal left boundary (HLB) = HZoomStart * 4 pixels

Horizontal right boundary = HLB + 360 pixels

The value of HZoomStart must be less than 0x5A.

1Fh	VZOOMSTART						R/W
[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
Reserved	VZoomStart[6:0]						

VZOOMSTART: Defines the top boundary of ZOOM in area. Default value is 0. The unit is 2 lines.

VZoomStart <6:0> Define the position of top boundary

Vertical top boundary (VTB) = VZoomStart * 2 lines

Vertical bottom boundary = VTB + 240 lines (for NTSC)

or = VTB + 288 lines (for PAL)

The value of VzoomStart must be less than 0x78 for NTSC system and 0x90 for PAL system.

When DisplayMode is set to ZOOM in mode, an area in each field defined by HzoomStart and VzoomStart will be zoomed in 2 times. The area size is 360x240 pixel-line in NTSC mode or 360x288 pixel-line in PAL mode. (HLB, VTB) defines the original point of the zoomed in area.

8.2.6 Overlay Control

20h	OVERLAYCTRL						R/W
[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
Reserved						BGColor	

OVERLAYCTRL: Defines the control configurations of overlay.

BGColor	<1:0>	Choose background color (default value is 0)
	00	Choose color 0 in color LUT
	01	Choose color 1 in color LUT
	10	Choose color 2 in color LUT
	11	Choose color 3 in color LUT

21h	BLINKCTRL						R/W
[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
Reserved				BlinkType		BlinkTime	

BLINKCTRL: Defines the control configurations of blink.

BlinkTime	<1:0>	Set the blinking time constant (default value is 0)
	00	32 frames of internal reference timing per blink
	01	64 frames of internal reference timing per blink
	10	128 frames of internal reference timing per blink
	11	256 frames of internal reference timing per blink
BlinkType	<3:2>	Choose blinking type (default value is 0)
	00	Blinking is defined by BlinkTime
	01	No blinking, just reverse the index color
	10	By pass
	11	Reserved

22h	ALPHA						R/W
[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
Reserved		Alpha[5:0]					

ALPHA: Defines the α factor for fading effect. Default value is 0.

Alpha <5:0> The range of α value is from 00h to 20h, that is, there are 33 levels of fade-in/fade-out effects.

output = input * α + overlay * (1-(α/32))

23h	FOREOP						R/W
[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
Color3Op		Color2Op		Color1Op		Color0Op	

FOREOP: Defines the overlay Boolean logic operations.

Color0Op <1:0> Select the Boolean logic operation between color 0 and video (default value is 0)

00 NOP operation: shows OSD bitmap image only

01 OR operation: displays the image after executing the OR Boolean logic operation of video and color 0

10 AND operation: displays the image after executing the AND Boolean logic operation of video and color 0

11 XOR operation: displays the image after executing the XOR Boolean logic operation of video and color 0

Color1Op <3:2> Select the Boolean logic operation between color 1 and video (default value is 0)

00 NOP operation: shows OSD bitmap image only

01 OR operation: displays the image after executing the OR Boolean logic operation of video and color 1

10 AND operation: displays the image after executing the AND Boolean logic operation of video and color 1

11 XOR operation: displays the image after executing the XOR Boolean logic operation of video and color 1

Color2Op <5:4> Select the Boolean logic operation between color 2 and video (default value is 0)

00 NOP operation: shows OSD bitmap image only

01 OR operation: displays the image after executing the OR Boolean logic operation of video and color 2

	10	AND operation: displays the image after executing the AND Boolean logic operation of video and color 2
	11	XOR operation: displays the image after executing the XOR Boolean logic operation of video and color 2
Color3Op	<7:6>	Select the Boolean logic operation between color 3 and video (default value is 0)
	00	NOP operation: shows OSD bitmap image only
	01	OR operation: displays the image after executing the OR Boolean logic operation of video and color 3
	10	AND operation: displays the image after executing the AND Boolean logic operation of video and color 3
	11	XOR operation: displays the image after executing the XOR Boolean logic operation of video and color 3

24h	LUT0Y						W
[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
LUT0Y[7:0]							
25h	LUT0U						W
[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
LUT0U[7:0]							
26h	LUT0V						W
[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
LUT0V[7:0]							

LUT0Y, LUT0U, LUT0V: Defines the Color 0 of Look-up Table (LUT). Default value is 0.

LUT0Y	<7:0>	Define the Y Luminance of color 0 in LUT
LUT0U	<7:0>	Define the U Chrominance of color 0 in LUT
LUT0V	<7:0>	Define the V Chrominance of color 0 in LUT

27h	LUT1Y						W
[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
LUT1Y[7:0]							
28h	LUT0U						W
[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
LUT1U[7:0]							
29h	LUT0V						W
[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
LUT1V[7:0]							

LUT1Y, LUT1U, LUT1V: Defines the Color 1 of Look-up Table (LUT). Default value is 0.

LUT1Y	<7:0>	Define the Y Luminance of color 1 in LUT
LUT1U	<7:0>	Define the U Chrominance of color 1 in LUT
LUT1V	<7:0>	Define the V Chrominance of color 1 in LUT

2Ah	LUT2Y						W
[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
LUT2Y[7:0]							
2Bh	LUT2U						W
[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
LUT2U[7:0]							
2Ch	LUT2V						W
[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
LUT2V[7:0]							

LUT2Y, LUT2U, LUT2V: Defines the Color 2 of Look-up Table (LUT). Default value is 0.

LUT2Y	<7:0>	Define the Y Luminance of color 2 in LUT
LUT2U	<7:0>	Define the U Chrominance of color 2 in LUT
LUT2V	<7:0>	Define the V Chrominance of color 2 in LUT

2Dh	LUT3Y						W
[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
LUT3Y[7:0]							
2Eh	LUT3U						W
[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
LUT3U[7:0]							
2Fh	LUT3V						W
[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
LUT3V[7:0]							

LUT3Y, LUT3U, LUT3V: Defines the Color 3 of Look-up Table (LUT). Default value is 0.

LUT3Y	<7:0>	Define the Y Luminance of color 3 in LUT
LUT3U	<7:0>	Define the U Chrominance of color 3 in LUT
LUT3V	<7:0>	Define the V Chrominance of color 3 in LUT

8.2.7 OSD1 Control

30h	OSDCONTROL1						R/W
[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
OSD1Blink_en	OsdEn1		Font2Byte1	Vzoom1		Hzoom1	

OSDCONTROL1: Defines the control configurations of OSD1 (On Screen Display 1)

Hzoom1	<1:0>	Select the horizontal zoom factor of OSD 1 (default value is 0)
	00	OSD horizontal pixel size = 1 times of video pixel
	01	OSD horizontal pixel size = 2 times of video pixel
	10	OSD horizontal pixel size = 4 times of video pixel
	11	OSD horizontal pixel size = 8 times of video pixel
Vzoom1	<3:2>	Select the vertical zoom factor of OSD 1 (default value is 0)
	00	OSD vertical pixel size = 2 times of video pixel
	01	OSD vertical pixel size = 4 times of video pixel
	10	OSD vertical pixel size = 8 times of video pixel
	11	OSD vertical pixel size = 16 times of video pixel

Font2Byte1	<4>	Select font character code mode (default value is 0)
	0	One-byte character code mode
	1	Two-byte character code mode
OsdEn1	<6:5>	OSD1 output selection (default value is 0)
	00	Disable OSD1
	01	Enable OSD1 in monitor output
	10	Enable OSD1 in VCR output
	11	Enable OSD1 in both monitor and VCR output
OSD1Blink_en	<7>	Enable OSD1 blink function (default value is 0)
	0	Disable OSD1 blink
	1	Enable OSD1 blink

The blink attribute in the Context RAM will be disabled if the OSD1Blink_en is set to 0.

31h	FONTSTADDR1						R/W
[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
FontStAddr1[7:0]							

FONTSTADDR1: Defines the start address of OSD 1 Font RAM. Default value is 0.

FontStAddr1	<7:0>	OSD1 Font RAM start address (Unit: 8 bytes)

OSD1 Font RAM start address = FontStAddr1 * 8

There is 4K Byte Font RAM built in AL700/701/710.

32h	FONTADDRUNIT1						R/W
[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
PixelDepth1	FontAddrUnit1			OSDBGColor1		OSDFGColor1	

FONTADDRUNIT1: Defines the unit of font address and foreground and background colors of OSD1. OSDFGColor1 and OSDBGColor1 are meaningful only in one-byte character code mode.

OSDFGColor1	<1:0>	Select foreground color of OSD1 (default value is 0)
	00	color 0 in LUT
	01	color 1 in LUT
	10	color 2 in LUT
	11	color 3 in LUT
OSDBGColor1	<3:2>	Select background color of OSD1 (default value is 0)

	00	color 0 in LUT
	01	color 1 in LUT
	10	color 2 in LUT
	11	color 3 in LUT
FontAddrUnit1	<6:4>	Choose the font address unit of OSD1 (default value is 0)
	000	Font address is multiple of 2^3 bytes
	001	Font address is multiple of 2^4 bytes
	010	Font address is multiple of 2^5 bytes
	011	Font address is multiple of 2^6 bytes
	100	Font address is multiple of 2^7 bytes
	101	Font address is multiple of 2^8 bytes
	110	Font address is multiple of 2^9 bytes
	111	Font address is multiple of 2^{10} bytes
	Font address = (Character Code) * (Font Address Unit) + (OSD1 Font RAM Start Address)	
	Character Code is the data retrieved from Context RAM.	
PixelDepth1	<7>	Choose the depth of pixel (default value is 0)
	0	1-bit mode
	1	2-bit mode

33h	FONTLINESIZE1						R/W
[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
Fontlinesize1 [7:0]							

FONTLINESIZE1: Defines the memory size for an OSD1 font line. Default value is 0.

Fontlinesize1	<7:0>	memory size of a font line (unit: 1 byte)

34h	OSDHSTART1						R/W
[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
OsdHStart1 [7:0]							

OSDHSTART1: Defines the horizontal start position of OSD1. Default value is 0.

OsdHStart1	<7:0>	OSD1 horizontal start position (unit: 8 pixels)

35h	OSDVSTART1						R/W
[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
OsdVStart1 [7:0]							

OSDVSTART1: Define the vertical start position of OSD1. Default value is 0.

OsdVStart1 <7:0> OSD1 vertical start position (unit: 4 lines)

36h	CONTEXTSTADDR1						R/W
[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
ContextStAddr1 [7:0]							

CONTEXTSTADDR1: Defines the start address of OSD1 Context RAM. Default value is 0.

ContextStAddr1 <7:0> OSD1 Context RAM start address (Unit: 4 bytes/8 bytes for one-byte/two-byte mode respectively)

One byte mode Start address of OSD1 Context RAM = ContextStAddr1 * 4

Two byte mode Start address of OSD1 Context RAM = ContextStAddr1 * 8

There is 1K Byte Context RAM built in AL700/701/710.

37h	RAMSTRIDE1						R/W
[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
RamStride1 [7:0]							

RAMSTRIDE1: Defines how much Context RAM memory occupied by each OSD1 row text. Default value is 0.

RamStride1 <7:0> Horizontal line stride of OSD1 Context RAM (Unit: 1 byte/2 bytes for one-byte/two-byte mode respectively)

38h	BMAPHSIZE1						R/W
[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
BmapHSize1 [7:0]							

BMAPHSIZE1: Defines the horizontal size of OSD1 bitmap. Default value is 0.

BMAPHSIZE1 = Actual horizontal size of OSD1 bitmap – 1

BmapHSize1 <7:0> OSD1 bitmap horizontal size (Unit: 1 OSD1 pixel)

The difference of BMAPHTOTAL1 and BMAPHSIZE1 defines the extra gap between two adjacent characters shown on OSD1 screen.

39h	BMAPHTOTAL1						R/W
[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
BmapHTotal1 [7:0]							

BMAPHTOTAL1: Defines the total horizontal size of OSD1 bitmap. Default value is 0.

BMAPHTOTAL1 = Actual total horizontal size of OSD1 bitmap – 1

BmapHTotal1 <7:0> OSD1 bitmap total horizontal size (Unit: 1 OSD1 pixel)

3Ah	BMAPVSIZE1						R/W
[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
BmapVSize1 [7:0]							

BMAPVSIZE1: Defines the vertical size of OSD1 bitmap. Default value is 0.

BMAPVSIZE1 = Actual vertical size of OSD1 bitmap – 1

BmapVSize1 <7:0> OSD1 bitmap vertical size (Unit: 1 OSD1 line)

The difference of BMAPVTOTAL1 and BMAPVSIZE1defines the extra gap between two adjacent row texts shown on OSD1 screen.

3Bh	BMAPVTOTAL1						R/W
[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
BmapVTotal1 [7:0]							

BMAPVTOTAL1: Defines the total vertical size of OSD1 bitmap. Default value is 0.

BMAPVTOTAL1 = Actual total vertical size of OSD1 bitmap – 1

BmapVTotal1 <7:0> OSD1 bitmap total vertical size (Unit: 1 OSD1 line)

3Ch	ICONHTOTAL1						R/W
[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
IconHTotal1 [7:0]							

ICONHTOTAL1: Defines the total horizontal number of OSD1 icons. Default value is 0.

ICONHTOTAL1 = Actual total horizontal number of OSD1 icons –1

IconHTotal1 <7:0> Total OSD1 horizontal icons (Unit: 1 icon)

Total horizontal icon number defines how many character codes should be retrieved from internal OSD Context RAM and shown on OSD screen per OSD row text.

3Dh	ICONVTOTAL1						R/W
[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
IconVTotal1 [7:0]							

ICONVTOTAL1: Defines the total vertical number of OSD1 icons. Default value is 0.

ICONVTOTAL1= Actual total vertical number of OSD1 icons –1

IconVTotal1 <7:0> Total OSD1 vertical icons (Unit: 1 icon)

Total vertical icon number defines how many row texts can be shown on OSD screen.

8.2.8 OSD2 Control

40h	OSDCONTROL2						R/W
[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
OSD2Blink_en	OsdEn2		Font2Byte2	Vzoom2		Hzoom2	

OSDCONTROL2: Defines the control configurations of OSD2 (On Screen Display 2)

Hzoom2 <1:0> Select the horizontal zoom factor of OSD 2 (default value is 0)

00 OSD horizontal pixel size = 1 times of video pixel

01 OSD horizontal pixel size = 2 times of video pixel

10 OSD horizontal pixel size = 4 times of video pixel

11 OSD horizontal pixel size = 8 times of video pixel

Vzoom2 <3:2> Select the vertical zoom factor of OSD 2 (default value is 0)

00 OSD vertical pixel size = 2 times of video pixel

01 OSD vertical pixel size = 4 times of video pixel

10 OSD vertical pixel size = 8 times of video pixel

11 OSD vertical pixel size = 16 times of video pixel

Font2Byte2 <4> Select font character code mode (default value is 0)

0 One-byte character code mode

1 Two-byte character code mode

OsdEn2 <6:5> OSD2 output selection (default value is 0)

00 Disable OSD2

01 Enable OSD2 in monitor output

10 Enable OSD2 in VCR output

	11	Enable OSD2 in both monitor and VCR output
OSD2Blink_en	<7>	Enable OSD2 blink function (default value is 0)
	0	Disable OSD2 blink
	1	Enable OSD2 blink

The blink attribute in the Context RAM will be disabled if the OSD2Blink_en is set to 0.

41h	FONTSTADDR2						R/W
[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
FontStAddr2[7:0]							

FONTSTADDR2: Defines the start address of OSD2 Font RAM. Default value is 0.

FontStAddr2	<7:0>	OSD2 Font RAM start address (Unit: 8 bytes)
		OSD2 Font RAM start address = FontStAddr2 * 8
		There is 4K Byte Font RAM built in AL700/701/710.

42h	FONTADDRUNIT2						R/W
[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
PixelDepth2	FontAddrUnit2			OSDBGColor2		OSDFGColor2	

FONTADDRUNIT2: Defines the unit of font address and foreground and background colors of OSD2. OSDFGColor2 and OSDBGColor2 are meaningful only in one-byte character code mode.

OSDFGColor2	<1:0>	Select foreground color of OSD2 (default value is 0)
	00	color 0 in LUT
	01	color 1 in LUT
	10	color 2 in LUT
	11	color 3 in LUT
OSDBGColor2	<3:2>	Select background color of OSD2 (default value is 0)
	00	color 0 in LUT
	01	color 1 in LUT
	10	color 2 in LUT
	11	color 3 in LUT
FontAddrUnit2	<6:4>	Choose the font address unit of OSD2 (default value is 0)
	000	Font address is multiple of 2^3 bytes

001 Font address is multiple of 2^4 bytes

010 Font address is multiple of 2^5 bytes

011 Font address is multiple of 2^6 bytes

100 Font address is multiple of 2^7 bytes

101 Font address is multiple of 2^8 bytes

110 Font address is multiple of 2^9 bytes

111 Font address is multiple of 2^{10} bytes

Font address = (Character Code) * (Font Address Unit)
+ (OSD2 Font RAM Start Address)

Character Code is the data retrieved from Context RAM.

PixelDepth2 <7> Choose the depth of pixel (default value is 0)

0 1-bit mode

1 2-bit mode

43h	FONTLINESIZE2						R/W
[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
Fontlinesize2 [7:0]							

FONTLINESIZE2: Defines the memory size for an OSD2 font line. Default value is 0.

Fontlinesize2 <7:0> memory size of a font line (unit: 1 byte)

44h	OSDHSTART2						R/W
[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
OsdHStart2 [7:0]							

OSDHSTART2: Defines the horizontal start position of OSD2. Default value is 0.

OsdHStart2 <7:0> OSD2 horizontal start position (unit: 8 pixels)

45h	OSDVSTART2						R/W
[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
OsdVStart2 [7:0]							

OSDVSTART2: Define the vertical start position of OSD2. Default value is 0.

OsdVStart2 <7:0> OSD2 vertical start position (unit: 4 lines)

46h	CONTEXTSTADDR2						R/W
[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
ContextStAddr2 [7:0]							

CONTEXTSTADDR2: Defines the start address of OSD2 Context RAM. Default value is 0.

ContextStAddr2 <7:0> OSD2 Context RAM start address (Unit: 4 bytes/8 bytes for one-byte/two-byte mode respectively)

One byte mode Start address of OSD2 Context RAM = ContextStAddr1 * 4

Two byte mode Start address of OSD2 Context RAM = ContextStAddr1 * 8

There is 1K Byte Context RAM built in AL700/701/710.

47h	RAMSTRIDE2						R/W
[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
RamStride2 [7:0]							

RAMSTRIDE2: Defines how much Context RAM memory occupied by each OSD2 row text. Default value is 0.

RamStride2 <7:0> Horizontal line stride of OSD2 Context RAM (Unit: 1 byte/2 bytes for one-byte/two-byte mode respectively)

48h	BMAPHSIZE2						R/W
[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
BmapHSize4 [7:0]							

BMAPHSIZE2: Defines the horizontal size of OSD2 bitmap. Default value is 0.

BMAPHSIZE2 = Actual horizontal size of OSD2 bitmap – 1

BmapHSize2 <7:0> OSD2 bitmap horizontal size (Unit: 1 OSD2 pixel)

The difference of BMAPHTOTAL2 and BMAPHSIZE2 defines the extra gap between two adjacent characters shown on OSD1 screen.

49h	BMAPHTOTAL2						R/W
[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
BmapHTotal2 [7:0]							

BMAPHTOTAL2: Defines the total horizontal size of OSD2 bitmap. Default value is 0.

BMAPHTOTAL2 = Actual total horizontal size of OSD2 bitmap – 1

BmapHTotal2 <7:0> OSD2 bitmap total horizontal size (Unit: 1 OSD2 pixel)

4Ah	BMAPVSIZE2						R/W
[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
BmapVSize2 [7:0]							

BMAPVSIZE2: Defines the vertical size of OSD2 bitmap. Default value is 0.

BMAPVSIZE2 = Actual vertical size of OSD2 bitmap – 1

BmapVSize2 <7:0> OSD2 bitmap vertical size (Unit: 1 OSD2 line)

The difference of BMAPVTOTAL2 and BMAPVSIZE2defines the extra gap between two adjacent row texts shown on OSD2 screen.

4Bh	BMAPVTOTAL2						R/W
[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
BmapVTotal2 [7:0]							

BMAPVTOTAL2: Defines the total vertical size of OSD2 bitmap. Default value is 0.

BMAPVTOTAL2 = Actual total vertical size of OSD2 bitmap – 1

BmapVTotal2 <7:0> OSD2 bitmap total vertical size (Unit: 1 OSD2 line)

4Ch	ICONHTOTAL2						R/W
[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
IconHTotal2 [7:0]							

ICONHTOTAL2: Defines the total horizontal number of OSD2 icons. Default value is 0.

ICONHTOTAL2 = Actual total horizontal number of OSD2 icons –1

IconHTotal2 <7:0> Total OSD2 horizontal icons (Unit: 1 icon)

Total horizontal icon number defines how many character codes should be retrieved from internal OSD Context RAM and shown on OSD screen per OSD row text.

4Dh	ICONVTOTAL2						R/W
[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
IconVTotal2 [7:0]							

ICONVTOTAL2: Defines the total vertical number of OSD2 icons. Default value is 0.

ICONVTOTAL2 = Actual total vertical number of OSD2 icons –1

IconVTotal2 <7:0> Total OSD2 vertical icons (Unit: 1 icon)

Total vertical icon number defines how many row texts can be shown on OSD screen.

8.2.9 RAM Access

50h	ADDRL						W
[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
Addr [7:0]							
51h	ADDRM						W
[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
Addr [15:8]							
52h	ADDRH						W
[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
OSDAdrst	Reserved		Target	Reserved		Addr [17:16]	

ADDRL, ADDRM, ADDRH: Defines the address of internal OSD Context RAM and Font RAM. Default address value is 0.

Addr [7:0]	<7:0>	Address [7:0]
Addr [15:8]	<7:0>	Address [15:8]
Addr [17:16]	<1:0>	Address [17:16]
Target	<4>	Select the Context RAM or Font RAM (default value is 0)
	0	OSD Context RAM
	1	Font RAM
OSDAdrst	<7>	Reset RAM address counter (default value is 0)
	0	Normal operation
	1	Reset RAM address counter to the initial value

53h	DATAPORT						W
[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
DATAPORT [7:0]							

DATAPORT: Defines the data port of internal OSD Context RAM and Font RAM. The data is written into the selected target RAM through this port. Default value is 0.

DATAPORT	<7:0>	Written data of internal OSD Context RAM or Font RAM

Writing data to register #53h will automatically increase the RAM address defined in registers #50h, #51h, and #52h.

OSD Context RAM (write only): There is 1K-byte OSD Context RAM built in AL700/701/710. Therefore, there only need 10 bits to address the OSD Context RAM.

ADDRH (#52h)								ADDRM (#51h)								ADDRL (#50h)							
7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0
0			0			Don't care								OsdRamAddr [9:0]									

For one byte data mode:

DATAPORT (#53h)							
7	6	5	4	3	2	1	0
Reserved	Character Code [6:0]						

For two byte data mode:

DATAPORT (#53h)								
7	6	5	4	3	2	1	0	
Character Code [7:0]								(For byte 1)
FG Color		BG Color		Blink	Character Code [10:8]			(For byte 2)

Character Code		Map to the font table to get the corresponding bit-map data
Blink	<3>	Enable blinking function (default value is 0)
	0	Normal
	1	Enable
BG Color	<5:4>	Select background color from LUT (default value is 0)
	00	Select Color 0 in LUT
	01	Select Color 1 in LUT
	10	Select Color 2 in LUT
	11	Select Color 3 in LUT
FG Color	<7:6>	Select foreground color from LUT
	00	Select Color 0 in LUT
	01	Select Color 1 in LUT
	10	Select Color 2 in LUT
	11	Select Color 3 in LUT

Font RAM (write only): There is 4K-byte Font RAM built in AL700/701/710. Therefore, there only need 12 bits to address the Font RAM.

ADDRH (#52h)								ADDRM (#51h)								ADDRL (#50h)							
7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0
0			1			Don't care		FontAddr [11:0]															

DATAPORT (#53h)							
7	6	5	4	3	2	1	0
FontBMP							

FontAddr = Character Code * FontAddrUnit + Font Line * Fontlinesize

More detailed information please refers to the OSD function description paragraph.

8.2.10 Image Upload Setting

58h	UPIMGCTR						R/W
[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
Reserved		Burst_en	UpImgRese	Reserved	Enable_UPI	Read_Sel	UpImgField

UPIMGCTR: Defines the control configurations of image upload

UpImgField	<0>	Choose what field to be uploaded (default value is 0)
	0	Upload ODD field
	1	Upload Even field
Read_Sel	<1>	Choose the mode of image upload (default value is 0)
	0	Upload color image
	1	Upload luminance color only
Enable_UPI	<2>	Enable image upload (default value is 0)
	0	Disable
	1	Enable
UpImgReset	<4>	Reset internal image read counter (default value is 0)
	0	Normal operation
	1	Reset internal read counter for image uploading
Burst_en	<5>	Select image read mode (default value is 0)
	0	Normal mode
	1	Burst mode

Internal image read counter will automatically increase when read UpImgYDP or UPImagCDP. To ensure image uploading correctly, the monitor output must be set to freeze mode and the internal image read counter must be reset before uploading an image.

59h	UPIMGYDP						R
[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
UpImgYDP [7:0]							

UPIMGYDP: Defines the data reading port for image Y luminance. Default value is 0.

UpImgYDP <7:0> Y luminance data of image

5Ah	UPIMGCDP						R
[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
UpImgCDP [7:0]							

UPIMGCDP: Defines the data reading port for image C chrominance. Default value is 0.

UpImgCDP <7:0> C chrominance data of image

8.2.11 External Encoder Interface Setting

60h	HSYNCWIDTH						R/W
[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
HsyncWidth[7:0]							
61h	HSYNCWIDTH						R/W
[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
Reserved						HsyncWidth[9:8]	

HSYNCWIDTH: Defines the HSYNC signal width. Default value is 0.

HsyncWidth [7:0] <7:0> Bits<7:0> of output HSYNC signal width (unit: pixel)

HsyncWidth [9:8] <1:0> Bits<9:8> of output HSYNC signal width (unit: pixel)

62h	VSYNCWIDTH						R/W
[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
VsyncWidth[7:0]							

VSYNCWIDTH: Defines the VSYNC signal width. Default value is 0.

VsyncWidth <7:0> Output VSYNC signal width (unit: line)

8.2.12 Motion Detection

6Bh	MOTIONADDR						W
[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
addr_var				addr_mean			

MOTIONADDR: Defines the address of Mean and Variance.

addr_mean	<3:0>	Choose mean address (default value is 0)
	0000	window [0]
	0001	window [1]
	0010	window [2]
	0011	window [3]
	0100	window [4]
	0101	window [5]
	0110	window [6]
	0111	window [7]
	1000	window [8]
	1001	window [9]
	1010	window [10]
	1011	window [11]
	1100	window [12]
	1101	window [13]
	1110	window [14]
	1111	window [15]
addr_var	<7:4>	Choose variance address (default value is 0)
	0000	window [0]
	0001	window [1]
	0010	window [2]
	0011	window [3]
	0100	window [4]
	0101	window [5]
	0110	window [6]
	0111	window [7]

1000 window [8]
1001 window [9]
1010 window [10]
1011 window [11]
1100 window [12]
1101 window [13]
1110 window [14]
1111 window [15]

6Ch	MEANDATA						R
[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
data_mean [7:0]							
6Dh	MEANDATA						R
[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
data_mean [15:8]							

MEANDATA: Defines the mean data of selected mean address. Default value is 0.

data_mean [7:0] <7:0> Low byte of mean data
data_mean [15:8] <7:0> High byte of mean data

6Eh	VARIANCEDATA						R
[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
data_var [7:0]							
6Fh	VARIANCEDATA						R
[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
data_var [15:8]							

VARIANCEDATA: Defines the variance data of selected variance address. Default value is 0.

data_ var [7:0] <7:0> Low byte of variance data
data_ var [15:8] <7:0> High byte of variance data

70h	MEANTH0						W
[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
th_mean0 [7:0]							
71h	MEANTH0						W
[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
th_mean0 [15:8]							

MEANTH0: Defines the threshold of mean data for window [3:0]. Default value is 0.

th_mean0 [7:0] <7:0> Low byte of threshold of mean data for window [3:0]

th_mean0 [15:8] <7:0> High byte of threshold of mean data for window [3:0]

72h	MEANTH1						W
[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
th_mean1 [7:0]							
73h	MEANTH1						W
[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
th_mean1 [15:8]							

MEANTH1: Defines the threshold of mean data for window [7:4]. Default value is 0.

th_mean1 [7:0] <7:0> Low byte of threshold of mean data for window [7:4]

th_mean1 [15:8] <7:0> High byte of threshold of mean data for window [7:4]

74h	MEANTH2						W
[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
th_mean2 [7:0]							
75h	MEANTH2						W
[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
th_mean2 [15:8]							

MEANTH2: Defines the threshold of mean data for window [11:8]. Default value is 0.

th_mean2 [7:0] <7:0> Low byte of threshold of mean data for window [11:8]

th_mean2 [15:8] <7:0> High byte of threshold of mean data for window [11:8]

76h	MEANTH3						W
[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
th_mean3 [7:0]							
77h	MEANTH3						W
[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
th_mean3 [15:8]							

MEANTH3: Defines the threshold of mean data for window [15:12]. Default value is 0.

th_mean3 [7:0]	<7:0>	Low byte of threshold of mean data for window [15:12]
th_mean3 [15:8]	<7:0>	High byte of threshold of mean data for window [15:12]

78h	VARIANCETH0						W
[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
th_var0 [7:0]							
79h	VARIANCETH0						W
[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
th_var0 [15:8]							

VARIANCETH0: Defines the threshold of variance data for window [3:0]. Default value is 0.

th_var0 [7:0]	<7:0>	Low byte of threshold of variance data for window [3:0]
th_var0 [15:8]	<7:0>	High byte of threshold of variance data for window [3:0]

7Ah	VARIANCETH1						W
[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
th_var1 [7:0]							
7Bh	VARIANCETH1						W
[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
th_var1 [15:8]							

VARIANCETH1: Defines the threshold of variance data for window [7:4]. Default value is 0.

th_var1 [7:0]	<7:0>	Low byte of threshold of variance data for window [7:4]

th_var1 [15:8] <7:0> High byte of threshold of variance data for window [7:4]

7Ch	VARIANCETH2						W
[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
th_var2 [7:0]							
7Dh	VARIANCETH2						W
[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
th_var2 [15:8]							

VARIANCETH2: Defines the threshold of variance data for window [11:8]. Default value is 0.

th_var2 [7:0] <7:0> Low byte of threshold of variance data for window [11:8]

th_var2 [15:8] <7:0> High byte of threshold of variance data for window [11:8]

7Eh	VARIANCETH3						W
[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
th_var3 [7:0]							
7Fh	VARIANCETH3						W
[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
th_var3 [15:8]							

VARIANCETH3: Defines the threshold of variance data for window [15:12]. Default value is 0.

th_var3 [7:0] <7:0> Low byte of threshold of variance data for window [15:12]

th_var3 [15:8] <7:0> High byte of threshold of variance data for window [15:12]

8.2.13 SDRAM Interface

80h	DRAMCTL0						R/W
[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
TRRD	TRP	TRCD	TRC			TRAS	

DRAMCTL0: Defines the control parameters of SDRAM.

TRAS <1:0> Choose the latency of RAS (default value is 00)

	00	5 SDRAM input clocks
	01	6 SDRAM input clocks
	10	7 SDRAM input clocks
	11	8 SDRAM input clocks
TRC	<4:2>	Choose the latency of RC (default value is 000)
	000	7 SDRAM input clocks
	001	8 SDRAM input clocks
	010	9 SDRAM input clocks
	011	10 SDRAM input clocks
	100	11 SDRAM input clocks
	101	12 SDRAM input clocks
	110	13 SDRAM input clocks
	111	14 SDRAM input clocks
TRCD	<5>	Choose the latency of RCD (default value is 0)
	0	2 SDRAM input clocks
	1	3 SDRAM input clocks
TRP	<6>	Choose the latency of RP (default value is 0)
	0	2 SDRAM input clocks
	1	3 SDRAM input clocks
TRRD	<7>	Choose the latency of RRD (default value is 0)
	0	2 SDRAM input clocks
	1	3 SDRAM input clocks

81h	DRAMCTL1						R/W
[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
Reserved	APON	Reserved	MEMCFG		TRW	TCL	TWR

DRAMCTL1: Defines the control parameters of SDRAM.

TWR	<0>	Choose the latency of WR (default value is 0)
	0	No latency
	1	1 SDRAM input clock
TCL	<1>	Choose the latency of CL (default value is 0)
	0	2 SDRAM input clocks

	1	3 SDRAM input clocks
TRW	<2>	Choose the latency of RW (default value is 0)
	0	No latency
	1	1 SDRAM input clock
MEMCFG	<4:3>	Select SDRAM type (default value is 0)
	00	1M x 16-bit
	01	4M x 16-bit
	10	Reserved
	11	Reserved
APON	<6>	Enable auto pre-charge (default value is 0)
	0	Disable
	1	Enable

82h	ENABLE_CTRL						R/W
[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
enable_rfsh	**enable_fdr**	**enable_qdr**	**enable_cfw**	**enable_cdw**	**enable_ccw**	**enable_cbw**	**enable_caw**

ENABLE_CTRL: Defines the control configurations of enable.

enable_caw	<0>	Enable FIFO write request of channel A in QUAD mode (default value is 0)
	0	Disable
	1	Enable
enable_cbw	<1>	Enable FIFO write request of channel B in QUAD mode (default value is 0)
	0	Disable
	1	Enable
enable_ccw	<2>	Enable FIFO write request of channel C in QUAD mode (default value is 0)
	0	Disable
	1	Enable
enable_cdw	<3>	Enable FIFO write request of channel D in QUAD mode (default value is 0)
	0	Disable
	1	Enable

enable_cfw	<4>	Enable FIFO write request of full channel in FULL mode (default value is 0)
	0	Disable
	1	Enable
enable_qdr	<5>	Enable FIFO read request of VCR output (default value is 0)
	0	Disable
	1	Enable
enable_fdr	<6>	Enable FIFO read request of monitor output (default value is 0)
	0	Disable
	1	Enable
enable_rfsh	<7>	Enable SDRAM refresh (default value is 0)
	0	Disable
	1	Enable

83h	MIN_REFRESH						R/W
[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
min_refresh [7:0]							

MIN_REFRESH: Defines minimum refresh times in one field period. Default value is 0.

min_refresh	<7:0>	Minimum refresh times (Unit: 32) Only available while enable_rfsh is enabled

84h	CAW_LEVEL						R/W
[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
Reserved		caw_level [5:0]					

CAW_LEVEL: Defines the full level of FIFO of channel A in QUAD capture mode. Default value is 8.

caw_level	<5:0>	Full level of FIFO of Channel A

85h	CBW_LEVEL						R/W
[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
Reserved		cbw_level [5:0]					

CBW_LEVEL: Defines the full level of FIFO of channel B in QUAD capture mode. Default value is 8.

cbw_level <5:0> Full level of FIFO of Channel B

86h	CCW_LEVEL						R/W
[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
Reserved	ccw_level [5:0]						

CCW_LEVEL: Defines the full level of FIFO of channel C in QUAD capture mode. Default value is 8.

ccw_level <5:0> Full level of FIFO of Channel C

87h	CDW_LEVEL						R/W
[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
Reserved	cdw_level [5:0]						

CDW_LEVEL: Defines the full level of FIFO of channel D in QUAD capture mode. Default value is 8.

cdw_level <5:0> Full level of FIFO of Channel D

88h	CFW_LEVEL						R/W
[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
Reserved	cfw_level [5:0]						

CFW_LEVEL: Defines the full level of FIFO in FULL video capture mode. Default value is 10h.

cfw_level <5:0> Full level of FIFO

89h	QDR_LEVEL						R/W
[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
Reserved	qdr_level [5:0]						

QDR_LEVEL: Defines the empty level of FIFO of VCR output. Default value is 10h.

qdr_level <5:0> Empty level of FIFO

8Ah	FDR_LEVEL						R/W
[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
Reserved	fdr_level [5:0]						

FDR_LEVEL: Defines the empty level of FIFO of monitor output. Default value is 10h.

fdr_level <5:0> Empty level of FIFO

9 Electrical Characteristics

9.1 Absolute Maximum Ratings

(Excessive ratings are harmful to the lifetime. Only for user guidelines, not tested.)

Parameter		3.3V Rating	Unit
V_{DD}	Supply Voltage	-0.3 ~ +3.8	V
V_P	Input Pin Voltage	-0.3 ~ +(V_{DD}+0.3)	V
I_O	Output Current	-20 ~ +20	mA
T_{AMB}	Ambient Op. Temperature	0 ~ +85	°C
T_{stg}	Storage Temperature	-40 ~ +125	°C
T_{VSOL}	Vapor Phase Soldering Temperature (15 Sec.)	220	°C

9.2 Recommended Operating Conditions

Parameter		3.3V Rating			Unit
		Min.	Typical	Max.	
V_{DD}	Supply Voltage	+3.0	+3.3	+3.6	V
V_{IH}	High Level Input Voltage	0.7 V_{DD}		V_{DD}	V
V_{IL}	Low Level Input Voltage	0		0.3 V_{DD}	V
T_{AMB}	Ambient Op. Temperature	0		+70	°C

9.3 DC Characteristics

(V_{DD} = 3.3V, Vss=0V. T_{AMB} = 0 to 70°C; Some parameters are guaranteed by design only, not production tested)

Parameter		3.3V Rating			Unit
		Min.	Typical	Max.	
V_{IH}	Hi-level Input Voltage	0.7 V_{DD}	-	V_{DD}	V
V_{IL}	Lo-level Input Voltage	0		0.3 V_{DD}	V
V_{OH}	Hi-level Output Voltage	2.4	-	V_{DD}	V
V_{OL}	Lo-level Output Voltage	-	-	+0.4	V
I_{LI}	Input Leakage Current	-5	-	+5	µA
I_{LO}	Output Leakage Current	-5	-	+5	µA

9.4 AC Characteristics

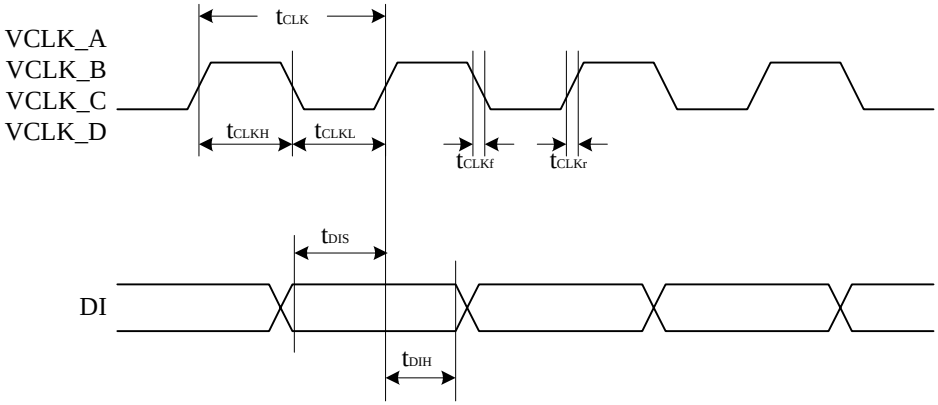
(V_{DD} = 3.3V, Vss=0V, T_{AMB} = 0 to 70°C; Some parameters are guaranteed by design only, not production tested)

Parameter		3.3V Rating			Unit
		Min.	Typical	Max.	
Power Supply Current					
I_{DD}	Operating Current @27MHz	-	220	-	mA
Decoder Interface					
t_{CLK}	Cycle time for VCLK_A, B, C, and D		27		MHz
δ_{CLK}	Duty Factor for CLK_A, B, C, and D (t_{CLKH} / f_{CLK})	40	50	60	%
t_{CLKr}	Rising time for VCLK_A, B, C, and D			3	ns
t_{CLKf}	Falling time for VCLK_A, B, C, and D			3	ns
t_{DIS}	Setup time for DI	5			ns
t_{DIH}	Hold time for DI	3			ns
Encoder Interface (Output loading C_L=15pF)					
t_{CK2}	2 times of cycle time for video output (VCLKX2)		18		ns
δ_{CK2}	Duty Factor for VCLKX2 (t_{CK2H} / t_{CK2})	40	50	60	%
t_{r2}	Rising time for VCLKX2			1.5	ns
t_{f2}	Falling time for VCLKX2			1.5	ns
t_{PD2}	Propagation delay for DO in 8-bit output mode	3			ns
t_{OH2}	Hold time for DO in 8-bit output mode	2			ns
t_{CK}	Cycle time for video output (VCLK)		36		ns
t_{dCK}	Clock delay for VCLK			5	ns
t_{r2}	Rising time for VCLK			3	ns
t_{f2}	Falling time for VCLK			3	ns
t_{PD}	Propagation delay for DO in 16-bit output mode	3			ns

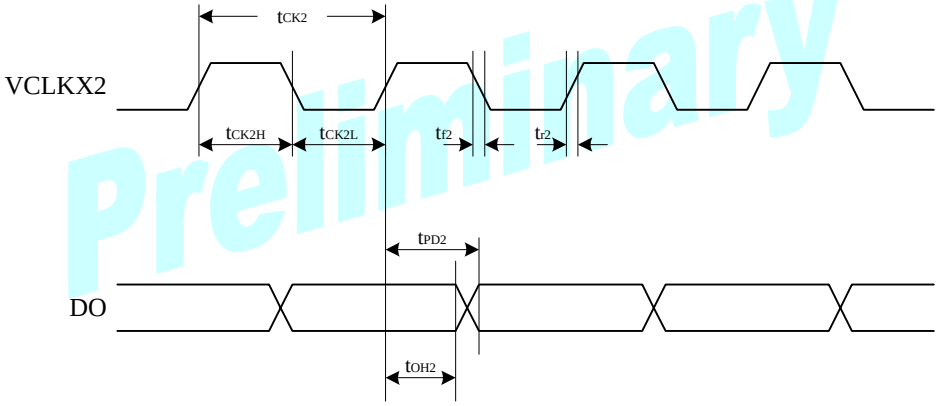
Parameter		3.3V Rating			Unit
		Min.	Typical	Max.	
t_{OH}	Hold time for DO in 16-bit output mode	2			ns
OSD Interface					
f_{CKOSD}	Frequency for external OSD		6.75		MHz
t_{CKOSD}	Cycle time for external OSD		1/ f_{CKOSD}		ns
δ_{CKOSD}	Duty Factor for OSD_CLK (t_{CKOSDH} / t_{CKOSD})	40	50	60	%
t_{CKOSDr}	Rising time for OSD_CLK			3	ns
t_{CKOSDf}	Falling time for OSD_CLK			3	ns
t_{CKVBH}	Pulse width high for OSD_VBLK	1/ f_{CKOSD}			ns
t_{CKVBr}	Rising time for OSD_VBLK	4		25	ns
t_{CKVBf}	Falling time for OSD_VBLK	4		25	ns
Serial Host Interface					
f_{SCL}	SCL (H_WRB) frequency			1	MHz
t_{SCLH}	Pulse width high for SCL	200			ns
t_{SCLL}	Pulse width low for SCL	200			ns
t_{SDAS}	Setup time for SDA (H_BUS7)	10			ns
t_{SDAH}	Hold time for SDA	3			ns
t_{SCLr}	Rising time for SCL and SDA			300	ns
t_{SCLf}	Falling time for SCL and SDA			300	ns
t_{STARTH}	Hold time for START condition	80			ns
t_{STOPS}	Setup time for STOP condition	80			ns
Parallel Host Interface					
f_{WRB}	H_WRB frequency			5	MHz
t_{WRBH}	Pulse width high for H_WRB	100			ns
t_{WRBL}	Pulse width low for H_WRB	100			ns
t_{BUSIS}	Input setup time for H_BUS	10			ns
t_{BUSIH}	Input hold time for H_BUS	3			ns
t_{WRBr}	Rising time for all signals			60	ns
t_{WRBf}	Falling time for all signals			60	ns
t_{HDRS}	Setup time for H_DENB, H_RDB	10			ns

Parameter		3.3V Rating			Unit
		Min.	Typical	Max.	
t_{HDRH}	Hold time for H_DENB, H_RDB	3			ns
t_{BUSPD}	Output delay time for H_BUS			40	ns
t_{BUSOH}	Output hold time for H_BUS	5			ns
Clock and Reset					
f_{XTI}	XTI		27		MHz
δ_{XTI}	Duty Factor for XTI (t_{XTIH} * f_{XTI})	40	50	60	%
f_{XTO}	XTO		f_{XTI}		MHz
f_{XTI_NTSC}	XTI_NTSC		28.6364		MHz
δ_{XTI_N}	Duty Factor for XTI_NTSC (t_{XTINH} * f_{XTI_NTSC})	40	50	60	%
f_{XTO_NTSC}	XTO_NTSC		f_{XTI_NTSC}		MHz
f_{XTI_PAL}	XTI_PAL		35.4690		MHz
δ_{XTI_P}	Duty Factor for XTI_PAL (t_{XTIPH}* f_{XTI_PAL})	40	50	60	%
f_{XTO_PAL}	XTO_PAL		f_{XTI_PAL}		MHz
f_{DMCLKI}	DMCLK_I	108			MHz
δ_{DMCLK}	Duty Factor for DMCLK_I (t_{DMCLKH}* f_{DMCLKI})	40	50	60	%
f_{DMCLKO}	DMCLK_O		f_{DMCLKI}		MHz
t_{RSTB}	Pulse width low for RSTB		1.32		ms

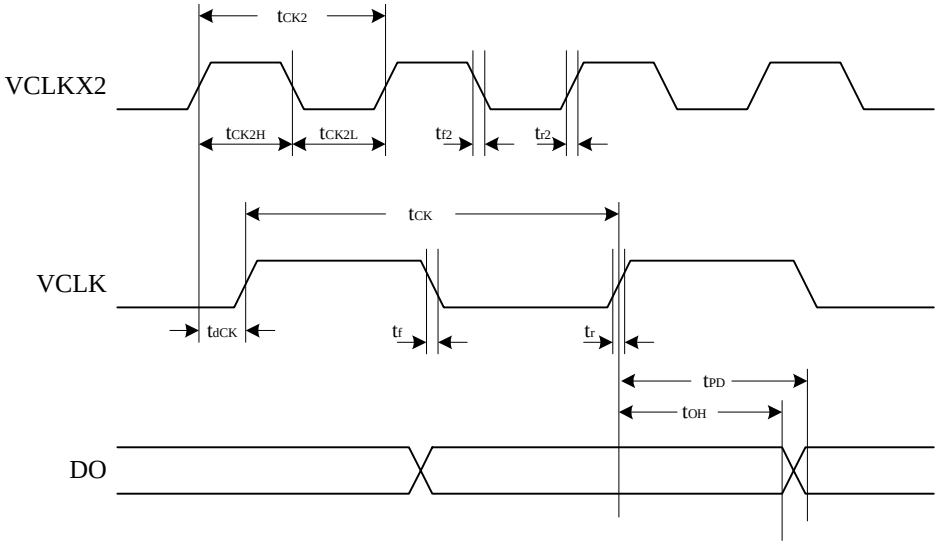
10 Timing Diagrams



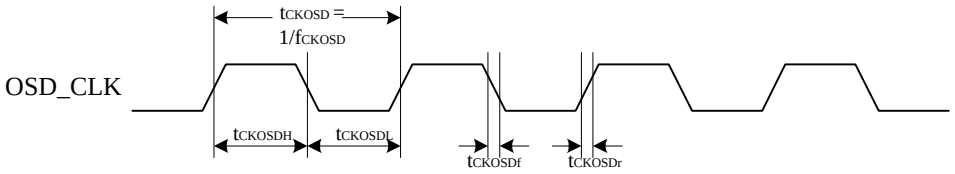
AL700/701/710 656 or 601 8-bit Input Timing



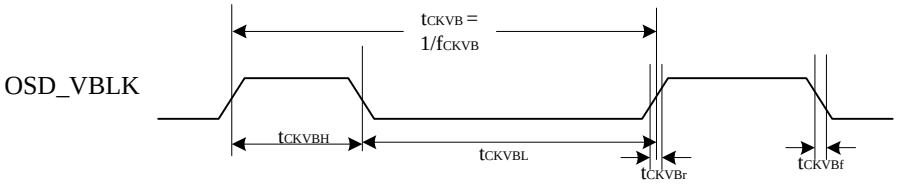
AL700/701/710 656 or 601 8-bit Output Timing



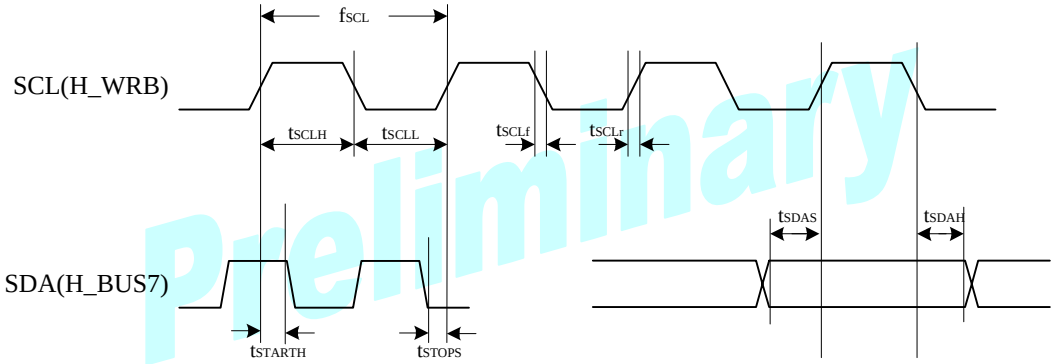
AL700/701/710 601 16-bit Output Timing



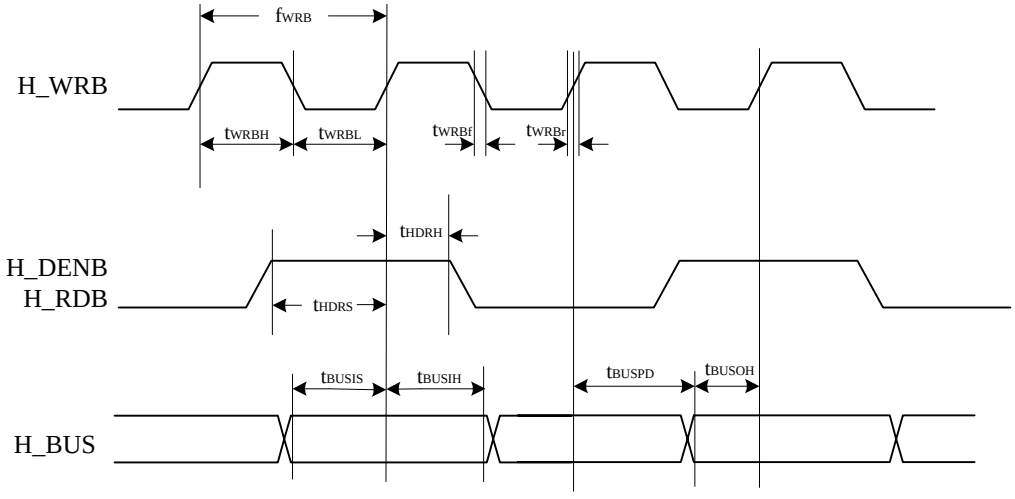
OSD Clock Output Timing



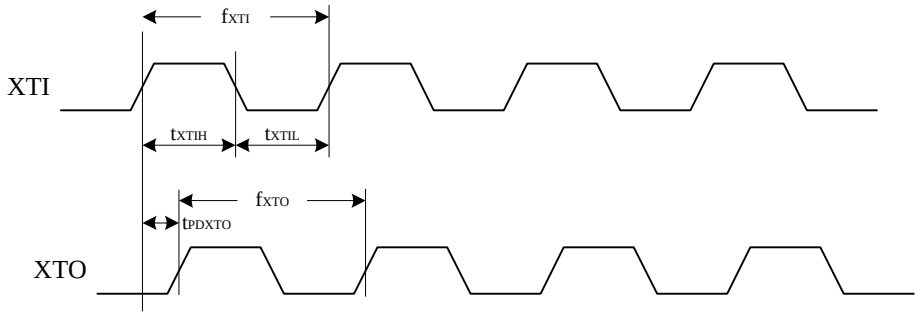
OSD Video Blank Control Timing



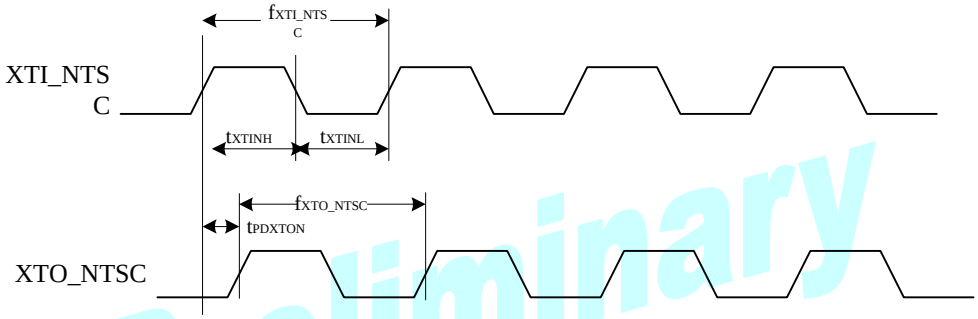
Serial Host Interface Timing



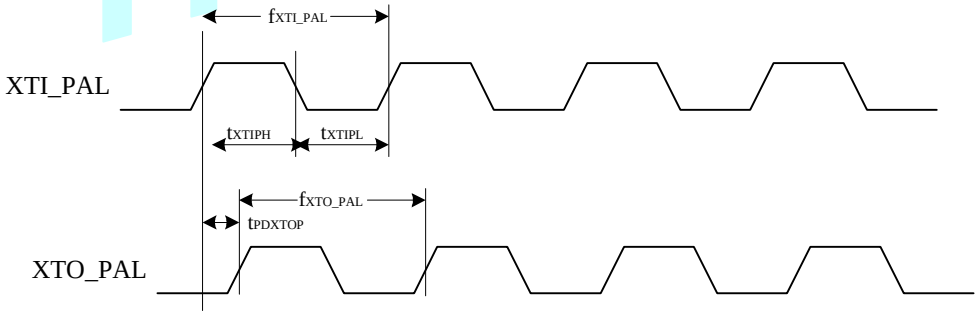
Parallel Host Interface Timing



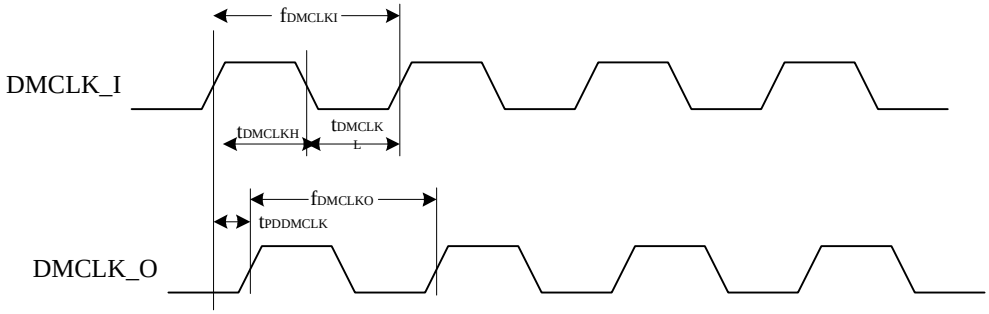
XTI/XTO Clock Timing



XTI_NTSC/XTO_NTSC Clock Timing

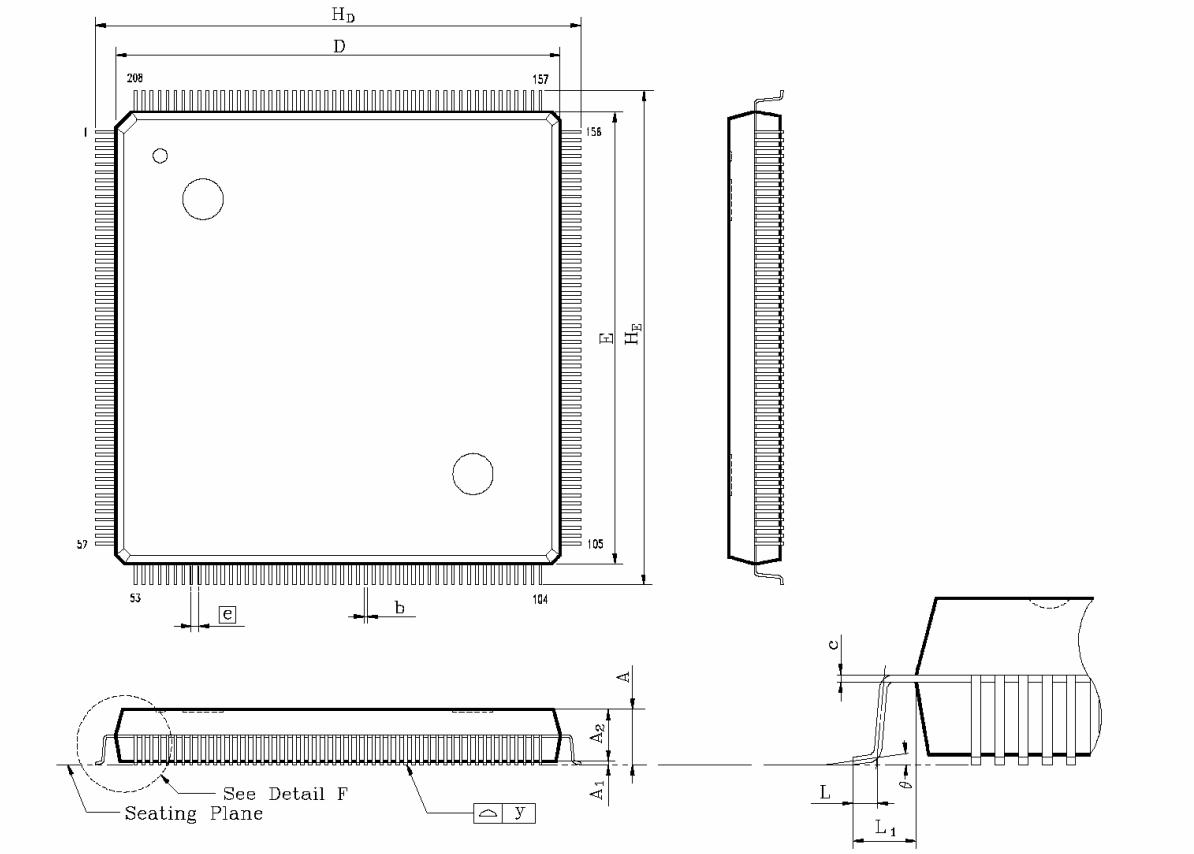


XTI_PAL/XTO_PAL Clock Timing



DMCLK_I/DMCLK_O Clock Timing

11 Mechanical Drawing-208 PIN PLASTICS PQFP



Symbol	Dimension in inch			Dimension in mm		
	Min	Typ	Max	Min	Typ	Max
A	0.136	0.144	0.152	3.45	**3.65**	3.85
A_1	0.004	0.010	0.036	0.10	**0.25**	0.91
A_2	0.119	0.128	0.136	3.02	**3.24**	3.46
b	0.004	0.008	0.012	0.10	**0.20**	0.30
c	0.002	0.006	0.010	0.04	**0.15**	0.26
D	1.093	1.102	1.112	27.75	**28.00**	28.25
E	1.093	1.102	1.112	27.75	**28.00**	28.25
e	0.012	0.020	0.031	0.30	**0.50**	0.80
H_D	1.169	1.205	1.240	29.70	**30.60**	31.50
H_E	1.169	1.205	1.240	29.70	**30.60**	31.50
L	0.010	0.020	0.030	0.25	**0.50**	0.75
L_1	0.041	0.051	0.061	1.05	**1.30**	1.55
y	-	-	0.004	-	-	0.10
θ	0°	-	12°	0°	-	12°

Note:

1. Dimension D & E do not include interlead flash.
2. Dimension b does not include dambar protrusion/intrusion.
3. Controlling dimension: Millimeter
4. General appearance spec. should be based on final visual inspection spec.

TITLE : 208L QFP (28x28 mm**2) FOOTPRINT 2.6mm PACKAGE OUTLINE DRAWING			
LEADFRAME MATERIAL:			
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CONTACT INFORMATION

Averlogic Technologies Corp.
4F, No. 514, Sec. 2, Cheng Kung Rd., Nei-Hu Dist., Taipei, Taiwan
Tel: +886 2-27915050
Fax: +886 2-27912132
E-mail: sales@averlogic.com.tw
URL: http://www.averlogic.com.tw

Averlogic Technologies, Inc.
90 Great Oaks Blvd. #204, San Jose, CA 95119, U.S.A.
Tel: 1 408 361-0400
Fax: 1 408 361-0404
E-mail: sales@averlogic.com
URL: http://www.averlogic.com