ZERO VOLTAGE SWITCH

Triac Control for Industrial Purpose in Static Switch, Burst Firing, Proportional Driver, Power Timer etc.

T-65-09

Technology: Bipolar

Features:

- Supply voltage monitoring
- Few external components
- Full wave drive – no d.c. current component in the load circuit
- Negative output current pulse up to 250 mA – short circuit protected
- Free available operational amplifier
- Ramp generator
- High resistant input sensor control
- Control terminal for continuous pulse circuit
- Reference voltage
- Logic output
- Pulse blocking

Case: DIP 16

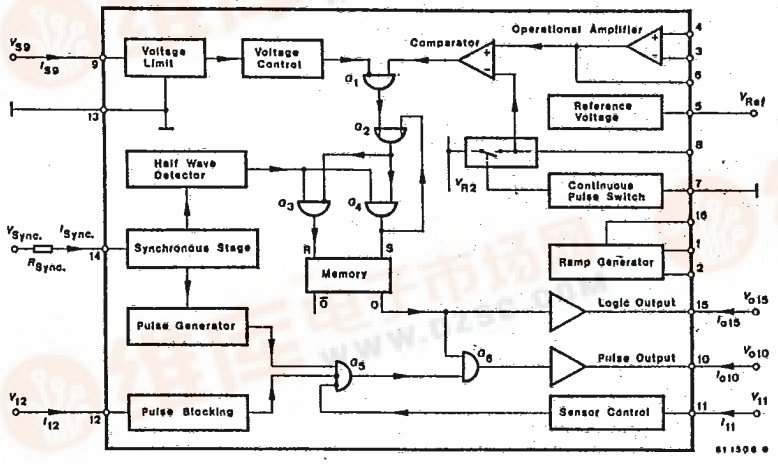


Fig. 1 Block diagram and pin connections

General description

Monolithic integrated triac control circuit, the U 106 BS, incorporates several additional circuits which allow the range of applications to be considerably extended without the need for additional active components. The operation of the circuit is best explained with reference to the block diagram shown in Fig. 1.

Supply voltage

The IC can be operated either from an AC supply (e.g. directly from the AC line through a series resistor) or from a DC supply, $-V_S = 7.3 \ldots 8.6$ V.
An internal supply monitor circuit ensures that the full-wave control circuit is activated only when the supply voltage exceeds the minimum voltage required by all logic circuits.

Pulse formation

Gate G_5 in the output logic produces a pulse of variable width every time the alternating voltage applied to Pin 14 via a synchronizing resistor goes through zero.
The full-wave control unit, comprising gates G_1 to G_4, a half-wave detector and RS-Flipflop, processes the output information derived from the synchronizing, voltage monitor and comparator stages so that only pulse sequences comprosing an even number of pulses are produced. Because each pulse train always starts with a positive half-cycle and ends with a negative half-cycle, the load circuit is completely free of DC.
The pulse amplifier can supply up to 250 mA of output current and incorporates a current limiter which fully protects the pulse output (Pin 10) against short circuits to ground (Pin 13).

Pulse control circuit

An internal operational amplifier and high-impedance comparator enable relatively insensitive sensors to be employed in the control circuit using only a few additional components.
Pin 7 accepts an additional definite voltage input (V_7), application of which causes by-passing the comparator input information (V_8) a continuous pulse train to be produced, provided the voltage applied to Pin 6 (V_6) does not exceed a specified rating.
If the high-impedance onput of the sensor monitor (Pin 11) is directly connected to the actual value generator then an open– or short-circuit in the sensor circuit causes immediate closure of output gate G_5.
This stage also allows single output pulses to be converted into bursts of shorter pulses—a great advantage when control and load circuits are to be galvanically isolated from each other by pulse transformers Fig. 18 .
An additional safety feature is the pulse blocking circuit which causes gate G_5 and hence the pulse output to be immediately blocked whenever Pin 12 is grounded (Pin 13) via a low-resistance link.

Additional functions

The ramp generator makes possible proportional burst firing control upto ca. 200 s duration using relatively low-value and inexpensive capacitors. A reference voltage for use in the comparator and operational amplifier is available from Pin 5, the voltage (approximately 5.1 V open circuit) can be reduced by connecting a resistor.
Pin 15 represents full-wave output logic with 20 mA loading capacity.

D.C. supply

Due to higher trigger sensitivity of the triac, the IC is supplied with negative voltage.
The supply input is limited by a bypass regulator so that a current supply via dropper resistor R_1 from mains is allowed. Voltage limitation is $-V_S = 7.3 \ldots 8.6$ V, when $I_S = 22$ mA (typ.).
The internal voltage monitoring take care that during the build up of a supply voltage the outputs are in action when the voltage $V_S \geqq |5.8|$.
According to the requirement supply can be taken as follows:

a) Direct from the mains (Fig. 2) or

b) via a mains transformer (Fig. 5) or

c) regulated DC supply, Fig. 6

Series resistance selection:

$$R_{1max} = 0.85 \frac{V_{Mmin} - V_{Smax}}{2\ I_{tot}}$$

$$I_{tot} = I_S + I_P + I_X$$

$$P(R_1) = \frac{(V_M - V_S)^2}{2\,R_1}$$

whereas
V_M = Mains voltage
V_S = Supply voltage limitation
I_{tot} = Total current
I_S = Supply current without load
I_P = Gate current requirement
I_X = Periphery current requirement

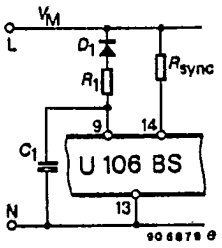
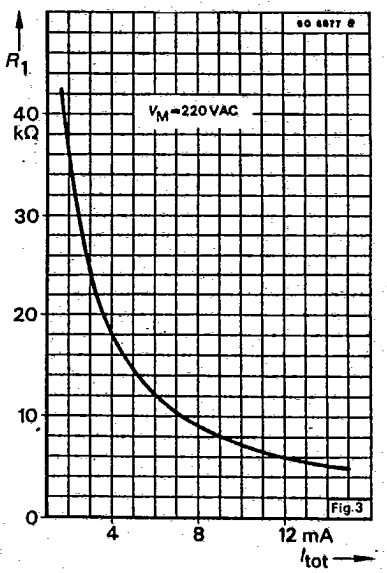


Fig. 2



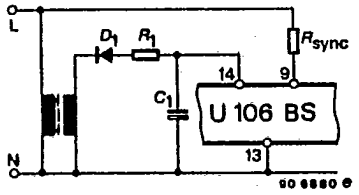
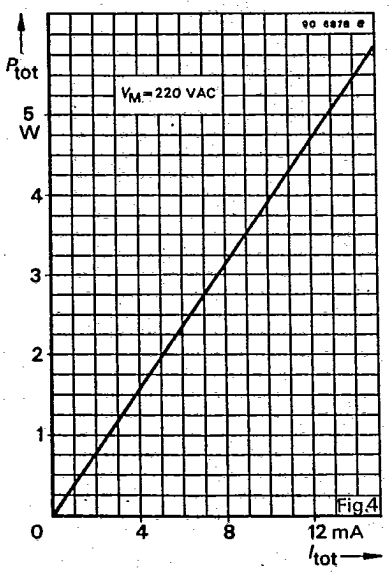


Fig. 5 Mains transformer (low voltage) supply voltage regulator



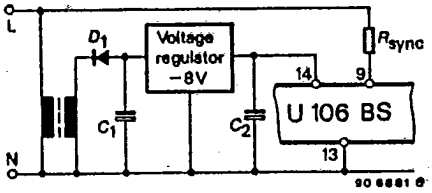


Fig. 6 Regulated DC supply

Pulse generation

The pulse width is determined by the value of synchronizing resistor $R_{sync.}$ (Fig. 7).

When the value of $R_{sync.}$ is calculated, it is essential that the maximum dissipation of the IC (approximately 400 mW) is taken into account. For the pulse generating circuit and half-wave detector discussed the minimum synchronizing current at maximum pulse width is

$I_{sync\ min} = 400\ \mu A$, $V_{14threshold} = 2.52\ V$, $t_{pmax} = 1.5\ ms$

$$R_{sync\ max} = \frac{V_M - 2.52\ V}{0.4\ mA}\ (k\Omega), \text{ and since}$$

$$I_{sync\ max} = 5\ mA,\ R_{sync\ min} = \frac{V_M - 10\ V}{5\ mA}\ (k\Omega)$$

If the load current is low and the dynamic holding current of the triac used is high, then it is possible to prolong the effect of the output pulse by delaying it with respect to the instant of zero crossover (see Fig. 8). This can be achieved by connecting a synchronizing capacitor $C_{sync.}$ as shown, which, in conjunction with $R_{sync.}$ and R_1 at Pin 14 forms a phase shift network. Shortly before and after the instant of zero crossover the input resistance R_1 presented at Pin 14 is 22 kΩ.

It is important that the effect of this resistance parallel to $C_{sync.}$ is taken into consideration, since it affects the ratio of the voltage divider incorporating $R_{sync.}$ and hence the length of the pulse, which is increased slightly above the value obtained with $R_{sync.}$ alone. The following values are quoted for guidance only:

$V_M = 220\ V\sim$; $R_{sync.} = 47\ k\Omega$, $C_{sync.} = 50\ nF$, $t_p = 200\ \mu s$, $\Delta t = 100\ \mu s$.

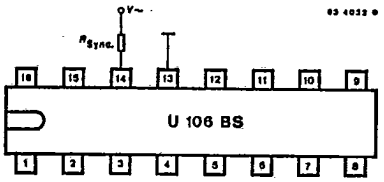


Fig. 7 Synchronisation circuit

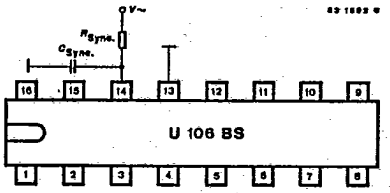


Fig. 8 Pulse delay circuit

Full-wave control

Operation of the full-wave control circuit is explained in terms of positive logic, reference being made to the appropriate block and pulse diagrams (Fig. 9 and 10). If the supply voltage is correct and the comparator or threshold detector receives a "pulse output" command, then G_1 as well as G_2 is in the H-state. If the half-wave detector subsequently changes to H, then G_4 changes to H also, and thereby sets the memory and enables G_6 to pass pulses received from G_5 to the output. The memory remains in this set condition if G_1 happens to change to L during a negative half-cycle, since G_4 holds G_2 at H.

When the falling edge of the half-wave signal G_4 goes to L, G_2 is blocked, whereby G_3 is ready. The next positive edge of the half-wave signal switches G_3 to H and the memory is reset.

If G_1 and G_2 happen to change from L to H state during a negative half-cycle, then the memory is also set, this is because G_4 is ready and the state of G_2 is directly transferred to the set input, whilst G_3 blocks (off) the reset input of the memory.

This means that the memory can change its state only while the half-wave detector produces an H-signal, i.e. change only during an negative half-cycle. Because there are two zero transitions of the sync voltage between successive negative half-cycle peaks, the output pulses are presented in pairs, always begining during the positive zero crossover and ending with a pulse having negative dv/dt.

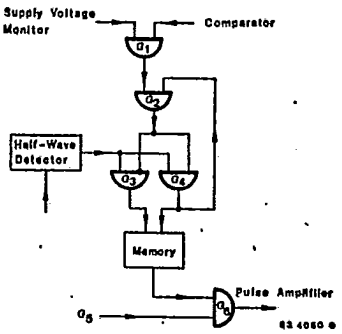


Fig. 9 Full-wave control logic

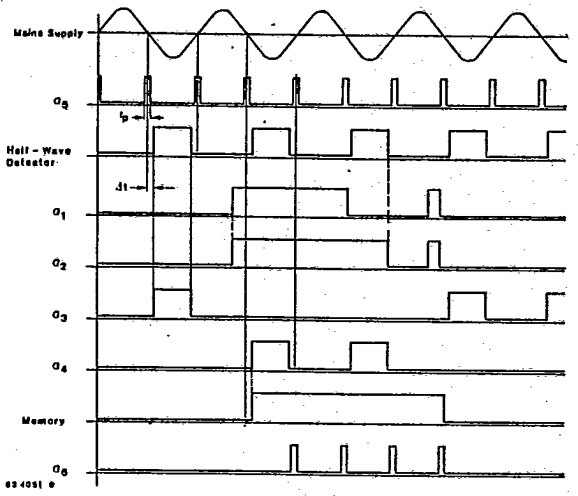


Fig. 10 Pulse diagram of the full-wave logic

Firing pulse output

Output current of the amplifier is limited to a typical value of 250 mA due to the internal current sink. A gate pulse of lower value i.e., $I_G = 50$ mA is just sufficient for firing the standard triac. To avoid unnecessary power loss at the IC due to series resistance R_G to reduce the firing current.

$$R_{G\,max} = \frac{V_{Smin} - 3V}{I_{G\,max}} = \frac{4.3V}{I_{G\,max}} \quad \text{whereas } I_G = I_O$$

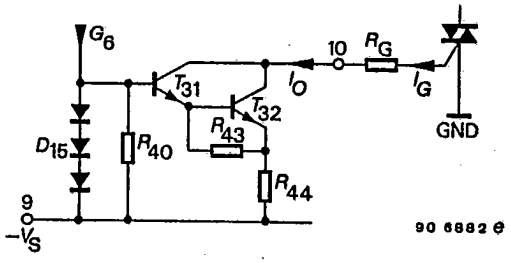


Fig. 11: Firing pulse output

The circuit can be made (by the connection of external components) to chop up the output pulse into a train of shorter pulses, Fig. 12. This considerably reduces the firing energy per unit time and allows the firing pulse to be effectively prolonged – a distinct advantage if triacs requiring a large dynamic holding current are to be used. Another advantage is that the size of any firing pulse transformer employed to separate the control circuit from the load circuit can be considerably reduced.
Recommended values: $C_1 = 0.047$ µF, $C_2 = 0.68$ µF, $R_1 = 1$ kΩ.

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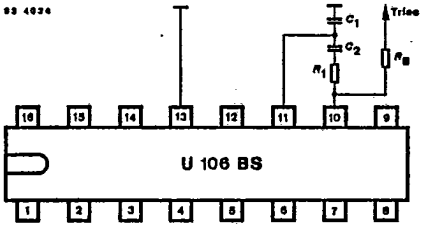


Fig. 12 Chopped output mode

Ramp generator

RC-Ramp generator supplies at Pin 16 signal as shown in diag. 13, whose duration is according to flicker standard for the application of symmetrical burst 1 control. Ramp duration T can be adjusted with the capacitor C_T whose current is controlled with R_T.

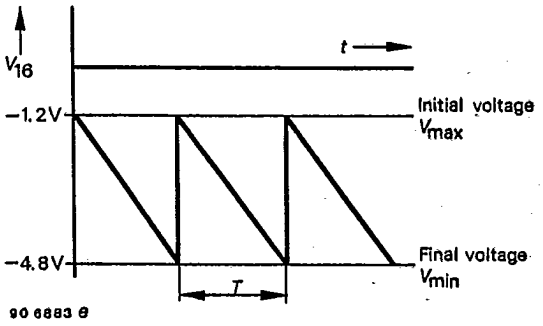


Fig. 13

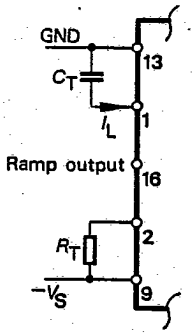


Fig. 14

Charge current of the capacitor can be calculated as follows:

$$I_L = \frac{0.8\ V}{R_T\ k\Omega + 11.5\ k\Omega} \qquad I_L \geq 3\ \mu A$$

$$0 < R_T < 250\ k\Omega$$

$$\Delta V = V_{max} - V_{min} = 4.8\ V - 1.2\ V = 3.6\ V$$

Operation amplifier, comparator, continuous pulse switch

Free available operation amplifier can be used as a high impedance test and control amplifier. Comparator being connected after operational amplifier compares the output signal with the reference signal at pin 8. According to the application, whether it is symmetrical burst–, two-point– or proportional control, the input Pin 8 can be connected internally with the ramp output of pin 16. Continuous pulse switch offers the possibility via control input Pin 7 ($V_7 = -V_S$), irrespective of comparator, to keep the reference or test input into continuous operation.

Sensor monitor, Pin 11

A separate input Pin 11 allows the sensor monitoring, in the event of broken wire and short circuit. In normal case, the voltage of one of the sensor monitor is defined inside the internal value of typ. $-V_{11} = 1.5 \ldots 6.4$ V. In case of defect, the sensor voltage of the monitor sensor for the monitoring window has the effect that it remains cut-off to the outputs of G_5.

Pulse blocking Pin 12

It offers the further possibility of output(s) to be switched across the gated G_5. The pulse blocking is active, if the control voltage is positive than $V_T = 2.2$ V.

Reference voltage source (Fig. 15)

A constant current of $I_K \approx 1$ mA is derived from transistor T_{50}. The off-load voltage available from Pin 5 is consequently:

$V_{Ref} = I_K \cdot R_{54} \approx 5.1$ V when $R_{54} = 5.1$ kΩ.

Connecting an external load (R_p) parallel to Pin 5 has the effect of reducing the voltage to:

$$V_{Ref} = I_K \cdot \frac{R_{54} \cdot R_p}{R_{54} + R_p} = 1 \text{ mA} \frac{5.1 \cdot R_p}{5.1 + R_p}, \quad \text{whereas } R_p \text{ in k}\Omega.$$

V_{Ref} therefore depends directly upon the resistance of the load. However, since the operational amplifier as well as the comparator has a very high input impedance, this loading effect can be ignored.

Full wave logic output (Fig. 23)

In switching position "1" of the full wave logic, T_{58} switches the supply voltage V_{S9} to Pin 15 ($I_O \leqq 20$ mA).

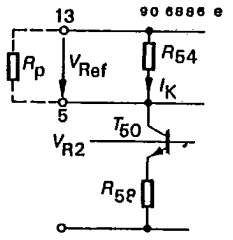


Fig. 15 Reference voltage source

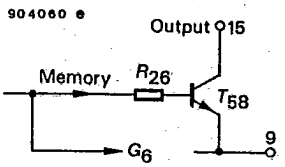


Fig. 16 Full wave logic output

Absolute maximum ratings
Reference point Pin 13

Supply current, Fig. 4, 5	Pin 9	$-I_S$	50		mA
Sync. current	Pin 14	$\pm I_{Sync.}$	10		mA
Output current	Pin 15	I_O	20		mA
	Pin 8	I_O	1		mA
	Pin 6	I_O	3		V
Input voltages Pins 2, 3, 4, 5, 7, 11, 12		V_I	$\leq V_S$		V
	Pin 14	V_{Isync}	$\leqq \pm V_S$		V
$I_{I8} \geqq$ mA	Pin 8	V_I	$\leq V_S$		V
	Pin 10	V_I	$-V_S \leqq V_I \leqq 2$		V
Junction temperature		T_j	125		°C
Operating-ambient temperature range		T_{amb}	0...70		°C
Storage temperature range		T_{stg}	−40...+125		°C
Power dissipation					
$T_{amb} = 45$ °C		P_{tot}	530		mW
$T_{amb} = 70$ °C		P_{tot}	365		mW

Maximum thermal resistance

Junction ambient		R_{thJA}	150		kW

Electrical characteristics Min. Typ. Max.

$V_S = 7.5$ V, reference point Pin 13, $T_{amb} = 25$ °C, unless otherwise specified

Supply voltage limitation	Pin 9	$-V_S$	7.3		8.6	V
Supply current	Pin 9	$-I_S$			22	mA
Supply voltage monitoring	Pin 9	$-V_{SON}$			5.8	V
Synchronisation						
Sync. current	Pin 14	$I_{Sync.}$	400			µA
Output pulse width, Fig. 7						
$R_{Sync.} =$ 47 kΩ, $V = 220$ V~		t_p		100		µs
$R_{Sync.} = 100$ kΩ, $V = 220$ V~		t_p		200		µs
Output pulse						
Output voltage						
$I_{o10} \leqq 250$ mA	Pin 10	$-v_o$		5		V
Output pulse current						
$R_O \leqq 25$ Ω, Fig. 11	Pin 10	I_o		250		mA
Operational amplifier						
Input offset voltage	Pin 3, 4	V_{IO}		15		mV
Input offset current	Pin 3, 4	I_{IO}		1		µA
Input bias current	Pin 3, 4	I_{IB}			1	µA
Open loop gain	Pin 6	G_{vo}		80		dB
Common mode rejection ratio	Pin 6	CMR		70		dB
Common mode input range	Pin 6	$-V_{IC}$	1		6	V

			Min.	Typ.	Max.	
Comparator						
Input offset voltage	Pin 6, 8	V_{IO}		10		mV
Input bias current	Pin 8	I_I			1	µA
Common mode input range	Pin 6, 8	$-V_{IC}$	1		6	V
Sensor Control						
Input current: Output pulse at Pin 10						
$-V_{I11} = 1.5...6.4$ V	Pin 11	$\pm I_I$			200	nA
No output pulse at Pin 10						
$-V_{I11} < 1.3$ V	Pin 11	I_I			1	µA
$-I_{I11} > 6.7$ V		$-I_I$			5	µA
Pulse blocking						
Trigger level no output pulse at Pin 10	Pin 12	$-V_I$		$<\|2.2\|$		V
Input current						
$-V_I > 3.5$ V	Pin 12	I_I			200	nA
$-V_I < 2.2$ V	Pin 12	I_I			40	µA
Continuous pulse switch						
Trigger level for continuous pulses at Pin 10 ON	Pin 7	$-V_I$		$>\|4.7\|$		V
OFF	Pin 7	$-V_I$		$<\|4.7\|$		V
Input current						
$-V_I > 5.0$ V	Pin 7	$-I_I$			200	nA
$-V_I < 4.5$ V	Pin 7	$+I_I$	20		800	µA
Logic output, Fig. 16						
$I_O = 20$ mA	Pin 15	$-V_O$	5.5			V
Ramp generator						
Series resistance	Pin 2-9	R_{V2}	0		200	kΩ
Period Fig. 13						
$R_{V2} = 200$ kΩ, $C_p = 10$ µF	Pin 16	T		10		s
Initial voltage	Pin 16	$-V_o$		1.2		V
Final voltage	Pin 16	$-V_o$		4.8		V
Reference voltage						
$I_{Ref} \leq 10$ µA	Pin 5	$-V_{Ref}$ [1]		5.1		V

[1] By loading the reference voltage with a resistance R between Pin 5 and Pin 13, the reference voltage is reduced to:

$$-V_{Ref} \approx \frac{5.1\ V}{1 + \frac{5.1\ k\Omega}{R}}$$

Applications

There are three main fields of application for the U 106 BS.

1. **Temperature control**
2. **Timer**
3. **Static switch**

The U106 BS can be used to realize a great variety of temperature control circuits simply by the addition of a few passive components, the inbuilt continuous pulse facility permitting, if necessary, control in two steps.

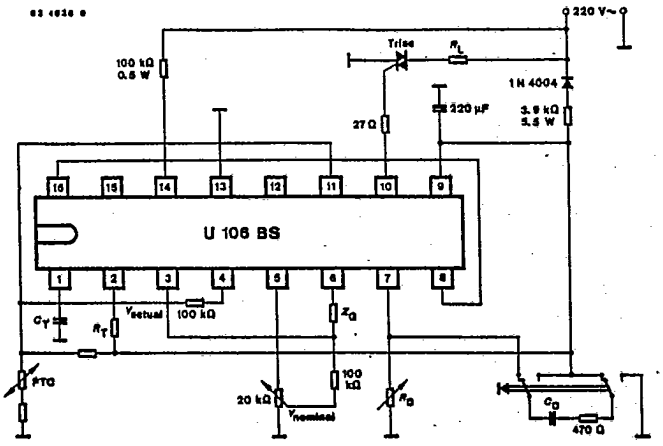


Fig. 17 Proportional controller with full-load switched-on

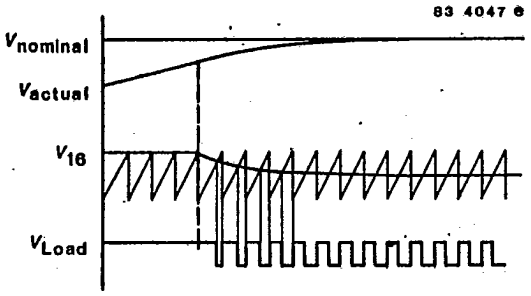
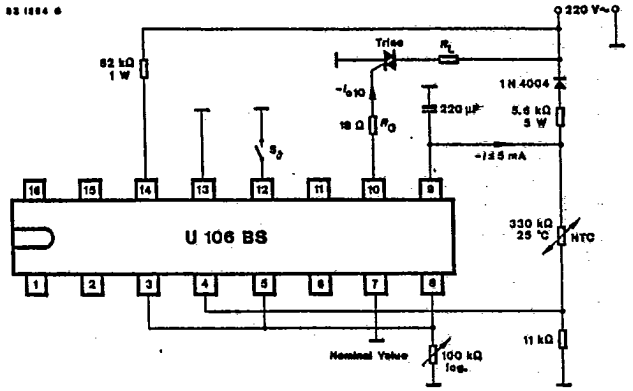


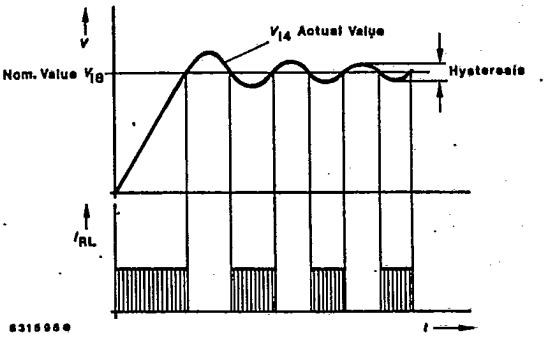
Fig. 18 Proportional control rate

As a typical example of this, the most important group of applications, the circuit of a proportional controller which operates in conjunction with a monitored PTC sensor and provides full-load switch-on facilities, is discussed (Fig. 17).

When the double-pole key is pressed, the charge on capacitor C_D is reversed so that on release of the button the Pin 7 potential is initially $-2\ V_S$ volt. The internal reference voltage V_{R2} is now applied to Pin 8 until capacitor C_D has reversed its charge again via R_D. This means that the time during which the full-wave logic is activated depends on the time constant $T_D \approx C_D \cdot R_D$, provided the measured variable does not exceed a given maximum value ($V_8 < V_{R2}$).
If, during the interval T_D, the actual value should unexpectedly exceed the limit, then the full-wave logic is immediately disabled by the comparator until the measured value has fallen to below the limit again.
After the elapse of the initial switch-on period the system continues to operate as a proportional controller (Fig. 18). The operational amplifier compares the desired value with the actual value and amplifies the deviation, which is then used to switch the comparator. Pin 8, the inverting input of the comparator, is connected to the output of the ramp generator, the period time of which (adjustable by choice of R_T and C_T) must be set so as to suit the controlled plant ($T_{ramp} < T_{heating\ system}$).

The action of this controller depends to a large extent on the nature and magnitude of the impedance Z_G connected in the negative feedback path.
An additional degree of safety is obtained if Pin 11 is linked with the sensor circuit. In this case the sensor monitor inhibits the firing pulse output not only in the event of an open- or short-circuit in the sensor circuit, but also in the event of a system fault which causes the measured value to rise above a set limit.
Therefore the values of the components used in the sensor circuit should be chosen so that the actual value always remains within the limits to which the sensor monitor is set.





t_p = 160 µs
I_{o10} ≧ 100 mA

Fig. 19 Two point control with excessive temperature protection switch (S_ϑ) 60...150 °C.

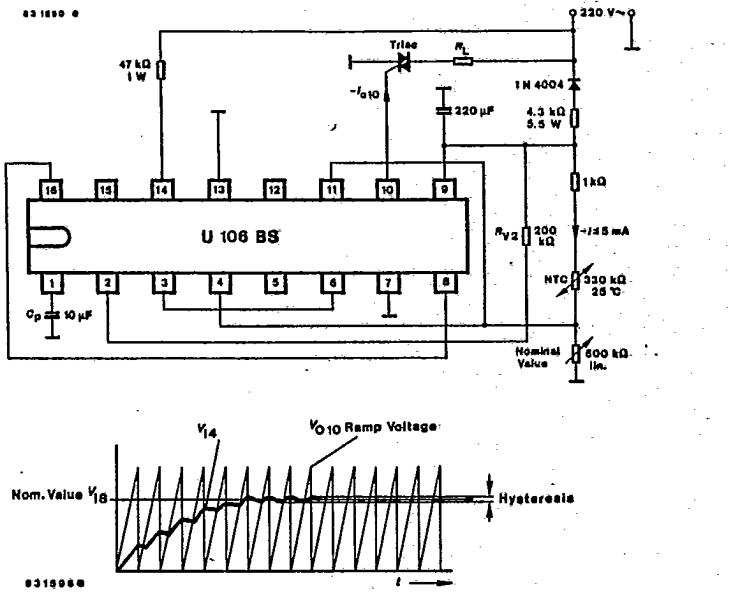


Fig. 20 Proportional control with sensor control and high nominal range 25...300 °C

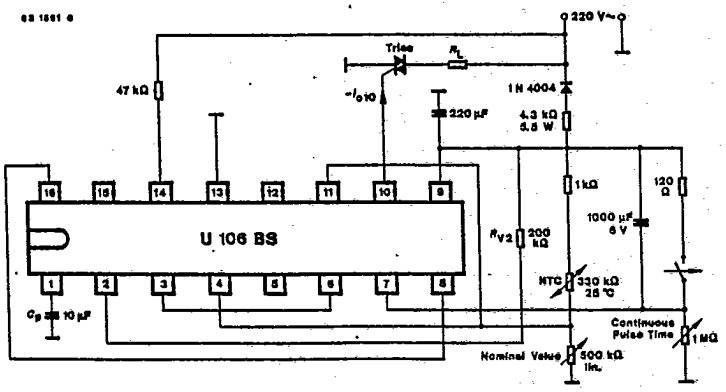


Fig. 21 Proportional control with adjustable continuous pulse circuit limiting boundary switch and transmission control

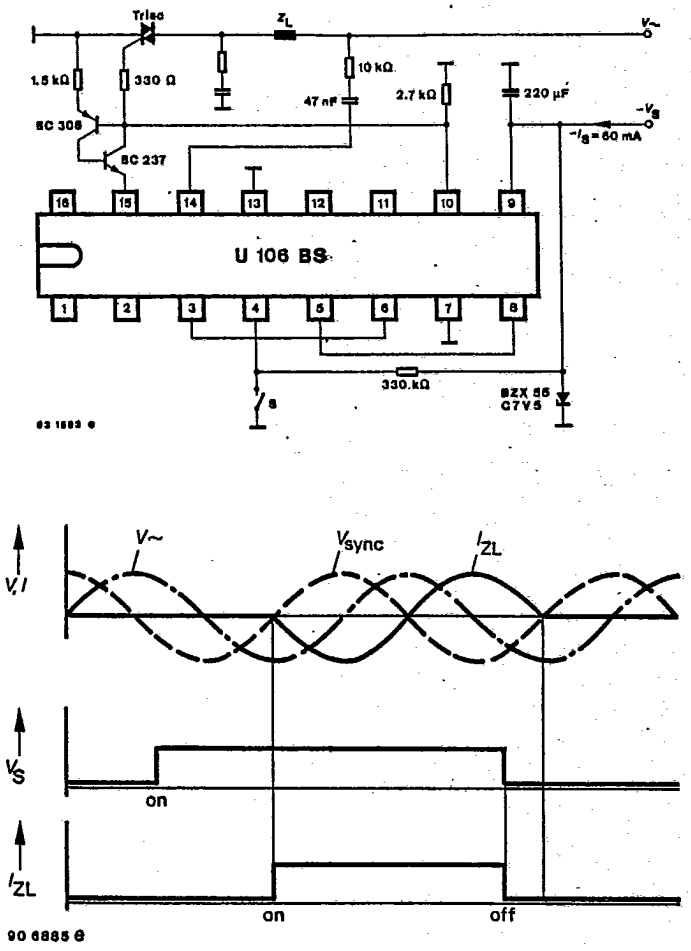


Fig. 22 Optimum switching of inductive loads

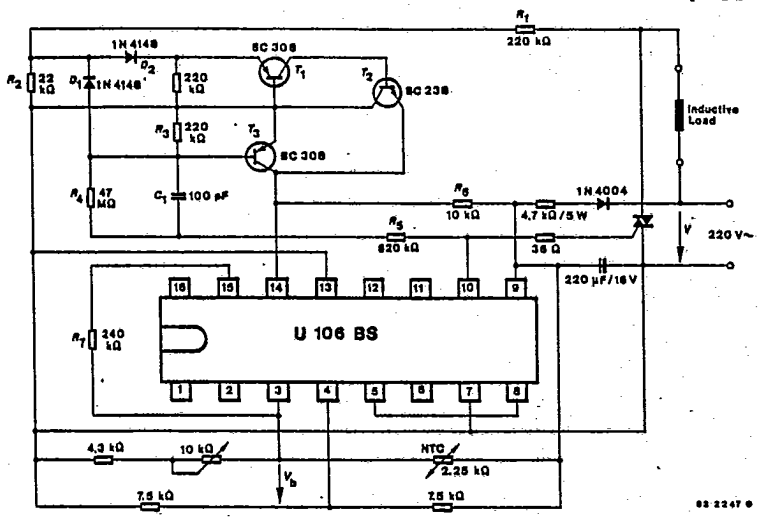


Fig. 23 Two-point temperature control circuit for inductive load

A description will be given of the circuit of a two-point temperature control circuit (Fig. 23) using the U 106 BS integrated zero-crossing switch which makes it possible to control the preselected temperature of a cooling arrangement between +10 °C and −10 °C in optimum fashion and independently of the cos φ of the inductive load used in each case (compressor motor).
The desired temperature is preselected on the 10 kΩ variable resistance of the measuring bridge. The bridge voltage v_b is applied to pin connections 3 and 4 of the U 106 BS, being passed through the operational amplifier of the latter to the comparator. The NTC also belonging to the bridge acts as a sensor. If the temperature of the latter is higher than the desired temperature, v_b becomes negative. This means that the logic of the U 106 BS releases the control pulses for the triac. If the NTC is cooled again after balancing the bridge (caused by the temperature inertia of the system), v_b becomes positive, i.e. the logic now blocks the pulse output. To prevent undesirable hunting of the circuit a small hysteresis is necessary which can be realized with resistor R_7. With $R_7 = 240$ kΩ an accuracy of approximately ±0.5° is obtained.
If an inductive load is to be operated independent of its cos φ with maximum power via triac, the triac has to be triggered during zero crossing of the load current. With normal circuitry, however, the U 106 BS supplies a trigger pulse to the triac at each voltage zero crossing. Thus, additional circuitry is necessary to generate the trigger pulse each time at the moment of current zero crossing.
If current flows through the inductive load, a potential is present at the main connections of the triac of the magnitude of only 1 V which is reduced by the voltage divider R_1/R_2 and is passed via diodes D_1 and D_2 to transistors T_1 and T_3. Here, T_1, T_2 and T_3 become nonconductive and via R_6 negative potential is present at Pin 14 of the U 106 BS. Thus, the output stage of the U 106 BS blocks as well.
If the triac extinguishes during current zero crossing, the voltage V at its main connections rises so sharply that via R_1 at positive half-wave transistors T_1, T_2 and T_3 are activated and with negative half-wave transistor T_3 is switched through. Thus, the potential at Pin 14 becomes practically zero and the triac is triggered. Resistors R_1 and R_2 are dimensioned so that the transistors switch through as from a voltage V of approximately 10 V.

In order to prevent repeated triggering of the triac during a half-wave – caused by holding current not yet being reached – a monoflop has been formed with components R_3, R_4, R_5, C_1 and transistor T_3 which is required anyway. So that this monoflop functions even at the positive half-wave, the diode D_1 ensures decoupling of transistor T_3 from the positive half-wave. T_3 is now activated by the negative control pulse which is taken via C_1 and R_5 from connection 10 until no further charging current flows through R_3. The monoflop is dimensioned so that the pulse duration T of the control pulse of the time constants t_1 corresponds to $t_1 = C_1 (R_3 + R_5) = T$.
After decay of the control pulse C_1 is discharged via R_4 ($t_2 = C_1 \cdot R_4$; $t_1 \ll t_2 < 10$ ms). Thus, the monoflop is prepared for the next current zero crossing.

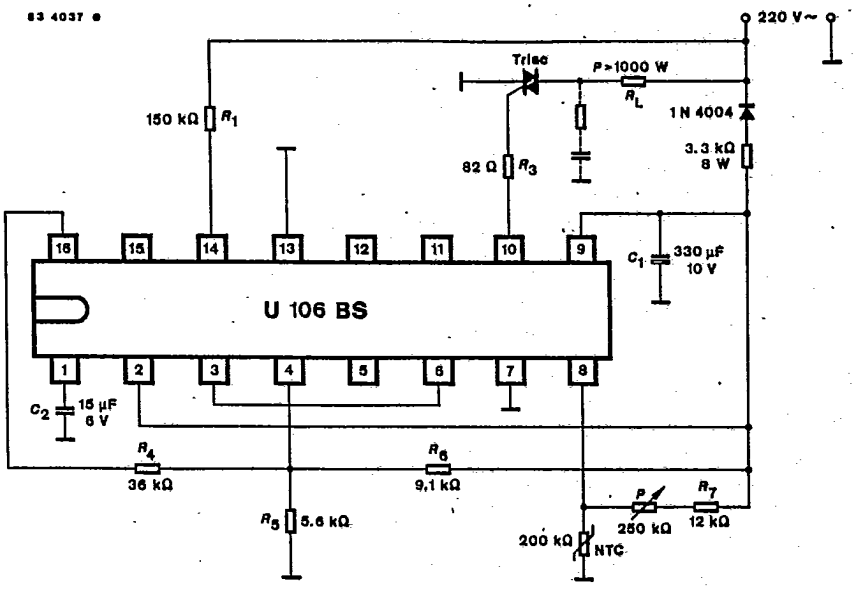


Fig. 24 Temperature control with superimposed proportional characteristic for a temperature range 30...110 °C and ±3 °C hysteresis.

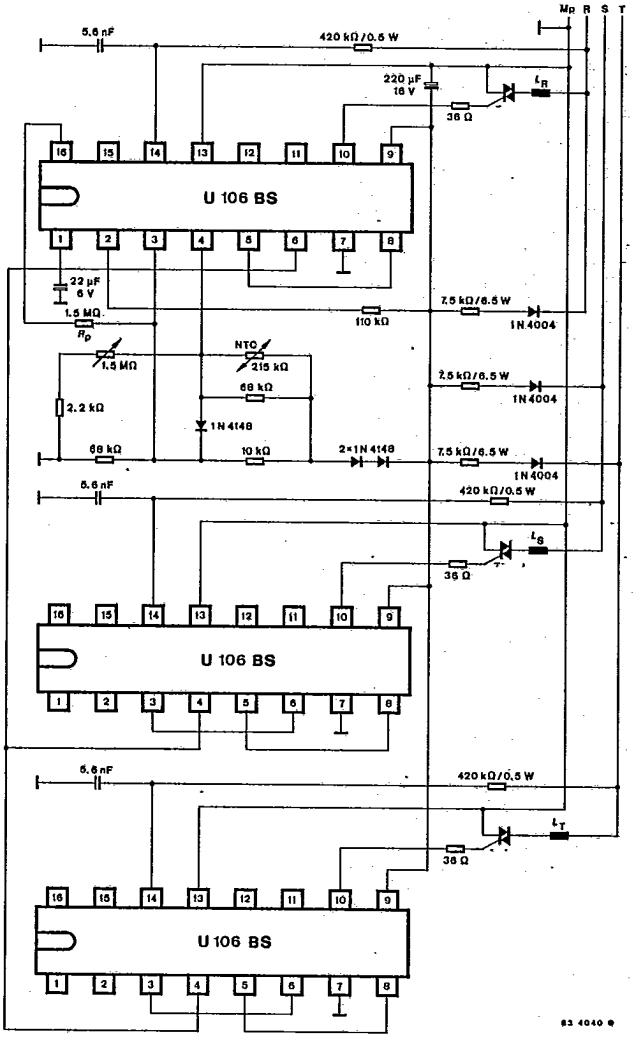


Fig. 25 Three-phase, two-point temperature control with superimposed proportional characteristic for a temperature range 60...280 °C

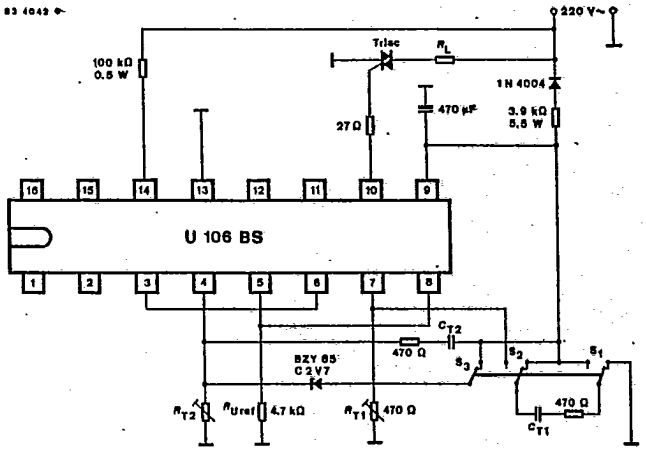


Fig. 26 One-shot switching delay circuit

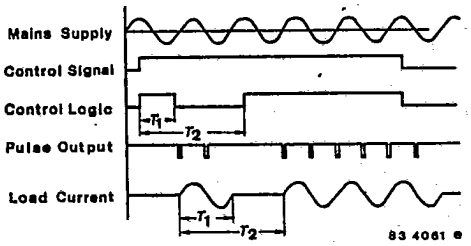


Fig. 27 Pulse diagram of a "one-shot" switching delay

Another important application for the U 106 BS is in a variety of timing circuits such as those used in traffic light control, exposure timers, pulse control circuits and many other devices.
As an example a one-shot switching delay circuit with the timing characteristics shown above is discussed (Fig. 26, 27).
As in the previous example, the length of the initial run-up period is determined by the timing constant C_{T1}, R_{T1}, whilst that of T_2 is determined by a second timing network formed by R_{T2} and C_{T2}. The operational amplifier functions as a voltage follower in an electrometer circuit, and the comparator compares V_{CT2} with a reference voltage set by choice of a resistor (R_{VRef}).
The Z-diode is necessary to keep the level of V_{CT2max} below that of the internal reference voltage V_{R2}, which, during the run-up period, is applied to the value of R_{Ref} should not be less than 4.7 kΩ to keep any additional current drain during interval T_1 within acceptable limits.

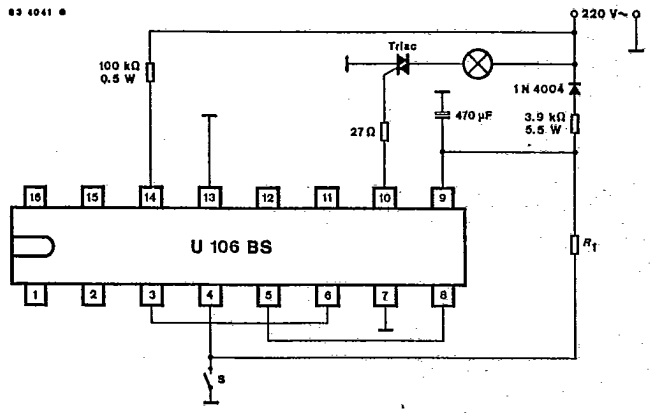


Fig. 28 Static switch

The main advantage of using the U 106 BS as a static switch is that it permits the magnitude of the initial switch-on surge to be controlled.
The filaments of incandescent lamps, for example, have a very low resistance when cold, and therefore should not be energized at an instant in the cycle when the instantaneous voltage is high, as in this case the magnitude of the surge current could be 18 times that of the rated current whereby zero current switching value reduces the surge current to 5 times the rated current.

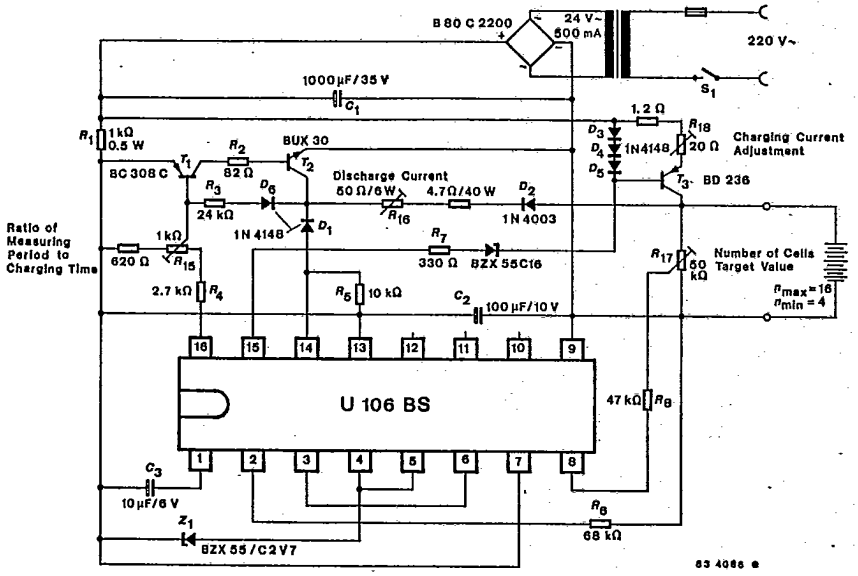


Fig. 29 Automatic charging unit for NC accumulators

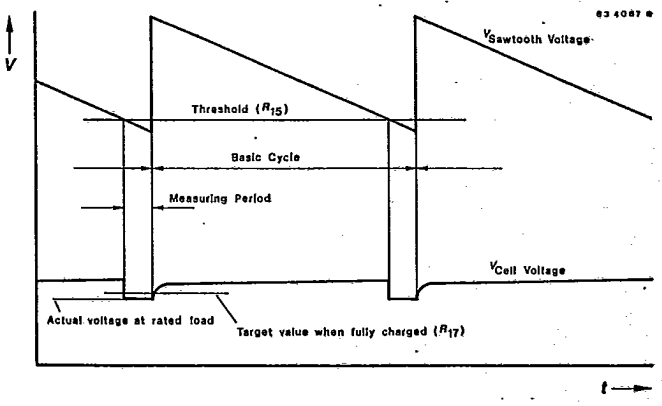


Fig. 30 Voltage diagram

The principle idea consists of measuring the cell voltage during a short period at rated load, and deciding on the basis of the result whether or not charging should be continued during the next basic cycle (Fig. 30). This basic cycle is generated with the aid of the sawtooth generator which is part of the U106BS. The frequency of this generator is determined by C_3 and R_6. The duty cycle (ratio of charging to measuring time) is adjusted with R_{15}. T_1 and T_2 form a threshold switch which connects the load resistor R_{16} to the accumulator during the measuring period. At the same time, the logic circuit is activated via D_1 and the synchronisation input, Pin 14. If the cell voltage tapped off from R_{17} is less than the target value set by Z_1 (or any other reference source), the logic circuit remains in the "on" condition, and the charging current supply T_3, D_3, D_4, and R_{18} is activated by the logic circuit output at Pin 15. If the cell voltage reaches the target value, the logic circuit flips in to the "off" state during the next measuring period, and the charging operation is interrupted. No further charging is carried out in the ensuing cycles, but periodic discharging still occurs in each measuring period, so that the cell voltage drops until the logic circuit flips back into the "on" state.

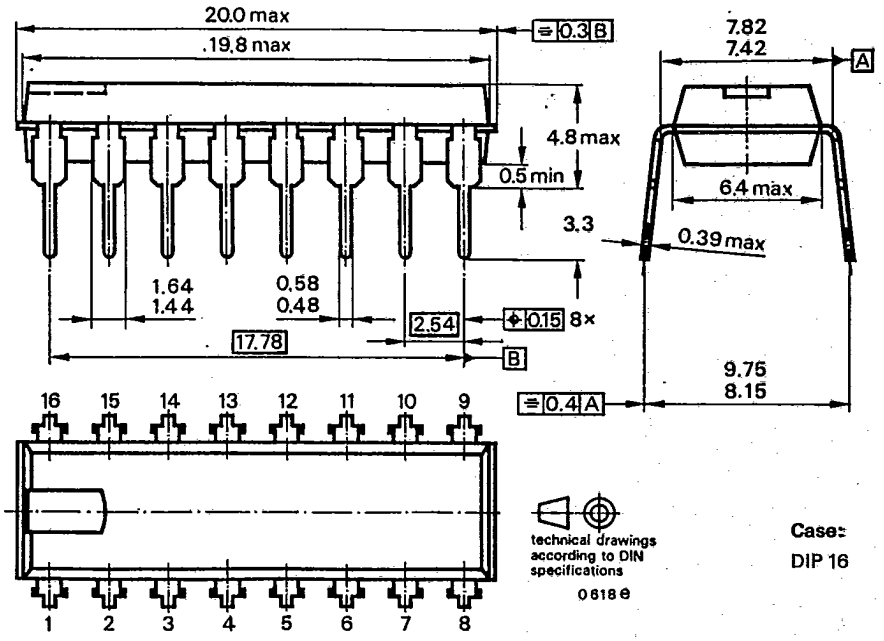
The transformer, bridge rectifier, and transistors T_2 and T_3 must be selected corresponding to the charging current. T_3 must also be cooled according to its power dissipation.

U 106 BS

TELEFUNKEN ELECTRONIC

T-65-09

Dimensions in mm



technical drawings according to DIN specifications

0618e

Case:
DIP 16