

# Quad Analog Switch/Quad Multiplexer

The MC14066B consists of four independent switches capable of controlling either digital or analog signals. This quad bilateral switch is useful in signal gating, chopper, modulator, demodulator and CMOS logic implementation.

The MC14066B is designed to be pin-for-pin compatible with the MC14016B, but has much lower ON resistance. Input voltage swings as large as the full supply voltage can be controlled via each independent control input.

- Triple Diode Protection on All Control Inputs
- Supply Voltage Range = 3.0 Vdc to 18 Vdc
- Linearized Transfer Characteristics
- Low Noise — 12 nV/ $\sqrt{\text{Cycle}}$ ,  $f \geq 1.0$  kHz typical
- Pin-for-Pin Replacement for CD4016, CD4016, MC14016B
- For Lower  $R_{ON}$ , Use The HC4066 High-Speed CMOS Device

### MAXIMUM RATINGS\* (Voltages Referenced to $V_{SS}$ )

Symbol	Parameter	Value	Unit
$V_{DD}$	DC Supply Voltage	- 0.5 to + 18.0	V
$V_{in}, V_{out}$	Input or Output Voltage (DC or Transient)	- 0.5 to $V_{DD} + 0.5$	V
$i_{in}$	Input Current (DC or Transient), per Control Pin	$\pm 10$	mA
$I_{sw}$	Switch Through Current	$\pm 25$	mA
$P_D$	Power Dissipation, per Package†	500	mW
$T_{stg}$	Storage Temperature	- 65 to + 150	$^{\circ}\text{C}$
$T_L$	Lead Temperature (8-Second Soldering)	260	$^{\circ}\text{C}$

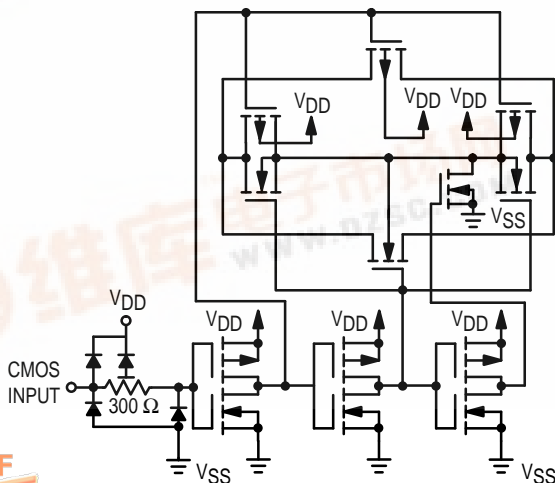
\* Maximum Ratings are those values beyond which damage to the may occur.

† Temperature Derating:

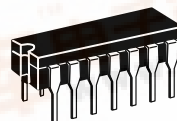
Plastic "P and D/DW" Packages: - 7.0 mW/ $^{\circ}\text{C}$  From 65 $^{\circ}\text{C}$  To 125 $^{\circ}\text{C}$

Ceramic "L" Packages: - 12 mW/ $^{\circ}\text{C}$  From 100 $^{\circ}\text{C}$  To 125 $^{\circ}\text{C}$

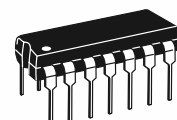
### CIRCUIT SCHEMATIC (1/4 OF CIRCUIT SHOWN)



## MC14066B



**L SUFFIX**  
 CERAMIC  
 CASE 632



**P SUFFIX**  
 PLASTIC  
 CASE 646



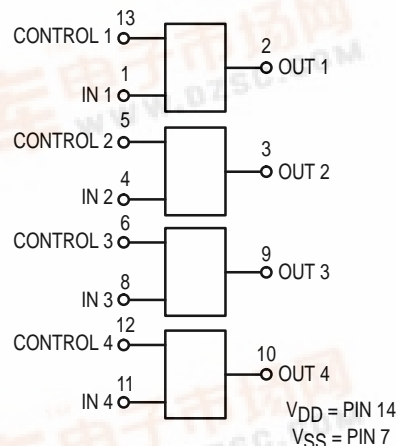
**D SUFFIX**  
 SOIC  
 CASE 751A

### ORDERING INFORMATION

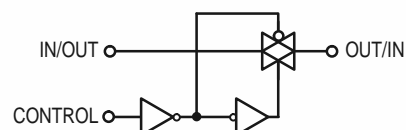
MC14XXXBCP	Plastic
MC14XXXBCL	Ceramic
MC14XXXBD	SOIC

$T_A = -55^{\circ}$  to  $125^{\circ}\text{C}$  for all packages.

### BLOCK DIAGRAM



### LOGIC DIAGRAM AND TRUTH TABLE (1/4 OF DEVICE SHOWN)



Control	Switch
0 = $V_{SS}$	OFF
1 = $V_{DD}$	ON

Logic Diagram Restrictions  
 $V_{SS} \leq V_{in} \leq V_{DD}$   
 $V_{SS} \leq V_{out} \leq V_{DD}$



## ELECTRICAL CHARACTERISTICS

Characteristic	Symbol	V <sub>DD</sub>	Test Conditions	- 55°C		25°C			125°C		Unit
				Min	Max	Min	Typ #	Max	Min	Max	

### SUPPLY REQUIREMENTS (Voltages Referenced to V<sub>EE</sub>)

Power Supply Voltage Range	V <sub>DD</sub>	—		3.0	18	3.0	—	18	3.0	18	V
Quiescent Current Per Package	I <sub>DD</sub>	5.0 10 15	Control Inputs: V <sub>in</sub> = V <sub>SS</sub> or V <sub>DD</sub> , Switch I/O: V <sub>SS</sub> ≤ V <sub>I/O</sub> ≤ V <sub>DD</sub> , and ΔV <sub>switch</sub> ≤ 500 mV**	— — —	0.25 0.5 1.0	— — —	0.005 0.010 0.015	0.25 0.5 1.0	— — —	7.5 15 30	μA
Total Supply Current (Dynamic Plus Quiescent, Per Package)	I <sub>D(AV)</sub>	5.0 10 15	T <sub>A</sub> = 25°C only The channel component, (V <sub>in</sub> - V <sub>out</sub> )/R <sub>on</sub> , is not included.)	Typical (0.07 μA/kHz) f + I <sub>DD</sub> (0.20 μA/kHz) f + I <sub>DD</sub> (0.36 μA/kHz) f + I <sub>DD</sub>							μA

### CONTROL INPUTS (Voltages Referenced to V<sub>SS</sub>)

Low-Level Input Voltage	V <sub>IL</sub>	5.0 10 15	R <sub>on</sub> = per spec, I <sub>off</sub> = per spec	— — —	1.5 3.0 4.0	— — —	2.25 4.50 6.75	1.5 3.0 4.0	— — —	1.5 3.0 4.0	V
High-Level Input Voltage	V <sub>IH</sub>	5.0 10 15	R <sub>on</sub> = per spec, I <sub>off</sub> = per spec	3.5 7.0 11	— — —	3.5 7.0 11	2.75 5.50 8.25	— — —	3.5 7.0 11	— — —	V
Input Leakage Current	I <sub>in</sub>	15	V <sub>in</sub> = 0 or V <sub>DD</sub>	—	±0.1	—	±0.00001	±0.1	—	±1.0	μA
Input Capacitance	C <sub>in</sub>	—		—	—	—	5.0	7.5	—	—	pF

### SWITCHES IN AND OUT (Voltages Referenced to V<sub>SS</sub>)

Recommended Peak-to-Peak Voltage Into or Out of the Switch	V <sub>I/O</sub>	—	Channel On or Off	0	V <sub>DD</sub>	0	—	V <sub>DD</sub>	0	V <sub>DD</sub>	V <sub>p-p</sub>
Recommended Static or Dynamic Voltage Across the Switch** (Figure 1)	ΔV <sub>switch</sub>	—	Channel On	0	600	0	—	600	0	300	mV
Output Offset Voltage	V <sub>OO</sub>	—	V <sub>in</sub> = 0 V, No Load	—	—	—	10	—	—	—	μV
ON Resistance	R <sub>on</sub>	5.0 10 15	ΔV <sub>switch</sub> ≤ 500 mV**, V <sub>in</sub> = V <sub>IL</sub> or V <sub>IH</sub> (Control), and V <sub>in</sub> = 0 to V <sub>DD</sub> (Switch)	— — —	800 400 220	— — —	250 120 80	1050 500 280	— — —	1200 520 300	Ω
ΔON Resistance Between Any Two Channels in the Same Package	ΔR <sub>on</sub>	5.0 10 15		— — —	70 50 45	— — —	25 10 10	70 50 45	— — —	135 95 65	Ω
Off-Channel Leakage Current (Figure 6)	I <sub>off</sub>	15	V <sub>in</sub> = V <sub>IL</sub> or V <sub>IH</sub> (Control) Channel to Channel or Any One Channel	—	±100	—	±0.05	±100	—	±1000	nA
Capacitance, Switch I/O	C <sub>I/O</sub>	—	Switch Off	—	—	—	10	15	—	—	pF
Capacitance, Feedthrough (Switch Off)	C <sub>I/O</sub>	—		—	—	—	0.47	—	—	—	pF

#Data labeled "Typ" is not to be used for design purposes, but is intended as an indication of the IC's potential performance.

\*\* For voltage drops across the switch (ΔV<sub>switch</sub>) > 600 mV (> 300 mV at high temperature), excessive V<sub>DD</sub> current may be drawn; i.e. the current out of the switch may contain both V<sub>DD</sub> and switch input components. The reliability of the device will be unaffected unless the Maximum Ratings are exceeded. (See first page of this data sheet.)



**ELECTRICAL CHARACTERISTICS\*** ( $C_L = 50$  pF,  $T_A = 25^\circ\text{C}$  unless otherwise noted.)

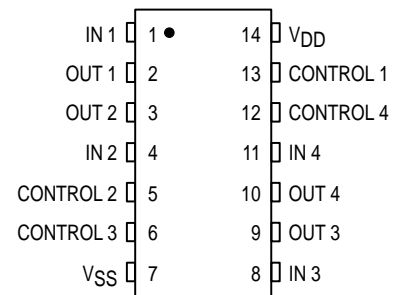
Characteristic	Symbol	V <sub>DD</sub> Vdc	Min	Typ #	Max	Unit
Propagation Delay Times Input to Output ( $R_L = 10$ k $\Omega$ ) $t_{PLH}, t_{PHL} = (0.17 \text{ ns/pF}) C_L + 15.5 \text{ ns}$ $t_{PLH}, t_{PHL} = (0.08 \text{ ns/pF}) C_L + 6.0 \text{ ns}$ $t_{PLH}, t_{PHL} = (0.06 \text{ ns/pF}) C_L + 4.0 \text{ ns}$	$t_{PLH}, t_{PHL}$	5.0 10 15	— — —	20 10 7.0	40 20 15	ns
Control to Output ( $R_L = 1$ k $\Omega$ ) (Figure 2) Output "1" to High Impedance	$t_{PHZ}$	5.0 10 15	— — —	40 35 30	80 70 60	ns
Output "0" to High Impedance	$t_{PLZ}$	5.0 10 15	— — —	40 35 30	80 70 60	ns
High Impedance to Output "1"	$t_{PZH}$	5.0 10 15	— — —	60 20 15	120 40 30	ns
High Impedance to Output "0"	$t_{PZL}$	5.0 10 15	— — —	60 20 15	120 40 30	ns
Second Harmonic Distortion ( $V_{in} = 1.77$ Vdc, RMS Centered @ 0.0 Vdc, $R_L = 10$ k $\Omega$ , $f = 1.0$ kHz)	—	5.0	—	0.1	—	%
Bandwidth (Switch ON) (Figure 3) ( $R_L = 1$ k $\Omega$ , 20 Log ( $V_{out}/V_{in}$ ) = -3 dB, $C_L = 50$ pF, $V_{in} = 5$ V <sub>p-p</sub> )	—	5.0	—	65	—	MHz
Feedthrough Attenuation (Switch OFF) ( $V_{in} = 5$ V <sub>p-p</sub> , $R_L = 1$ k $\Omega$ , $f_{in} = 1.0$ MHz) (Figure 3)	—	5.0	—	-50	—	dB
Channel Separation (Figure 4) ( $V_{in} = 5$ V <sub>p-p</sub> , $R_L = 1$ k $\Omega$ , $f_{in} = 8.0$ MHz) (Switch A ON, Switch B OFF)	—	5.0	—	-50	—	dB
Crosstalk, Control Input to Signal Output (Figure 5) ( $R_1 = 1$ k $\Omega$ , $R_L = 10$ k $\Omega$ , Control $t_{TLH} = t_{THL} = 20$ ns)	—	5.0	—	300	—	mV <sub>p-p</sub>

\* The formulas given are for the typical characteristics only at 25°C.

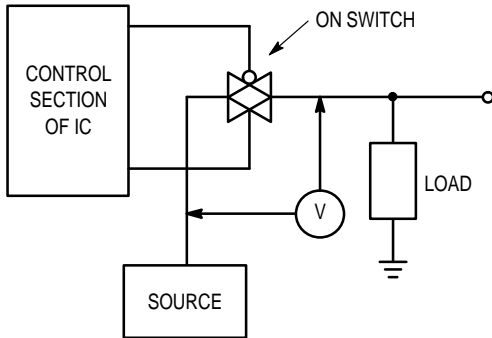
#Data labelled "Typ" is not to be used for design purposes but is intended as an indication of the IC's potential performance.

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation,  $V_{in}$  and  $V_{out}$  should be constrained to the range  $V_{SS} \leq (V_{in} \text{ or } V_{out}) \leq V_{DD}$ . Unused inputs must always be tied to an appropriate logic voltage level (e.g., either  $V_{SS}$  or  $V_{DD}$ ). Unused outputs must be left open.

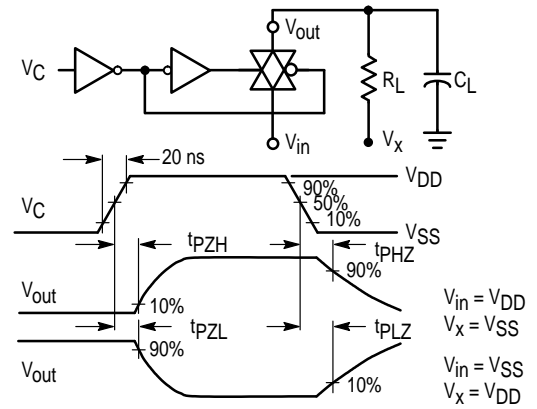
**PIN ASSIGNMENT**



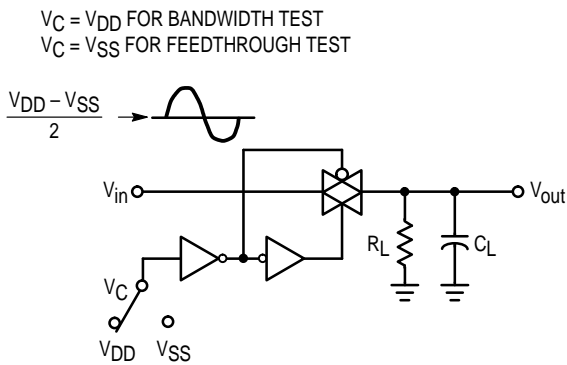
## TEST CIRCUITS



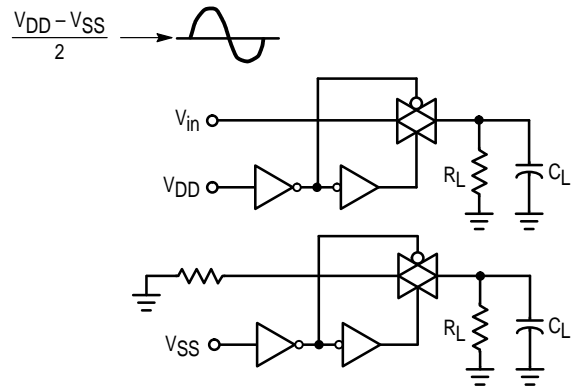
**Figure 1.  $\Delta V$  Across Switch**



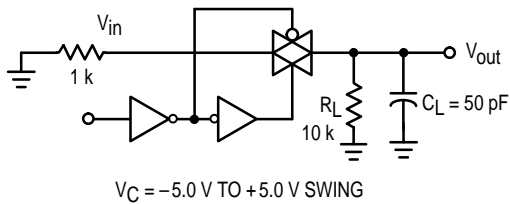
**Figure 2. Turn-On Delay Time Test Circuit and Waveforms**



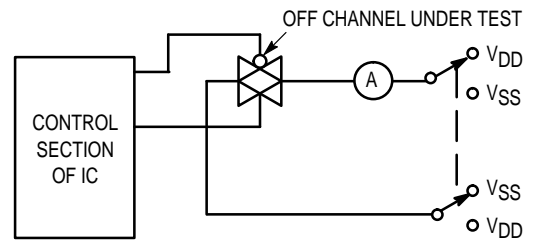
**Figure 3. Bandwidth and Feedthrough Attenuation**



**Figure 4. Channel Separation**



**Figure 5. Crosstalk, Control to Output**



**Figure 6. Off Channel Leakage**



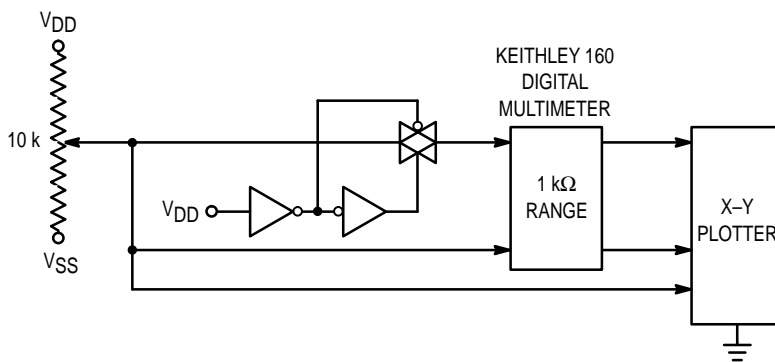


Figure 7. Channel Resistance ( $R_{ON}$ ) Test Circuit

TYPICAL RESISTANCE CHARACTERISTICS

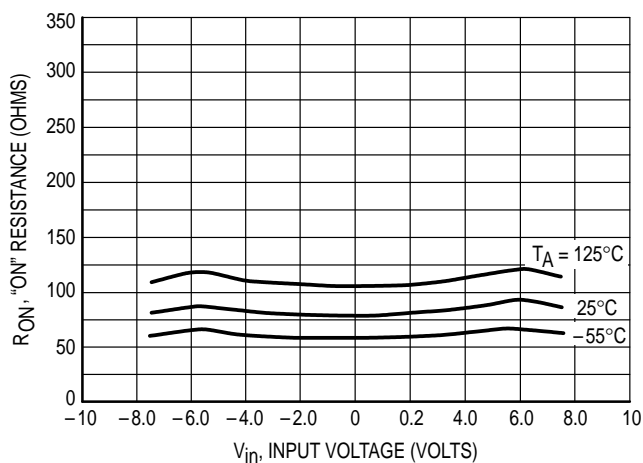


Figure 8.  $V_{DD} = 7.5 \text{ V}$ ,  $V_{SS} = -7.5 \text{ V}$

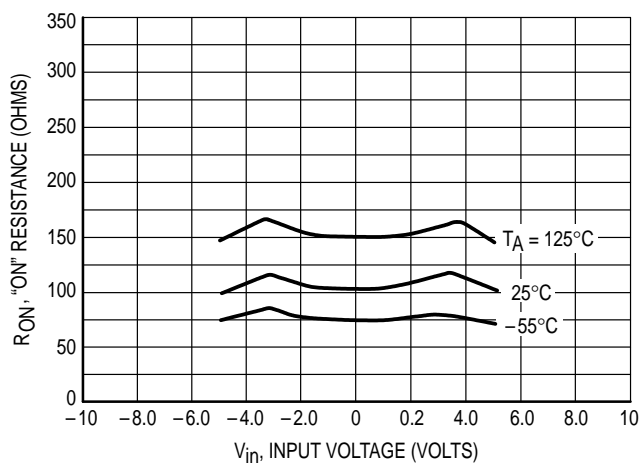


Figure 9.  $V_{DD} = 5.0 \text{ V}$ ,  $V_{SS} = -5.0 \text{ V}$

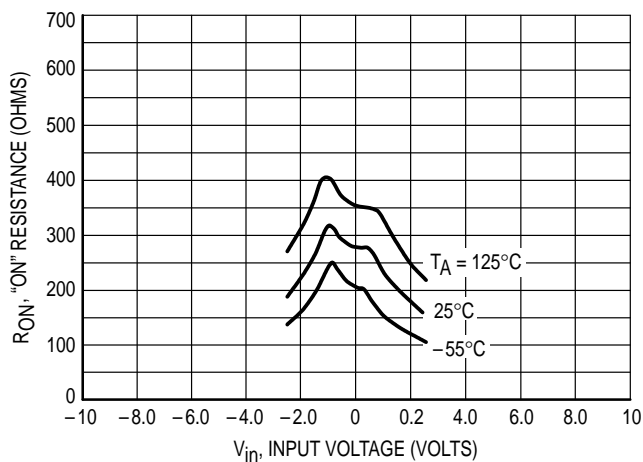


Figure 10.  $V_{DD} = 2.5 \text{ V}$ ,  $V_{SS} = -2.5 \text{ V}$

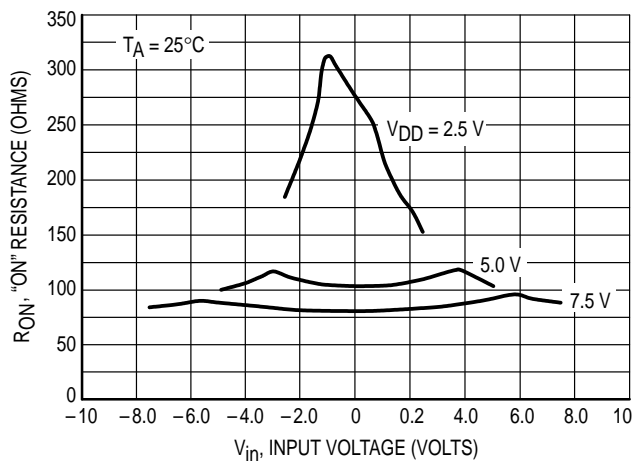


Figure 11. Comparison at  $25^\circ\text{C}$ ,  $V_{DD} = -V_{SS}$



## APPLICATIONS INFORMATION

Figure A illustrates use of the Analog Switch. The 0-to-5 volt digital control signal is used to directly control a 5 volt peak-to-peak analog signal.

The digital control logic levels are determined by  $V_{DD}$  and  $V_{SS}$ . The  $V_{DD}$  voltage is the logic high voltage, the  $V_{SS}$  voltage is logic low. For the example,  $V_{DD} = +5\text{ V} = \text{logic high}$  at the control inputs;  $V_{SS} = \text{GND} = 0\text{ V} = \text{logic low}$ .

The maximum analog signal level is determined by  $V_{DD}$  and  $V_{SS}$ . The analog voltage must not swing higher than  $V_{DD}$  or lower than  $V_{SS}$ .

The example shows a 5 volt peak-to-peak signal which

allows no margin at either peak. If voltage transients above  $V_{DD}$  and/or below  $V_{SS}$  are anticipated on the analog channels, external diodes ( $D_X$ ) are recommended as shown in Figure B. These diodes should be small signal types able to absorb the maximum anticipated current surges during clipping.

The *absolute* maximum potential difference between  $V_{DD}$  and  $V_{SS}$  is 18.0 volts. Most parameters are specified up to 15 volts which is the *recommended* maximum difference between  $V_{DD}$  and  $V_{SS}$ .

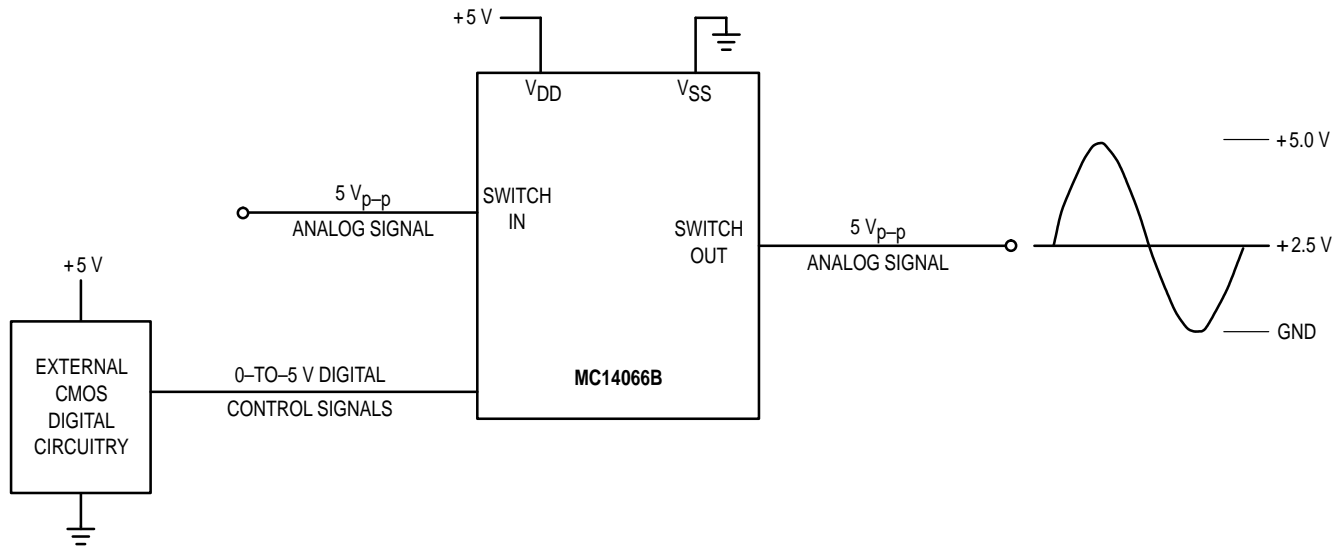


Figure A. Application Example

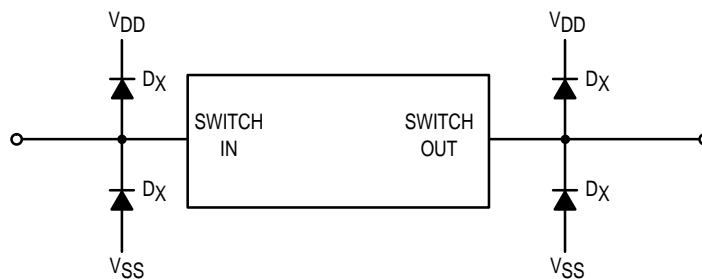
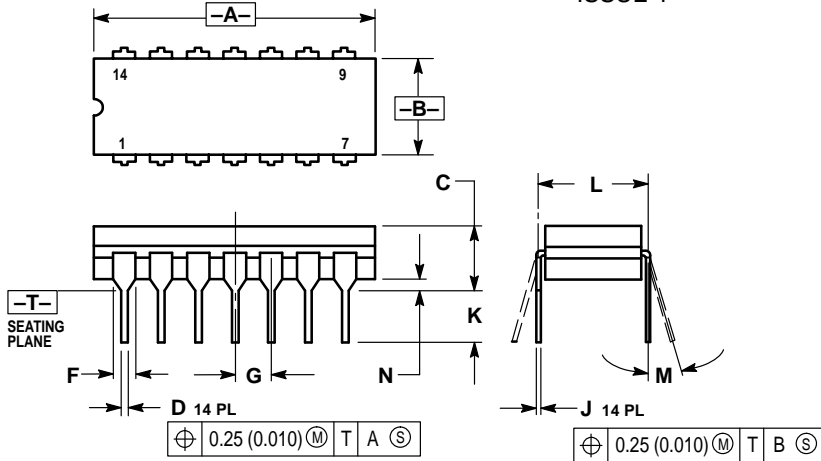


Figure B. External Germanium or Schottky Clipping Diodes



## OUTLINE DIMENSIONS

### L SUFFIX CERAMIC DIP PACKAGE CASE 632-08 ISSUE Y

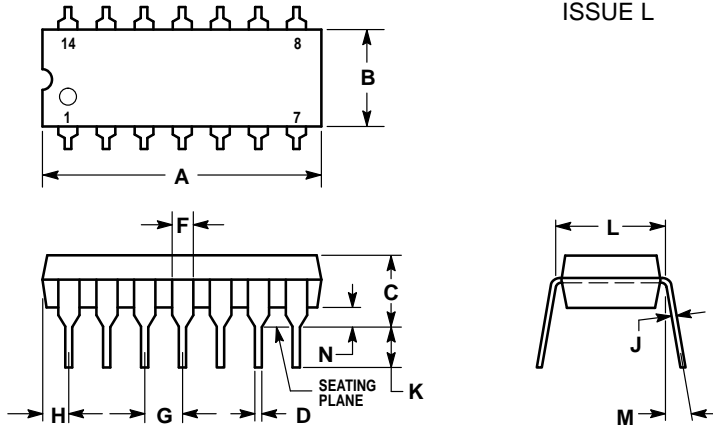


**NOTES:**

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. DIMENSION L TO CENTER OF LEAD WHEN FORMED PARALLEL.
4. DIMENSION F MAY NARROW TO 0.76 (0.030) WHERE THE LEAD ENTERS THE CERAMIC BODY.

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.750	0.785	19.05	19.94
B	0.245	0.280	6.23	7.11
C	0.155	0.200	3.94	5.08
D	0.015	0.020	0.39	0.50
F	0.055	0.065	1.40	1.65
G	0.100 BSC		2.54 BSC	
J	0.008	0.015	0.21	0.38
K	0.125	0.170	3.18	4.31
L	0.300 BSC		7.62 BSC	
M	0° 15°		0° 15°	
N	0.020	0.040	0.51	1.01

### P SUFFIX PLASTIC DIP PACKAGE CASE 646-06 ISSUE L



**NOTES:**

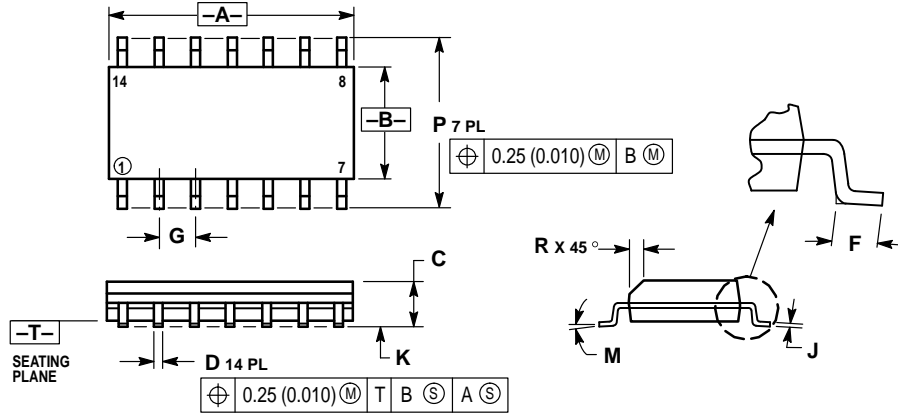
1. LEADS WITHIN 0.13 (0.005) RADIUS OF TRUE POSITION AT SEATING PLANE AT MAXIMUM MATERIAL CONDITION.
2. DIMENSION L TO CENTER OF LEADS WHEN FORMED PARALLEL.
3. DIMENSION B DOES NOT INCLUDE MOLD FLASH.
4. ROUNDED CORNERS OPTIONAL.

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.715	0.770	18.16	19.56
B	0.240	0.260	6.10	6.60
C	0.145	0.185	3.69	4.69
D	0.015	0.021	0.38	0.53
F	0.040	0.070	1.02	1.78
G	0.100 BSC		2.54 BSC	
H	0.052	0.095	1.32	2.41
J	0.008	0.015	0.20	0.38
K	0.115	0.135	2.92	3.43
L	0.300 BSC		7.62 BSC	
M	0° 10°		0° 10°	
N	0.015	0.039	0.39	1.01



## OUTLINE DIMENSIONS


### D SUFFIX PLASTIC SOIC PACKAGE CASE 751A-03 ISSUE F



**NOTES:**

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSIONS A AND B DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 (0.005) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	8.55	8.75	0.337	0.344
B	3.80	4.00	0.150	0.157
C	1.35	1.75	0.054	0.068
D	0.35	0.49	0.014	0.019
F	0.40	1.25	0.016	0.049
G	1.27 BSC		0.050 BSC	
J	0.19	0.25	0.008	0.009
K	0.10	0.25	0.004	0.009
M	0°	7°	0°	7°
P	5.80	6.20	0.228	0.244
R	0.25	0.50	0.010	0.019

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