FUJITSU SEMICONDUCTOR
DATA SHEET

DS04-13501-2E

LINEAR IC

R-2R TYPE 8-BIT D/A CONVERTER WITH OPERATIONAL AMPLIFIER OUTPUT BUFFERS

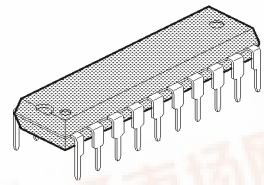
MB88346B

■ DESCRIPTION

The Fujitsu MB88346B is an R-2R type 8-bit resolution digital-to-analog converter (DAC), designed for interface with a wide range of general 4-bit and 8-bit microcontrollers including Fujitsu's MB88200 family, MB8850 family, and MB88500 family 4-bit single-chip microcontrollers.

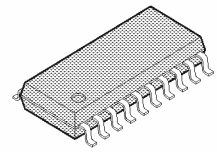
The MB88346B has an 8-bit x 12-channel D/A converter with operational amplifier output buffers. Digital data are input serially by individual channel units. The loaded digital data are converted into analog DC voltages by the D/A converter in 20 µs settling time. Also, the MB88346B has operational amplifier output buffers. These operational amplifier output buffers are connected to each channel of the D/A converter, and provide high current drive capability. The MB88346B is suitable for electronic volumes and replacement for potentiometers for adjustment, in addition to normal D/A converter applications.

MB88346B-P



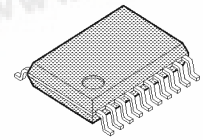
PLASTIC DIP
(DIP-20P-M02)

MB88346B-PF



PLASTIC SOP
(FPT-20P-M01)

MB88346B-PFV



PLASTIC SSOP
(FPT-20P-M03)

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields. However, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit.

■ FEATURES

- Conversion method : R-2R resistor ladder
- 8-bit x 12-channel D/A converter with operational amplifier output buffers
- Max. 2.5MHz Serial data input
- Serial data output for cascade connection
- Max. 20 µs DAC output settling time
- Max. +1.0/-1.0 mA analog output sink/source current
- Two separate power supply/ground lines for MCU interface block/ operational amplifier output buffer block and D/A converter block
- Pin compatible with MB88341
- Single +5V power supply
- Wide operating temperature range: -20°C to +85°C
- Silicon-gate CMOS process
- Three package options :
  20-pin plastic DIP (Suffix : -P), 20-pin plastic SOP (Suffix : -PF),
  20-pin plastic SSOP(Suffix : -PFV)

■ PIN ASSIGNMENT

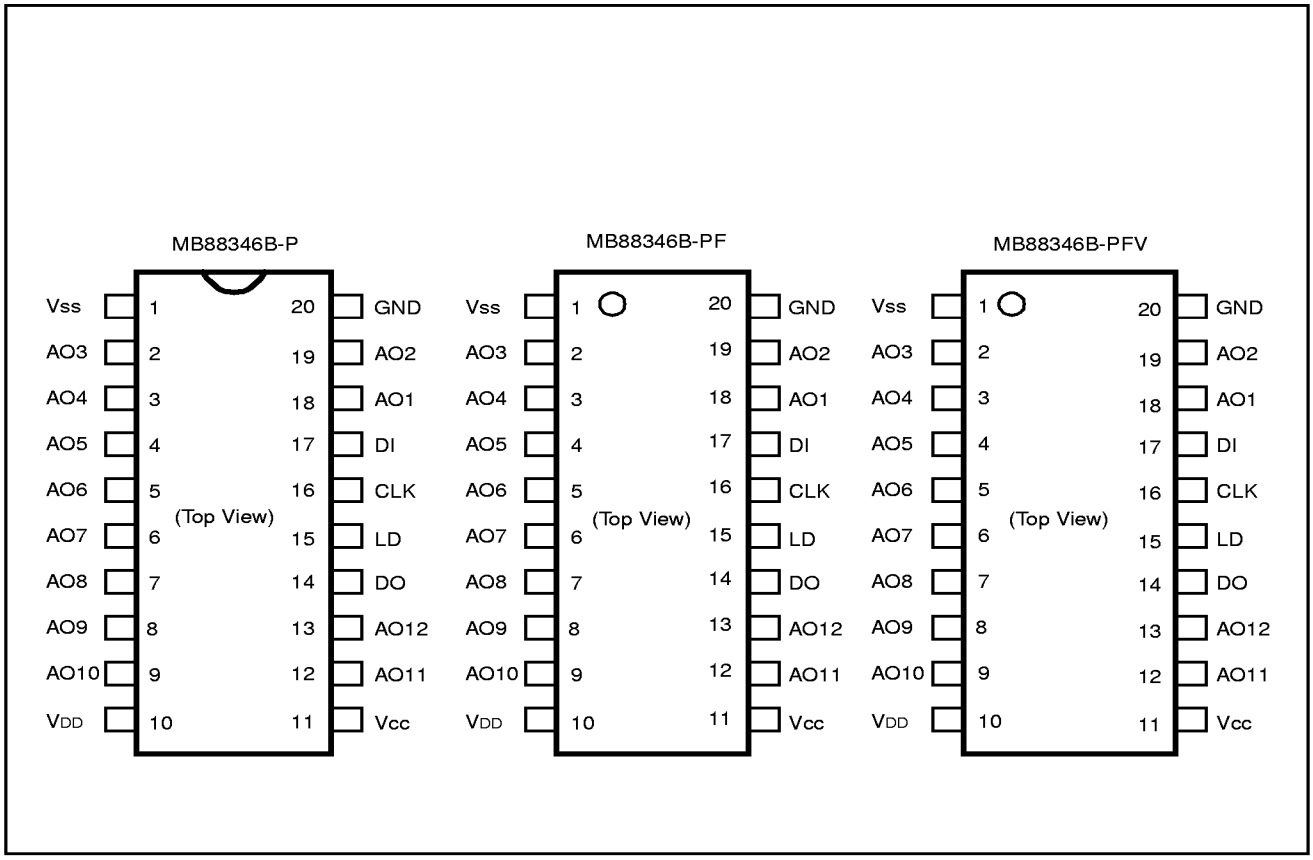
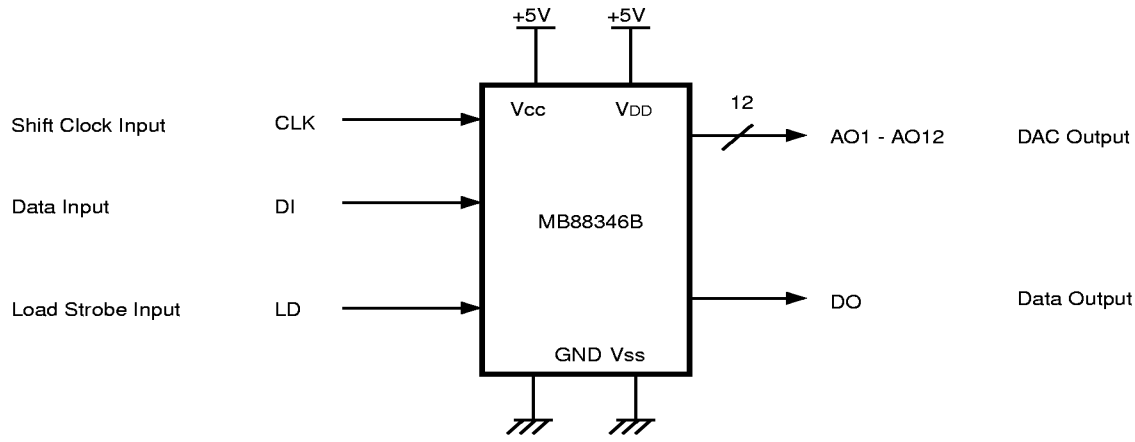
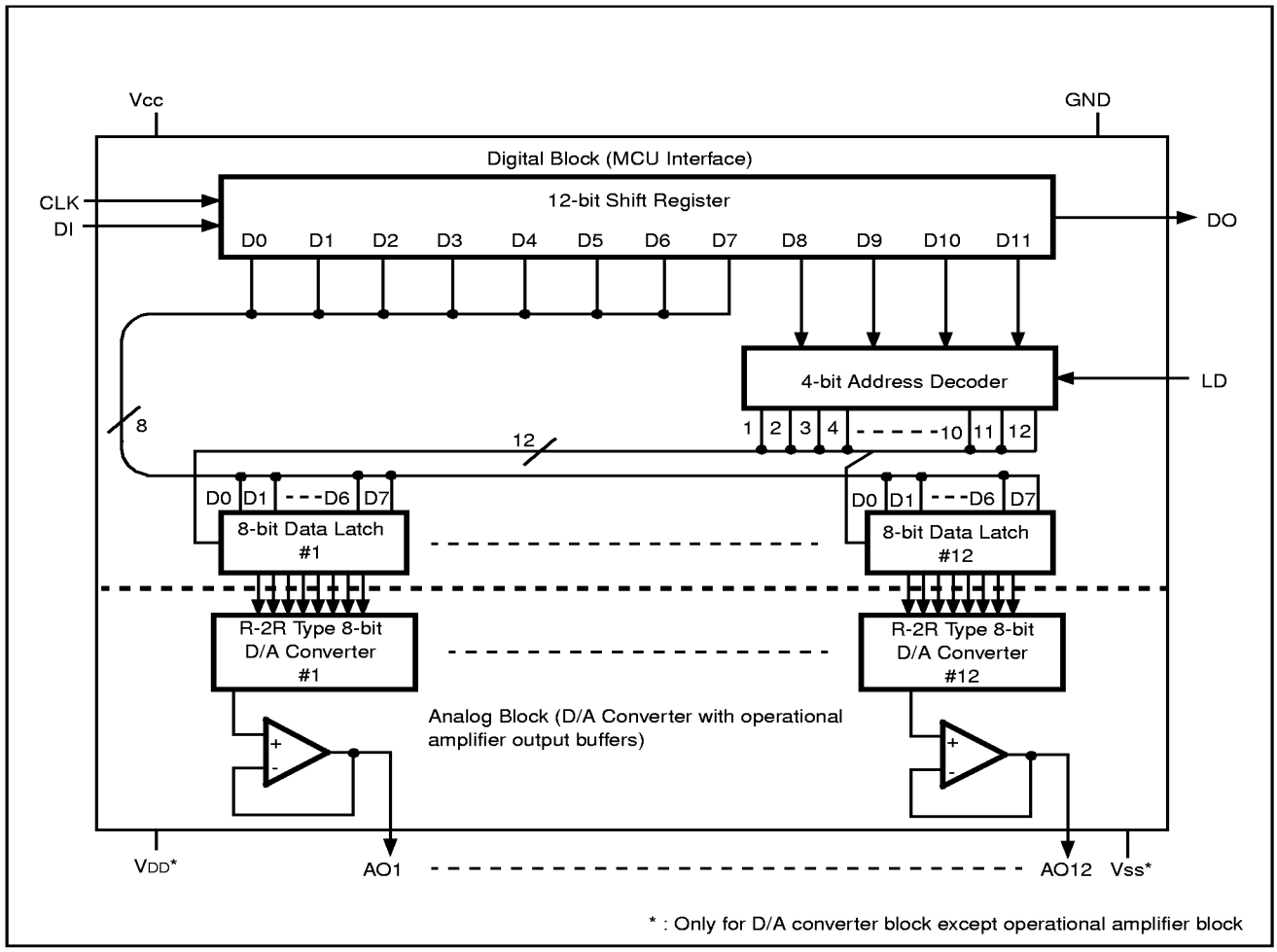


Figure 1 Logic Symbol



■ BLOCK DIAGRAM



■ PIN DESCRIPTION

PIN ASSIGNMENT and Tableshow the pin assignment and pin description of the MB88346B.

Table 1 Pin Description

Symbol	Pin No.	Type	Name & Function
Power Supply			
VCC	11	-	+5V DC power supply pin for the digital block (MCU interface) and operational amplifier output buffers.
GND	20	-	Ground pin for the digital block (MCU interface) and operational amplifier output buffers.
VDD	10	-	DC power supply pin for the analog block (D/A converter) except operational amplifier output buffers.
VSS	1	-	Ground pin for the analog block (D/A converter) except operational amplifier output buffers.
Control Input			
CLK	16	I	Shift clock input to the internal 12-bit shift register: At the rising edge of CLK data on the DI pin is shifted into the LSB of the shift register and contents of the shift register are shifted right (to the MSB).
LD	15	I	Load strobe input for a 12-bit address/data : A high level on the LD pin latches a 4-bit address (upper 4 bits: D11 to D8) of the internal 12-bit shift register into the internal address decoder, and writes 8-bit data (lower 8 bits: D7 to D0) of the shift register into an internal data latch selected by the latched address.
Data Input/Output			
DI	17	I	Serial address/data input to the internal 12-bit shift register: The address/data format is that upper 4 bits (D11 to D8) indicate an address and lower 8 bits (D7 to D0) indicate data. The D11 (MSB) is the first-in bit and D0 (LSB) is the last-in bit.
DO	14	O	Serial address/data output from the internal 12-bit shift register: This is an output pin of the MSB bit data of the 12-bit shift register. This pin allows a cascade connection of the device.
DAC Output			
AO1 AO2 AO3 AO4 AO5 AO6 AO7 AO8 AO9 AO10 AO11 AO12	18 19 2 3 4 5 6 7 8 9 12 13	O	8-bit resolution D/A converter outputs : 12 channels of DAC outputs (AO1 to AO12) are provided. Each output channel has an operational amplifier output buffer for analog output data.

■ FUNCTIONAL DESCRIPTION

OVERVIEW

The MB88346B is an R-2R resistor ladder type, 8-bit resolution digital-to-analog converter (DAC) device. The MB88346B has 12 channels of D/A converters with operational amplifier output buffers. 8-bit digital data are loaded into internal data latches by individual DAC channel units. The loaded digital data are converted into analog DC voltages through the internal D/A converter in max. 20 µs settling time. And the analog DC voltages source/sink the output current through the operational amplifier output buffers. For cascade connection, a serial data output is provided.

DEVICE CONFIGURATION

As illustrated in BLOCK DIAGRAM, the MB88346B device is composed by the digital block (MCU interface) and analog block (D/A converter with operational amplifier output buffers). The digital block consists of a 12-bit shift register, a 4-bit address decoder, and 12-channels of 8-bit data latches. The analog block includes 12 channels of 8-bit D/A converters with operational amplifier output buffers connecting to the data latches. For electrically stable operation the power supply and ground lines are separate between the digital block (MCU interface) and operational amplifier output buffers, and analog block except operational amplifier output buffers.

DEVICE OPERATION

Figure 2 shows the input/output timing. A 12-bit address/data is serially input into the shift register through the DI pin synchronously with the rising edge of CLK. The format of the shift register is shown in Figure 3. The lower 8 bits (D7 to D0) are data bits to be converted, and the upper 4 bits are address bits (D11 to D8) to select a data latch to be written. A high level on the LD pin loads the address decoder with the 4-bit address to select a data latch, and writes the 8-bit data into a selected data latch. Figure 4 shows the data latch address map, and Table, address decoding. 8-bit data written into individual data latches are converted into analog DC voltages, dividing the supply voltage |V_{DD}-Vss| through R-2R resistor ladders of D/A converters. The operational amplifier output buffers at individual D/A converter outputs can source up to 1.0 mA of the output current. Figure 5 shows a configuration of the R-2R resistor ladder D/A converter with operational amplifier, and Table 3analog DC voltages corresponding to each digital data.

Figure 2 Input/Output Timing

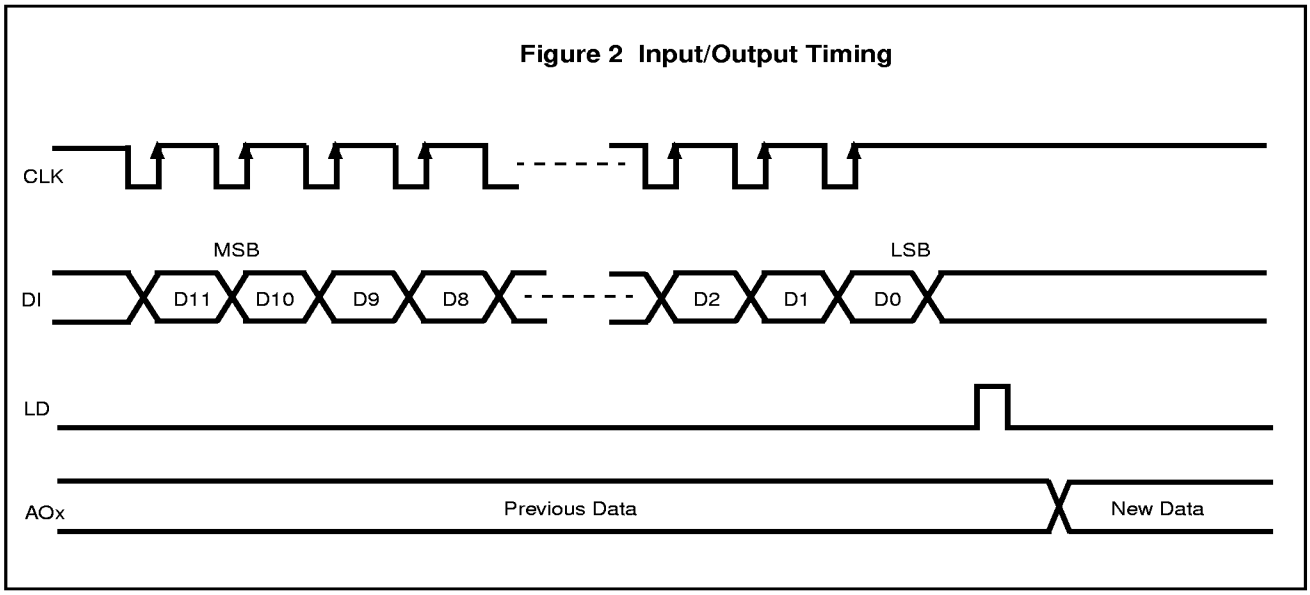


Figure 3 Shift Register Format

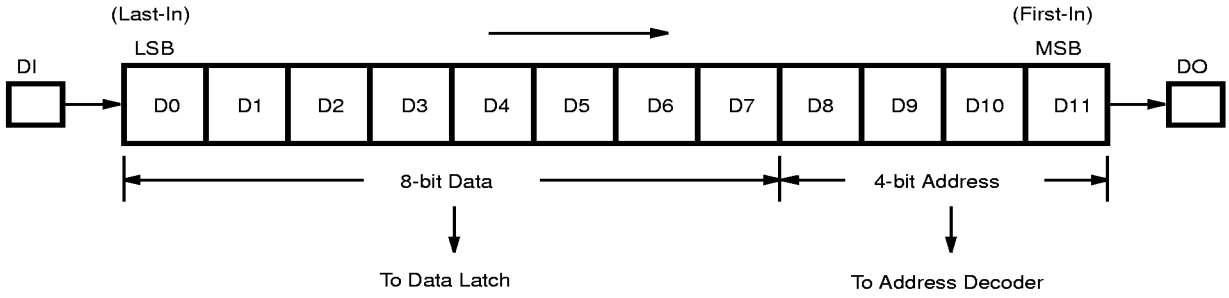


Figure 4 Data Latch Address Map

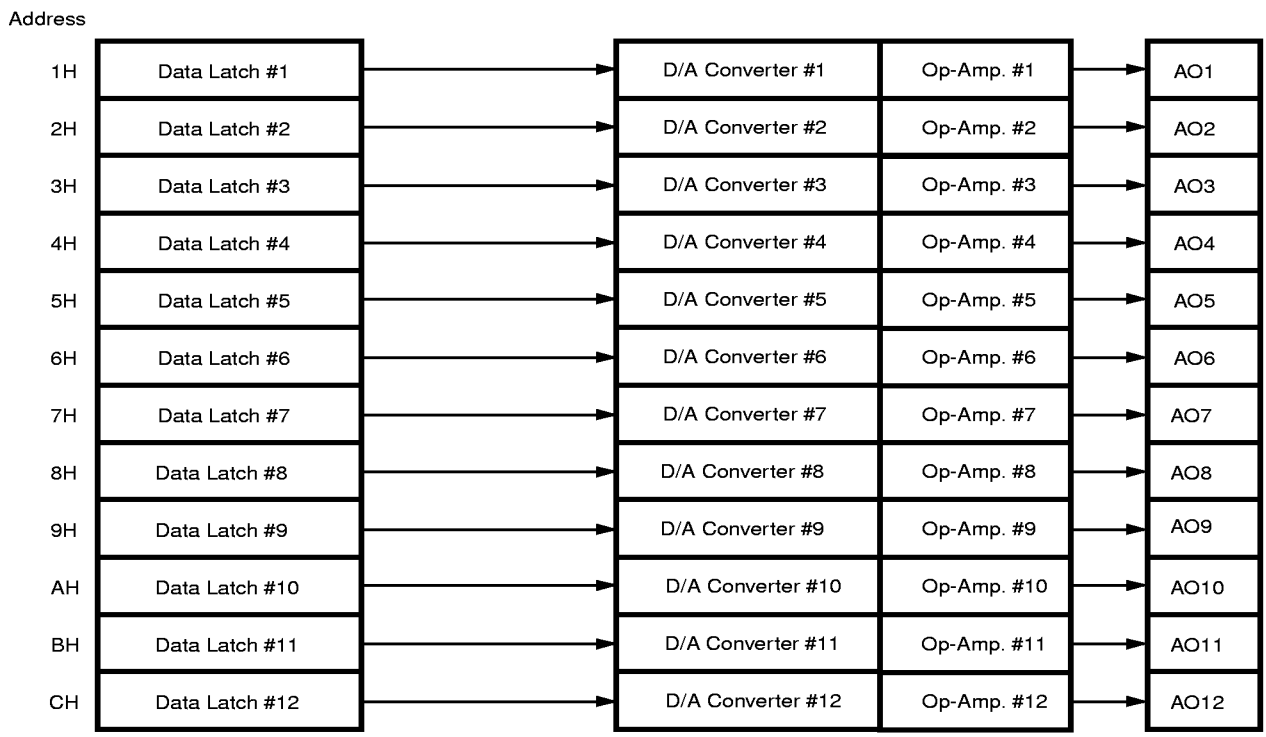
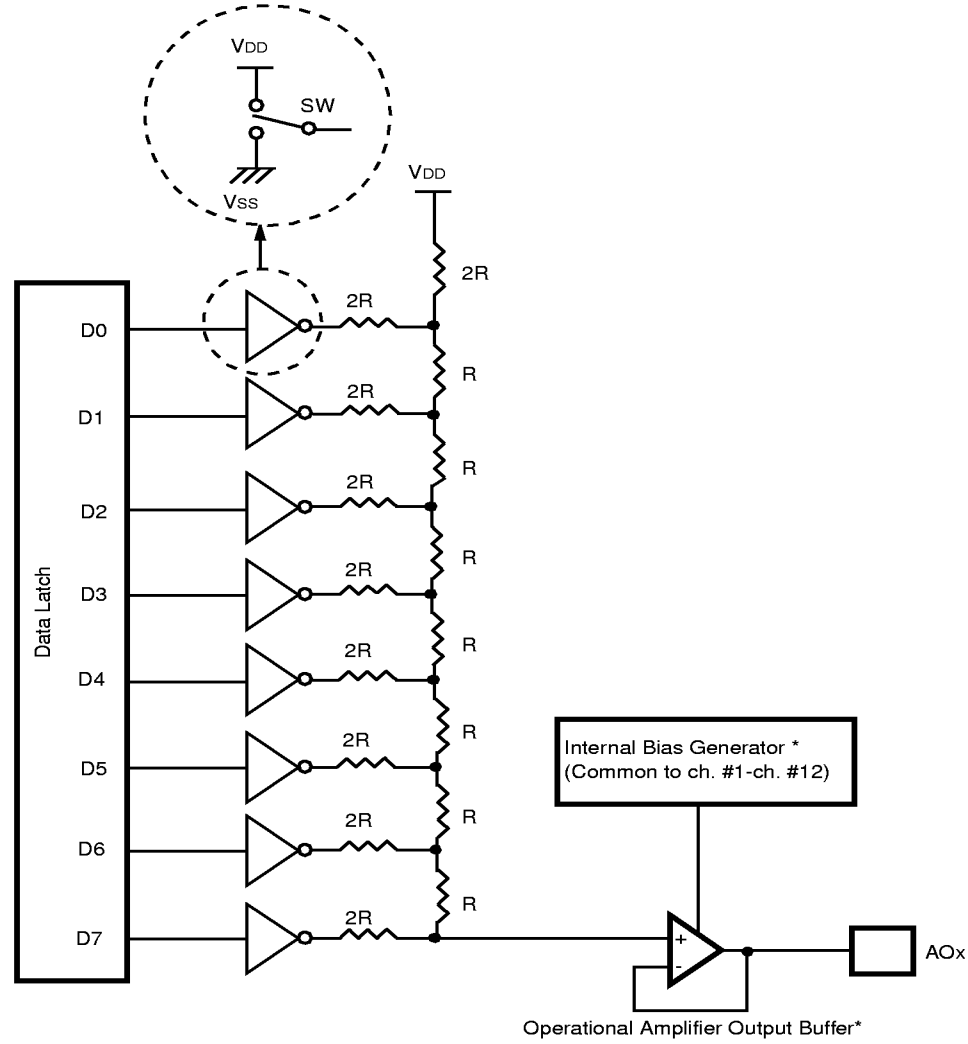


Figure 5 Configuration of R-2R Resistor Ladder D/A Converter



* : Powered/grounded by the VCC and GND pins.

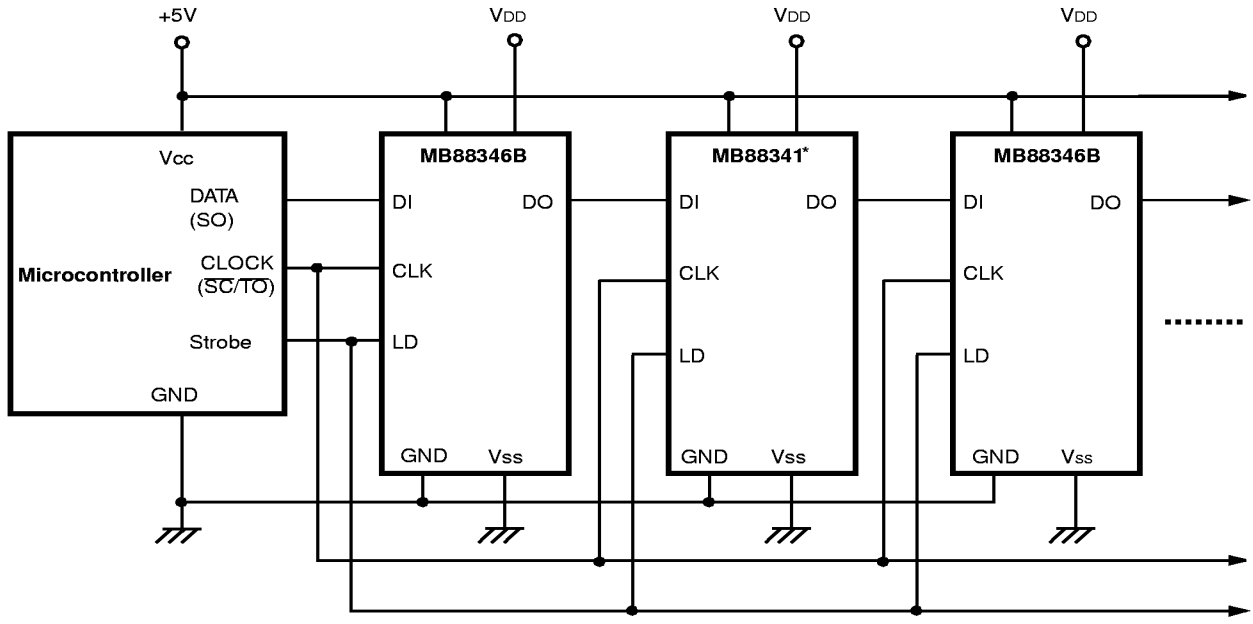
Table 2 Address Decoding

Address				Data Latch Selected
D8	D9	D10	D11	MB88346B
0	0	0	0	Deselected
0	0	0	1	Data Latch #1
0	0	1	0	Data Latch #2
0	0	1	1	Data Latch #3
0	1	0	0	Data Latch #4
0	1	0	1	Data Latch #5
0	1	1	0	Data Latch #6
0	1	1	1	Data Latch #7
1	0	0	0	Data Latch #8
1	0	0	1	Data Latch #9
1	0	1	0	Data Latch #10
1	0	1	1	Data Latch #11
1	1	0	0	Data Latch #12
1	1	0	1	Deselected
1	1	1	0	Deselected
1	1	1	1	Deselected

Table 3 Data Conversion

Data								DAC Output Level
D7	D6	D5	D4	D3	D2	D1	D0	AOx
0	0	0	0	0	0	0	0	≈ V_{SS}
0	0	0	0	0	0	0	1	≈ (V_{DD}-V_{SS}) x 1/255 + V_{SS}
0	0	0	0	0	0	1	0	≈ (V_{DD}-V_{SS}) x 2/255 + V_{SS}
0	0	0	0	0	0	1	1	≈ (V_{DD}-V_{SS}) x 3/255 + V_{SS}
⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮
1	1	1	1	1	1	1	0	≈ (V_{DD}-V_{SS}) x 254/255 + V_{SS}
1	1	1	1	1	1	1	1	≈ V_{DD}

Figure 6 Cascade Connection Example

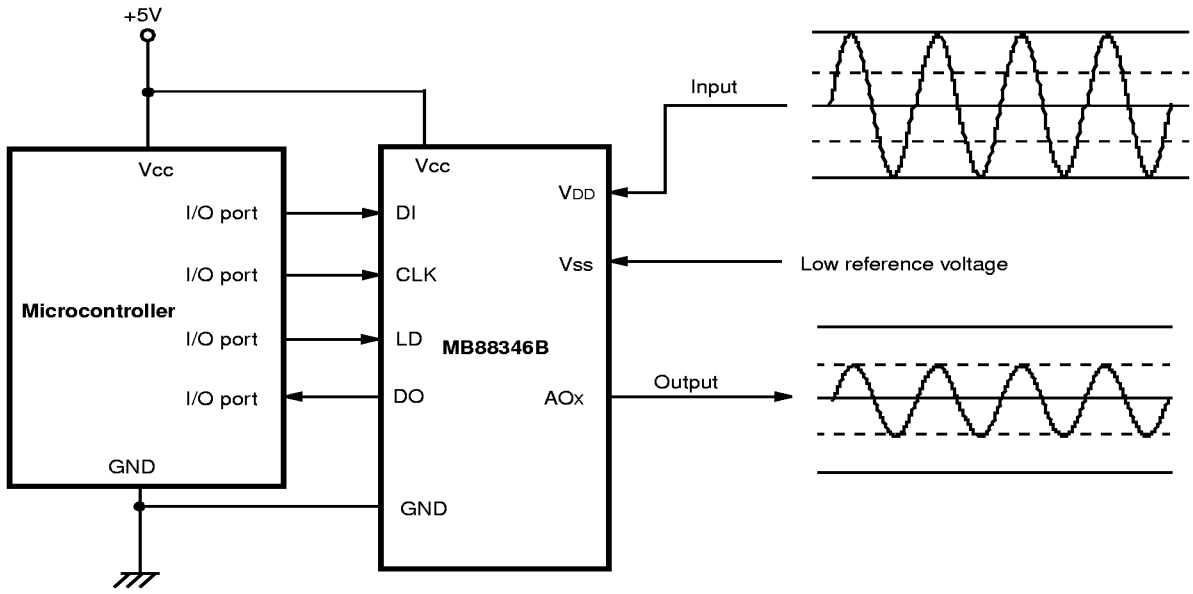


* : MB88346B can be used mixed with MB88341.

■ APPLICATION DESCRIPTION

The MB88346B is suitable for electronic volumes and replacement for adjustment potentiometers, in addition to normal D/A converter applications. Figure 7 illustrates application example for a gain control.

Figure 7 Application Example - Gain Control



■ ELECTRICAL CHARACTERISTICS

ABSOLUTE MAXIMUM RATINGS (See NOTE)

Parameter	Symbol	Rating			Unit	Condition
		Min	Typ	Max		
Supply Voltage	V_{CC}	-0.3	-	7.0	V	Ta = +25°C GND = 0 V $V_{DD} \leq V_{CC}$,
	V_{DD}	-0.3	-	7.0	V	
Input Voltage	V_{IN}	-0.3	-	Vcc+0.3	V	Ta = +25°C GND = 0 V
Output Voltage	V_{OUT}	-0.3	-	Vcc+0.3	V	
Power Dissipation	P_D	-	-	250	mW	
Operating Ambient Temperature	Ta	-20	-	+85	°C	
Storage Temperature	T_{STG}	-55	-	+150	°C	

NOTE : Permanent device damage may occur if the above ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Value			Unit	Condition
		Min	Typ	Max		
Supply Voltage (for MCU Interface/Op.-Amp. Block)	V_{CC}	4.5	5.0	5.5	V	$V_{CC} \geq V_{DD}$
	GND	-	0	-	V	
Supply Voltage (for Analog Block*)	V_{CC}	2.0	-	V_{CC}	V	V_{DD}-$V_{SS} \geq 2.0V$
	V_{SS}	GND	-	V_{CC}-2.0	V	
Analog Output Source Current	I_{AL}	-	-	+1.0	mA	
Analog Output Sink Current	I_{AH}	-	-	+1.0	mA	
Analog Output Load Capacitance for oscillation limit	C_{AL}	-	-	1.0	µF	
Operating Ambient Temperature	Ta	-20	-	+85	°C	

* : Except operational amplifier output buffer block

■ DC CHARACTERISTICS

(Recommended operating conditions unless otherwise noted.)

Digital Block (MCU Interface)

Parameter	Symbol	Value			Unit	Condition
		Min	Typ	Max		
Active Supply Current (V_{CC}) *	I_{CC}	-	2.5	4.5	mA	CLK = 1MHz, Unloaded
Input Leakage Current (CLK, DI, and LD)	I_{ILK}	-10	-	+10	µA	V_{IN} = 0 to Vcc
Input Low Voltage (CLK, DI, and LD)	V_{IL}	-	-	0.2•Vcc	V	
Input High Voltage (CLK, DI, and LD)	V_{IH}	0.5•Vcc	-	-	V	
Output Low Voltage (DO)	V_{OL}	-	-	0.4	V	I_{OL} = 2.5 mA
Output High Voltage (DO)	V_{OH}	Vcc-0.4	-	-	V	I_{OH} = -400 µA

* : Including the supply current to the operational amplifier block

Analog Block (D/A Converters with Operational Amplifier Output Buffers)

Parameter	Symbol	Value			Unit	Condition
		Min	Typ	Max		
Supply Current (V_{DD}) **	I_{DD}	-	0.2	0.5	mA	Unloaded
Min. Analog Output Voltage 1 (AO_X)	V_{AOL1}	V_{SS}	-	V_{SS}+0.1	V	V_{DD}=Vcc, V_{SS}=GND=0V Unloaded, Didital Data=#00
Min. Analog Output Voltage 2 (AO_X)	V_{AOL2}	V_{SS}-0.2	V_{SS}	V_{SS}+0.2	V	V_{DD}=Vcc=5.0V, V_{SS}=GND=0V I_{AL}=+500µA, Digital Data=#00
Min. Analog Output Voltage 3 (AO_X)	V_{AOL3}	V_{SS}	-	V_{SS}+0.2	V	V_{DD}=Vcc=5.0V, V_{SS}=GND=0V I_{AH}=+500µA, Digital Data=#00
Min. Analog Output Voltage 4 (AO_X)	V_{AOL4}	V_{SS}-0.3	V_{SS}	V_{SS}+0.3	V	V_{DD}=Vcc=5.0V, V_{SS}=GND=0V I_{AL}=+1.0mA, Digital Data=#00
Min. Analog Output Voltage 5 (AO_X)	V_{AOL5}	V_{SS}	-	V_{SS}+0.3	V	V_{DD}=Vcc=5.0V, V_{SS}=GND=0V I_{AH}=+1.0mA, Digital Data=#00
Max. Analog Output Voltage 1 (AO_X)	V_{AOH1}	V_{DD}-0.1	-	V_{DD}	V	V_{DD}=Vcc, V_{SS}=GND=0V Unloaded, Digital Data=#FF
Max. Analog Output Voltage 2 (AO_X)	V_{AOH2}	V_{DD}-0.2	-	V_{DD}	V	V_{DD}=Vcc=5.0V, V_{SS}=GND=0V I_{AL}=+500µA, Digital Data=#FF
Max. Analog Output Voltage 3 (AO_X)	V_{AOH3}	V_{DD}-0.2	V_{DD}	V_{DD}+0.2	V	V_{DD}=Vcc=5.0V, V_{SS}=GND=0V I_{AH}=+500µA, Digital Data=#FF

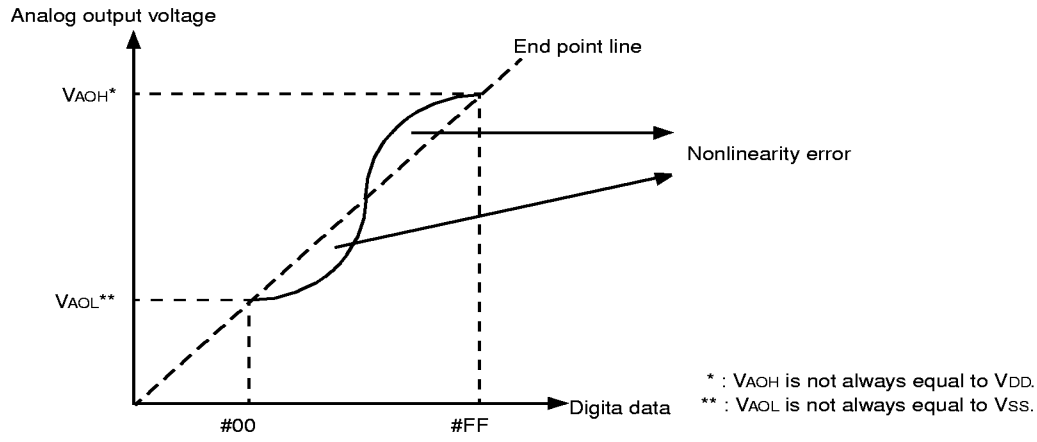
** : Excluding the supply current to the operational amplifier block

Analog Block (D/A Converters with Operational Amplifier Output Buffers) - Continued

Parameter	Symbol	Value			Unit	Condition
		Min	Typ	Max		
Max. Analog Output Voltage 4 (AOx)	V_{AOH4}	V_{DD}-0.3	-	V_{DD}	V	V_{DD}=Vcc=5V, V_{SS}=GND=0V, I_{AL}=+1.0mA, Digital Data=#FF
Max. Analog Output Voltage 5 (AOx)	V_{AOH5}	V_{DD}-0.3	V_{DD}	V_{DD}+0.3	V	V_{DD}=Vcc=5V, V_{SS}=GND=0V, I_{AH}=+1.0mA, Digital Data=#FF
Resolution (AOx)	Res	-	8	-	bit	Monotonicity
Differential Error* (AOx)	DE	-1.0	0	+1.0	LSB	Unloaded, V_{DD}≤Vcc-0.1V, V_{SS}≥0.1V
Nonlinearity Error** (AOx)	LE	-1.5	0	+1.5	LSB	Unloaded, V_{DD}≤Vcc-0.1V, V_{SS}≥0.1V, See Figure 8.

* : The difference from the ideal increment value when the digital data is increased by 1 bit.
** : The difference between the input-output curve for the straight line (ideal line) that connects the output voltage of the channel when #00 is set, and the output voltage when #FF is set.

Figure 8 Definition of Nonlinearity Error



■ AC CHARACTERISTICS

(Recommended operating conditions unless otherwise noted.)

Parameter	Symbol	Value		Unit	Condition
		Min	Max		
Clock Low Time	t_{CLK}	200	-	ns	
Clock High Time	t_{CKH}	200	-	ns	
Clock Rise Time	t_{Cr}	-	200	ns	
Clock Fall Time	t_{Cf}	-	200	ns	
Data Setup Time	t_{DCH}	30	-	ns	
Data Hold Time	t_{CHD}	60	-	ns	
Load Strobe High Time	t_{LDH}	100	-	ns	
Load Strobe Setup Time	t_{CHL}	200	-	ns	
Load Strobe Hold Time	t_{LDC}	100	-	ns	
DAC Output Settling Time	t_{LDD}	-	20	µs	*R_{AL} = 10 kΩ , C_{AL} = 50 pF
Data Output Delay Time	t_{DO}	70	350	ns	**C_L = 20 pF (Min.), 100 pF (Max.)

Figure 9 AC Test Conditions

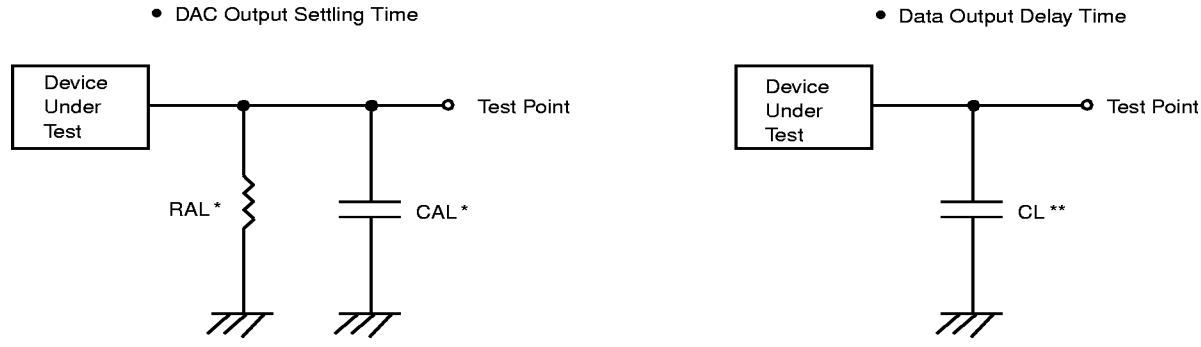


Figure 10 Input/Output Timing

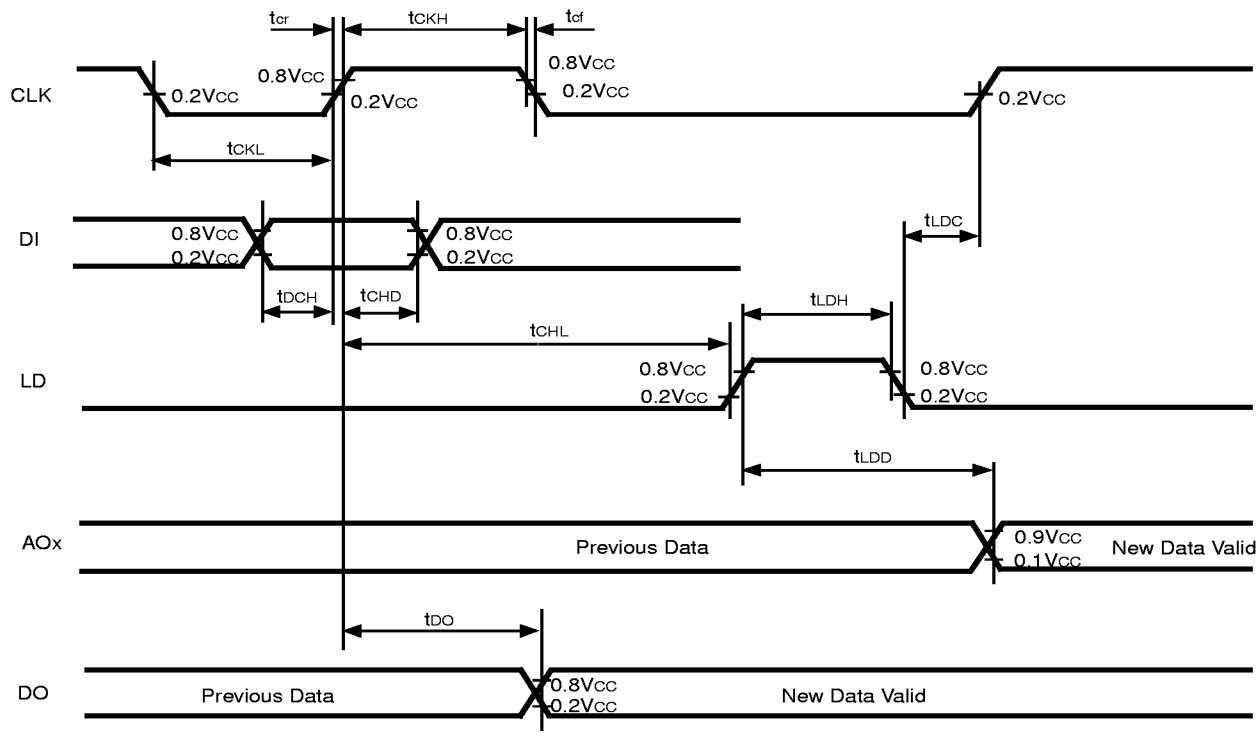
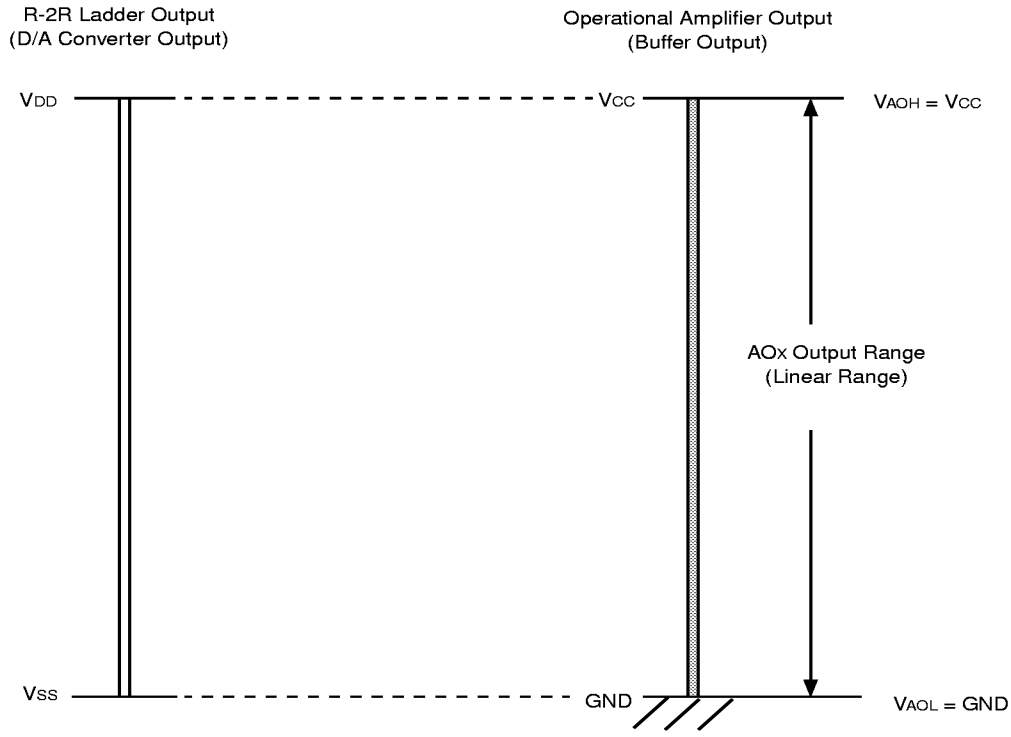


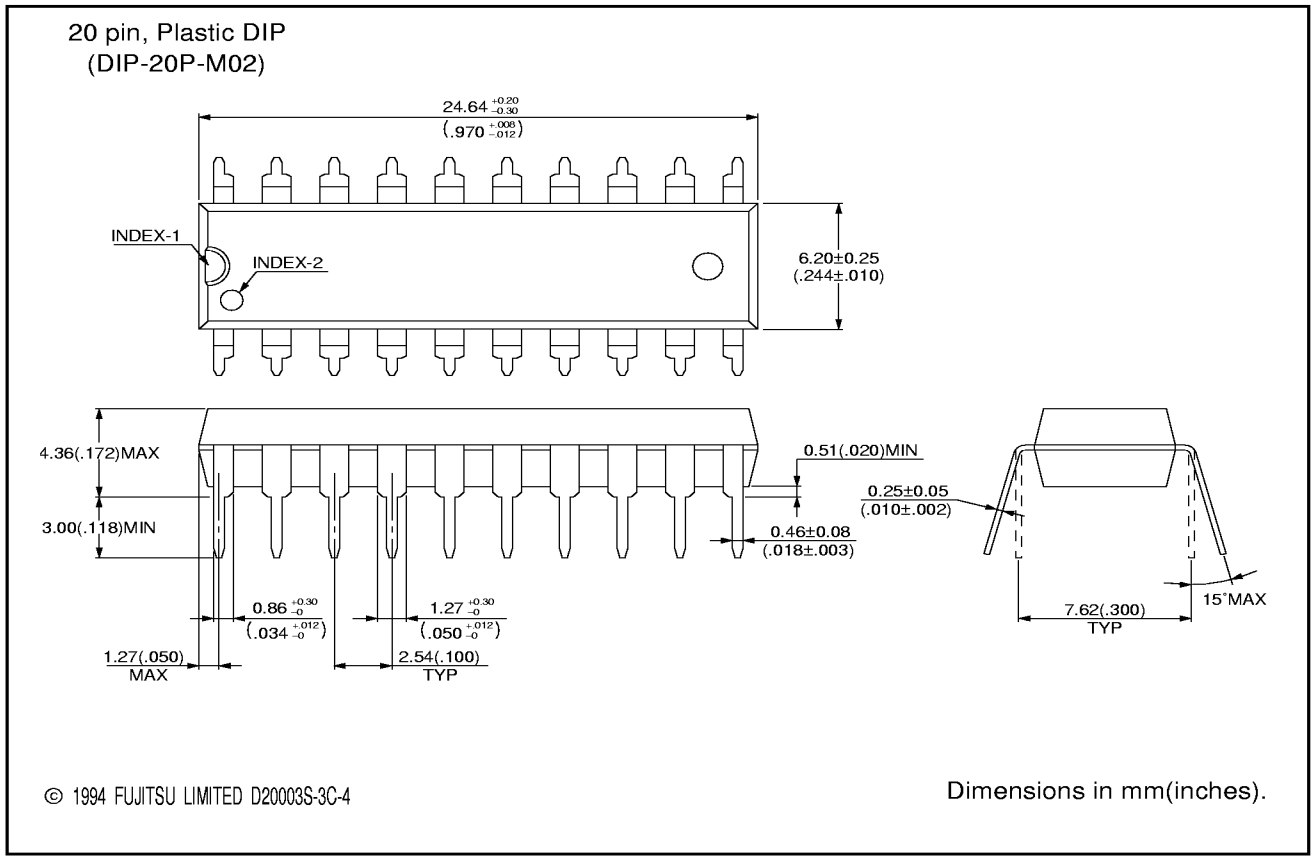
Figure 11 Analog Output Voltage Range



Notes: V_{DD}=V_{CC}
V_{SS}=GND

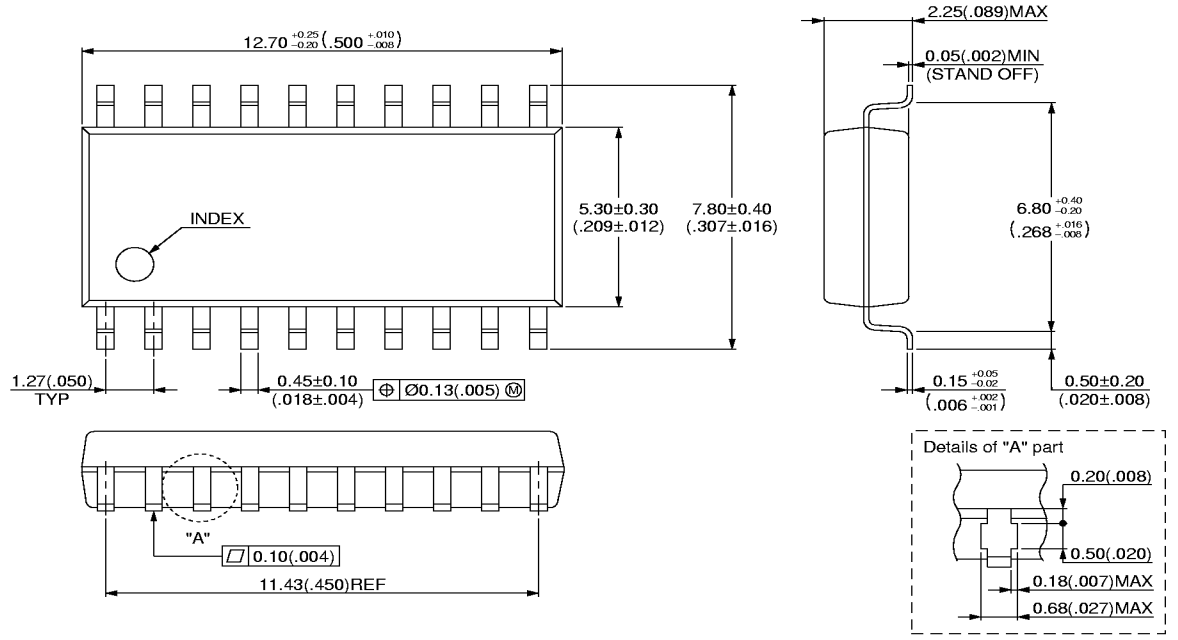
■ PACKAGE DIMENSIONS

MB88346B-P



MB88346B-PF

20 pin, Plastic SOP
(FPT 20P-M01)



Dimensions in mm(inches).

MB88346B-PFV