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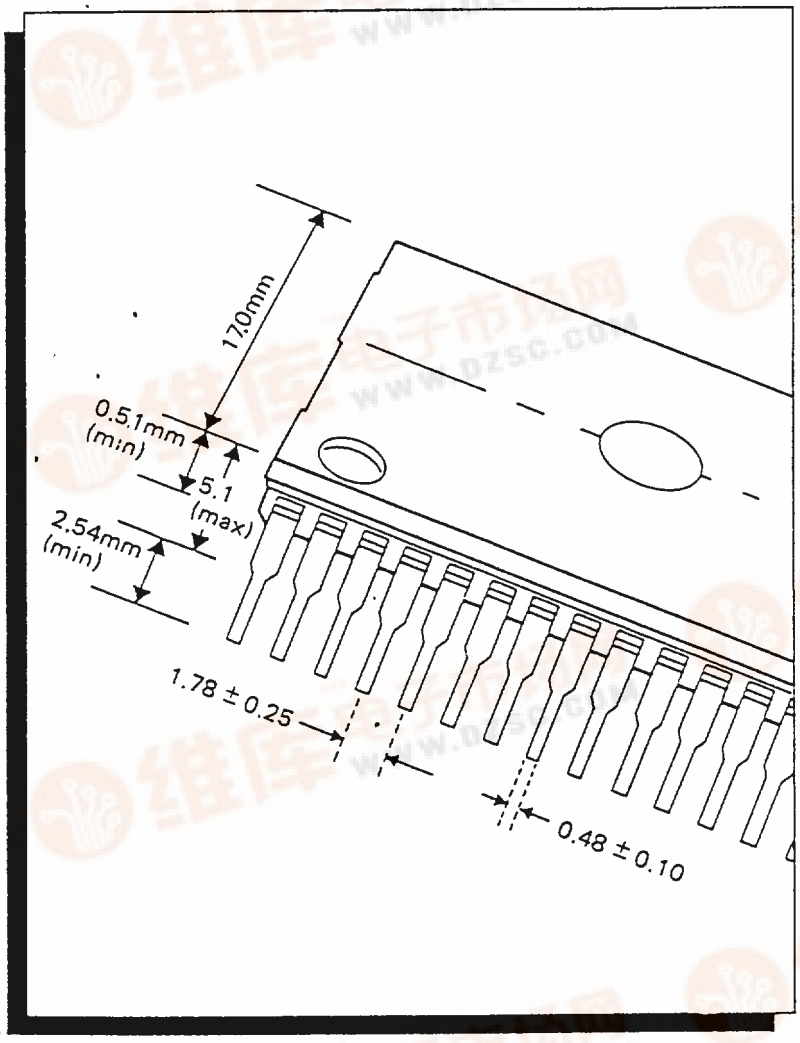
HD64180 FAMILY

HIGH-INTEGRATION CMOS MICROCONTROLLERS



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HD64180 - INNOVATION WITH EXPERIENCE

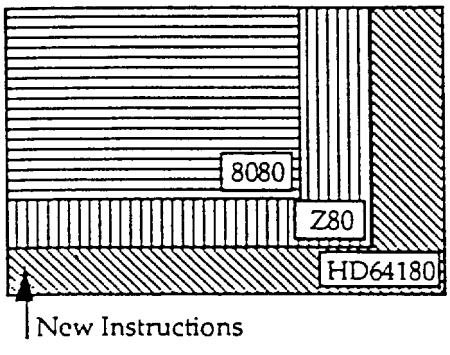
Are you looking for new ways of further improving your production or perhaps starting to consider ideas for an entirely new product range? Either way the choice of the ideal microprocessor for your application can be difficult.

It is likely you already have considerable expertise in both hardware and software techniques which are specific to your field. However, with advances in semiconductor technology seeming to make yesterday's devices obsolete, how is your investment in established areas still going to be an asset?

Since its introduction, the HD64180 microprocessor from Hitachi based upon state-of-the-art 1.3µm CMOS technology, has made a major contribution to solving this dilemma since :

- it is upwardly compatible with existing 8-bit industry standard software
- the combination of a powerful processor and advanced peripherals on a single chip, enable the 64180 to provide very high system performance

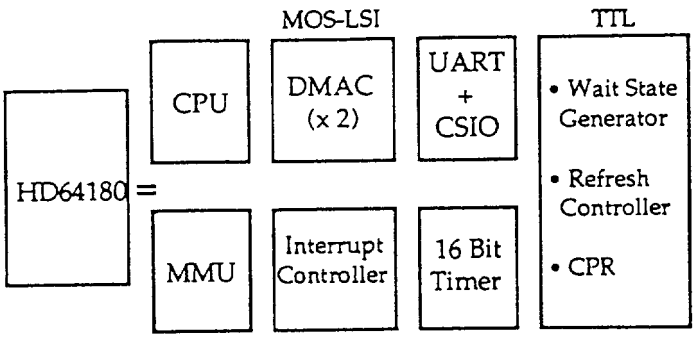
Software Compatibility



The 64180 is upwardly compatible with Z80, 8080, 8085 and NSC 800 instruction set.

It incorporates 12 new instructions which provide increased processing efficiency together with low power operation modes.

Peripheral Integration



Hitachi advanced CMOS technology has made available a level of peripheral integration which would not have previously been considered possible.

The block diagram above shows the equivalent chip count required to match the features incorporated in the 64180.

Building upon the success of the original device the HD64180R0, a family of devices are now available which increase further the range of potential applications for the HD64180.

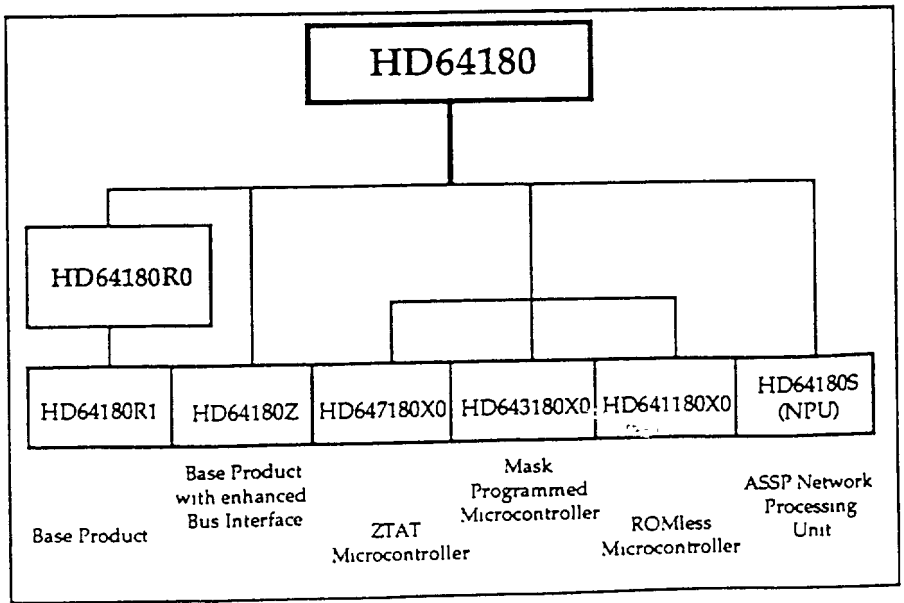
The range includes ROMless microprocessors, microcontrollers with EPROM, ZTAT one time programmable and mask programmed variants.

ZTAT stands for Zero Turn Around Time and the CMOS EPROM on-chip can bring many advantages to product development and marketing.

The latest addition to the 64180 family is the Network Processing Unit (NPU). The NPU is the newest innovation for the 64180 family. It is a cell based application-specific standard product designed for all networking and communications oriented applications.

Put all this together with a variety of powerful development support tools, high level language compilers and cross assemblers from both Hitachi and 3rd party suppliers, the HD64180 family is sure to be the right choice for today and tomorrow!

The Family Group



- HD64180R1

The R1 mask is the base member of the family and is a fully upward compatible replacement for the original HD64180R0.

- HD64180Z

The Z mask has almost identical features as the R1 plus the ability to interface more simply to '80' family peripherals.

- HD64180X

The X combines the basic 180 features with the addition of on-chip EPROM, RAM and I/O facilities which make it an ideal candidate for a minimum component solution.

- HD643180X

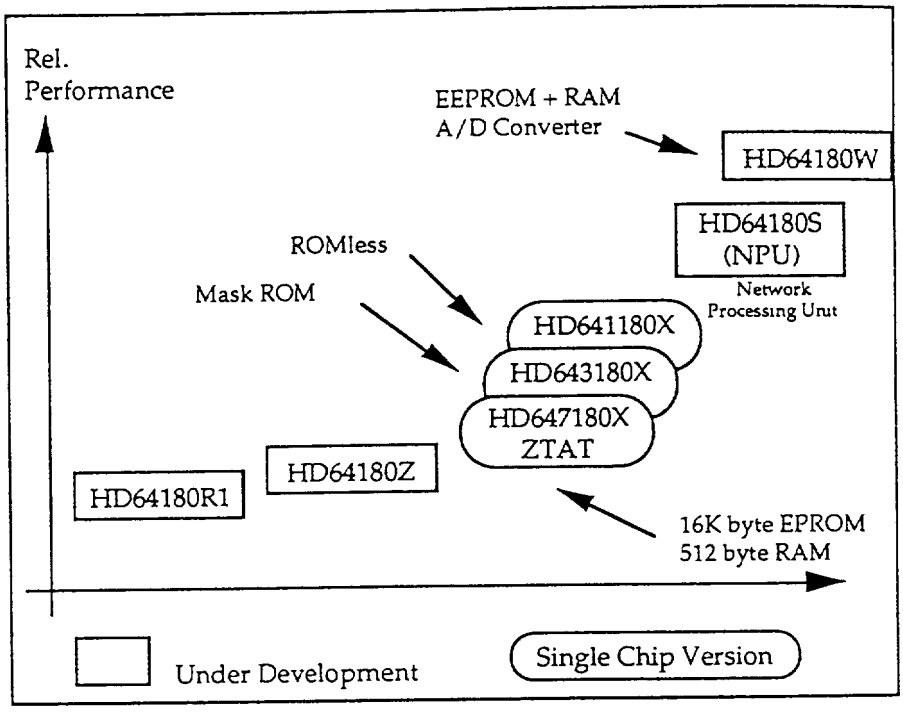
This device is equivalent to the 647180X but its on-chip program memory is of the mask programmed type.

- HD641180X

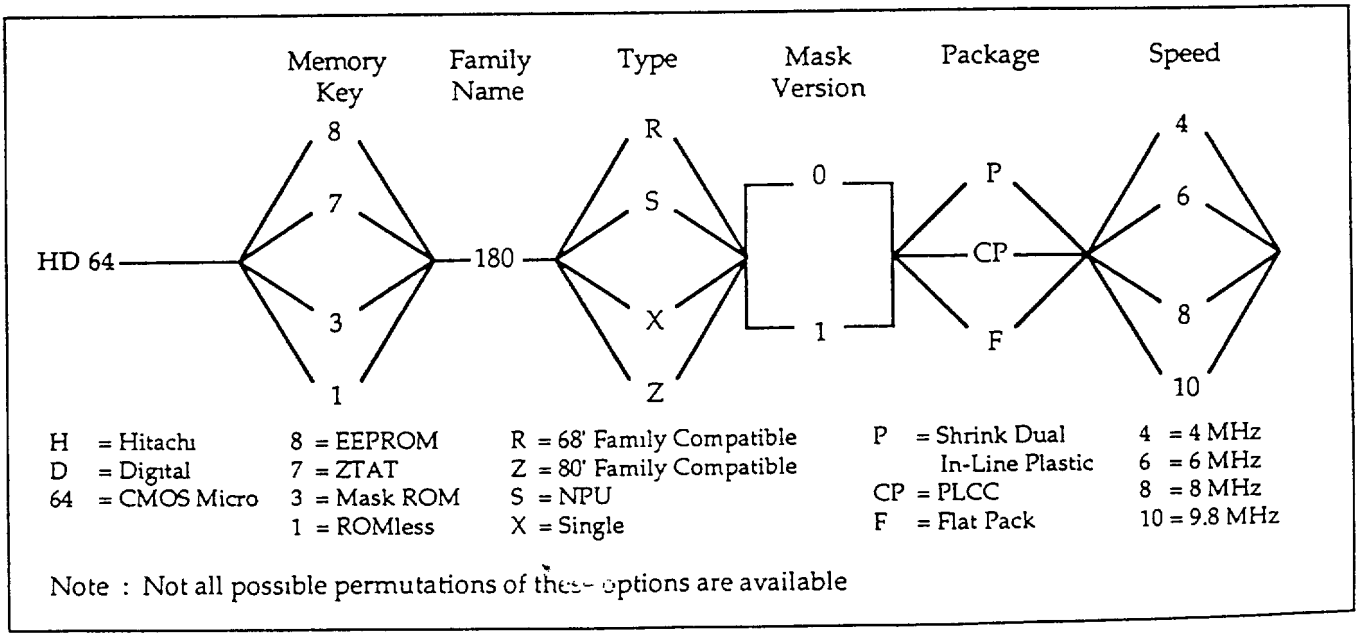
The HD641180X provides the same facilities as the HD647180X and HD643180X in a ROMless form.

- HD64180S

The HD64180S Network Processing Unit is a ROMless device that features a multiprotocol serial interface which can support many industry standard communications protocols.



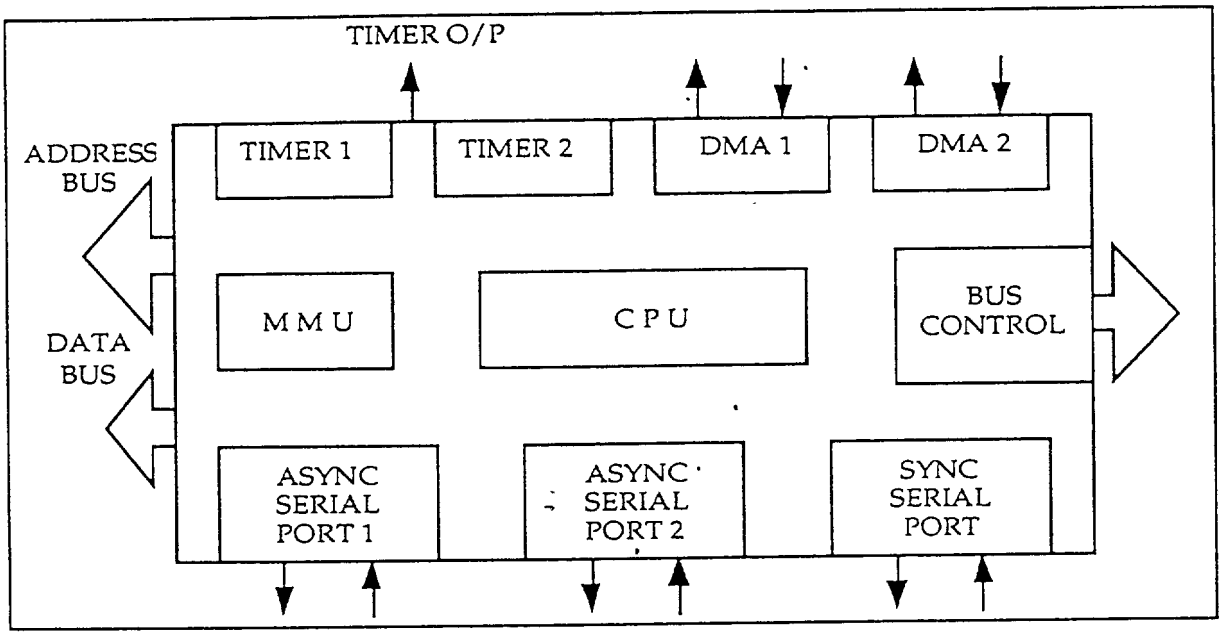
HD64180 Series Evolution



HD64180 Microprocessor Variants

HD64180 - A SYSTEM ON A CHIP

Based upon a microcoded execution unit and advanced CMOS technology, the 64180 is an 8-bit CPU which provides the benefits of high performance, reduced system costs and low power operation while maintaining compatibility with the large base of industry standard 8-bit software. Performance is improved by virtue of high operating frequency, pipelining, enhanced instruction set and integrated memory management unit (MMU) with up to 1M bytes physical memory address space. Low power consumption during normal CPU operation is supplemented by three specific software controlled low power standby modes. When combined with CMOS VLSI memories and peripherals, the 64180 is ideal in system applications requiring high performance, battery powered operation and standard software compatibility.



64180R1/Z Block Diagram

THE HD64180R1 AND HD64180Z

The HD64180R1 is the base member of the 64180 family. It includes the high performance CPU which is shared by all 64180 family members.

Hardware Features - High Performance, High Integration CPU

1) Operating frequency to 10MHz
2) On-chip MMU supports up to 1M bytes Memory and 64k bytes I/O Address Space
3) Two channel DMAC with Memory-Memory, Memory I/O and Memory-Memory Mapped I/O Transfer capability
4) WAIT input and Wait State [illegible] Memory [illegible]
5) Programmable Dynamic RAM Refresh Addressing and Timing
6) Two channel, full Duplex Asynchronous Serial Communication Interface (ASCI) wih programmable Baud Rate Generator and Modem Control Handshake Signals
7) Clock Serial I/O Port (CSI/O) with high speed operation (200k bits / second at 4MHz)
8) Two channel 16-bit Programmable Reload Timer (PRT) for Counting, Timing and Output Waveform Generation
9) Versatile Interrupt Controller manages four external and eight internal interrupt sources
10) On-chip Clock Generator

Software Features - Enhanced 8-bit Software Architecture

1) Fully compatible with CP/M-80™, CP/M Plus™ and existing systems and application sofware
2) Twelve new instructions including Multiply
3) On-chip I/O address relocation register for board level compatibility and existing systems and software
4) SLEEP instruction - IOSTOP mode and SYSTEM STOP mode for low power operation

Block Diagram

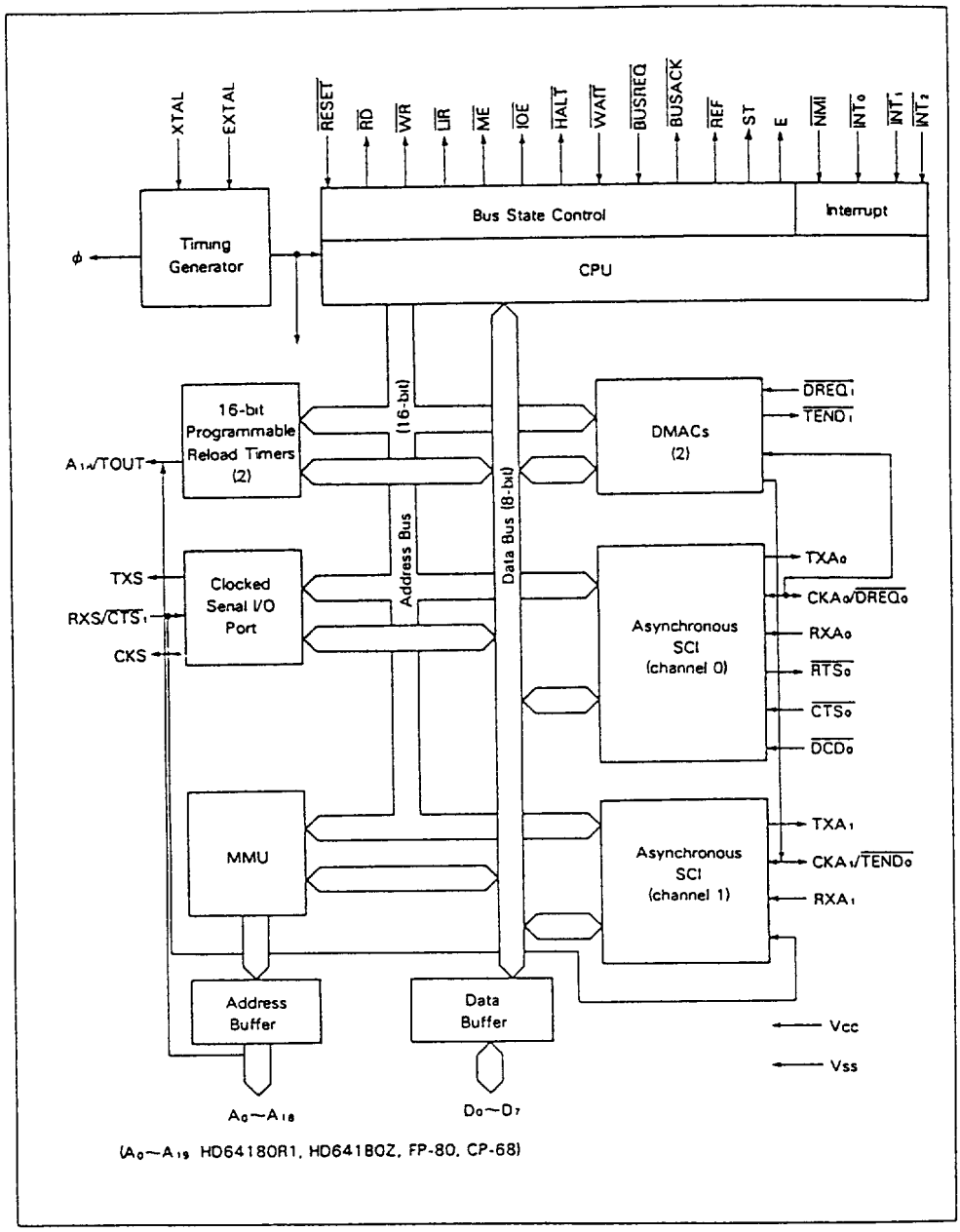


Figure 1.1.1 Block Diagram

HD64180Z - Extra Features :

The Z Mask of the 64180 family differs only slightly from the R1 base device. The HD64180Z includes an extra register which can be programmed to increase the flexibility of the device's bus interface. The main functions of this register are :

VLSI CMOS Process Technology

1) Low power operation

   75mW at at 6MHz
   45mW SLEEP Mode
   25mW IOSTOP Mode
   18mW SYSTEM STOP

2) Vcc = 5V ± 10%
   Fully TTL compatible

Note : CP/M-80 and CP/M Plus are registered trademarks of Digital Research, Inc.

1) To adjust bus timing to enable a simpler interface to various Z80* family peripherals

2) To enable an extra interrupt acknowledge cycle - this allows the HD64180Z to operate correctly with the daisy chained interrupt acknowledge scheme, employed by many Z80* family peripheral devices.

* Z80 is a trademark of Zilog Corp

ZTAT™ - EXPANDING PERFORMANCE FURTHER

What is ZTAT™?

ZTAT™ standard for Zero Turn Around Time. Hitachi's ZTAT microprocessors are powerful single chip devices which feature CMOS EPROM on-chip. Available in a low cost plastic package, the devices can be programmed by the user as they are electrically equivalent to standard EPROMs.

This combination of 'local' programming and a single chip makes available what is in fact a user-programable masked device.

What are the Advantages?

You want to sell equipment. We would also like you to be successful for obvious reasons and the unique advantages that ZTAT™ brings will help you be more successful by enabling :-

You get to market earlier :

Shorter development cycles means earlier availability of an innovative product in an eager market place. This means higher prices - there is less competition - and earlier cash flow.

You offer innovation :

By offering your customer an advantage.

- Portability - by use of low power CMOS technology
- Small size - by use of highly integrated single chip microcomputers and innovative packaging
- High performance - high speed processing
- Lower system cost - single chip CMOS devices in plastic packages allow smaller power supplies

You offer performance :

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additional peripheral items enable very powerful single chip designs to be produced utilising :

54 I/O Lines
16 Bit Timers
Analogue Comparator
] Enabling control and processing of real time events

HD647180X - 64180 ZTAT™ SPECIFICATION

The HD647180X is the first in a new family of processors which combines the existing benefits of the 64180 with the outstanding advantages of ZTAT technology.

As well as being fully software compatible with the other family members, the 647180 has additional hardware features over the existing devices.

Standard 64180 Features

- Asynchronous SCI (2 channels)
- Clocked Serial I/O
- MMU with 1M byte Address Capability
- DMAC (2 channels)
- Wait State Generator
- DRAM Refresh Controller
- 2 Channel 16-bit Reloadable Timer

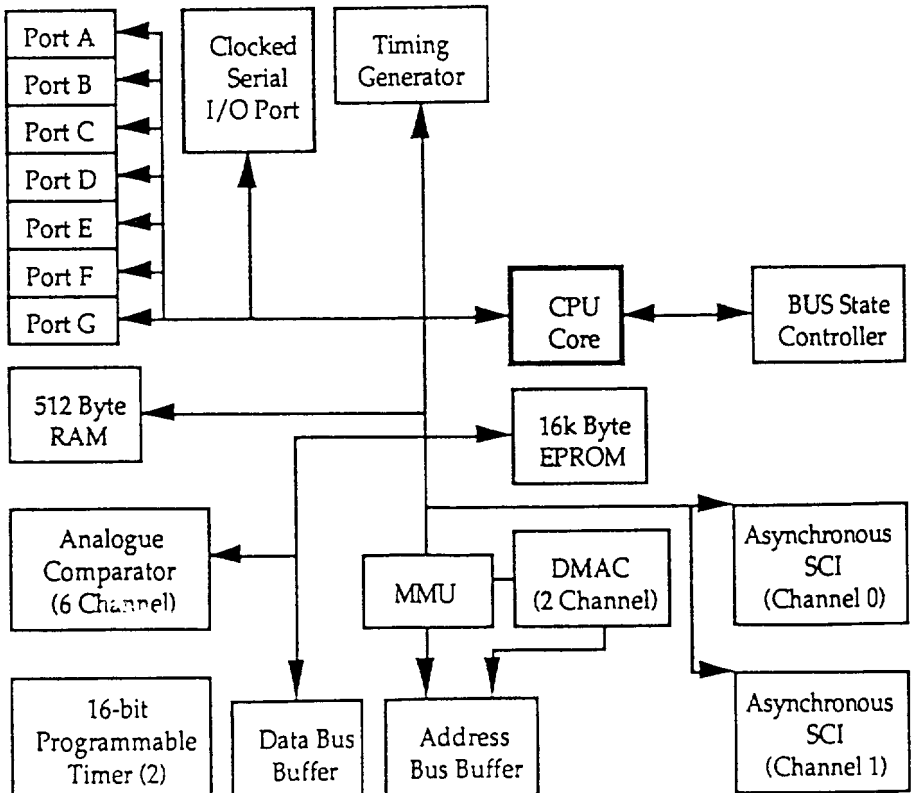
With additional :

- 54 I/O Lines (8 which will sink up to 10mA)
- 16K EPROM on-chip
- 512 bytes on-chip RAM
- 6 channel analogue comparator
- 16 bit programmable timer
- Input capture register
- Output compare
- Timer overflow interrupt

In addition, there is the HD643180X mask programmed device offering the same facilities as the ZTAT part but with the added advantage of a lower unit cost for high volume production runs.

The final member of the X mask group, the HD641180X, offers all the features of the HD647180X but in a ROMless device.

HD647180X Block Diagram



HD64180S - THE NETWORK PROCESSOR UNIT

Based on the powerful HD64180 CPU core, the NPU combines the benefits of high performance and reduced system costs whilst maintaining compatability with the large base of industry standard 8 bit software. CPU operating performance is improved by virtue of high clock speeds and pipelined instructions as well as an enhanced instruction set and integral MMU which will address up to 1M bytes physical address space. The combination of this high performance CPU core with an equally high performance Multi-protocol Serial Comms Interface (MSCI) ensures that the NPU is ideally suited to be a serial bus network controller.

Major Functions

CPU
- Software-compatible with HD64180Z
- 80 type bus interface
- On-chip MMU (1 Mbyte physical address space)

DMAC
- 2 channels
- DMA transfer between memory and memory, memory and I/O (memory-mapped I/O), and memory and MSCI
- Chained-block transfer between memory and MSCI
- Internal interrupt requests available

Multiprotocol Serial Communications Interface
- Full duplex channel
- Asynchronous, byte synchronous (mono, bi or external synchronous) or bit synchronous (HDLC or loop) selectable
- Transmit / receive control using modem control signals (RTSM, CTSM and DCDM)
- Internal Advanced Digital PLL (ADPLL)
  - clock extraction
  - receive data and / or receive clock noise suppression
- On-chip baud rate generator
- Internal interrupt requests available
- Maximum transfer rate 7.1 Mbps (with 10MHz clock)

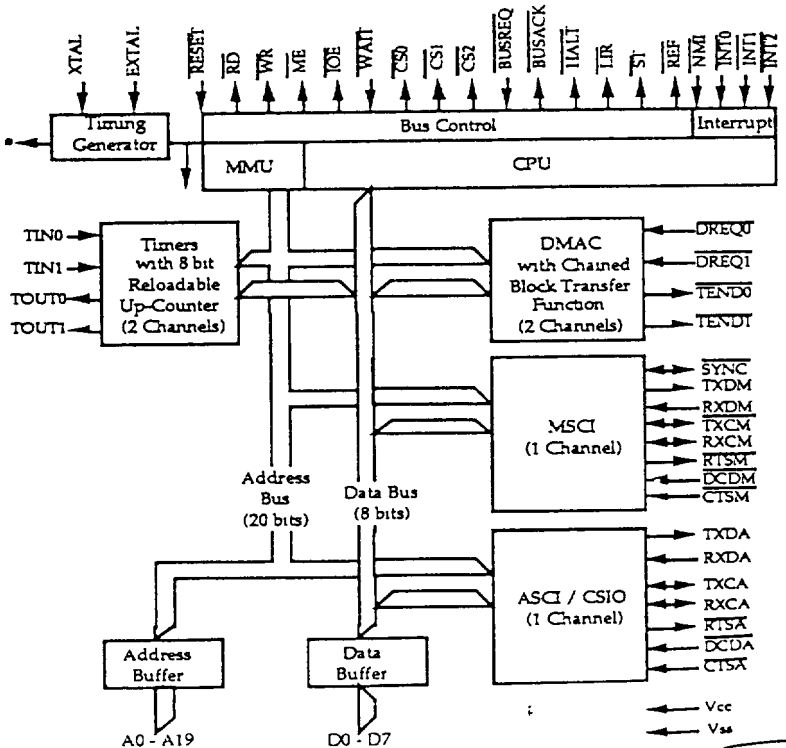
Asynchronous Serial Communications Interface / Clocked Serial I/O Port
- Full duplex channel
- Asynchronous or clocked serial mode (selectable)
- Transmit / receive control using mode control signals (RTSA, CTSA amd DCDA)
- On-chip baud rate generator
- Internal interrupt requests available

Timers
- 2 channels
- 8-bit reloadable up-counter
- Output waveform generator and external event count functions
- Internal interrupt requests available

Interrupt Controller
- 4 external interrupt lines (NM1, INT0, INT1 and INT2)
- 15 internal interrupt sources

Memory Access Support Function
- Internal refresh controller
- Internal wait state controller

Other Functions
- On-chip clock oscillator circuit
- Low power dissipation modes (sleep and system stop)



HD64180 FAMILY - CPU OVERVIEW

The HD64180 combines a high performance CPU core with many of the systems and I/O resources required by a broad range of applications.

The CPU core consists of six functional blocks :

- Clock Generator
- Bus State Controller
- Interrupt Controller
- Memory Management Unit (MMU)
- Central Processing Unit (CPU)
- DMA Controller

CPU Architecture

The six CPU core functional blocks are described in this section :

Clock Generator :
The HD64180 contains a crystal oscillator and system clock (ø) generator. A crystal can be directly connected or an external clock input can be provided. In either case, the system clock ø is equal to one-half the input clock. For example, a crystal or external clock input of 8MHz corresponds with a system clock rate of ø = 4MHz. Also, the system clock is programmably prescaled to generate timing for the on-chip I/O and system support devices.

Bus State Controller :
Performs all status / control bus activity. This includes external bus cycle wait state timing. RESET, DRAM refresh and master DMA bus exchange generates 'dual-bus' control signals for compatibility with peripheral devices from 8080 / 6800 families.

Interrupt Controller :
Monitors and prioritises the four external and eight internal interrupt sources. A variety of interrupt response modes are programmable.

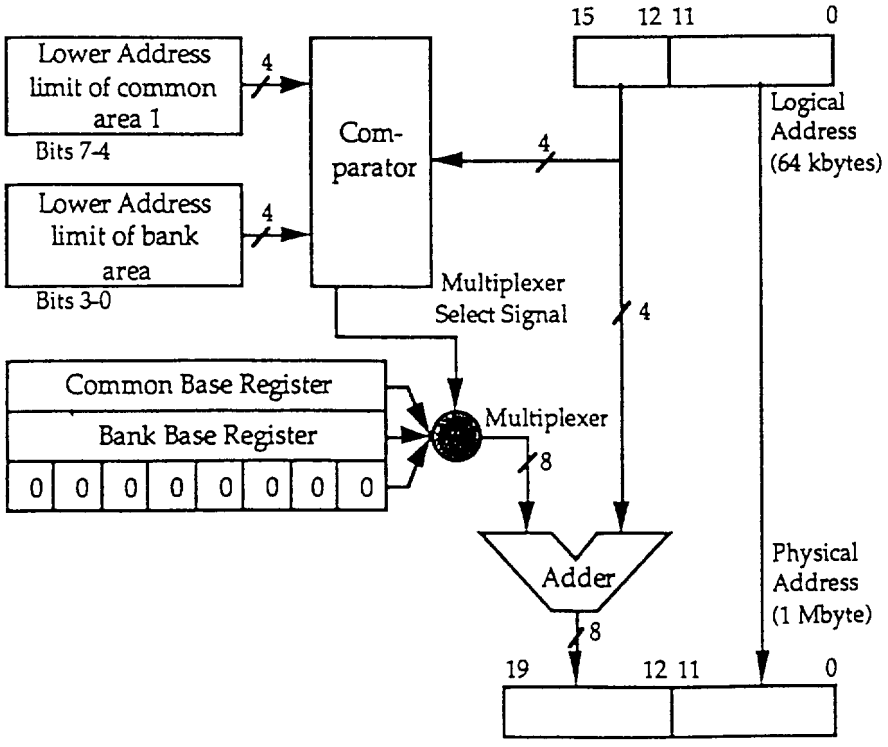
Memory Management Unit :
Maps the CPU 64K bytes logical memory address space into up to 1M bytes physical memory address space. The MMU organisation preserves software object code compatibility while providing extended memory access and uses an efficient 'common area - bank area' scheme. I/O accesses bypass the MMU.

Whether address translation takes place depends on the type of CPU cycle as follows :-

Memory Cycles :
Address Translation occurs for all memory access cycles including instruction and operand fetches, memory data reads and writes, hardware interrupt vector fetch and software interrupt restarts.

I/O Cycles :
The MMU is logically bypassed for I/O cycles. The 16-bit logical I/O address space corresponds directly with the 16-bit physical I/O address space. The high order bits (A16-A19) of the physical address are always 0 during I/O cycles.

DMA Cycles :
When the HD64180 on-chip DMAC is using the external bus, the MMU is physically bypassed. The source and destination registers in the DMAC are directly output on the physical address bus (A0-A19).



MMU Block Diagram

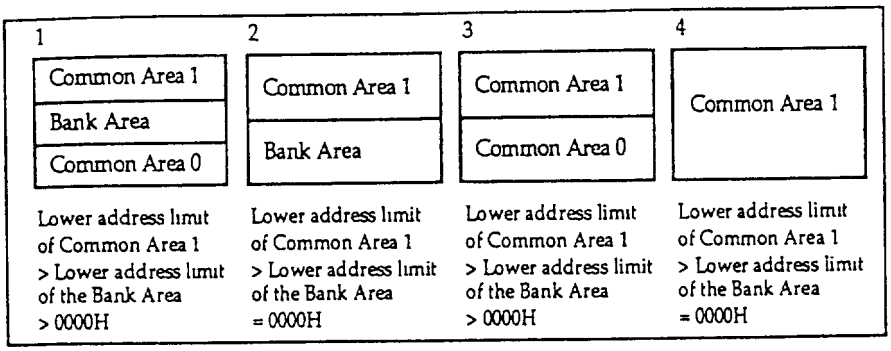
MMU Registers

Three MMU registers are used to program a specific configuration of logical and physical memory :-

- MMU Common / Bank Area Register (CBAR)
- MMU Common Base Register (CBR)
- MMU Bank Base Register (BBR)

CBAR is used to define the logical memory organisation while CBR and BBR are used to relocate logical areas within the physical address space. The resolution for both setting boundaries within the logical

Logical Memory Organisation



space and relocation within the physical space is 4K bytes.

The CAR field of CBAR determines the start address of Common Area 1 (Upper Common) and by default, the end address of the Bank Area. The BAR field determines the start address of the Bank Area and by default, the end address of Common Area 0 (Lower Common).

The CA and BA fields of CBAR may be freely programmed subject only to the restriction that CA may never be less than BA.

DMA Controller (DMAC)

The HD64180 contains a two channel DMA (Direct Memory Access) controller which supports high speed data transfer. Both channels (channel 0 and channel 1) have the following capabilities. At 6MHz system clock data can be transferred at 1 megabyte per second.

Memory Address Space :
Memory source and destination addresses can be directly specified anywhere within the 1M byte physical address space using up to 20 bit source and destination memory addresses. In addition, memory transfers can arbitrarily cross 64K bytes physical address boundaries without CPU intervention.

Transfer Rate :
Each byte transfer can occur every six clock cycles. Wait states can be inserted in DMA cycles for slow memory or I/O devices At the system clock (ø) = 6MHz, the DMA transfer rate is as high as 1.0 megabytes / second (no wait states).

Each channel has additional specific capabilities :

Channel 0 :
- Memory - Memory, Memory - I/O, memory - Memory Mapped I/O Transfers
- Memory Address Increment, Decrement, No-change
- Burst or Cycle Steal memory - memory transfer
- DMA to and from both ASCI Channels
- Higher priority than DMAC Channel 1

Channel 1 :
- Memory - I/O Transfer
- Memory Address Increment, Decrement

Interrupts

The HD64180 CPU has twelve interrupt sources, four external and eight internal, with fixed priority.

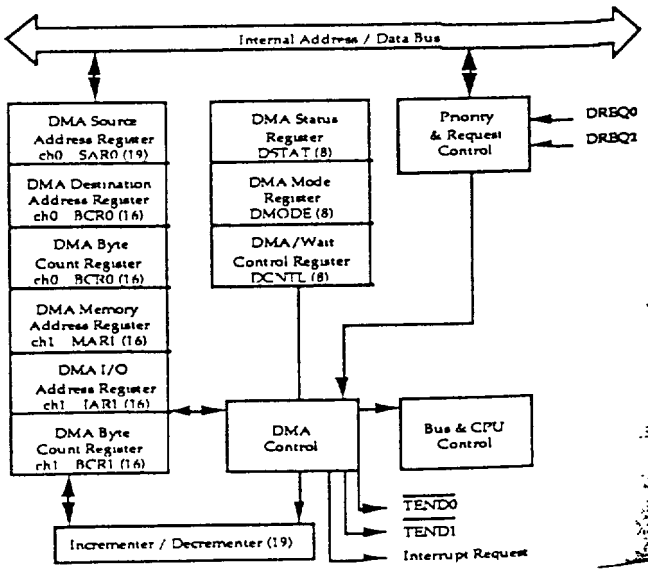
Higher Priority
1) TRAP (undefined op-code trap)
2) NMI (non maskable interrupt)
3) INT0 (maskable interrupt level 0)
4) INT1 (maskable Interrupt level 1)
5) INT2 (maskable interrupt level 2)
6) Timer 0
7) Timer 1
8) DMA channel 0
9) DMA channel 1
10) Clocked Serial I/O Port
11) Asynchronous SCI channel 0
12) Asynchronous SCI channel 1
Low Priority

Trap Interrupt

The HD64180 generates a non-maskable TRAP interrupt when an undefined op-code fetch occurs. This feature can be used to increase software reliability, implement an 'extended' instruction set, or both. TRAP may occur during op-code fetch cycles and also if an undefined op-code is fetched during the interrupt acknowledge cycle for INT0 when Mode 0 is used.

HALT, SLEEP and Low Power Operation

The HD64180 can operate in 4 different modes, HALT mode and



DMAC Block Diagram

three low power operation modes - SLEEP, IOSTOP and SYSTEM STOP. Note that in all operating modes, the basic CPU clock (XTAL, EXTAL) must remain active.

HALT Mode

HALT mode is entered by execution of the HALT instruction and has the following characteristics :

- The internal CPU clock remains active
- All internal and external interrupts can be received
- Bus exchange (BUSREQ and BUSACK) can occur
- Dynamic RAM refresh cycle (REF) insertion continues at the programmed interval
- I/O operations (ASCI, CSI/O and PRT) continue
- The DMAC can operate
- The HALT output pin is asserted LOW
- The external bus activity consists of repeated 'dummy' fetches of the op-code following the HALT instruction

Essentially, the HD64180 operates normally in HALT mode except the instruction execution is stopped.

SLEEP Mode

SLEEP mode is entered by execution of the two byte SLEEP instruction. SLEEP mode has the following characteristics.

- The internal CPU clock stops, reducing power consumption
- The internal crystal oscillator does not stop
- Internal and extral interrupt inputs can be received
- DRAM refresh cycles stop
- I/O operations using on-chip peripherals continue
- The internal DMAC stop
- BUSREQ can be received and acknowledged
- Address outputs go HIGH and all other control signal output become inactive (HIGH)
- Da

SLEEP mode is exited in one of two ways :

RESET exit from SLEEP Mode
If the RESET input is held LOW for more than 3 clock cycles, the HD64180 will exit SLEEP mode and begin the normal RESET sequence with execution starting at address (logical and physical) 0.

Interupt exit from SLEEP Mode
The SLEEP mode is exited by detection of an external or internal interrupt.

IOSTOP Mode

IOSTOP mode is entered by setting the IOSTP bit of the I/O Control Register to 1. In this case, on-chip I/O (ASCI, CSI/O, PRT) stops operating, reducing power consumption. However, the CPU continues to operate. Recovery from IOSTOP mode is be resetting the IOSTP bit in ICR to 0.

SYSTEM STOP Mode

SYSTEM STOP mode is the combination of SLEEP and IOSTOP modes. SYSTEM STOP mode is enetered by setting the IOSTP bit in ICR = 1 followed by execution of the SLEEP instruction. Recovery from SYSTEM STOP mode is the same as recovery from SLEEP mode, noting that internal I/O sources (disabled by IOSTOP) cannot guarantee a recovery interrupt.

Improved Software Capability

The 64180 is object code compatible with standard 8 bit operating systems and application software. The instruction set also contains 12 new instructions which when combined with the pipeline architecture, improve system performance, reliability and efficiency.

New Instructions

In addition to the standard instruction set, the following new instructions are available :

SLP-SLEEP
The SLP instruction causes the HD64180 to enter SLEEP low power consumption mode.

MLT - Multiply
The MLT performs unsigned multiplication on two 8 bit numbers yielding a 16 bit result. MLT may specify BC, DE, HL or 16 SP registers. In all cases, the bit result is returned in that register.

INO g, (m) - Input, Immediate I/O Address
The contents of the immediately specified 8 bit I/O address are input into the specified register. When I/O is accessed, 00H is output in high-order bits of address automatically.

OUTO g, (m) - Output, Immediate I/O Address
The contents of the specified register are output to the immediately specified 8 bit I/O address. When I/O is accessed, 00H is output in high-order bits of address automatically.

OTIM, OTIMR, OTDM, OTDMR - Block I/O
The contents of memory pointed to by HL is output to the I/O address in (C). The memory address (HL) and I/O address (C) are incremented in OTIM and OTIMR and decremented in OTDM and OTDMR respectively. B register is decremented. The OTDMR and OTDMR variants repeat the above sequence until register B is decremented to 0. Since the I/O address (C) is automatically incremented or decremented, these instructions are useful for block I/O (such as HD64180 on-chip I/O) initialisation. When I/O is accessed, 00H is output in high order bits of address automatically.

TSTIOm - Test I/O Port
The contents of the I/O port addressed by C are ANDed with immediately specified 8 bit data and the status flags are updated. The I/O is accessed, 00H is output in higher bits of address automatically.

TSTg - Test Register
The contents of the specified are ANDed with the accumulator (A) and the status flags are updated. The accumulator and specified register are not changed (non-destructive AND).

TDTm - Test Immediate
The contents of the immediatly specified 8 bit data are ANDed with the accumulator (A) and the status flags are updated. The accumulator is not changed (non-destructive AND).

TDT (HL) - Test Memory
The contents of memory pointed to by HL are ANDed with the accumulator (A) and the status flags are updated. The memory contents and accumulator are not changed (non-desructive AND).

HD64180 - SOFTWARE ARCHITECTURE

Registers

The HD64180 main registers (Register Set GR) consist of an 8 bit accumulator (A), 8 bit status flag register (F) and three general purpose registers (BC, DE, HL). These latter registers may be treated as 16 bit registers or as individual 8 bit registers depending on the instruction being executed. The main registers also include Special Registers which consist of the interrupt Vector (I), R Counter (R), two 16 bit index registers (IX and IY), stack pointer (SP) and the program counter (PC).

The HD64180 also includes an alternate register set (Register Set GR') for the accumulator, flag and general purpose registers. While these registers are not directly accessible, their contents can be programmably exchanged at high speed with those of the main register set. This capability may be used for high speed context switch or for storing key, frequently accessed variables.

GR Register Set

Accumulator (A)	Flag Register (F)
B Register	C Register
D Register	E Register
H Register	L Register

GR General-purpose Registers

8 bits — 8 bits

GR' Register Set

Accumulator (A')	Flag Register (F')
B' Register	C' Register
D' Register	E' Register
H' Register	L' Register

GR' General-purpose Registers

8 bits — 8 bits

Dedicated Register Set

Interrupt Vector Register (I)	R Counter (R)
Index Register (IX)	
Index Register (IY)	
Stack Pointer (SP)	
ProgramCounter (PC)	

16 bits

Register Description

Accumulators (A and A')

The accumulators are the primary registers used for 8-bit arithmetic, logical and shift operations.

Flag Registers (F and F')

Flag registers indicate the status of the operation result.

General-Purpose Registers B, C, D, E, H and L

The six 8-bit general-purpose registers in register set GR are used for operations and addressing. Registers B and C, D and E, or H and L can be used together as 16-bit registers.

General-Purpose Registers B', C', D', E', H' and L'

The six 8-bit general-purpose registers in register set GR' function in the same way as registers B, C, D, E, H and L.

Interrupt Vector Register (I)

The interrupt vector register specifies the high order byte of a 16-bit interrupt vector. This register is used for INT0 mode 2, INT1, INT2 and internal interrupts except TRAP.

R Counter (R)

The 7-bit counter indicates the number of executed opcode fetch cycles.

S	Z	-	H	-	P/V	N	C

F Register

Index Registers (IX and IY)

The 16-bit index registers are used for index addressing and 16-bit operations.

Stack Pointer (SP)

The 16-bit stack pointer register holds the address of the top of the stack.

Program Counter (PC)

The 16-bit program counter register holds the logical address of the next instruction to be executed.

Flag (F) Description

The flag register stores the logical state reflecting the results of instruction execution. The contents of the flag register are used to control program flow and instruction operation.

S : Sign (bit 7) :

S stores the state of the most significant bit (bit 7) of the result. This is useful for operations with signed numbers in which values with bit 7 = 1 are interpreted as negative.

Z : Zero (bit 6) :

Z is set = 1 when instruction execution results containing 0. Otherwise, Z is reset = 0.

H : Half Carry (bit 4) :

H is used by the DAA (Decimal Adjust Accumulator) instruction to reflect, borrow or carry from the least significant 4 bits and thereby adjust the results of BCD addition and subtraction.

P/V : Parity / Overflow (bit 2):

PV serves a dual purpose. For logical operations P/V is set = 1 if the number of 1 bits in the result is even and P/V is reset = 0 if the number of 1 bits in the result is odd. For two's complement arithmetic, P/V is set = 1 if the operation produces a result which is outside the allowable range (+127 to -128 for 8 bit operations, +32767 to -32768 for 16 bit operations)

N : Negative (bit 1) :

N is set = 1 if the last arithmetic instruction was a subtract operation (SUB, DEC, CP, etc.), and N is reset = 0 if the last arithmetic instruction was an addition operation (ADD, INC, etc.).

C : Carry (bit0) :

C is set = 1 when a carry (addition) or borrow (subtraction) from the most significant bit of the result occurs. C is also affected by accumulator logic operations such as shifts and rotates.

Addressing Modes

The HD64180 instruction set includes eight addressing modes :

Register Direct (REG)

Many op-codes contain bit fields specifying registers to be used for the operation. The exact bit field definition varies depending on instruction as follows.

Implied Register (IMP)

Certain op-codes automatically imply register usage, such as the arithmetic operations which inherently reference the accumulator, Index Registers, Stack Pointer, and General-Purpose Registers.

Relative (REL)

Relative addressing mode is only used by the conditional and unconditional branch instructions. The branch displacement (relative to the contents of the program counter) is contained in the instruction.

Register Indirect (REG)

The memory operand address is contained in one of the 16-bit General- purpose Registers (BD, DE and HL).

Indexed (INDX)

The memory operand address is calculated using the contents of an Index Register (IX or IY) and an 8 bit signed displacement specified in the instruction.

Extended (EXT)

The memory operand address is specified by two bytes contained in the instruction.

I/O (IO)

IO addressing mode is used by I/O instructions. This mode specifies I/O address (IOE = 0) and outputs then as follows :

- An operand is output to A0 - A7. The contents of accumulator is output to A8 - A15
- The contents of Register B is output to A0 - A7. The contents of Register C is output to A8 - A15
- An operand is output to A0 - A7. 00H is output to A8 - A15. (Useful for internal I/O register access)
- The contents of Register C is output to A0 - A7. 00H is output to A8 - A15. (Useful for internal I/O register access)

I/O RESOURCES

The I/O provided by the 64180 devices varies from device to device, an overview is provided below.

Asynchronous Serial Communication Interface (ASCI)

The HD64180 on-chip ASCI has two independent full duplex channels. Based on full programmability of the following functions, the ASCI can directly communicate with a wide variety of standard UARTs (Universal Asynchronous Receiver Trans- mitter) including the HD6350 CMOS ACIA and the Serial Communication Interface (SCI) contained in H8, H16 and 6301 processors.

The key functions for ASCI are shown below. Each channel is independently programmable.

- Full duplex communication
- 7 or 8 bit data length
- Program controlled 9th data bit for multiprocessor communication
- 1 or 2 stop bits
- Odd, even, no parity
- Programmable baud rate generator, /16 and /64 modes. Speed to 38.4k bits per second (CPU fc = 6.144MHz)
- Modem control signals - channel 0 has DCD0, CTS0 and RTS0 channel 1 has CTS1
- Programmable interrupt condition enable and disable
- Operate with on-chip DMAC

Clocked Serial I/O Port (CSI/O)

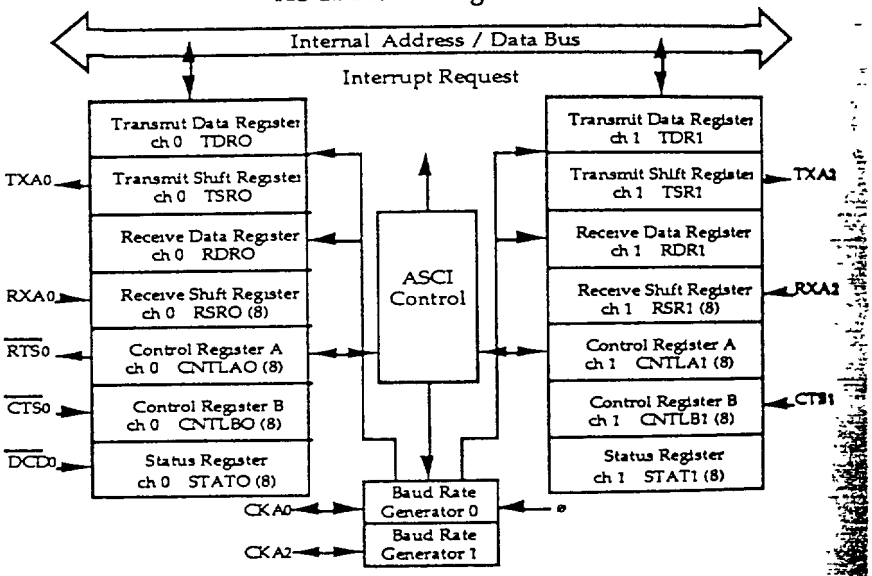
The HD64180 includes a simple, high speed clock synchronous serial I/O port. The CSI/O includes transmit / receive (half duplex), fixed 8 bit data and internal or external data clock selection. High speed operation (baud rate as high as 200k bits / second at fc = 4MHz) is provided.

The CSI/O is ideal for implementing a multiprocessor communication link between the HD64180 and the HMCS400 Series (4 bit) and the HD6301 Series (8 bit) single chip controllers as well as additional HD64180 CPU's. These secondary devices may typically perform a portion of the system I/O processing such as keyboard scan / decode, LCD interface, etc.

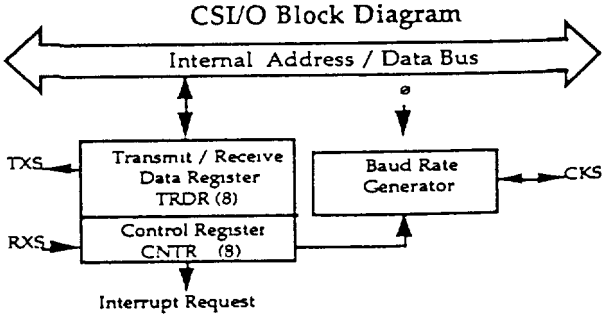
Programmable Reload Timer (PRT)

The HD64180 contains a two channel 16 bit Programmable Reload Timer. Each PRT channel contains a 16 bit down counter and a 16 bit reload register. The down counter can be directly read and written and a down counter overflow interrupt can be programmably enabled or disabled. In addition, PRT channel 1 has aTOUT output pin (pin 31 - multiplexed with A18) which can be set HIGH or LOW and toggled. Thus PRT1 can perform programmable output waveform generation.

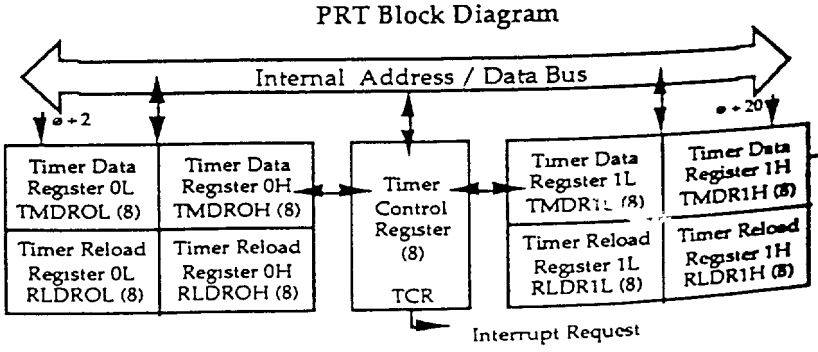
ASCI Block Diagram



CSI/O Block Diagram



PRT Block Diagram



MULTIPROTOCOL SERIAL COMMUNICATIONS INTERFACE (MSCI)

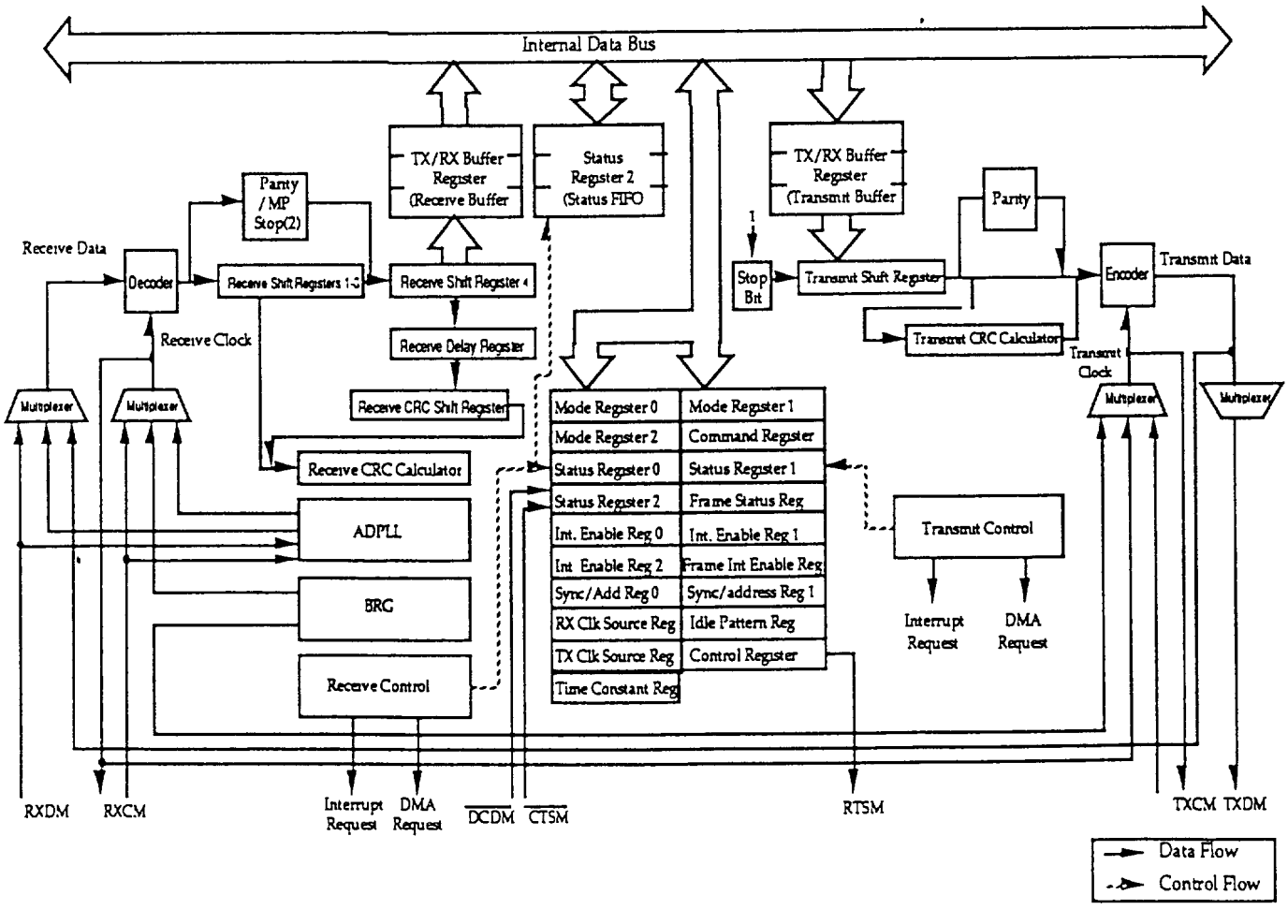
The most important peripheral on the NPU is the Multiprotocol Serial Communications Interface. This is the peripheral that enables the processor to operate as a powerful serial communications bus controller. The MSCI is capable of supporting three different operating modes : asynchronous, byte synchronous and bit synchronous.

The MSCI includes the following functions :-

- program-selectable operating modes; asynchronous, byte synchronous and bit synchronous
- transmission codes NRZ, NRZI, Manchester, FM0 and FM1 are supported. (Only NRZ code is supported in the asynchronous mode.)
- full duplex communications, auto echo and local loop back functions are available
- separate transmit and receive buffers are provided for each three stages
- modem control signals RTSM, CTSM and DCDM can be automatically controlled using the auto-enable function :-

  RTSM (Request To Send) - general-purpose output / transmission request
  CTSM (Clear To Send) - general-purpose input / transmit enable / transition-triggered interrupt
  DCDM (Data Carrier Detect) - general-purpose input / receive carrier detection / transition-triggered interrupt
- programmable on-chip baud rate generator for transmission and reception
- clock is program-selectable from three sources: external clock input, on-chip baud rate generator output, and internal ADPLL (Advanced Digital PLL) output
- noise suppression function for receive clock and receive data
- data transmission rate of 7.1 Mbps for a 10MHz system clock
- four internal interrupt signals : RXRDY, TXRDY, RXINT and TXINT

MSCI Block Diagram



Development Support - The Path To Success

Clearly, to enable the full benefit of the advanced silicon to be realised in the shortest possible time, software support must match the device in availability and performance. Hitachi is an innovator in development equipment, producing systems, software and emulators to support our range of processors.

HS180ASE - Adaptive System Emulator

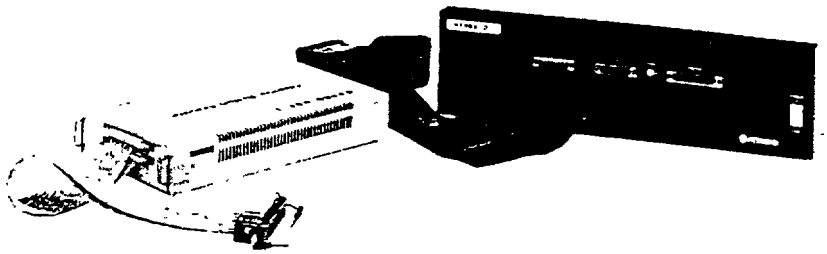
This is a real time emulator for the HD64180 which can interface to a variety of host systems. Program generation would be typically carried out on the host computer, such as PC or VAX and then down loaded into the memory of the emulator. The emulator can then be controlled directly by a dumb terminal. The unit features a floppy disc which can be used to load or save user programs without requiring access to the host system.

Features

- Supports real time evaluation up to 10MHz
- Interfaces with host via standard RS232C link
- Object program may be loaded or saved directly on internal floppy disc
- Real time trace facility
- Memory mapping in 4K units between emulator and target system
- Line assembler and full disassembler facilities
- Symbolic debugging facilities
- Coverage feature giving indication of memory usage

HS180ASE Options

Processor	Emulator	Buffer Box	Standard Header
HD64180R1	HS180AST01H	HS180ABX02H	64 pin dil (shrink)
HD64180Z	HS180AST01H	HD180ABX03H	64 pin dil (shrink)
HD647180X HD643180X HD641180X	HS180AST01H	HD180ABX04H	PLCC 84
HD64180S	HS180AST01H	HD180ABX05H	PLCC 84



Hitachi Software Support

We have introduced a range of powerful cross assemblers to run on the most popular most computers.

3rd Party Development Support

We realise you may already have a development system or host that you wish to continue using. For these reasons we give full details of third party software and emulators which are available for prototype development.

SUPPLIER	SOFTWARE	HOST	
		IBM PC	VAX
Kontron 0923 45991	X-Ass	●	×
	C-Compiler	●	×
Microtec 0256 57551	X-Ass	●	●
	C-Compiler	●	●
Ashling +353-61-334466	X-Ass	●	
	C-Compiler		
Pentica 0734 792101	X-Ass	●	●
	C-Compiler	●	●
R.T.S. 0624 26021	X-Ass	●	●
	C-Compiler		
Crossware 0763 61539	X-Ass	●	
	C-Compiler	●	●
I.A.R. + 018 157920	X-Ass	●	●
	C-Compiler	●	●
Creative Data +089 854 3080	X-Ass	●	●
	C-Compiler	●	●
M.S.S 0494 41661	X-Ass	●	●
	C-Compiler	●	●
Dux 0420 [illegible]	X-Ass	●	●
	C-Compiler	●	●
Hewlett Packard 0734 784774	X-Ass	●	
	C-Compiler		

● Available
× Under Development

HD64180 - PACKAGE OPTIONS

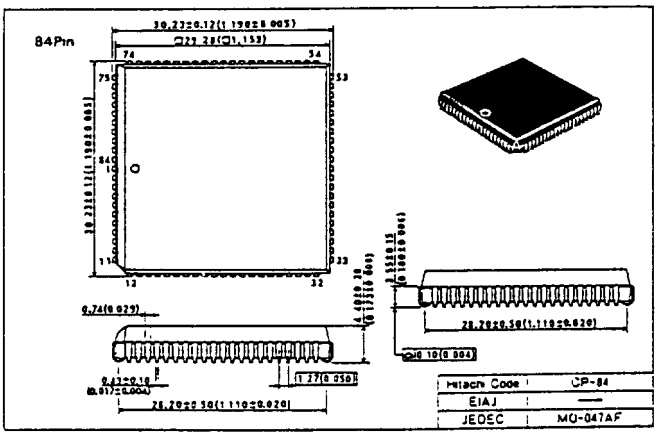
In order to support the package most suitable for your application, the HD64180 is available in both through-hole and surface mounting packages.

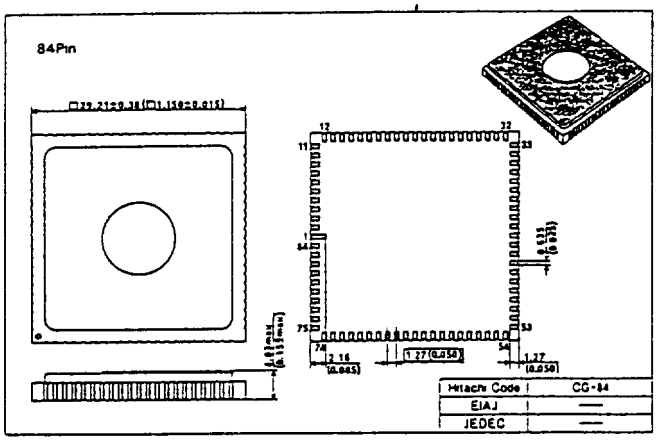
DIL
The popular dual-in-line package features through-hole mounting for socketing and easy assembly. The shrink packages have pins on a 0.07 inch pitch. A 64 pin shrink package (DP-64S) occupys the almost the same area as a standard 40 DIL package.

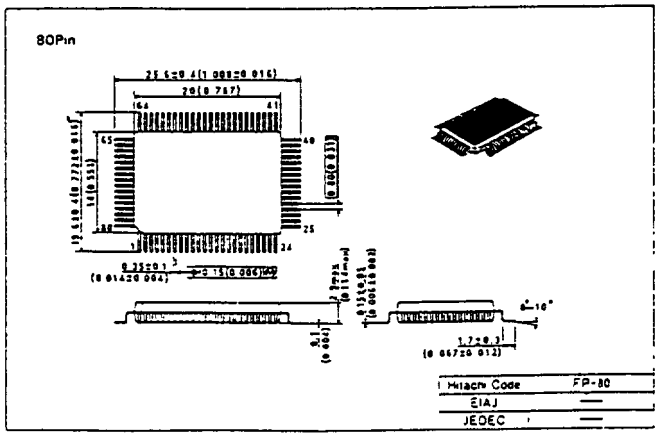
PLCC
The plastic leaded chip carrier is a surface mounting package which features the 'J' bend lead frame. The package has good environmental performance and is available in wide temperatuire range version.

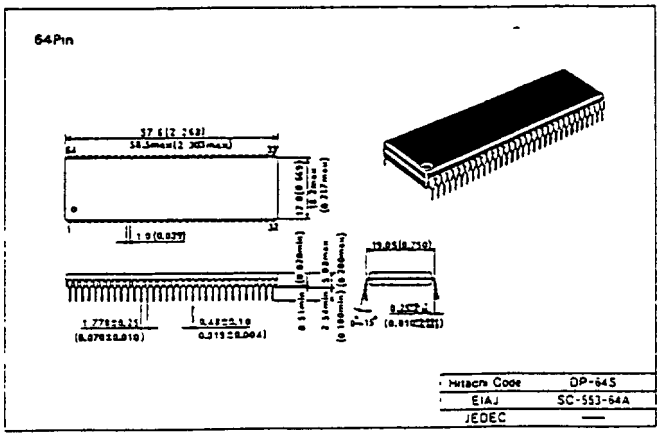
FPP
The flat plastic package us a surface mounting package which features the 'gull wing' style lead frame. This package achieves very high package density.

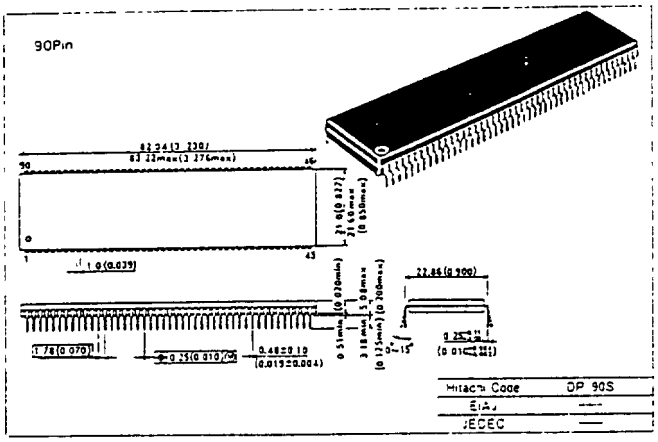
Package \ Processor	HD64180R1/2	HD647180 HD643180 HD64180	HD64180S
DP-64S	●		
DP-90S		●	
CP-68	●		
CP-84		●	
LCC-84		●	
FP-80	●	●	●

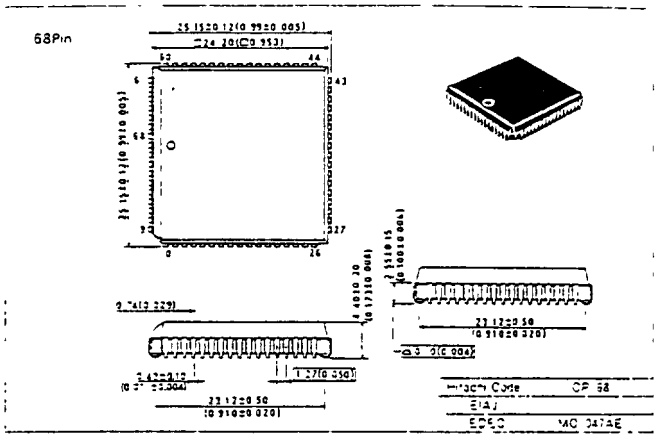


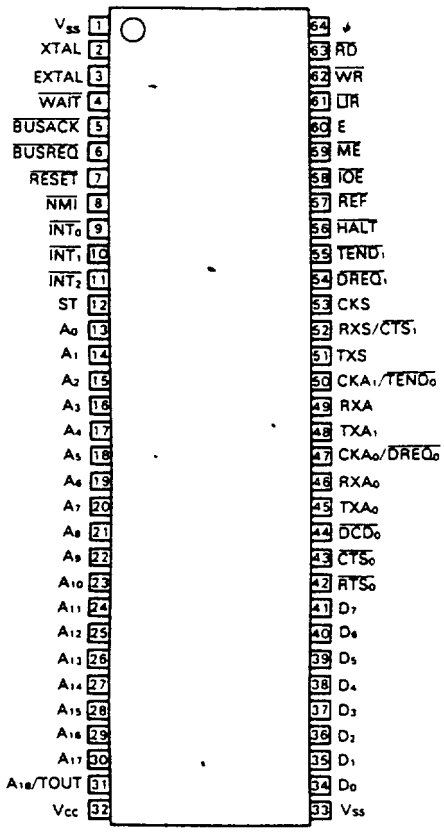




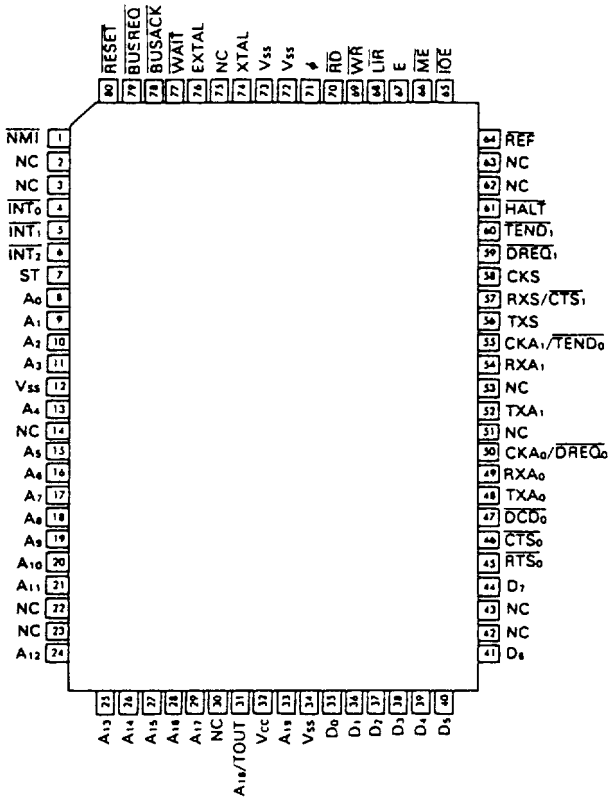




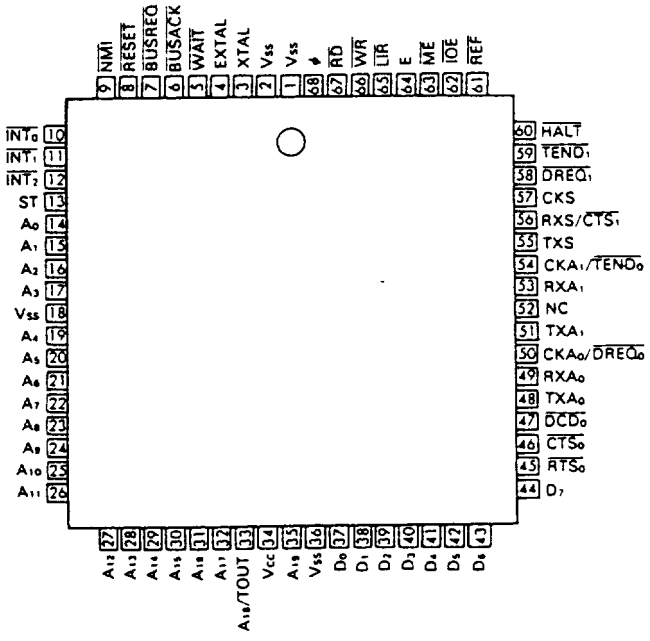




(DP-64S)



(FP-80)

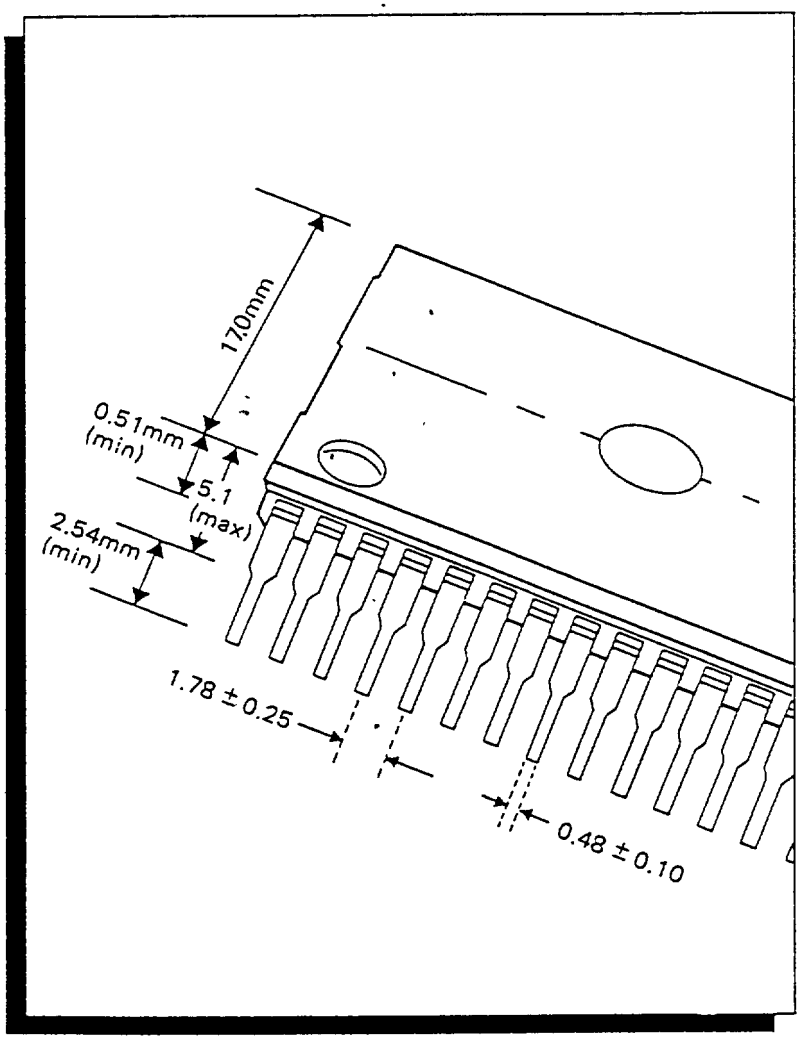


(CP-68)

NC. Not connected.
Please leave the
NC pins open.

HD64180 FAMILY

HIGH INTEGRATION CMOS MICROCONTROLLERS



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HD64180 - INNOVATION WITH EXPERIENCE

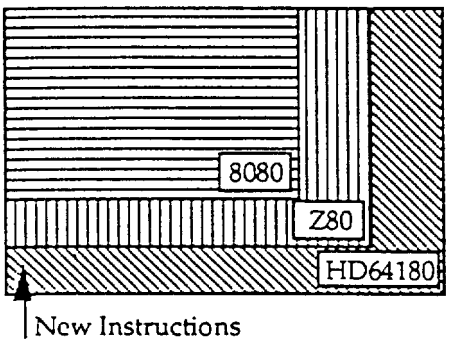
Are you looking for new ways of further improving your production or perhaps starting to consider ideas for an entirely new product range? Either way the choice of the ideal microprocessor for your application can be difficult.

It is likely you already have considerable expertise in both hardware and software techniques which are specific to your field. However, with advances in semiconductor technology seeming to make yesterday's devices obsolete, how is your investment in established areas still going to be an asset?

Since its introduction, the HD64180 microprocessor from Hitachi based upon state-of-the-art 1.3µm CMOS technology, has made a major contribution to solving this dilemma since :

- it is upwardly compatible with existing 8-bit industry standard software
- the combination of a powerful processor and advanced peripherals on a single chip, enable the 64180 to provide very high system performance

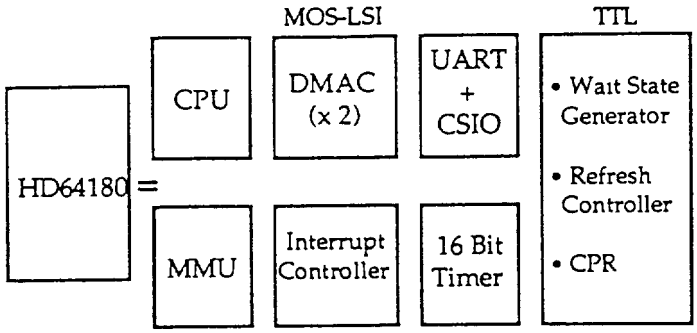
Software Compatibility



The 64180 is upwardly compatible with Z80, 8080, 8085 and NSC 800 instruction set.

It incorporates 12 new instructions which provide increased processing efficiency together with low power operation modes.

Peripheral Integration



Hitachi advanced CMOS technology has made available a level of peripheral integration which would not have previously been considered possible.

The block diagram above shows the equivalent chip count required to match the features incorporated in the 64180.

Building upon the success of the original device the HD64180R0, a family of devices are now available which increase further the range of potential applications for the HD64180.

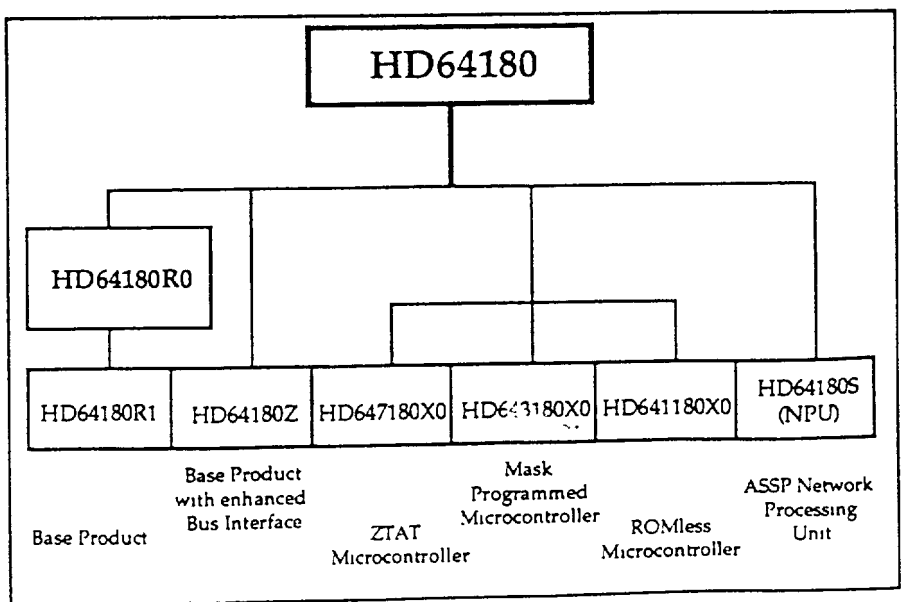
The range includes ROMless microprocessors, microcontrollers with EPROM, ZTAT one time programmable and mask programmed variants.

ZTAT stands for Zero Turn Around Time and the CMOS EPROM on-chip can bring many advantages to product development and marketing.

The latest addition to the 64180 family is the Network Processing Unit (NPU). The NPU is the newest innovation for the 64180 family. It is a cell based application-specific standard product designed for all networking and communications oriented applications.

Put all this together with a variety of powerful development support tools, high level language compilers and cross assemblers from both Hitachi and 3rd party suppliers, the HD64180 family is sure to be the right choice for today and tomorrow!

The Family Group



- HD64180R1

  The R1 mask is the base member of the family and is a fully upward compatible replacement for the original HD64180R0.

- HD64180Z

  The Z mask has almost identical features as the R1 plus the ability to interface more simply to '80' family peripherals.

- HD64180X

  The X combines the basic 180 features with the addition of on-chip EPROM, RAM and I/O facilities which make it an ideal candidate for a minimum component solution.

- HD643180X

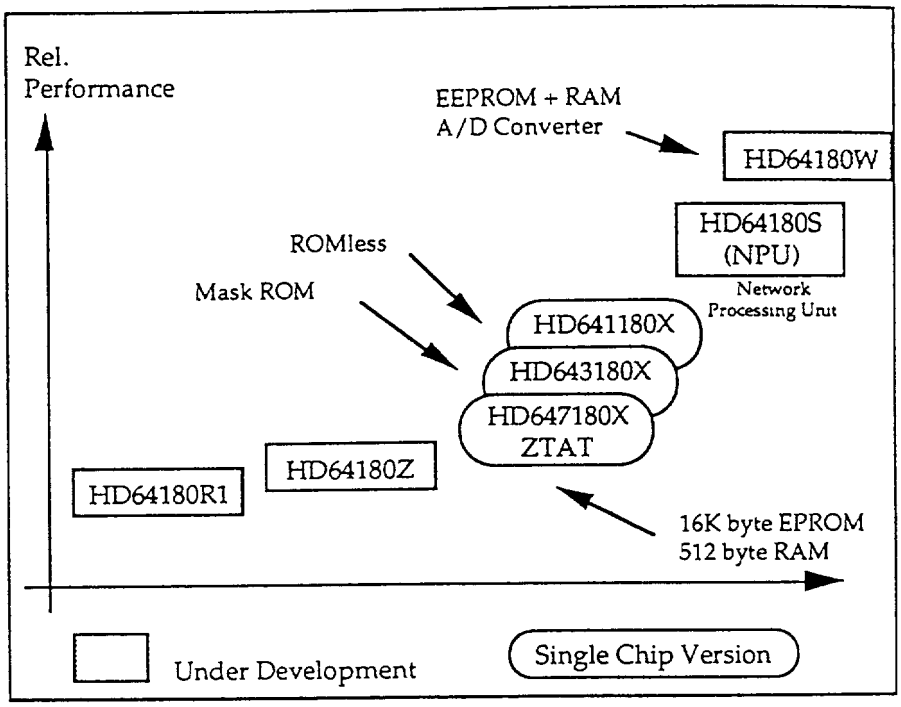
  This device is equivalent to the 647180X but its on-chip program memory is of the mask programmed type.

- HD641180X

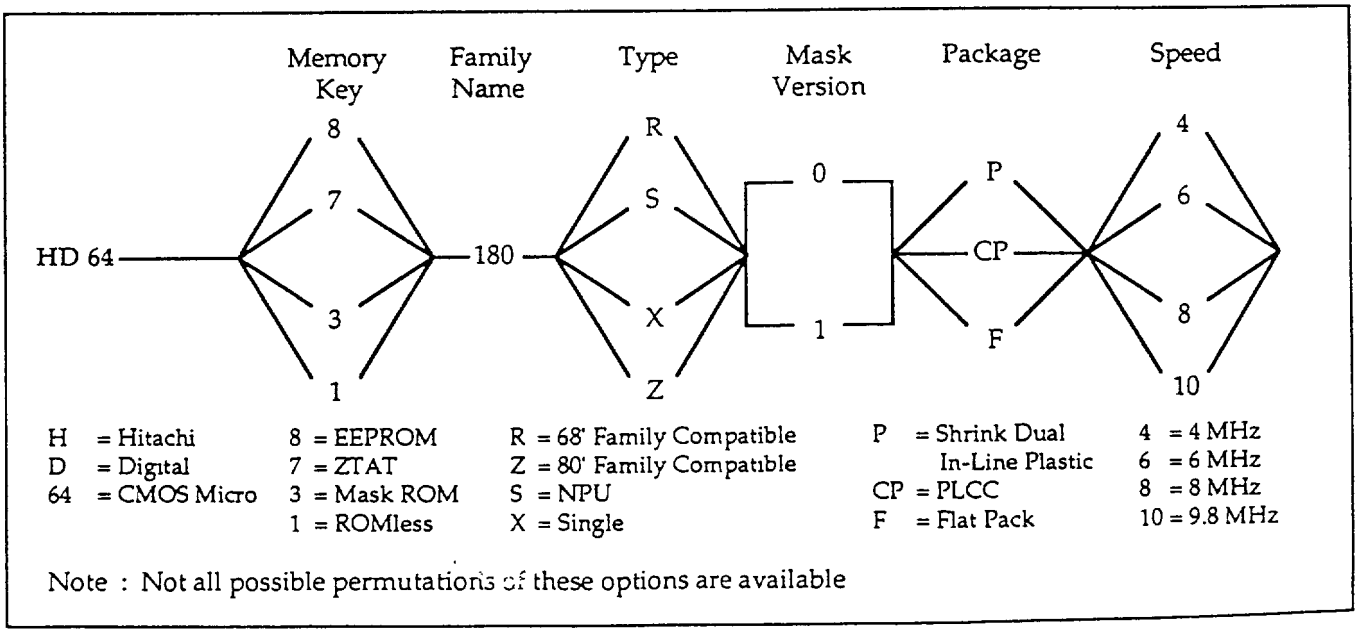
  The HD641180X provides the same facilities as the HD647180X and HD643180X in a ROMless form.

- HD64180S

  The HD64180S Network Processing Unit is a ROMless device that features a multiprotocol serial interface which can support many industry standard communications protocols.



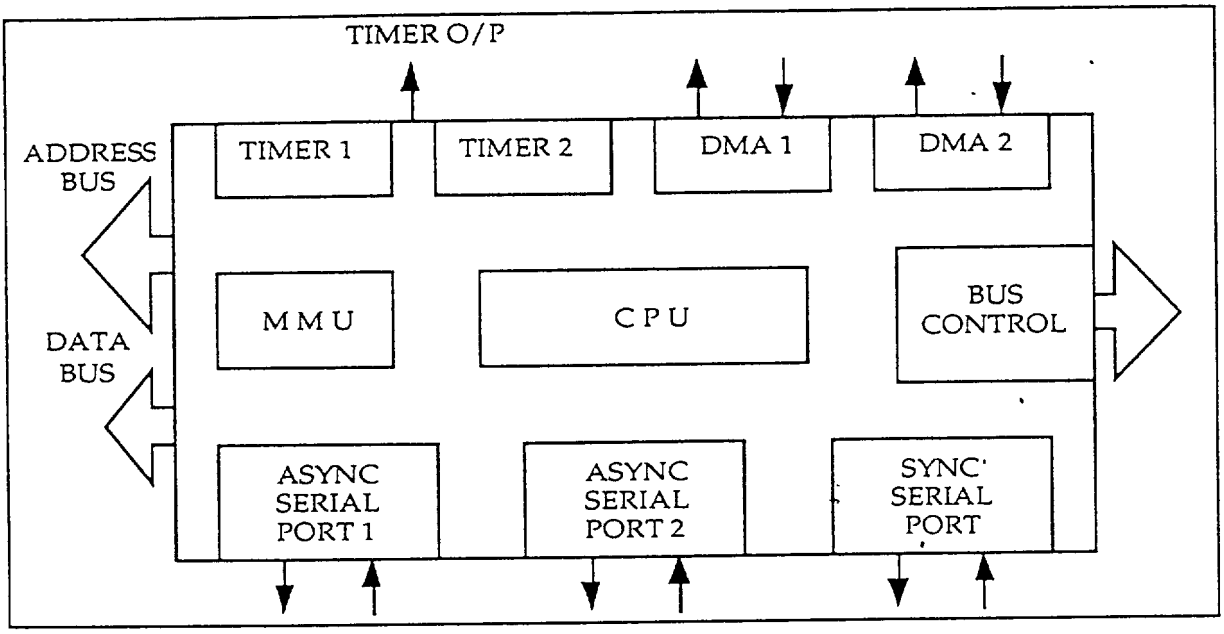
HD64180 Series Evolution



HD64180 Microprocessor Variants

HD64180 - A SYSTEM ON A CHIP

Based upon a microcoded execution unit and advanced CMOS technology, the 64180 is an 8-bit CPU which provides the benefits of high performance, reduced system costs and low power operation while maintaining compatibility with the large base of industry standard 8-bit software. Performance is improved by virtue of high operating frequency, pipelining, enhanced instruction set and integrated memory management unit (MMU) with up to 1M bytes physical memory address space. Low power consumption during normal CPU operation is supplemented by three specific software controlled low power standby modes. When combined with CMOS VLSI memories and peripherals, the 64180 is ideal in system applications requiring high performance, battery powered operation and standard software compatibility.



64180R1/Z Block Diagram

THE HD64180R1 AND HD64180Z

The HD64180R1 is the base member of the 64180 family. It includes the high performance CPU which is shared by all 64180 family members.

Hardware Features - High Performance, High Integration CPU

1) Operating frequency to 10MHz
2) On-chip MMU supports up to 1M bytes Memory and 64k bytes I/O Address Space
3) Two channel DMAC with Memory-Memory, Memory I/O and Memory-Memory Mapped I/O Transfer capability
4) WAIT input and Wait State [illegible] Memory [illegible]
5) Programmable Dynamic RAM Refresh Addressing and Timing
6) Two channel, full Duplex Asynchronous Serial Communication Interface (ASCI) wih programmable Baud Rate Generator and Modem Control Handshake Signals
7) Clock Serial I/O Port (CSI/O) with high speed operation (200k bits / second at 4MHz)
8) Two channel 16-bit Programmable Reload Timer (PRT) for Counting, Timing and Output Waveform Generation
9) Versatile Interrupt Controller manages four external and eight internal interrupt sources
10) On-chip Clock Generator

Software Features - Enhanced 8-bit Software Architecture

1) Fully compatible with CP/M-80™, CP/M Plus™ and existing systems and application sofware
2) Twelve new instructions including Multiply
3) On-chip I/O address relocation register for board level compatibility and existing systems and software
4) SLEEP instruction - IOSTOP mode and SYSTEM STOP mode for low power operation

Block Diagram

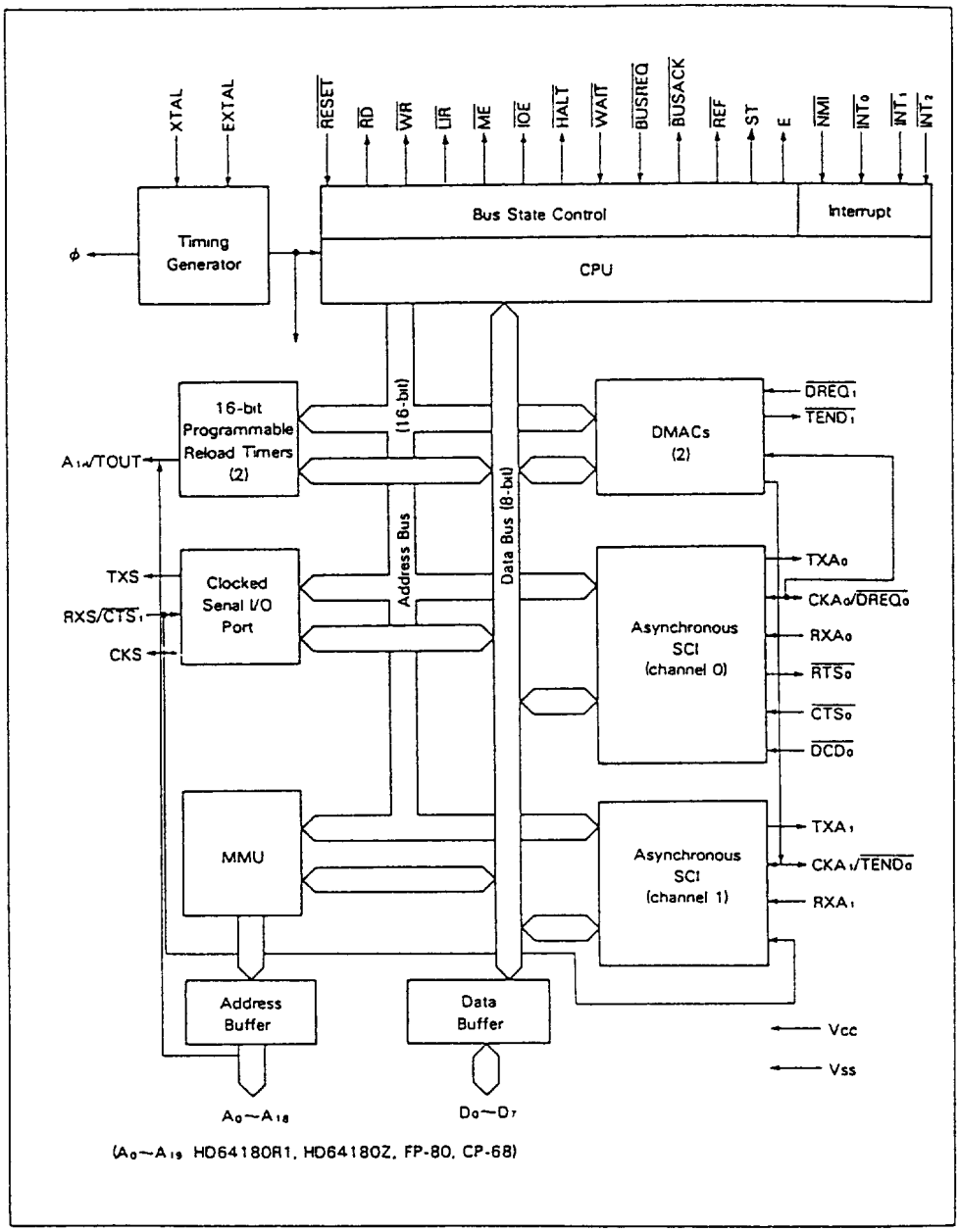


Figure 1.1.1 Block Diagram

HD64180Z - Extra Features :

The Z Mask of the 64180 family differs only slightly from the R1 base device. The HD64180Z includes an extra register which can be programmed to increase the flexibility of the device's bus interface. The main functions of this register are :

VLSI CMOS Process Technology

1) Low power operation

   75mW at at 6MHz
   45mW SLEEP Mode
   25mW IOSTOP Mode
   18mW SYSTEM STOP

2) Vcc = 5V ± 10%
   Fully TTL compatible

Note : CP/M-80 and CP/M Plus are registered trademarks of Digital Research, Inc

1) To adjust bus timing to enable a simpler interface to various Z80* family peripherals

2) To enable an extra interrupt acknowledge cycle - this allows the HD64180Z to operate correctly with the daisy chained interrupt acknowledge scheme, employed by many Z80* family peripheral devices.

* Z80 is a trademark of Zilog Corp.

ZTAT™ - EXPANDING PERFORMANCE FURTHER

What is ZTAT™?

ZTAT™ standard for Zero Turn Around Time. Hitachi's ZTAT microprocessors are powerful single chip devices which feature CMOS EPROM on-chip. Available in a low cost plastic package, the devices can be programmed by the user as they are electrically equivalent to standard EPROMs.

This combination of 'local' programming and a single chip makes available what is in fact a user-programable masked device.

What are the Advantages?

You want to sell equipment. We would also like you to be successful for obvious reasons and the unique advantages that ZTAT™ brings will help you be more successful by enabling :-

You get to market earlier :

Shorter development cycles means earlier availability of an innovative product in an eager market place. This means higher prices - there is less competition - and earlier cash flow.

You offer innovation :

By offering your customer an advantage.

- Portability - by use of low power CMOS technology
- Small size - by use of highly integrated single chip microcomputers and innovative packaging
- High performance - high speed processing
- Lower system cost - single chip CMOS devices in plastic packages allow smaller power supplies

You offer performance :

In ...dard feat... the additional peripheral items enable very powerful single chip designs to be produced utilising :

54 I/O Lines
16 Bit Timers
Analogue Comparator
] Enabling control and processing of real time events

HD647180X - 64180 ZTAT™ SPECIFICATION

The HD647180X is the first in a new family of processors which combines the existing benefits of the 64180 with the outstanding advantages of ZTAT technology.

As well as being fully software compatible with the other family members, the 647180 has additional hardware features over the existing devices.

Standard 64180 Features

- Asynchronous SCI (2 channels)
- Clocked Serial I/O
- MMU with 1M byte Address Capability
- DMAC (2 channels)
- Wait State Generator
- DRAM Refresh Controller
- 2 Channel 16-bit Reloadable Timer

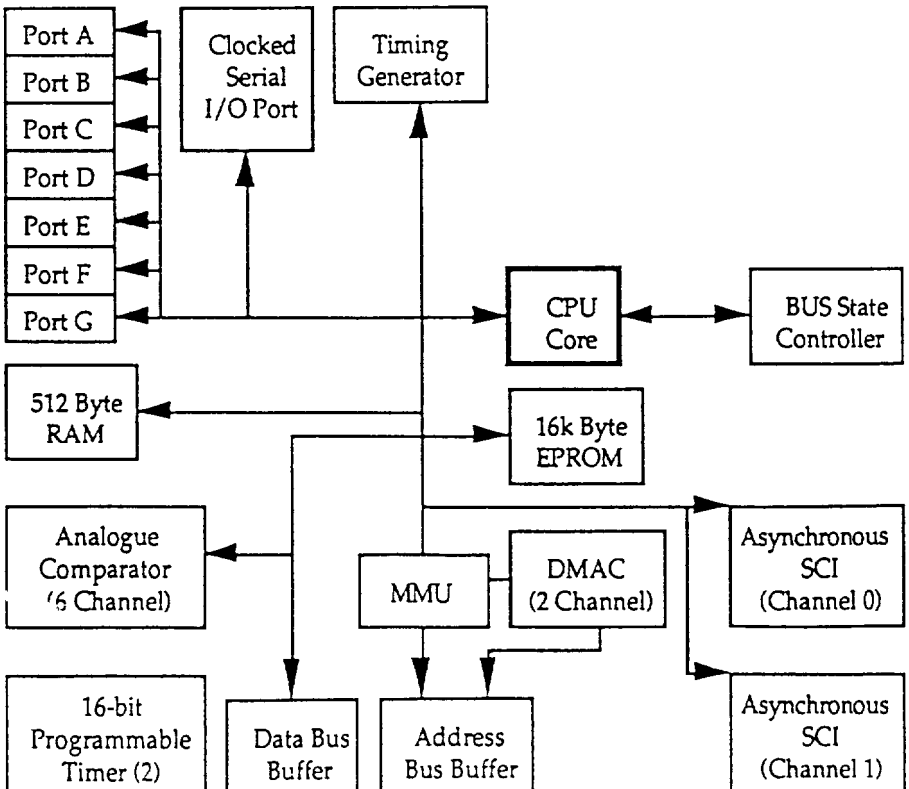
With additional :

- 54 I/O Lines (8 which will sink up to 10mA)
- 16K EPROM on-chip
- 512 bytes on-chip RAM
- 6 channel analogue comparator
- 16 bit programmable timer
- Input capture register
- Output compare
- Timer overflow interrupt

In addition, there is the HD643180X mask programmed device offering the same facilities as the ZTAT part but with the added advantage of a lower unit cost for high volume production runs.

The final member of the X mask group, the HD641180X, offers all the features of the HD647180X but in a ROMless device.

HD647180X Block Diagram



HD64180S - THE NETWORK PROCESSOR UNIT

Based on the powerful HD64180 CPU core, the NPU combines the benefits of high performance and reduced system costs whilst maintaining compatability with the large base of industry standard 8 bit software. CPU operating performance is improved by virtue of high clock speeds and pipelined instructions as well as an enhanced instruction set and integral MMU which will address up to 1M bytes physical address space. The combination of this high performance CPU core with an equally high performance Multi-protocol Serial Comms Interface (MSCI) ensures that the NPU is ideally suited to be a serial bus network controller.

Major Functions

CPU
- Software-compatible with HD64180Z
- 80 type bus interface
- On-chip MMU (1 Mbyte physical address space)

DMAC
- 2 channels
- DMA transfer between memory and memory, memory and I/O (memory-mapped I/O), and memory and MSCI
- Chained-block transfer between memory and MSCI
- Internal interrupt requests available

Multiprotocol Serial Communications Interface
- Full duplex channel
- Asynchronous, byte synchronous (mono, bi or external synchronous) or bit synchronous (HDLC or loop) selectable
- Transmit / receive control using modem control signals (RTSM, CTSM and DCDM)
- Internal Advanced Digital PLL (ADPLL)
  - clock extraction
  - receive data and / or receive clock noise suppression
- On-chip baud rate generator
- Internal interrupt requests available
- Maximum transfer rate 7.1 Mbps (with 10MHz clock)

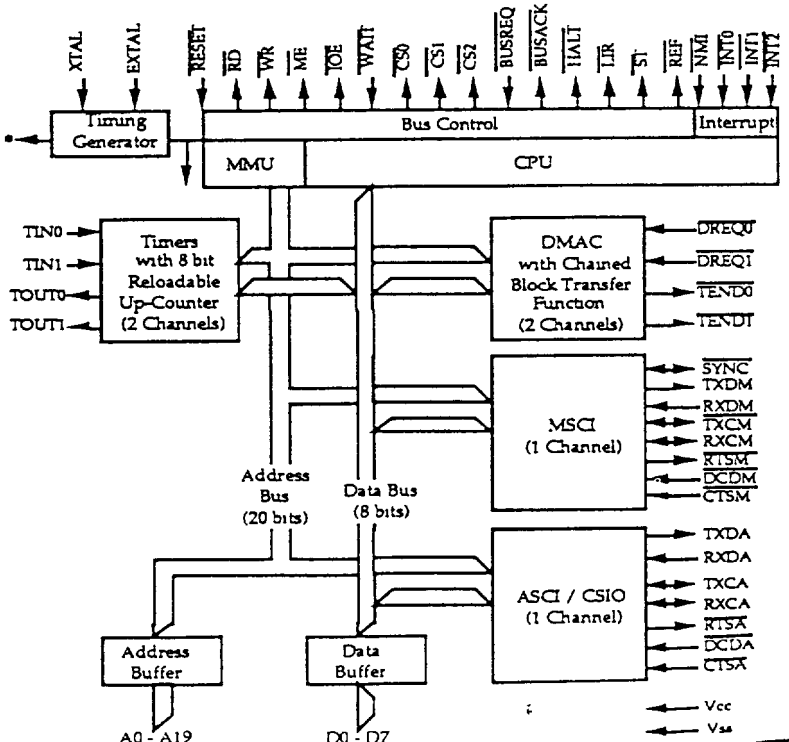
Asynchronous Serial Communications Interface / Clocked Serial I/O Port
- Full duplex channel
- Asynchronous or clocked serial mode (selectable)
- Transmit / receive control using mode control signals (RTSA, CTSA amd DCDA)
- On-chip baud rate generator
- Internal interrupt requests available

Timers
- 2 channels
- 8-bit reloadable up-counter
- Output waveform generator and external event count functions
- Internal interrupt requests available

Interrupt Controller
- 4 external interrupt lines (NM1, INT0, INT1 and INT2)
- 15 internal interrupt sources

Memory Access Support Function
- Internal refresh controller
- Internal wait state controller

Other Functions
- On-chip clock oscillator circuit
- Low power dissipation modes (sleep and system stop)



HD64180 FAMILY - CPU OVERVIEW

The HD64180 combines a high performance CPU core with many of the systems and I/O resources required by a broad range of applications.

The CPU core consists of six functional blocks :

- Clock Generator
- Bus State Controller
- Interrupt Controller
- Memory Management Unit (MMU)
- Central Processing Unit (CPU)
- DMA Controller

CPU Architecture

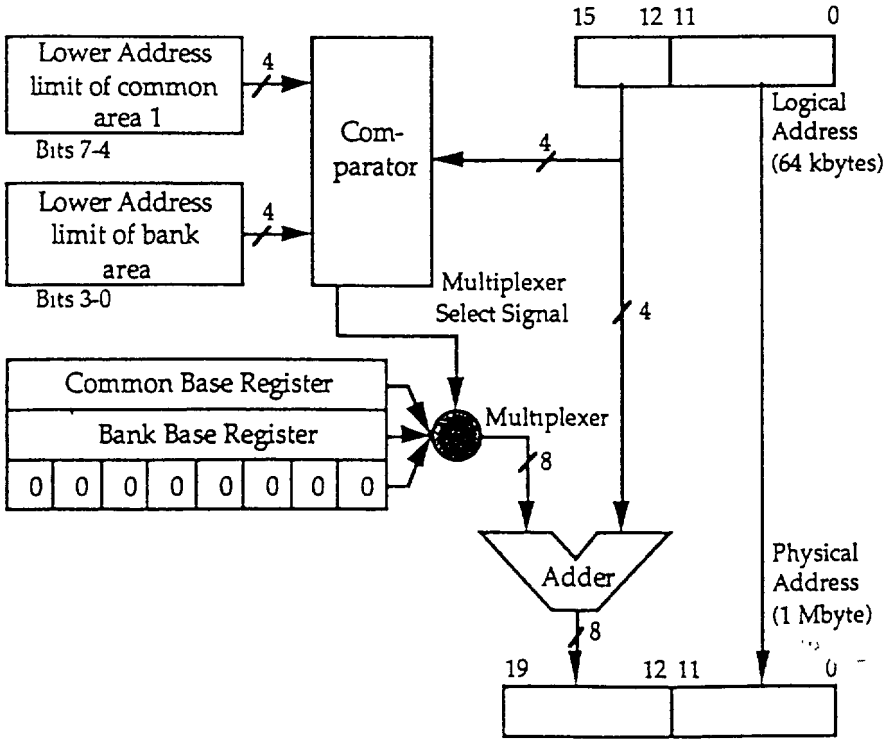
The six CPU core functional blocks are described in this section :

Clock Generator :
The HD64180 contains a crystal oscillator and system clock (ø) generator. A crystal can be directly connected or an external clock input can be provided. In either case, the system clock ø is equal to one-half the input clock. For example, a crystal or external clock input of 8MHz corresponds with a system clock rate of ø = 4MHz. Also, the system clock is programmably prescaled to generate timing for the on-chip I/O and system support devices.

Bus State Controller :
Performs all status / control bus activity. This includes external bus cycle wait state timing. RESET, DRAM refresh and master DMA bus exchange generates 'dual-bus' control signals for compatibility with peripheral devices from 8080 / 6800 families.

Interrupt Controller :
Monitors and prioritises the four external and eight internal interrupt sources. A variety of interrupt response modes are programmable.

Memory Management Unit :
Maps the CPU 64K bytes logical memory address space into up to 1M bytes physical memory address space. The MMU organisation preserves software object code compatibility while providing extended memory access and uses an efficient 'common area - bank area' scheme. I/O accesses bypass the MMU.



MMU Block Diagram

Whether address translation takes place depends on the type of CPU cycle as follows :-

Memory Cycles :
Address Translation occurs for all memory access cycles including instruction and operand fetches, memory data reads and writes, hardware interrupt vector fetch and software interrupt restarts.

I/O Cycles :
The MMU is logically bypassed for I/O cycles. The 16-bit logical I/O address space corresponds directly with the 16-bit physical I/O address space. The high order bits (A16-A19) of the physical address are always 0 during I/O cycles.

DMA Cycles :
When the HD64180 on-chip DMAC is using the external bus, the MMU is physically bypassed. The source and destination registers in the DMAC are directly output on the physical address bus (A0-A19).

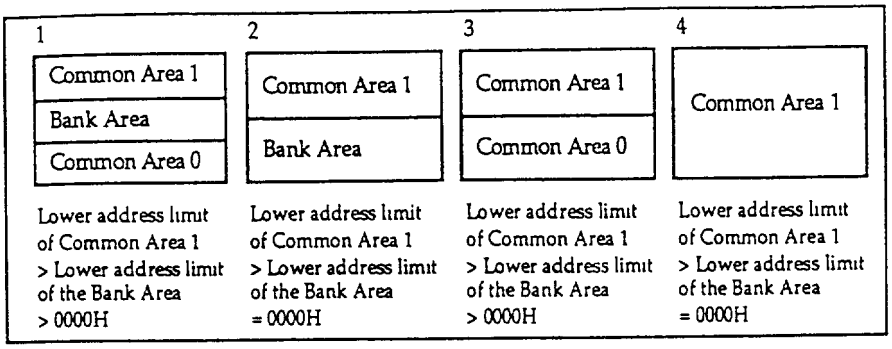
MMU Registers

Three MMU registers are used to program a specific configuration of logical and physical memory :-

- MMU Common / Bank Area Register (CBAR)
- MMU Common Base Register (CBR)
- MMU Bank Base Register (BBR)

CBAR is used to define the logical memory organisation while CBR and BBR are used to relocate logical areas within the physical address space. The resolution for both setting boundaries within the logical

Logical Memory Organisation



space and relocation within the physical space is 4K bytes.

The CAR field of CBAR determines the start address of Common Area 1 (Upper Common) and by default, the end address of the Bank Area. The BAR field determines the start address of the Bank Area and by default, the end address of Common Area 0 (Lower Common).

The CA and BA fields of CBAR may be freely programmed subject only to the restriction that CA may never be less than BA.

DMA Controller (DMAC)

The HD64180 contains a two channel DMA (Direct Memory Access) controller which supports high speed data transfer. Both channels (channel 0 and channel 1) have the following capabilities. At 6MHz system clock data can be transferred at 1 megabyte per second.

Memory Address Space :
Memory source and destination addresses can be directly specified anywhere within the 1M byte physical address space using up to 20 bit source and destination memory addresses. In addition, memory transfers can arbitrarily cross 64K bytes physical address boundaries without CPU interventio:..

Transfer Rate :
Each byte transfer can occur every six clock cycles. Wait states can be inserted in DMA cycles for slow memory or I/O devices. At the system clock (ø) = 6MHz, the DMA transfer rate is as high as 1.0 megabytes / second (no wait states).

Each channel has additional specific capabilities :

Channel 0 :
- Memory - Memory, Memory - I/O, memory - Memory Mapped I/O Transfers
- Memory Address Increment, Decrement, No-change
- Burst or Cycle Steal memory - memory transfer
- DMA to and from both ASCI Channels
- Higher priority than DMAC Channel 1

Channel 1 :
- Memory - I/O Transfer
- Memory Address Increment, Decrement

Interrupts

The HD64180 CPU has twelve interrupt sources, four external and eight internal, with fixed priority.

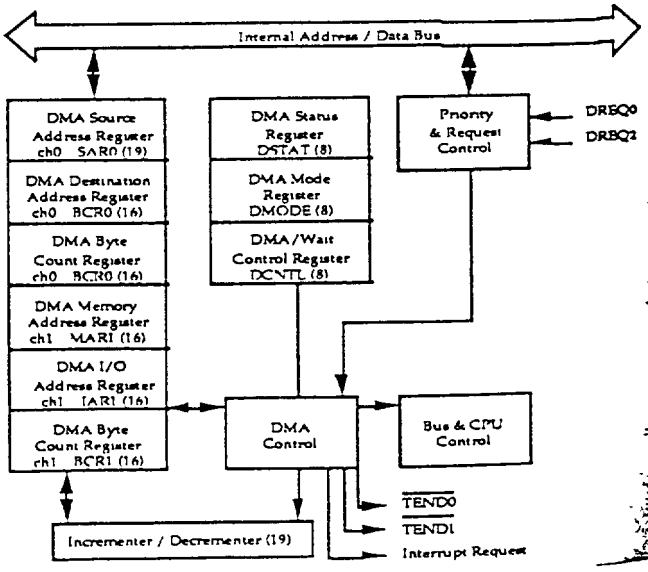
Higher Priority
1) TRAP (undefined op-code trap)
2) NMI (non maskable interrupt)
3) INT0 (maskable interrupt level 0)
4) INT1 (maskable Interrupt level 1)
5) INT2 (maskable interrupt level 2)
6) Timer 0
7) Timer 1
8) DMA channel 0
9) DMA channel 1
10) Clocked Serial I/O Port
11) Asynchronous SCI channel 0
12) Asynchronous SCI channel 1
Low Priority

Trap Interrupt

The HD64180 generates a non-maskable TRAP interrupt when an undefined op-code fetch occurs. This feature can be used to increase software reliability, implement an 'extended' instruction set, or both. TRAP may occur during op-code fetch cycles and also if an undefined op-code is fetched during the interrupt acknowledge cycle for INT0 when Mode 0 is used.

HALT, SLEEP and Low Power Operation

The HD64180 can operate in 4 different modes, HALT mode and



DMAC Block Diagram

three low power operation modes - SLEEP, IOSTOP and SYSTEM STOP. Note that in all operating modes, the basic CPU clock (XTAL, EXTAL) must remain active.

HALT Mode

HALT mode is entered by execution of the HALT instruction and has the following characteristics :

- The internal CPU clock remains active
- All internal and external interrupts can be received
- Bus exchange (BUSREQ and BUSACK) can occur
- Dynamic RAM refresh cycle (REF) insertion continues at the programmed interval
- I/O operations (ASCI, CSI/O and PRT) continue
- The DMAC can operate
- The HALT output pin is asserted LOW
- The external bus activity consists of repeated 'dummy' fetches of the op-code following the HALT instruction

Essentially, the HD64180 operates normally in HALT mode except the instruction execution is stopped.

SLEEP Mode

SLEEP mode is entered by execution of the two byte SLEEP instruction. SLEEP mode has the following characteristics.

- The internal CPU clock stops, reducing power consumption
- The internal crystal oscillator does not stop
- Internal and extral interrupt inputs can be received
- DRAM refresh cycles stop
- I/O operations using on-chip peripherals continue
- The internal DMAC stop
- BUSREQ can be received and acknowledged
- Address outputs go HIGH and all other control signal output become inactive (HIGH)
- Di

SLEEP mode is exited in one of two ways :

RESET exit from SLEEP Mode
If the RESET input is held LOW for more than 3 clock cycles, the HD64180 will exit SLEEP mode and begin the normal RESET sequence with execution starting at address (logical and physical) 0.

Interupt exit from SLEEP Mode
The SLEEP mode is exited by detection of an external or internal interrupt.

IOSTOP Mode

IOSTOP mode is entered by setting the IOSTP bit of the I/O Control Register to 1. In this case, on-chip I/O (ASCI, CSI/O, PRT) stops operating, reducing power consumption. However, the CPU continues to operate. Recovery from IOSTOP mode is be resetting the IOSTP bit in ICR to 0.

SYSTEM STOP Mode

SYSTEM STOP mode is the combination of SLEEP and IOSTOP modes. SYSTEM STOP mode is enetered by setting the IOSTP bit in ICR = 1 followed by execution of the SLEEP instruction. Recovery from SYSTEM STOP mode is the same as recovery from SLEEP mode, noting that internal I/O sources (disabled by IOSTOP) cannot guarantee a recovery interrupt.

Improved Software Capability

The 64180 is object code compatible with standard 8 bit operating systems and application software. The instruction set also contains 12 new instructions which when combined with the pipeline architecture, improve system performance, reliability and efficiency.

New Instructions

In addition to the standard instruction set, the following new instructions are available :

SLP-SLEEP
The SLP instruction causes the HD64180 to enter SLEEP low power consumption mode.

MLT - Multiply
The MLT performs unsigned multiplication on two 8 bit numbers yielding a 16 bit result. MLT may specify BC, DE, HL or 16 SP registers. In all cases, the bit result is returned in that register.

INO g, (m) - Input, Immediate I/O Address
The contents of the immediately specified 8 bit I/O address are input into the specified register. When I/O is accessed, 00H is output in high-order bits of address automatically.

OUTO g, (m) - Output, Immediate I/O Address
The contents of the specified register are output to the immediately specified 8 bit I/O address. When I/O is accessed, 00H is output in high-order bits of address automatically.

OTIM, OTIMR, OTDM, OTDMR - Block I/O
The contents of memory pointed to by HL is output to the I/O address in (C). The memory address (HL) and I/O address (C) are incremented in OTIM and OTIMR and decremented in OTDM and OTDMR respectively. B register is decremented. The OTDMR and OTDMR variants repeat the above sequence until register B is decremented to 0. Since the I/O address (C) is automatically incremented or decremented, these instructions are useful for block I/O (such as HD64180 on-chip I/O) initialisation. When I/O is accessed, 00H is output in high order bits of address automatically.

TSTIOm - Test I/O Port
The contents of the I/O port addressed by C are ANDed with immediately specified 8 bit data and the status flags are updated. The I/O is accessed, 00H is output in higher bits of address automatically.

TSTg - Test Register
The contents of the specified are ANDed with the accumulator (A) and the status flags are updated. The accumulator and specified register are not changed (non-destructive AND).

TDTm - Test Immediate
The contents of the immediatly specified 8 bit data are ANDed with the accumulator (A) and the status flags are updated. The accumulator is not changed (non-destructive AND).

TDT (HL) - Test Memory
The contents of memory pointed to by HL are ANDed with the accumulator (A) and the status flags are updated. The memory contents and accumulator are not changed (non-desructive AND).

HD64180 - SOFTWARE ARCHITECTURE

Registers

The HD64180 main registers (Register Set GR) consist of an 8 bit accumulator (A), 8 bit status flag register (F) and three general purpose registers (BC, DE, HL). These latter registers may be treated as 16 bit registers or as individual 8 bit registers depending on the instruction being executed. The main registers also include Special Registers which consist of the interrupt Vector (I), R Counter (R), two 16 bit index registers (IX and IY), stack pointer (SP) and the program counter (PC).

The HD64180 also includes an alternate register set (Register Set GR') for the accumulator, flag and general purpose registers. While these registers are not directly accessible, their contents can be programmably exchanged at high speed with those of the main register set. This capability may be used for high speed context switch or for storing key, frequently accessed variables.

GR Register Set

Accumulator (A)	Flag Register (F)
B Register	C Register
D Register	E Register
H Register	L Register

8 bits — 8 bits

GR General-purpose Registers

GR' Register Set

Accumulator (A')	Flag Register (F')
B' Register	C' Register
D' Register	E' Register
H' Register	L' Register

8 bits — 8 bits

GR' General-purpose Registers

Dedicated Register Set

Interrupt Vector Register (I)	R Counter (R)
Index Register	(IX)
Index Register	(IY)
Stack Pointer	(SP)
ProgramCounter	(PC)

16 bits

Register Description

Accumulators (A and A')

The accumulators are the primary registers used for 8-bit arithmetic, logical and shift operations.

Flag Registers (F and F')

Flag registers indicate the status of the operation result.

General-Purpose Registers B, C, D, E, H and L

The six 8-bit general-purpose registers in register set GR are used for operations and addressing. Registers B and C, D and E, or H and L can be used together as 16-bit registers.

General-Purpose Registers B', C', D', E', H' and L'

The six 8-bit general-purpose registers in register set GR' function in the same way as registers B, C, D, E, H and L.

Interrupt Vector Register (I)

The interrupt vector register specifies the high order byte of a 16-bit interrupt vector. This register is used for INT0 mode 2, INT1, INT2 and internal interrupts except TRAP.

R Counter (R)

The 7-bit counter indicates the number of executed opcode fetch cycles.

S	Z	-	H	-	P/V	N	C

F Register

Index Registers (IX and IY)

The 16-bit index registers are used for index addressing and 16-bit operations.

Stack Pointer (SP)

The 16-bit stack pointer register holds the address of the top of the stack.

Program Counter (PC)

The 16-bit program counter register holds the logical address of the next instruction to be executed.

Flag (F) Description

The flag register stores the logical state reflecting the results of instruction execution. The contents of the flag register are used to control program flow and instruction operation.

S : Sign (bit 7) :

S stores the state of the most significant bit (bit 7) of the result. This is useful for operations with signed numbers in which values with bit 7 = 1 are interpreted as negative.

Z : Zero (bit 6) :

Z is set = 1 when instruction execution results containing 0. Otherwise, Z is reset = 0.

H : Half Carry (bit 4) :

H is used by the DAA (Decimal Adjust Accumulator) instruction to reflect, borrow or carry from the least significant 4 bits and thereby adjust the results of BCD addition and subtraction.

P/V : Parity / Overflow (bit 2):

PV serves a dual purpose. For logical operations P/V is set = 1 if the number of 1 bits in the result is even and P/V is reset = 0 if the number of 1 bits in the result is odd. For two's complement arithmetic, P/V is set = 1 if the operation produces a result which is outside the allowable range (+127 to -128 for 8 bit operations, +32767 to -32768 for 16 bit operations)

N : Negative (bit 1) :

N is set = 1 if the last arithmetic instruction was a subtract operation (SUB, DEC, CP, etc.), and N is reset = 0 if the last arithmetic instruction was an addition operation (ADD, INC, etc.).

C : Carry (bit0) :

C is set = 1 when a carry (addition) or borrow (subtraction) from the most significant bit of the result occurs. C is also affected by accumulator logic operations such as shifts and rotates.

Addressing Modes

The HD64180 instruction set includes eight addressing modes :

Register Direct (REG)

Many op-codes contain bit fields specifying registers to be used for the operation. The exact bit field definition varies depending on instruction as follows.

Implied Register (IMP)

Certain op-codes automatically imply register usage, such as the arithmetic operations which inherently reference the accumulator, Index Registers, Stack Pointer, and General-Purpose Registers.

Relative (REL)

Relative addressing mode is only used by the conditional and unconditional branch instructions. The branch displacement (relative to the contents of the program counter) is contained in the instruction.

Register Indirect (REG)

The memory operand address is contained in one of the 16-bit General- purpose Registers (BD, DE and HL).

Indexed (INDX)

The memory operand address is calculated using the contents of an Index Register (IX or IY) and an 8 bit signed displacement specified in the instruction.

Extended (EXT)

The memory operand address is specified by two bytes contained in the instruction.

I/O (IO)

IO addressing mode is used by I/O instructions. This mode specifies I/O address (IOE = 0) and outputs then as follows :

- An operand is output to A0 - A7. The contents of accumulator is output to A8 - A15
- The contents of Register B is output to A0 - A7. The contents of Register C is output to A8 - A15
- An operand is output to A0 - A7. 00H is output to A8 - A15. (Useful for internal I/O register access)
- The contents of Register C is output to A0 - A7. 00H is output to A8 - A15. (Useful for internal I/O register access)

I/O RESOURCES

The I/O provided by the 64180 devices varies from device to device, an overview is provided below.

Asynchronous Serial Communication Interface (ASCI)

The HD64180 on-chip ASCI has two independent full duplex channels. Based on full programmability of the following functions, the ASCI can directly communicate with a wide variety of standard UARTs (Universal Asynchronous Receiver Trans- mitter) including the HD6350 CMOS ACIA and the Serial Communication Interface (SCI) contained in H8, H16 and 6301 processors.

The key functions for ASCI are shown below. Each channel is independently programmable.

- Full duplex communication
- 7 or 8 bit data length
- Program controlled 9th data bit for multiprocessor communication
- 1 or 2 stop bits
- Odd, even, no parity
- Programmable baud rate generator, /16 and /64 modes. Speed to 38.4k bits per second (CPU fc = 6.144MHz)
- Modem control signals - channel 0 has DCDO, CTSO and RTSO channel 1 has CTS1
- Programmable interrupt condition enable and disable
- Operate with on-chip DMAC

Clocked Serial I/O Port (CSI/O)

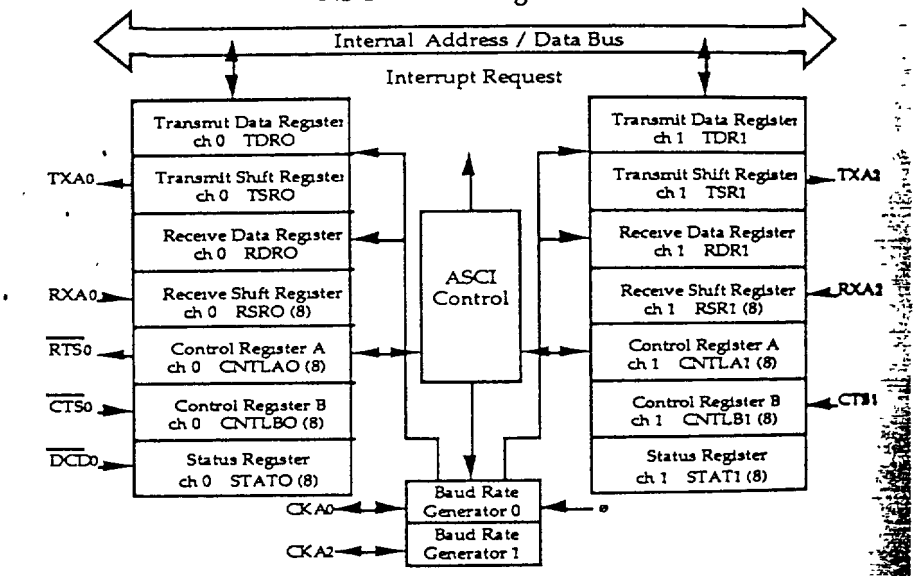
The HD64180 includes a simple, high speed clock synchronous serial I/O port. The CSI/O includes transmit / receive (half duplex), fixed 8 bit data and internal or external data clock selection. High speed operation (baud rate as high as 200k bits /) is provided.

The CSI/O is ideal for implementing a multiprocessor communication link between the HD64180 and the HMCS400 Series (4 bit) and the HD6301 Series (8 bit) single chip controllers as well as additional HD64180 CPU's. These secondary devices may typically perform a portion of the system I/O processing such as keyboard scan / decode, LCD interface, etc.

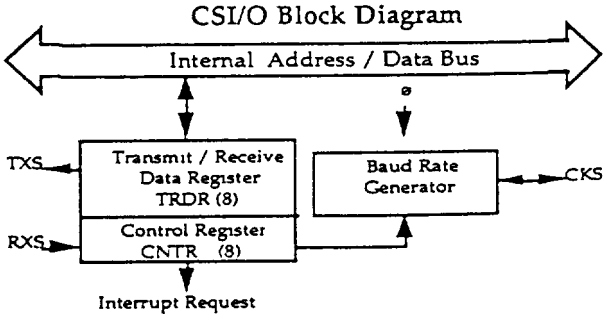
Programmable Reload Timer (PRT)

The HD64180 contains a two channel 16 bit Programmable Reload Timer. Each PRT channel contains a 16 bit down counter and a 16 bit reload register. The down counter can be directly read and written and a down counter overflow interrupt can be programmably enabled or disabled. In addition, PRT channel 1 has aTOUT output pin (pin 31 - multiplexed with A18) which can be set HIGH or LOW and toggled. Thus PRT1 can perform programmable output waveform generation.

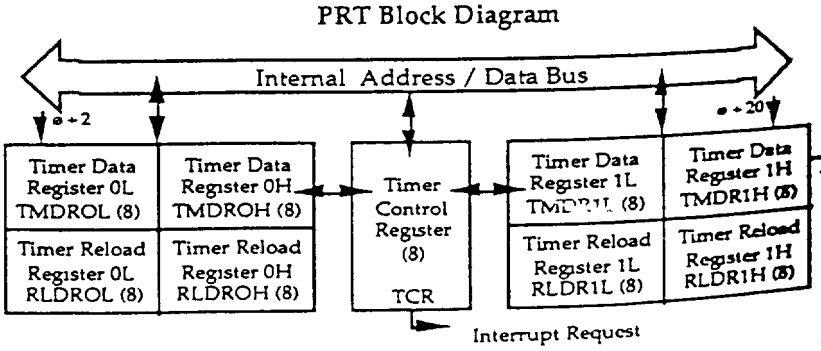
ASCI Block Diagram



CSI/O Block Diagram



PRT Block Diagram



MULTIPROTOCOL SERIAL COMMUNICATIONS INTERFACE (MSCI)

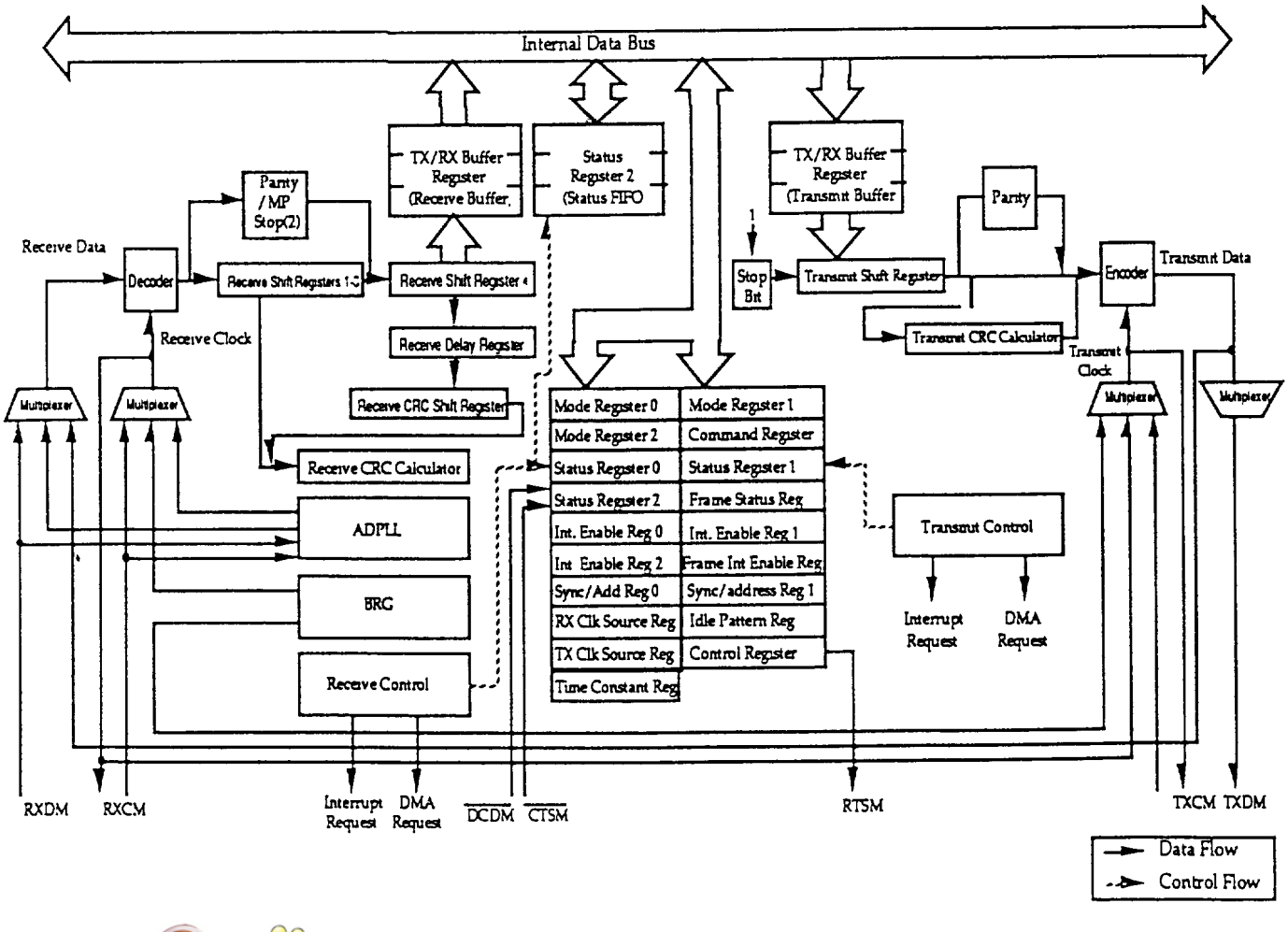
The most important peripheral on the NPU is the Multiprotocol Serial Communications interface. This is the peripheral that enables the processor to operate as a powerful serial communications bus controller. The MSCI is capable of supporting three different operating modes : asynchronous, byte synchronous and bit synchronous.

The MSCI includes the following functions :-

- program-selectable operating modes; asynchronous, byte synchronous and bit synchronous
- transmission codes NRZ, NRZI, Manchester, FM0 and FM1 are supported. (Only NRZ code is supported in the asynchronous mode.)
- full duplex communications, auto echo and local loop back functions are available
- separate transmit and receive buffers are provided for each three stages
- modem control signals RTSM, CTSM and DCDM can be automatically controlled using the auto-enable function :-

  RTSM (Request To Send) - general-purpose output / transmission request
  CTSM (Clear To Send) - general-purpose input / transmit enable / transition-triggered interrupt
  DCDM (Data Carrier Detect) - general-purpose input / receive carrier detection / transition-triggered interrupt
- programmable on-chip baud rate generator for transmission and reception
- clock is program-selectable from three sources: external clock input, on-chip baud rate generator output, and internal ADPLL (Advanced Digital PLL) output
- noise suppression function for receive clock and receive data
- data transmission rate of 7.1 Mbps for a 10MHz system clock
- four internal interrupt signals : RXRDY, TXRDY, RXINT and TXINT

MSCI Block Diagram



Development Support - The Path To Success

Clearly, to enable the full benefit of the advanced silicon to be realised in the shortest possible time, software support must match the device in availability and performance. Hitachi is an innovator in development equipment, producing systems, software and emulators to support our range of processors.

HS180ASE - Adaptive System Emulator

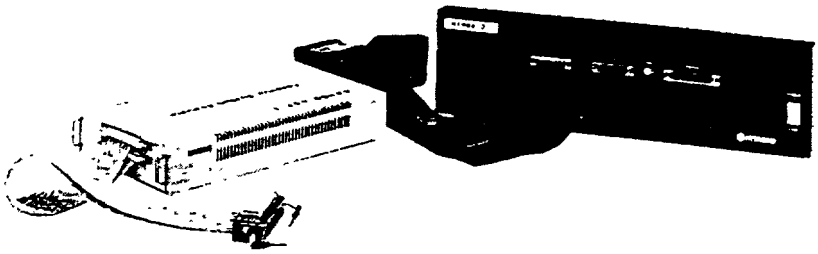
This is a real time emulator for the HD64180 which can interface to a variety of host systems. Program generation would be typically carried out on the host computer, such as PC or VAX and then down loaded into the memory of the emulator. The emulator can then be controlled directly by a dumb terminal. The unit features a floppy disc which can be used to load or save user programs without requiring access to the host system.

Features

- Supports real time evaluation up to 10MHz
- Interfaces with host via standard RS232C link
- Object program may be loaded or saved directly on internal floppy disc
- Real time trace facility
- Memory mapping in 4K units between emulator and target system
- Line assembler and full disassembler facilities
- Symbolic debugging facilities
- Coverage feature giving indication of memory usage

HS180ASE Options

Processor	Emulator	Buffer Box	Standard Header
HD64180R1	HS180AST01H	HS180ABX02H	64 pin dil (shrink)
HD64180Z	HS180AST01H	HD180ABX03H	64 pin dil (shrink)
HD647180X HD643180X HD641180X	HS180AST01H	HD180ABX04H	PLCC 84
HD64180S	HS180AST01H	HD180ABX05H	PLCC 84



Hitachi Software Support

We have introduced a range of powerful cross assemblers to run on the most popular most computers.

3rd Party Development Support

We realise you may already have a development system or host that you wish to continue using. For these reasons we give full details of third party software and emulators which are available for prototype development.

SUPPLIER	SOFTWARE	HOST	
		IBM PC	VAX
Kontron 0923 45991	X-Ass	●	×
	C-Compiler	●	×
Microtec 0256 57551	X-Ass	●	●
	C-Compiler	●	●
Ashling +353-61-334466	X-Ass	●	
	C-Compiler		
Pentica 0734 792101	X-Ass	●	●
	C-Compiler	●	●
R.T.S. 0624 26021	X-Ass	●	●
	C-Compiler		
Crossware 0763 61539	X-Ass	●	
	C-Compiler	●	●
I.A.R. + 018 157920	X-Ass	●	●
	C-Compiler	●	●
Creative Data +089 854 3080	X-Ass	●	●
	C-Compiler	●	●
M.S.S 0494 41661	X-Ass	●	●
	C-Compiler	●	●
Dux 0420 63742	X-Ass	●	●
	C-Compiler	●	●
Hewlett Packard 0734 784774	X-Ass	●	
	C-Compiler		

● Available
× Under Development

HD64180 - PACKAGE OPTIONS

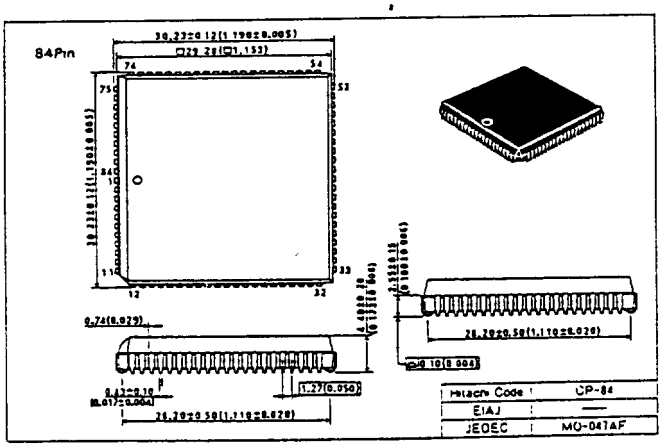
In order to support the package most suitable for your application, the HD64180 is available in both through-hole and surface mounting packages.

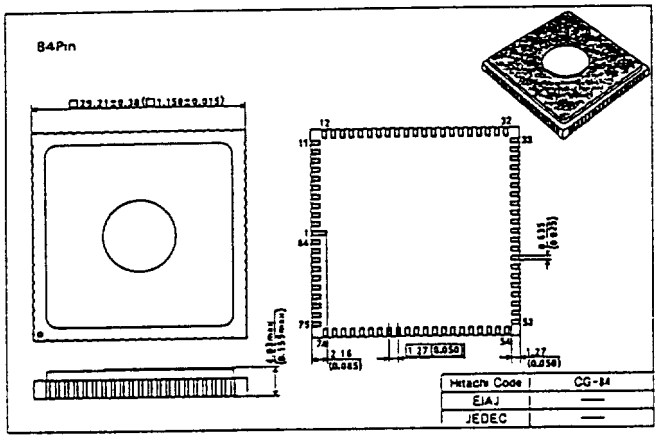
DIL
The popular dual-in-line package features through-hole mounting for socketing and easy assembly. The shrink packages have pins on a 0.07 inch pitch. A 64 pin shrink package (DP-64S) occupys the almost the same area as a standard 40 DIL package.

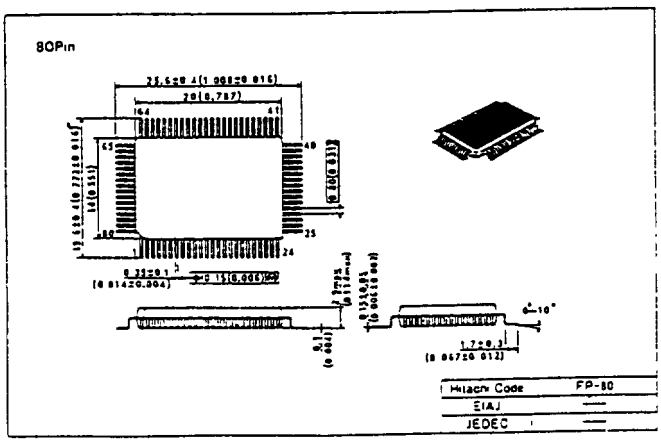
PLCC
The plastic leaded chip carrier is a surface mounting package which features the 'J' bend lead frame. The package has good environmental performance and is available in wide temperatuire range version.

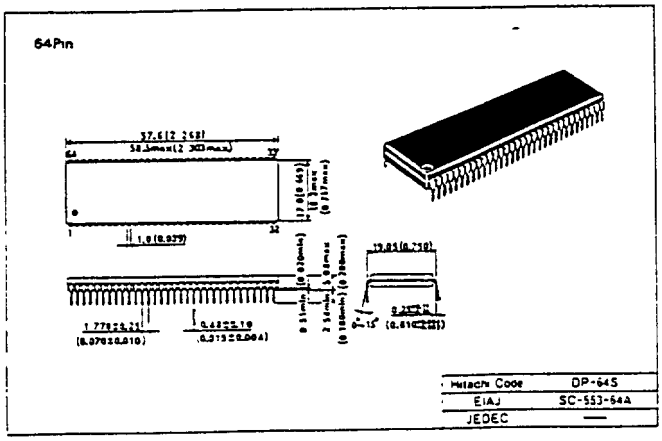
FPP
The flat plastic package us a surface mounting package which features the 'gull wing' style lead frame. This package achieves very high package density.

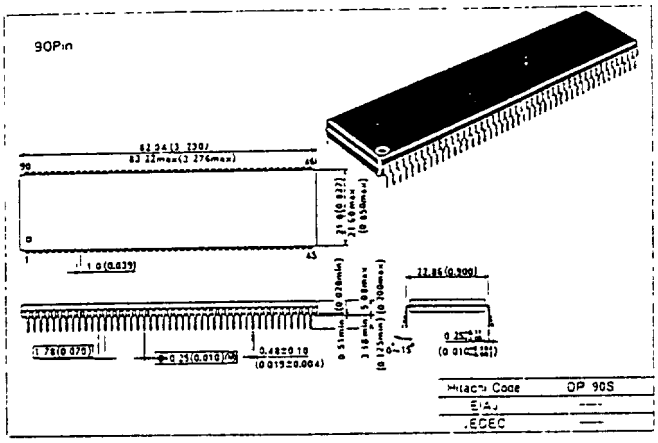
Processor / Package	HD64180R1/2	HD647180 HD643180 HD64180	HD64180S
DP-64S	●		
DP-90S		●	
CP-68	●		
CP-84		●	
LCC-84		●	
FP-80	●	●	●

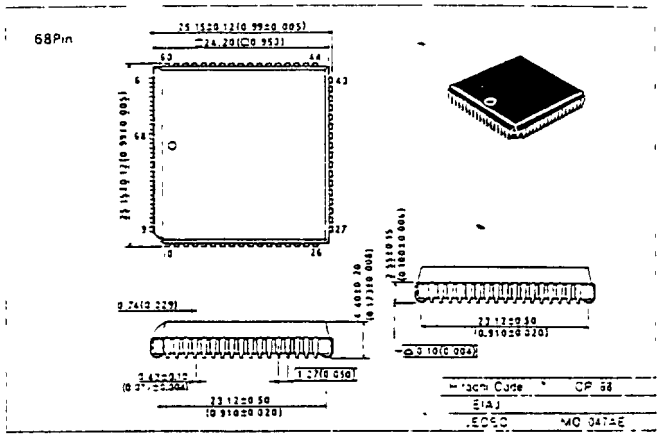


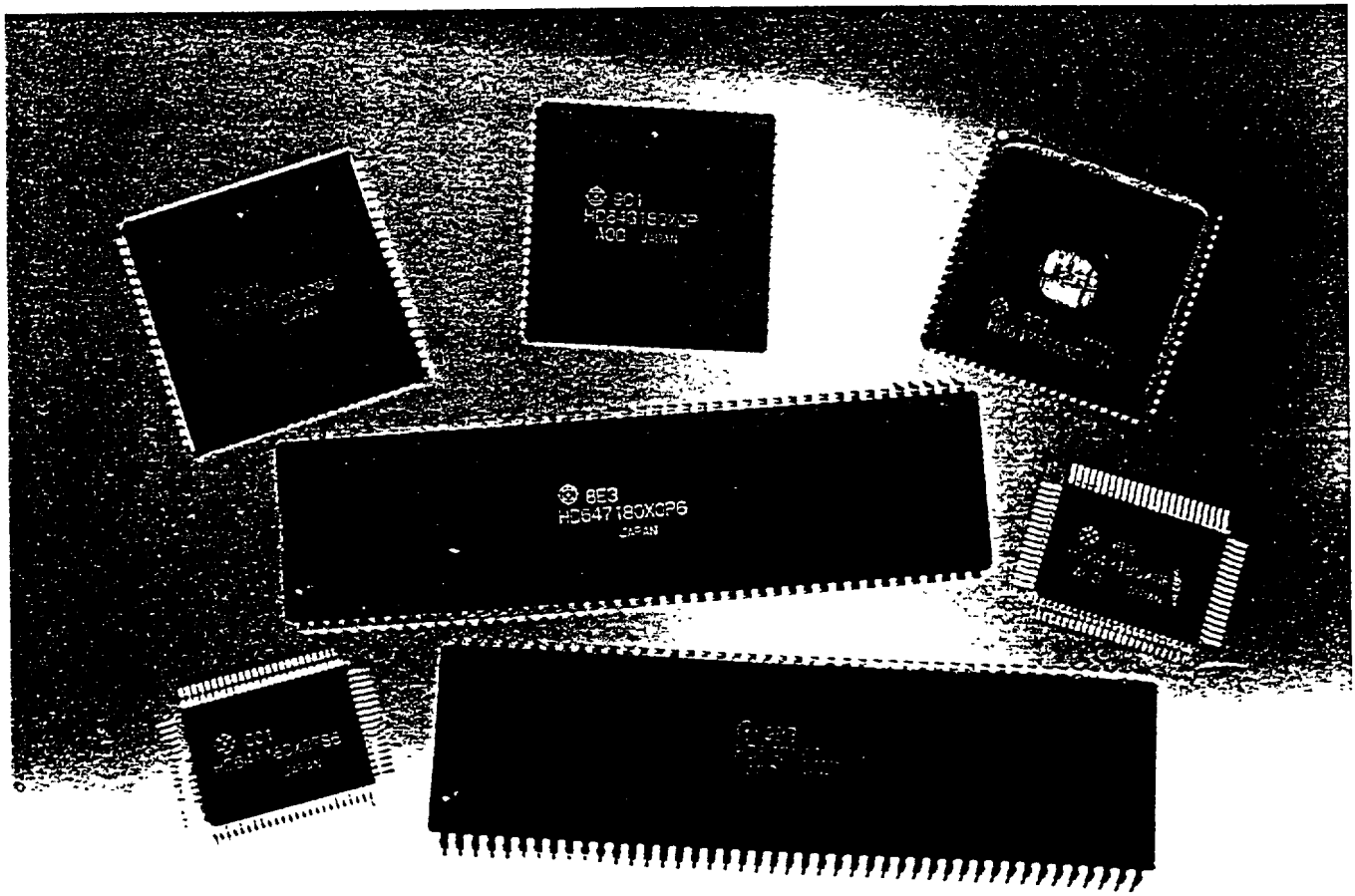












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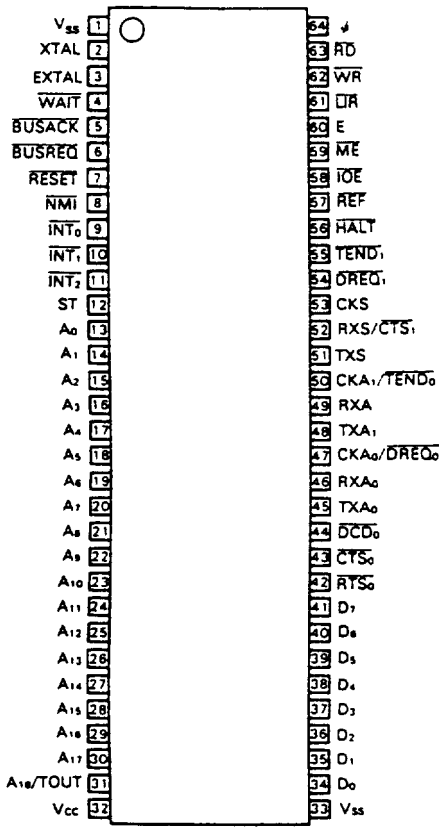

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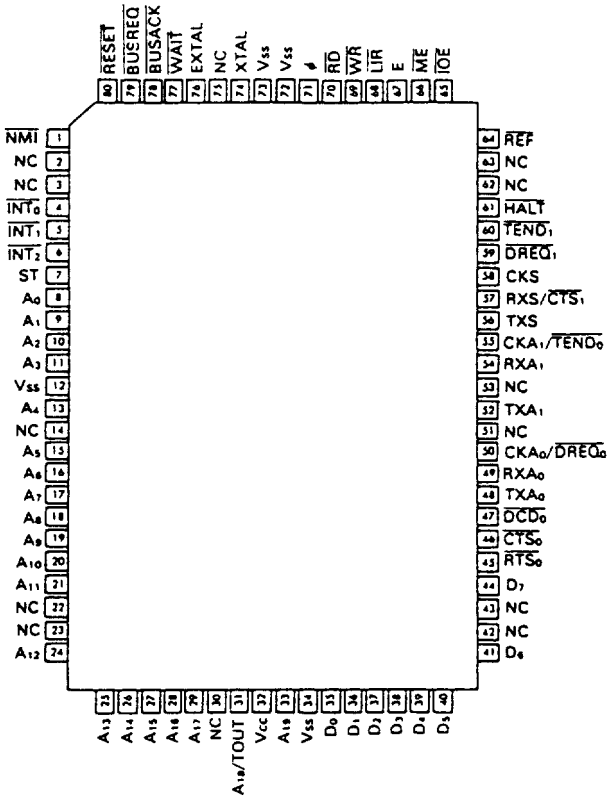

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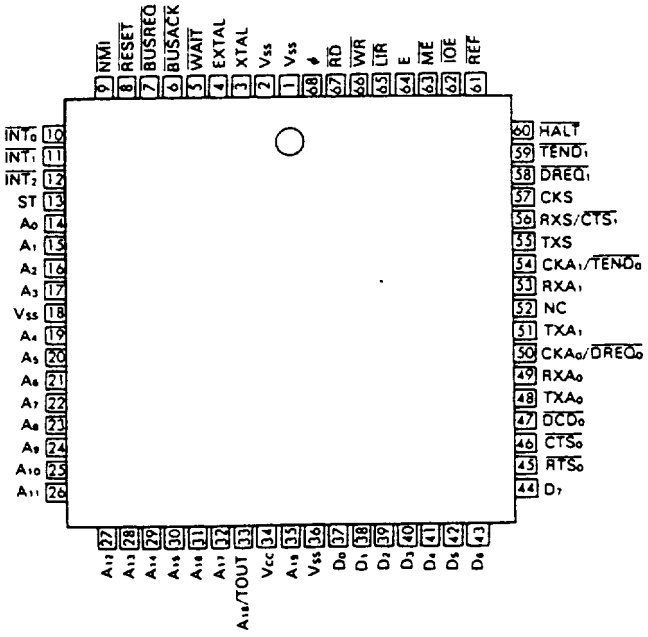

(CP-68)

NC: Not connected.
Please leave the
NC pins open