1.0 INTRODUCTION

The Special Environment Intel386 EX Embedded Processor is a highly integrated, 32-bit, fully static CPU optimized for harsh environment, embedded control applications. With a 16-bit external data bus, a 26-bit external address bus, and Intel's System Management Mode (SMM), the Special Environment Intel386 EX embedded processor brings the vast software library of Intel386 architecture to embedded systems. It provides the performance benefits of 32-bit programming with the cost savings associated with 16-bit hardware systems.

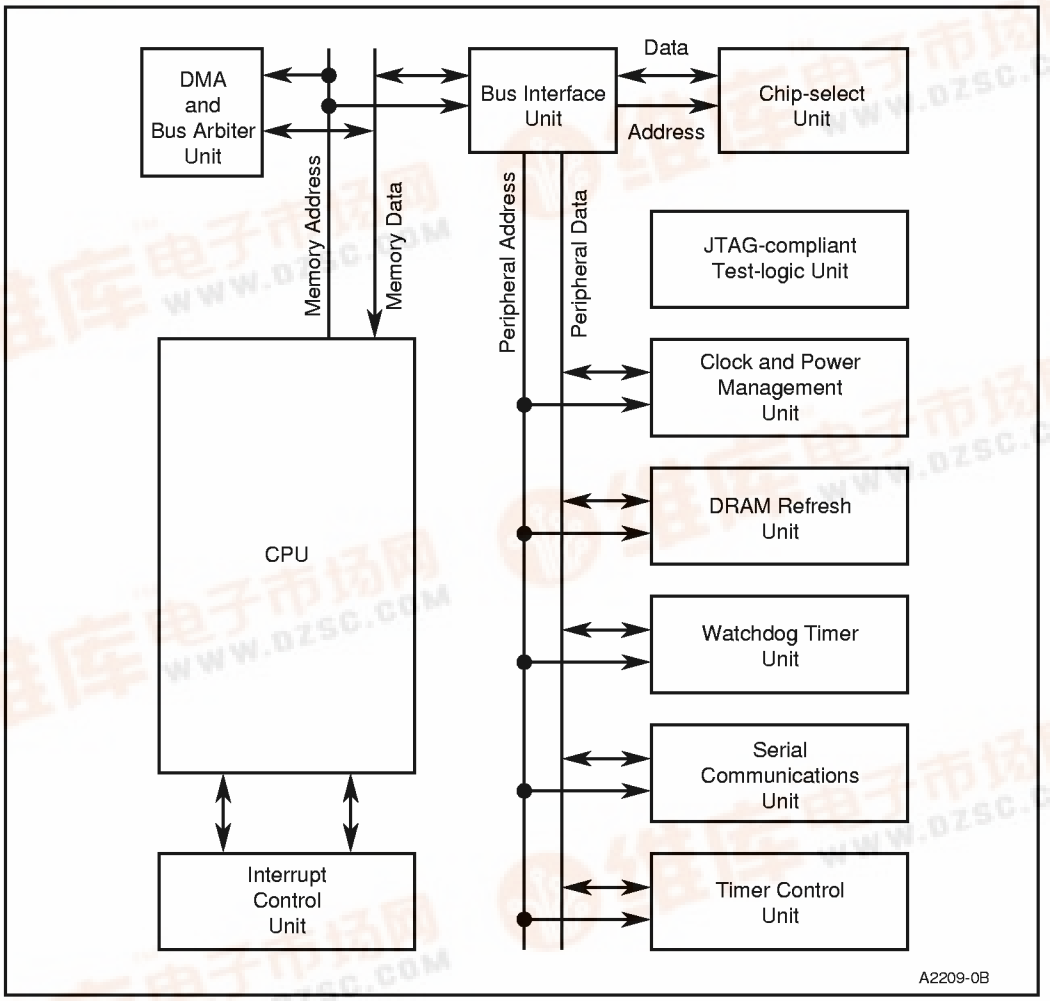


Figure 1. Intel386™ EX Embedded Processor Block Diagram

2.0 PIN ASSIGNMENT

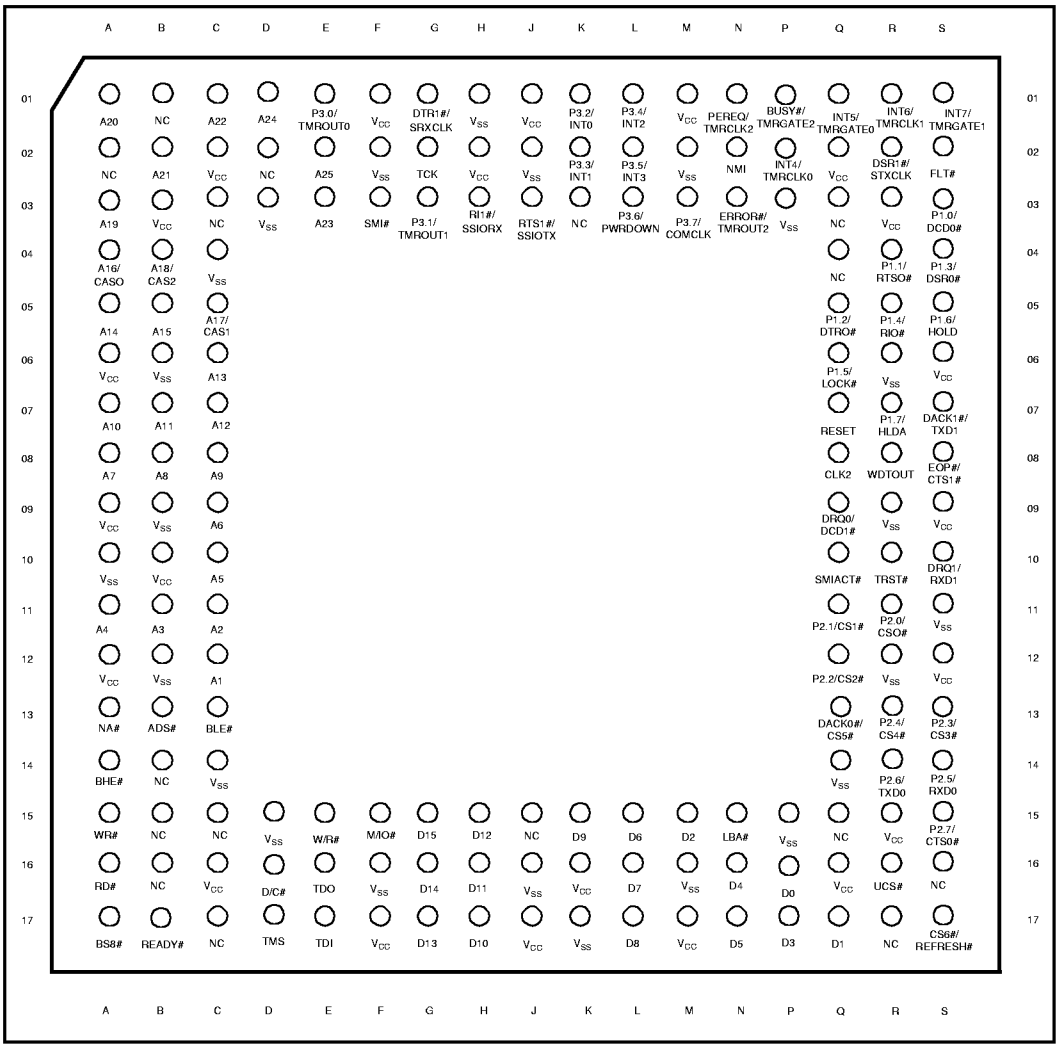


Figure 2. 168-Lead Pin Grid Array Pinout (Bottom View — Pin Side)

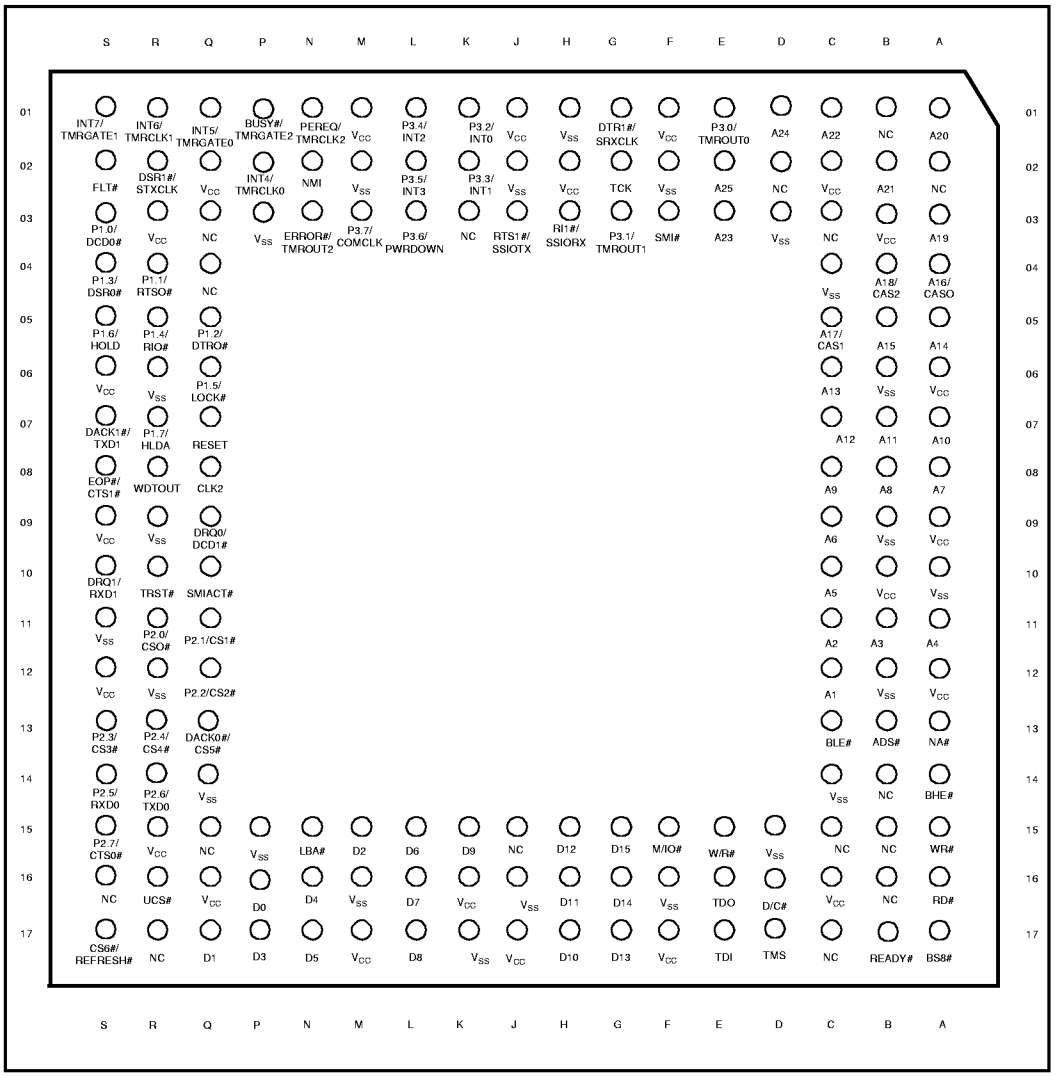


Figure 3. 168-Lead Pin Grid Array Pinout (Top View — Component Side)

Table 1. 168-Lead Pin Grid Array Pin Assignment

Pin	Symbol	Pin	Symbol	Pin	Symbol	Pin	Symbol
A1	A20	C9	A6	J15	NC	Q10	SMIACT#
A2	NC	C10	A5	J16	V_{SS}	Q11	P2.1/CS1#
A3	A19	C11	A2	J17	V_{CC}	Q12	P2.2/CS2#
A4	A16/CAS0	C12	A1	K1	P3.2/INT0	Q13	DACK0#/CS5#
A5	A14	C13	BLE#	K2	P3.3/INT1	Q14	V_{SS}
A6	V_{CC}	C14	V_{SS}	K3	NC	Q15	NC
A7	A10	C15	NC	K15	D9	Q16	V_{CC}
A8	A7	C16	V_{CC}	K16	V_{CC}	Q17	D1
A9	V_{CC}	C17	NC	K17	V_{SS}	R1	INT6/TMRCLK1
A10	V_{SS}	D1	A24	L1	P3.4/INT2	R2	DSR1#/STXCLK
A11	A4	D2	NC	L2	P3.5/INT3	R3	V_{CC}
A12	V_{CC}	D3	V_{SS}	L3	P3.6/PWRDOWN	R4	P1.1/RTS0#
A13	NA#	D15	V_{SS}	L15	D6	R5	P1.4/RI0#
A14	BHE#	D16	D/C#	L16	D7	R6	V_{SS}
A15	WR#	D17	TMS	L17	D8	R7	P1.7/HLDA
A16	RD#	E1	P3.0/TMROUT0	M1	V_{CC}	R8	WDTOUT
A17	BS8#	E2	A25	M2	V_{SS}	R9	V_{SS}
B1	NC	E3	A23	M3	P3.7/COMCLK	R10	TRST#
B2	A21	E15	W/R#	M15	D2	R11	P2.0/CS0#
B3	V_{CC}	E16	TDO	M16	V_{SS}	R12	V_{SS}
B4	A18/CAS2	E17	TDI	M17	V_{CC}	R13	P2.4/CS4#
B5	A15	F1	VCC	N1	PEREQ/TMRCLK2	R14	P2.6/TXD0
B6	V_{SS}	F2	VSS	N2	NMI	R15	V_{CC}
B7	A11	F3	SMI#	N3	ERROR#/TMROUT2	R16	UCS#
B8	A8	F15	M/IO#	N15	LBA#	R17	NC
B9	V_{SS}	F16	V_{SS}	N16	D4	S1	INT7/TMRGATE1
B10	V_{CC}	F17	V_{CC}	N17	D5	S2	FLT#
B11	A3	G1	DTR1#/SRXCLK	P1	BUSY#/TMRGATE2	S3	P1.0/DCD0#
B12	V_{SS}	G2	TCK	P2	INT4/TMRCLK0	S4	P1.3/DSR0#
B13	ADS#	G3	P3.1/TMROUT1	P3	V_{SS}	S5	P1.6/HOLD
B14	NC	G15	D15	P15	V_{SS}	S6	V_{CC}
B15	NC	G16	D14	P16	D0	S7	DACK1#/TXD1
B16	NC	G17	D13	P17	D3	S8	EOP#/CTS1#
B17	READY#	H1	V_{SS}	Q1	INT5/TMRGATE0	S9	V_{CC}
C1	A22	H2	V_{CC}	Q2	V_{CC}	S10	DRQ1/RXD1
C2	V_{CC}	H3	RI1#/SSIORX	Q3	NC	S11	V_{SS}
C3	NC	H15	D12	Q4	NC	S12	V_{CC}
C4	V_{SS}	H16	D11	Q5	P1.2/DTR0#	S13	P2.3/CS3#
C5	A17/CAS1	H17	D10	Q6	P1.5/LOCK#	S14	P2.5/RXD0
C6	A13	J1	V_{CC}	Q7	RESET	S15	P2.7/CTS0#
C7	A12	J2	V_{SS}	Q8	CLK2	S16	NC
C8	A9	J3	RTS1#/SSIOTX	Q9	DRQ0/DCD1#	S17	CS6#/REFRESH#

NOTE: NC indicates that the pin is not connected.

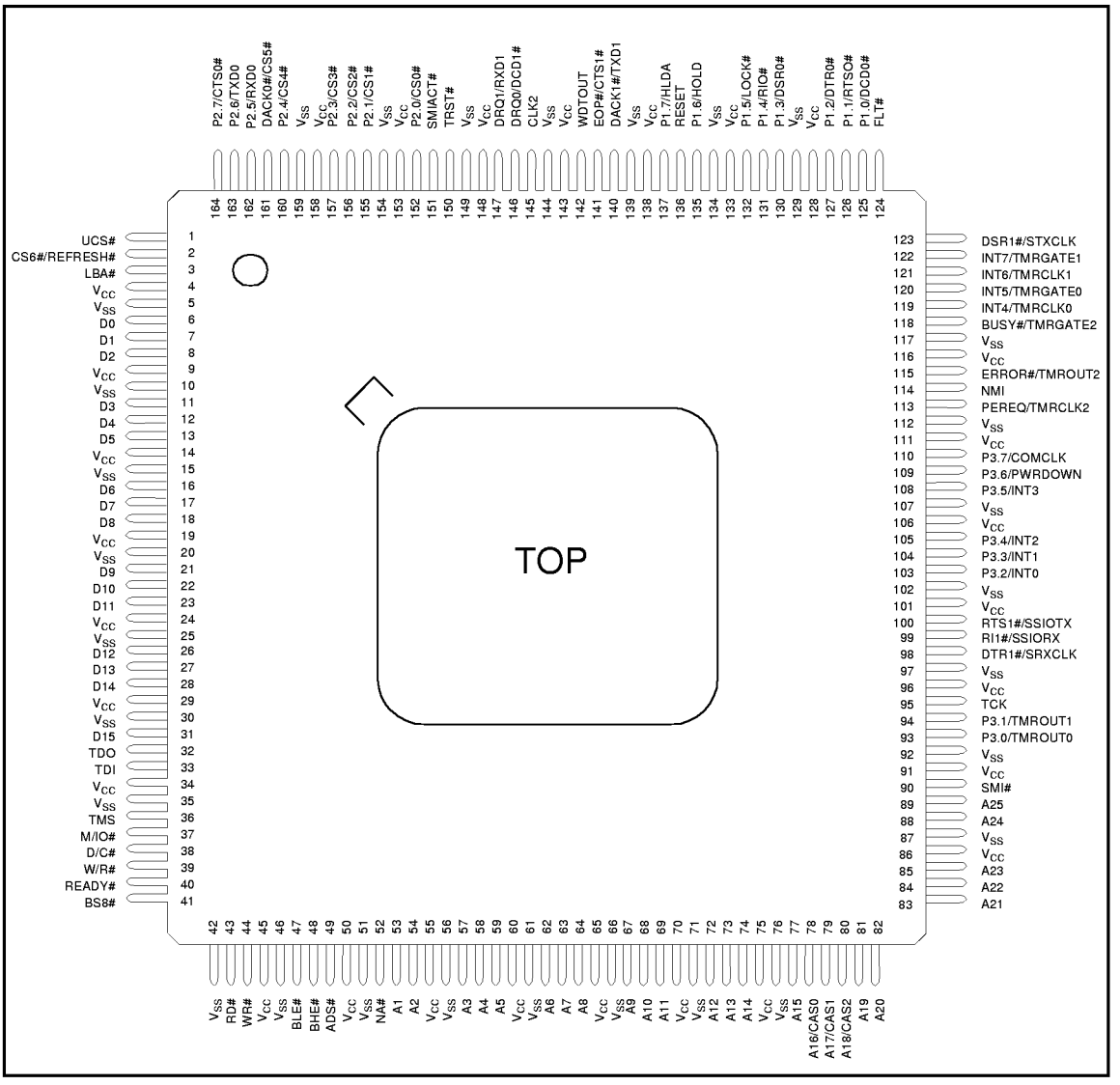


Figure 4. 164-Pin CQFP Pin Assignment

Table 2. 164-Pin CQFP Pin Assignment

Pin	Symbol	Pin	Symbol	Pin	Symbol	Pin	Symbol
1	UCS#	42	VSS	83	A21	124	FLT#
2	CS6#/REFRESH#	43	RD#	84	A22	125	P1.0/DCD0#
3	LBA#	44	WR#	85	A23	126	P1.1/RTS0#
4	V_{CC}	45	V_{CC}	86	V_{CC}	127	P1.2/DTR0#
5	V_{SS}	46	V_{SS}	87	V_{SS}	128	V_{CC}
6	D0	47	BLE#	88	A24	129	V_{SS}
7	D1	48	BHE#	89	A25	130	P1.3/DSR0#
8	D2	49	ADS#	90	SMI#	131	P1.4/RI0#
9	V_{CC}	50	V_{CC}	91	V_{CC}	132	P1.5/LOCK#
10	V_{SS}	51	V_{SS}	92	V_{SS}	133	V_{CC}
11	D3	52	NA#	93	P3.0/TMROUT0	134	V_{SS}
12	D4	53	A1	94	P3.1/TMROUT1	135	P1.6/HOLD
13	D5	54	A2	95	TCK	136	RESET
14	V_{CC}	55	V_{CC}	96	V_{CC}	137	P1.7/HLDA
15	V_{SS}	56	V_{SS}	97	V_{SS}	138	V_{CC}
16	D6	57	A3	98	DTR1#/SRXCLK	139	V_{SS}
17	D7	58	A4	99	RI1#/SSIORX	140	DACK1#/TXD1
18	D8	59	A5	100	RTS1#/SSIOTX	141	EOP#/CTS1#
19	V_{CC}	60	V_{CC}	101	V_{CC}	142	WDTOUT
20	V_{SS}	61	V_{SS}	102	V_{SS}	143	V_{CC}
21	D9	62	A6	103	P3.2/INT0	144	V_{SS}
22	D10	63	A7	104	P3.3/INT1	145	CLK2
23	D11	64	A8	105	P3.4/INT2	146	DRQ0/DCD1#
24	V_{CC}	65	V_{CC}	106	V_{CC}	147	DRQ1/RXD1
25	V_{SS}	66	V_{SS}	107	V_{SS}	148	V_{CC}
26	D12	67	A9	108	P3.5/INT3	149	V_{SS}
27	D13	68	A10	109	P3.6/PWRDOWN	150	TRST#
28	D14	69	A11	110	P3.7/COMCLK	151	SMIACT#
29	V_{CC}	70	V_{CC}	111	V_{CC}	152	P2.0/CS0#
30	V_{SS}	71	V_{SS}	112	V_{SS}	153	V_{CC}
31	D15	72	A12	113	PEREQ/TMRCLK2	154	V_{SS}
32	TDO	73	A13	114	NMI	155	P2.1/CS1#
33	TDI	74	A14	115	ERROR#/TMROUT2	156	P2.2/CS2#
34	V_{CC}	75	V_{CC}	116	V_{CC}	157	P2.3/CS3#
35	V_{SS}	76	V_{SS}	117	V_{SS}	158	V_{CC}
36	TMS	77	A15	118	BUSY#/TMRGATE2	159	V_{SS}
37	M/IO#	78	A16/CAS0	119	INT4/TMRCLK0	160	P2.4/CS4#
38	D/C#	79	A17/CAS1	120	INT5/TMRGATE0	161	DACK0#/CS5#
39	W/R#	80	A18/CAS2	121	INT6/TMRCLK1	162	P2.5/RXD0
40	READY#	81	A19	122	INT7/TMRGATE1	163	P2.6/TXD0
41	BS8#	82	A20	123	DSR1#/STXCLK	164	P2.7/CTS0#

NOTE: NC indicates that the pin is not connected.

3.0 PIN DESCRIPTION

Table 3 lists the Special Environment Intel386™ EX embedded processor pin descriptions. These definitions are used in the pin descriptions:

#	The named signal is active low.
I	Standard CMOS input signal.
O	Standard CMOS output signal.
I/O	Input and output signal.
I/OD	Input and open-drain output signal.
ST	Schmitt-triggered input signal.
P	Power pin.
G	Ground pin.

Table 3. Pin Descriptions (Sheet 1 of 4)

Symbol	Type	Name and Function
A25:1	O	**Address Bus** outputs physical memory or port I/O addresses. These signals are valid when ADS# is active and remain valid until the next T1, T2P, or Ti. During HOLD cycles they are driven to a high-impedance state. A18:16 are multiplexed with CAS2:0.
ADS#	O	**Address Status** indicates that the processor is driving a valid bus-cycle definition and address (W/R#, D/C#, M/IO#, A25:1, BHE#, BLE#) onto its pins.
BHE#	O	**Byte High Enable** indicates that the processor is transferring a high data byte.
BLE#	O	**Byte Low Enable** indicates that the processor is transferring a low data byte.
BS8#	I	**Bus Size** indicates that an 8-bit device is currently being addressed.
BUSY#	I	**Busy** indicates that the math coprocessor is busy. If BUSY# is sampled low at the falling edge of RESET, the processor performs an internal self test. BUSY# is multiplexed with TMRGATE2.
CAS2:0	O	**Cascade Address** carries the slave address information from the 82C59A master interrupt module during interrupt acknowledge bus cycles. CAS2:0 are multiplexed with A18:16.
CLK2	ST	**Clock Input** is connected to an external clock that provides the fundamental timing for the device.
COMCLK	I	**Serial Communications Baud Clock** is an alternate clock source for the asynchronous serial ports. COMCLK is multiplexed with P3.7.
CS6:0#	O	**Chip-selects** (lower) are activated when the address of a memory or I/O bus cycle is within the address region programmed by the user. They are multiplexed as follows: CS6# with REFRESH#, CS5# with DACK0#, and CS4:0# with P2.4:0.
CTS1:0#	I	**Clear to Send SIO1 and SIO0** prevent the transmission of data to the asynchronous serial port's RXD1 and RXD0 pins, respectively. CTS1# is multiplexed with EOP#, and CTS0# is multiplexed with P2.7. CTS1# requires an external pull-up resistor.
D15:0	I/O	**Data Bus** inputs data during memory read, I/O read, and interrupt acknowledge cycles and outputs data during memory and I/O write cycles. During writes, this bus is driven during phase 2 of T1 and remains active until phase 2 of the next T1, T1P, or Ti. During reads, data is latched on the falling edge of phase 2.

Table 3. Pin Descriptions (Sheet 2 of 4)

Symbol	Type	Name and Function
DACK1:0#	O	**DMA Acknowledge 1 and 0** signal to an external device that the processor has acknowledged the corresponding DMA request and is relinquishing the bus. DACK1# is multiplexed with TXD1, and DACK0# is multiplexed with CS5#.
D/C#	O	**Data/Control** indicates whether the current bus cycle is a data cycle (memory or I/O read or write) or a control cycle (interrupt acknowledge, halt, or code fetch).
DCD1:0#	I	**Data Carrier Detect SIO1 and SIO0** indicate that the modem or data set has detected the corresponding asynchronous serial channel's data carrier. DCD1# is multiplexed with DRQ0, and DCD0# is multiplexed with P1.0.
DRQ1:0	I	**DMA External Request 1 and 0** indicate that a peripheral requires DMA service. DRQ1 is multiplexed with RXD1, and DRQ0 is multiplexed with DCD1#.
DSR1:0#	I	**Data Set Ready SIO1 and SIO0** indicate that the modem or data set is ready to establish a communication link with the corresponding asynchronous serial channel. DSR1# is multiplexed with STXCLK, and DSR0# is multiplexed with P1.3.
DTR1:0#	O	**Data Terminal Ready SIO1 and SIO0** indicate that the corresponding asynchronous serial channel is ready to establish a communication link with the modem or data set. DTR1# is multiplexed with SRXCLK, and DTR0# is multiplexed with P1.2.
EOP#	I/OD	**End of Process** indicates that the processor has reached terminal count during a DMA transfer. An external device can also pull this pin low. EOP# is multiplexed with CTS1#.
ERROR#	I	**Error** indicates that the math coprocessor has an error condition. ERROR# is multiplexed with TMROUT2.
FLT#	I	**Float** forces all bidirectional and output signals except TDO to a high-impedance state.
HLDA	O	**Bus Hold Acknowledge** indicates that the processor has surrendered control of its local bus to another bus master. HLDA is multiplexed with P1.7.
HOLD	I	**Bus Hold Request** allows another bus master to request control of the local bus. HLDA active indicates that bus control has been granted. HOLD is multiplexed with P1.6.
INT7:0	I	**Interrupt Requests** are maskable inputs that cause the CPU to suspend execution of the current program and then execute an interrupt acknowledge cycle. They are multiplexed as follows: INT7 with TMRGATE1, INT6 with TMRCLK1, INT5 with TMRGATE0, INT4 with TMRCLK0, and INT3:0 with P3.5:2.
LBA#	O	**Local Bus Access** is asserted whenever the processor provides the READY# signal to terminate a bus transaction. This occurs when an internal peripheral address is accessed or when the chip-select unit provides the READY# signal.
LOCK#	O	**Bus Lock** prevents other bus masters from gaining control of the system bus. LOCK# is multiplexed with P1.5.
M/IO#	O	**Memory/IO** Indicates whether the current bus cycle is a memory cycle or an I/O cycle. When M/IO# is high, the bus cycle is a memory cycle; when M/IO# is low, the bus cycle is an I/O cycle.
NA#	I	**Next Address** requests address pipelining.
NMI	ST	**Nonmaskable Interrupt Request** is a non-maskable input that causes the CPU to suspend execution of the current program and execute an interrupt acknowledge cycle.

Table 3. Pin Descriptions (Sheet 3 of 4)

Symbol	Type	Name and Function
PEREQ	I	**Processor Extension Request** indicates that the math coprocessor has data to transfer to the processor. PEREQ is multiplexed with TMRCLK2.
P1.7:0	I/O	**Port 1, Pins 7:0** are multipurpose bidirectional port pins. They are multiplexed as follows: P1.7 with HLDA, P1.6 with HOLD, P1.5 with LOCK#, P1.4 with RI0#, P1.3 with DSR0#, P1.2 with DTR0#, P1.1 with RTS0#, and P1.0 with DCD0#.
P2.7:0	I/O	**Port 2, Pins 7:0** are multipurpose bidirectional port pins. They are multiplexed as follows: P2.7 with CTS0#, P2.6 with TXD0, P2.5 with RXD0, and P2.4:0 with CS4:0#.
P3.7:0	I/O	**Port 3, Pins 7:0** are multipurpose bidirectional port pins. They are multiplexed as follows: P3.7 with COMCLK, P3.6 with PWRDOWN, P3.5:2 with INT3:0, and P3.1:0 with TMROUT1:0.
PWRDOWN	O	**Powerdown** indicates that the processor is in powerdown mode. PWRDOWN is multiplexed with P3.6.
RD#	O	**Read Enable** indicates that the current bus cycle is a read cycle.
READY#	I/O	**Ready** indicates that the current bus transaction has completed. An external device or an internal signal can drive READY#. Internally, the chip-select wait-state logic can generate the ready signal and drive the READY# pin active.
RESET	ST	**Reset** suspends any operation in progress and places the processor into a known reset state.
REFRESH#	O	**Refresh** indicates that the current bus cycle is a refresh cycle. REFRESH# is multiplexed with CS6#.
RI1:0#	I	**Ring Indicator SIO1 and SIO0** indicate that the modem or data set has received a telephone ringing signal. RI1# is multiplexed with SSIORX, and RI0# is multiplexed with P1.4.
RTS1:0#	O	**Request-to-send SIO1 and SIO0** indicate that corresponding asynchronous serial channel is ready to exchange data with the modem or data set. RTS1# is multiplexed with SSIOTX, and RTS0# is multiplexed with P1.1.
RXD1:0	I	**Receive Data SIO1 and SIO0** accept serial data from the modem or data set to the corresponding asynchronous serial channel. RXD1 is multiplexed with DRQ1, and RXD0 is multiplexed with P2.5.
SMI#	ST	**System Management Interrupt** invokes System Management Mode (SMM). SMI# is the highest priority external interrupt. It is latched on its falling edge and it forces the CPU into SMM upon completion of the current instruction. SMI# is recognized on an instruction boundary and at each iteration for repeat string instructions. SMI# cannot interrupt LOCKed bus cycles or a currently executing SMM. If the processor receives a second SMI# while it is in SMM, it will latch the second SMI# on the SMI# falling edge. However, the processor must exit SMM by executing a resume instruction (RSM) before it can service the second SMI#.
SMIACT#	O	**System Management Interrupt Active** indicates that the processor is operating in System Management Mode (SMM). It is asserted when the processor initiates an SMM sequence and remains asserted (low) until the processor executes the resume instruction (RSM).
SRXCLK	I/O	**SSIO Receive Clock** synchronizes data being accepted by the synchronous serial port. SRXCLK is multiplexed with DTR1#.
SSIORX	I	**SSIO Receive Serial Data** accepts serial data (most-significant bit first) being sent to the synchronous serial port. SSIORX is multiplexed with RI1#.
SSIOTX	O	**SSIO Transmit Serial Data** sends serial data (most-significant bit first) from the synchronous serial port. SSIOTX is multiplexed with RTS1#.

Table 3. Pin Descriptions (Sheet 4 of 4)

Symbol	Type	Name and Function
STXCLK	I/O	**SSIO Transmit Clock** synchronizes data being sent by the synchronous serial port. STXCLK is multiplexed with DSR1.
TCK	I	**TAP (Test Access Port) Controller Clock** provides the clock input for the JTAG logic.
TDI	I	**TAP (Test Access Port) Controller Data Input** is the serial input for test instructions and data.
TDO	O	**TAP (Test Access Port) Controller Data Output** is the serial output for test instructions and data.
TMRCLK2:0	I	**Timer/Counter Clock Inputs** can serve as external clock inputs for the corresponding timer/counters. (The timer/counters can also be clocked internally.) They are multiplexed as follows: TMRCLK2 with PEREQ, TMRCLK1 with INT6, and TMRCLK0 with INT4.
TMRGATE2:0	I	**Timer/Counter Gate Inputs** can control the corresponding timer/counter's counting (enable, disable, or trigger, depending on the programmed mode). They are multiplexed as follows: TMRGATE2 with BUSY#, TMRGATE1 with INT7, and TMRGATE0 with INT5.
TMROUT2:0	O	**Timer/Counter Outputs** provide the output of the corresponding timer/counter. The form of the output depends on the programmed mode. They are multiplexed as follows: TMROUT2 with ERROR#, TMROUT1 with P3.1, and TMROUT0 with P3.0.
TMS	I	**TAP (Test Access Port) Controller Mode Select** controls the sequence of the TAP controller's states.
TRST#	ST	**TAP (Test Access Port) Controller Reset** resets the TAP controller at power-up and each time it is activated.
TXD1:0	O	**Transmit Data SIO1 and SIO0** transmit serial data from the individual serial channels. TXD1 is multiplexed with DACK1#, and TXD0 is multiplexed with P2.6.
UCS#	O	**Upper Chip-select** is activated when the address of a memory or I/O bus cycle is within the address region programmed by the user.
V_{CC}	P	**System Power** provides the nominal DC supply input. Connected externally to a V_{CC} board plane.
V_{SS}	G	**System Ground** provides the 0V connection from which all inputs and outputs are measured. Connected externally to a ground board plane.
WDTOUT	O	**Watchdog Timer Output** indicates that the watchdog timer has expired.
W/R#	O	**Write/Read** indicates whether the current bus cycle is a write cycle or a read cycle. When W/R# is high, the bus cycle is a write cycle; when W/R# is low, the bus cycle is a read cycle.
WR#	O	**Write Enable** indicates that the current bus cycle is a write cycle.

4.0 FUNCTIONAL DESCRIPTION

The Special Environment Intel386™ EX embedded processor is a fully static, 32-bit processor optimized for harsh environment embedded applications. It features low power and low voltage capabilities, integration of many commonly used peripherals, and a 32-bit programming architecture compatible with the large software base of Intel386 processors. The following sections provide an overview of the integrated peripherals.

4.1 Clock Generation and Power Management Unit

The clock generation circuit includes a divide-by-two counter, a programmable divider for generating a prescaled clock (PSCLK), a divide-by-two counter for generating baud-rate clock inputs, and Reset circuitry. The CLK2 input provides the fundamental timing for the chip. It is divided by two internally to generate a 50% duty cycle Phase1 (PH1) and Phase 2 (PH2) for the core and integrated peripherals. For power management, separate clocks are routed to the core (PH1C/PH2C) and the peripheral modules (PH1P/PH2P).

Two Power Management modes are provided for flexible power-saving options. During Idle mode, the clocks to the CPU core are frozen in a known state (PH1C low and PH2C high), while the clocks to the peripherals continue to toggle. In Powerdown mode, the clocks to both core and peripherals are frozen in a known state (PH1C low and PH2C high). The Bus Interface Unit will not honor any DMA, DRAM refresh, or HOLD requests in Powerdown mode because the clocks to the entire device are frozen.

4.2 Chip-select Unit

The Chip-select Unit (CSU) decodes bus cycle address and status information and enables the appropriate chip-selects. The individual chip-selects become valid in the same bus state as the address and become inactive when either a new address is selected or the current bus cycle is complete.

The CSU is divided into eight separate chip-select regions, each of which can enable one of the eight chip-select pins. Each chip-select region can be mapped into memory or I/O space. A memory-mapped chip-select region can start on any $2^{(n+1)}$ Kbyte address location (where n = 0–15, depending upon the mask register). An I/O-mapped chip-select region can start on any $2^{(n+1)}$ byte address location (where n = 0–15, depending upon the mask register). The size of the region is also dependent upon the mask used.

4.3 Interrupt Control Unit

The Interrupt Control Unit (ICU) contains two 82C59A modules connected in a cascade mode. The 82C59A modules make up the heart of the ICU. These modules are similar to the industry-standard 82C59A architecture.

The Interrupt Control Unit directly supports up to eight external (INT7:0) and up to eight internal interrupt request signals. Pending interrupt requests are posted in the Interrupt Request Register, which contains one bit for each interrupt request signal. When an interrupt request is asserted, the corresponding Interrupt Request Register bit is set. The 82C59A module can be programmed to recognize either an active-high level or a positive transition on the interrupt request lines. An internal Priority Resolver decides which pending interrupt request (if more than one exists) is the highest priority, based on the programmed operating mode. The Priority Resolver controls the single interrupt request line to the CPU. The Priority Resolver's default priority scheme places the master interrupt controller's IR0 as the highest priority and the master's IR7 as the lowest. The priority can be modified through software.

Besides the eight interrupt request inputs available, additional interrupts can be supported by cascaded external 82C59A modules. Up to four external 82C59A units can be cascaded to the master through connections to the INT3:0 pins. In this configuration, the interrupt acknowledge (INTA#) signal can be decoded externally using the ADS#, D/C#, W/R#, and M/IO# signals.

4.4 Timer Control Unit

The Timer Control Unit (TCU) has the same basic functionality as the industry-standard 82C54 counter/timer. The TCU provides three independent 16-bit counters, each capable of handling clock inputs up to 8 MHz. This maximum frequency must be considered when programming the input clocks for the counters. Six programmable timer modes allow the counters to be used as event counters, elapsed-time indicators, programmable one-shots, and in many other applications. All modes are software programmable.

4.5 Watchdog Timer Unit

The Watchdog Timer (WDT) unit consists of a 32-bit down-counter that decrements every PH1P cycle, allowing up to 4.3 billion count intervals. The WDTOUT pin is driven high for sixteen CLK2 cycles when the down-counter reaches zero (the WDT times out). The WDTOUT signal can be used to reset the chip, to request an interrupt, or to indicate to the user that a ready-hang situation has occurred. The down-counter can also be updated with a user-defined 32-bit reload value under certain conditions. Alternatively, the WDT unit can be used as a bus monitor or as a general-purpose timer.

4.6 Asynchronous Serial I/O Unit

The asynchronous Serial I/O (SIO) unit is a Universal Asynchronous Receiver/Transmitter (UART). Functionally, it is equivalent to the National Semiconductor* NS16450 and INS8250. The Special Environment Intel386™ EX embedded processor contains two full-duplex, asynchronous serial channels.

The SIO unit converts serial data characters received from a peripheral device or modem to parallel data and converts parallel data characters received from the CPU to serial data. The CPU can read the status of the serial port at any time during its operation. The status information includes the type and condition of the transfer operations being performed and any errors (parity, framing, overrun, or break interrupt).

Each asynchronous serial channel includes full modem control support (CTS#, RTS#, DSR#, DTR#, RI#, and DCD#) and is completely programmable. The programmable options include character length (5, 6, 7, or 8 bits), stop bits (1, 1.5, or 2), and parity (even, odd, forced, or none). In addition, it contains a programmable baud-rate generator capable of clock rates from 0 to 512 Kbaud.

4.7 Synchronous Serial I/O Unit

The Synchronous Serial I/O (SSIO) unit provides for simultaneous, bidirectional communications. It consists of a transmit channel, a receive channel, and a dedicated baud-rate generator. The transmit and receive channels can be operated independently (with different clocks) to provide non-lockstep, full-duplex communications; either channel can originate the clocking signal (Master Mode) or receive an externally generated clocking signal (Slave Mode).

The SSIO provides numerous features for ease and flexibility of operation. With a maximum clock input of 12.5 MHz to the baud-rate generator, the SSIO can deliver a baud rate of 5 Mbits per second. Each channel is double buffered. The two channels share the baud-rate generator and a multiply-by-two transmit and receive clock. The SSIO supports 16-bit serial communications with independently enabled transmit and receive functions and gated interrupt outputs to the interrupt controller.

4.8 Parallel I/O Unit

The Special Environment Intel386™ EX embedded processor has three 8-bit, general-purpose I/O ports. All port pins are bidirectional, with CMOS-level input and outputs. All pins have both a standard operating mode and a peripheral mode (a multiplexed function), and all have similar sets of control registers located in I/O address space. Ports 1 and 2 provide 8 mA of drive capability, while port 3 provides 16 mA.

4.9 DMA and Bus Arbiter Unit

The DMA controller is a two-channel DMA; each channel operates independently of the other. Within the operation of the individual channels, several different data transfer modes are available. These modes can be combined in various configurations to provide a very versatile DMA controller. Its feature set has enhancements beyond the 8237 DMA family; however, it can be configured such that it can be used in an 8237-like mode. Each channel can transfer data between any combination of memory and I/O with any combination (8 or 16 bits) of data

path widths. An internal temporary register that can disassemble or assemble data to or from either an aligned or a nonaligned destination or source optimizes bus bandwidth

The bus arbiter, a part of the DMA controller, works much like the priority resolving circuitry of a DMA. It receives service requests from the two DMA channels, the external bus master, and the DRAM Refresh controller. The bus arbiter requests bus ownership from the core and resolves priority issues among all active requests when bus mastership is granted.

Each DMA channel consists of three major components: the Requestor, the Target, and the Byte Count. These components are identified by the contents of programmable registers that define the memory or I/O device being serviced by the DMA. The Requestor is the device that requires and requests service from the DMA controller. Only the Requestor is considered capable of initializing or terminating a DMA process. The Target is the device with which the Requestor wishes to communicate. The DMA process considers the Target a slave that is incapable of controlling the process. The Byte Count dictates the amount of data that must be transferred.

4.10 Refresh Control Unit

The Refresh Control Unit (RCU) simplifies dynamic memory controller design with its integrated address and clock counters. Integrating the RCU into the processor allows an external DRAM controller to use chip-selects, wait state logic, and status lines. The RCU consists of:

- a programmable-interval timer that keeps track of time
- bus arbitration logic to gain control of the bus to run refresh cycles
- row address generation logic to individually refresh DRAM rows
- refresh cycle-start logic

The 13-bit address counter that forms the refresh address supports DRAM with up to 13 rows of memory cells (13 refresh address bits). This includes all practical DRAM sizes for the 64 Mbyte address space.

4.11 JTAG Test-logic Unit

The JTAG Test-Logic Unit (TLU) provides access to the device pins and to a number of other testable areas on the device. It is fully compliant with the IEEE 1149.1 standard and thus interfaces with five dedicated pins: TRST#, TCK, TMS, TDI, and TDO. It contains the Test Access Port (TAP) finite-state machine, a 4-bit instruction register, a 32-bit identification register, and a single-bit bypass register. The TLU also contains the necessary logic to generate clock and control signals for the Boundary Scan chain.

Since the TLU has its own clock and reset signals, it can operate autonomously. Thus, while the rest of the processor is in Reset or Powerdown, the JTAG unit can read or write various register chains.

5.0 DESIGN CONSIDERATIONS

This section describes the instruction set and component and revision identifiers.

5.1 Instruction Set

The Special Environment Intel386™ EX embedded processor uses the same instruction set as the Intel386 SX microprocessor with the following exceptions:

- The Special Environment Intel386™ EX embedded processor has one new instruction: the Resume instruction (RSM). It causes the processor to exit System Management Mode (SMM).
- The Special Environment Intel386™ EX embedded processor requires more clock cycles than the Intel386 SX microprocessor to execute some instructions.

Table 7 lists these instructions and the Intel386 EX microprocessor Clocks Per Instructions (CPI). For the equivalent Intel386 SX microprocessor CPI, refer to the “Instruction Set Clock Count Summary” table in the *Intel386™ SX Microprocessor* data sheet (order number 240187).

5.2 Component and Revision Identifiers

To assist users, the processor holds a component identifier and revision identifier in its DX register after reset.

- The upper 8 bits of DX hold the component identifier. (The lower nibble, 3H, identifies the Intel386 architecture, while the upper nibble, 2H, identifies the second member of the Intel386 microprocessor family.)
- The lower 8 bits of DX hold the revision level identifier.

Table 4. Component and Revision Identifier Register

DX Register

15	8	7	0
Component Identifier		Revision Level Identifier	
2H	3H	09H	

Generally, the revision identifier chronologically tracks those component steppings that have improvements or distinction from previous steppings. The revision identifier tracks that of the Intel386 CPU whenever possible; steppings that change only peripherals are not assigned new stepping numbers. The revision identifier value is not guaranteed to change with every stepping revision or to follow a uniform numerical sequence. Intel has sole discretion over these characteristics of the component. The initial revision identifier for the Intel386 EX microprocessor is 09H.

5.3 Package Thermal Specifications

The Special Environment Intel386™ EX embedded processor is specified for operation with case temperature (T_{CASE}) within the range of -55°C to +125°C. The case temperature can be measured in any environment to determine whether the processor is within the specified operating range. The case temperature should be measured at the center of the top surface opposite the pins.

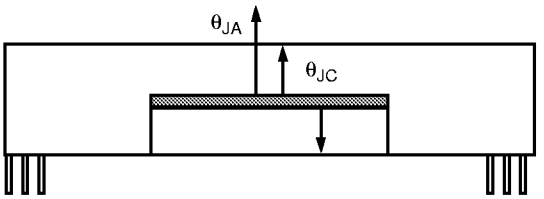
An increase in the ambient temperature (T_A) causes a proportional increase in the case temperature (T_{CASE}) and the junction temperature (T_J). A packaged device produces thermal resistance between junction and case temperatures (θ_{JC}) and between junction and ambient temperatures (θ_{JA}). The relationships between the temperature and thermal resistance parameters are expressed by these equations (P = power dissipated as heat = $V_{CC} \times I_{CC}$):

1. $T_J = T_{CASE} + P \times \theta_{JC}$
2. $T_A = T_J - P \times \theta_{JA}$
3. $T_{CASE} = T_A + P \times [\theta_{JA} - \theta_{JC}]$

A safe operating temperature can be calculated from equation 1 by using the maximum safe T_C of 125°C, the maximum power drawn by the chip in the specific design, and the θ_{JC} value from Tables 5 or 6. The θ_{JA} value depends on the airflow (measured at the top of the chip) provided by the system ventilation. The θ_{JA} values are given for reference only and are not guaranteed.

Table 5. 168-Lead PGA Package Thermal Characteristics

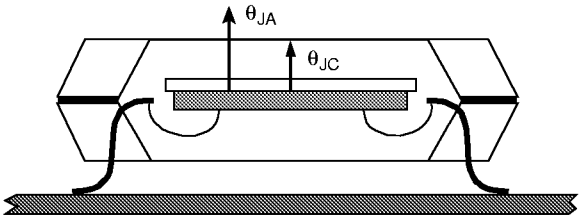
Parameter	Thermal Resistance — °C/Watt
θ_{JC} (Junction-to-Case)	3
θ_{JA} (Junction-to-Ambient)	22



NOTE: This table applies to a PGA device plugged into a socket or soldered directly into a board.

Table 6. 164-Lead CQFP Package Thermal Characteristics

Parameter	Thermal Resistance — °C/Watt
θ_{JC} (Junction-to-Case)	8.5
θ_{JA} (Junction-to-Ambient)	29.5



NOTE: This table applies to a PQFP device soldered directly into board.

Table 7. Clocks Per Instruction

Instruction	Clock Count		
	Virtual 8086 Mode (Note 1)	Real Address Mode or Virtual 8086 Mode	Protected Virtual Address Mode (Note 3)
POPA		28	35
IN: Fixed Port Variable Port	 27 28	 14 15	 7/29 8/29
OUT: Fixed Port Variable Port	 27 28	 14 15	 7/29 9/29
INS	30	17	9/32
OUTS	31	18	10/33
REP INS	31+6*n* (Note 2)	17+6*n* (Note 2)	10+6*n*/32+6*n* (Note 2)
REP OUTS	30+8*n* (Note 2)	16+8*n* (Note 2)	10+8*n*/31+8*n* (Note 2)
HLT		7	7
MOV CR0, reg		10	10
RSM	338	338	338

NOTES:

1. The clock count values in this column apply if I/O permission allows I/O to the port in virtual 8086 mode. If the I/O bit map denies permission, exception fault 13 occurs; see clock counts for the INT 3 instruction in the "Instruction Set Clock Count Summary" table in the *Intel386™ SX Microprocessor* data sheet (order number 240187).
2. *n* = the number of times repeated.
3. When two clock counts are listed, the smaller value refers to a register operand and the larger value refers to a memory operand.

6.0 DC SPECIFICATIONS

6.1 Maximum Ratings

ABSOLUTE MAXIMUM RATINGS*

Storage Temperature −65°C to +150°C

Case Temperature Under Bias −55°C to +125°C

Supply Voltage with Respect to V_{SS} −0.5V to 6.5V

Voltage on Other Pins −0.5V to V_{CC} + 0.5V

NOTICE: This document contains information on products in the sampling and initial production phases of development. The specifications are subject to change without notice. Verify with your local Intel Sales office that you have the latest data sheet before finalizing a design.

WARNING: *Stressing the device beyond the "Absolute Maximum Ratings" may cause permanent damage. These are stress ratings only. Operation beyond the "Operating Conditions" is not recommended and extended exposure beyond the "Operating Conditions" may affect device reliability.*

Although the Special Environment Intel386™ EX embedded processor contains protective circuitry to resist damage from static electric discharge, always take precautions to avoid high static voltages or electric fields.

6.2 Operating Conditions

Table 8. SE1 (QML)

Symbol	Description	Min	Max	Units
T_C	Case Temperature (Instant On)	-55	+125	°C
V_{CC}	Digital Supply Voltage	4.75	5.25	V

Table 9. SE2 (QML)

Symbol	Description	Min	Max	Units
T_C	Case Temperature (Instant On)	-40	+125	°C
V_{CC}	Digital Supply Voltage	4.75	5.25	V

Table 10. DC Characteristics

Symbol	Parameter	Min.	Max.	Unit	Test Condition
V_{IL}	Input Low Voltage	–0.5	$0.3V_{CC}$	V	
V_{IH}	Input High Voltage	$0.7V_{CC}$	V_{CC} + 0.5	V	
V_{OL}	Output Low Voltage All pins except Port 3 Port 3		 0.40 0.40	 V V	V_{CC} = 4.75V to 5.25V I_{OL} = 8 mA I_{OL} = 16 mA
V_{OH}	Output High Voltage All pins except Port 3 Port 3	 V_{CC}–0.8 V_{CC}–0.8		 V V	V_{CC} = 4.75V to 5.25V I_{OH} = –8 mA I_{OH} = –16 mA
I_{LI}	Input Leakage Current		±15	µA	$0 \le V_{IN} \le V_{CC}$
I_{LO}	Output Leakage Current		±15	µA	$0.45V \le V_{OUT} \le V_{CC}$
I_{CC}	Supply Current		250	mA	25 MHz, 5.25V Note 1
I_{IDLE}	Idle Mode Current		85	mA	25 MHz, 5.25V
I_{PD}	Powerdown Current		100	µA	
C_S	Pin Capacitance (any pin to V_{SS})		10	pF	

NOTE:
1. This parameter is measured while the device is in Reset mode.

7.0 AC SPECIFICATIONS

Table 11 lists output delays, input setup requirements, and input hold requirements. All AC specifications are relative to the CLK2 rising edge crossing the V_{CC}/2 level.

Figure 5 shows the measurement points for AC specifications. Inputs must be driven to the indicated voltage levels when AC specifications are measured. Output delays are specified with minimum and maximum limits measured as shown. The minimum delay times are hold times provided to external circuitry. Input setup and hold times are specified as minimums, defining the smallest acceptable sampling window. Within the sampling window, a synchronous input signal must be stable for correct operation.

Outputs ADS#, W/R#, CS5:0#, UCS#, D/C#, M/IO#, LOCK#, BHE#, BLE#, REFRESH#/CS6#, READY#, LBA#, A25:1, HLDA and SMIACT# change only at the beginning of phase one. D15:0 (write cycles) and PWRDOWN change only at the beginning of phase two. RD# and WR# change to their active states at the beginning of phase two, and to their inactive states (end of cycle) at the beginning of phase one.

The READY#, HOLD, BUSY#, ERROR#, PEREQ, BS8#, and D15:0 (read cycles) inputs are sampled at the beginning of phase one. The NA#, SMI#, and NMI inputs are sampled at the beginning of phase two.

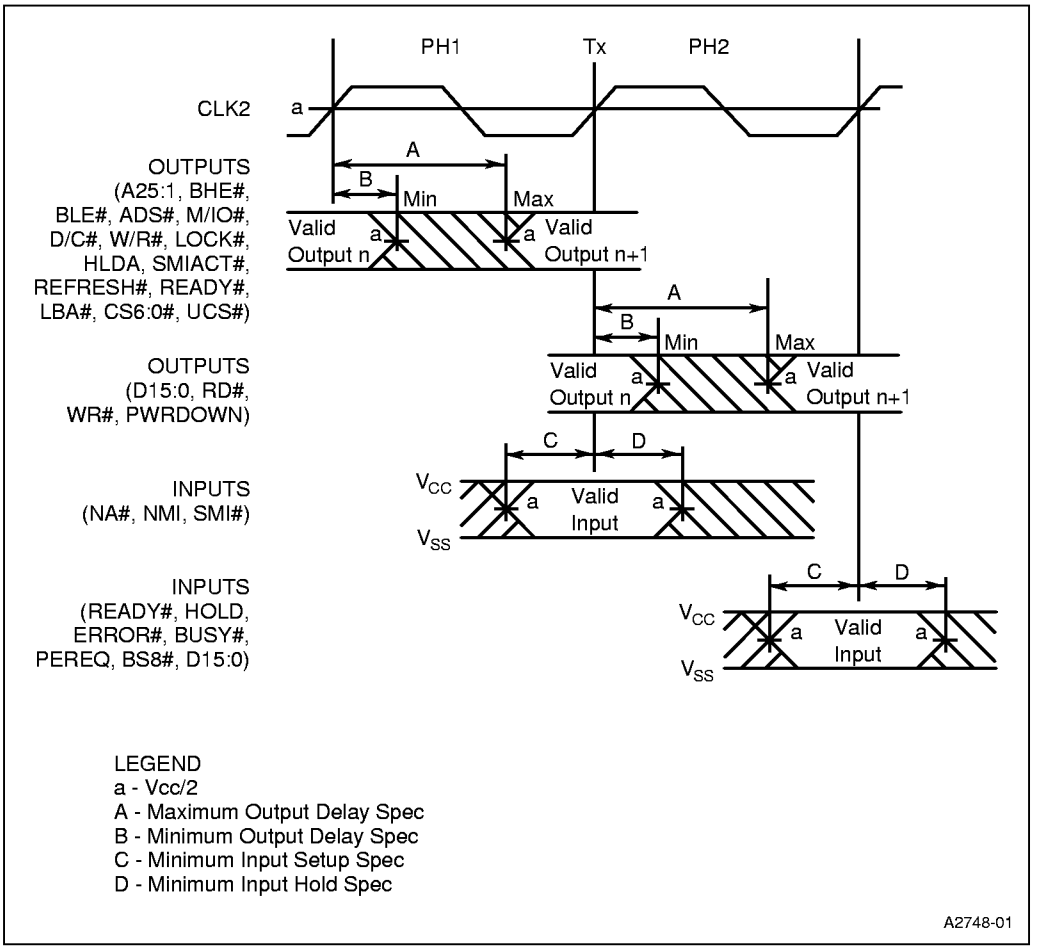


Figure 5. Drive Levels and Measurement Points for AC Specifications

Table 11. AC Characteristics (Sheet 1 of 5)

Symbol	Parameter	25 MHz 4.75 V to 5.25 V		Test Condition
		Min. (ns)	Max. (ns)	
	Operating Frequency	0	25	one-half CLK2 frequency in MHz (Note 1)
t1	CLK2 Period	20		
t2a	CLK2 High Time	7		at $V_{CC}/2$ (Note 2)
t2b	CLK2 High Time	4		at V_{CC} – 0.8V for HV, at V_{CC} – 0.6V for LV (Note 2)
t3a	CLK2 Low Time	7		at $V_{CC}/2$ (Note 2)
t3b	CLK2 Low Time	5		at 0.8V (Note 2)
t4	CLK2 Fall Time		7	V_{CC} – 0.8V to 0.8V for HV, V_{CC} – 0.6V to 0.8V for LV (Note 2)
t5	CLK2 Rise Time		7	0.8V to V_{CC} –0.8V for HV, 0.8V to V_{CC} –0.6V for LV (Note 2)
t6	A25:1 Valid Delay	4	29	C_L = 50 pF (Note 3)
t7	A25:1 Float Delay	4	36	(Note 4)
t8	BHE#, BLE#, LOCK# Valid Delay	4	29	C_L = 50 pF (Note 3)
t8a	SMIACT# Valid Delay	4	29	C_L = 50 pF (Note 3)
t9	BHE#, BLE#, LOCK# Float Delay	4	30	(Note 4)
t10	M/IO#, D/C#, W/R#, ADS#, REFRESH# Valid Delay	4	29	C_L = 50 pF (Note 3)
t10a	RD#, WR# Valid Delay	4	29	

NOTES:

1. Tested at maximum operating frequency and guaranteed by design characterization at lower operating frequencies.
2. These are not tested. They are guaranteed by characterization.
3. Tested with C_L set at 50 pF. Timings are guaranteed with C_L set at 75 pF.
4. Float condition occurs when maximum output current becomes less than I_{LO} in magnitude. Float delay is not fully tested.
5. These inputs may be asynchronous to CLK2. The setup and hold specifications are given for testing purposes to ensure recognition within a specific CLK2 period.
6. These specifications are for information only and are not tested. They are intended to assist the designer in selecting memory speeds. For each wait state in the design add two CLK2 cycles to the specification.

Table 11. AC Characteristics (Sheet 2 of 5)

Symbol	Parameter	25 MHz 4.75 V to 5.25 V		Test Condition
		Min. (ns)	Max. (ns)	
t11	M/IO#, D/C#, W/R#, REFRESH#, ADS# Float Delay	4	39	(Note 4)
t12	D15:0 Write Data Valid Delay	4	28	C_L = 50 pF (Note 3)
t13	D15:0 Write Data Float delay	4	24	(Note 4)
t14	HLDA Valid Delay	4	27	C_L = 50 pF (Note 3)
t15	NA# Setup Time	5		
t16	NA# Hold Time	10		
t19	READY# Setup Time	9		
t19a	BS8# Setup Time	11		
t20	READY#, BS8# Hold Time	4		
t21	D15:0 Read Setup Time	5		
t22	D15:0 Read Hold Time	5		
t23	HOLD Setup Time	9		
t24	HOLD Hold Time	5		
t25	RESET Setup Time	8		
t26	RESET Hold Time	4		
t27	NMI Setup Time	12		(Note 5)
t27a	SMI# Setup Time	12		(Note 5)
t28	NMI Hold Time	6		(Note 5)
t28a	SMI# Hold Time	6		(Note 5)
t29	PEREQ, ERROR#, BUSY# Setup Time	6		(Note 5)
t30	PEREQ, ERROR#, BUSY# Hold Time	6		(Note 5)
t31	READY# Valid Delay	4	32	
t32	READY# Float Delay	4	34	

NOTES:

1. Tested at maximum operating frequency and guaranteed by design characterization at lower operating frequencies.
2. These are not tested. They are guaranteed by characterization.
3. Tested with C_L set at 50 pF. Timings are guaranteed with C_L set at 75 pF.
4. Float condition occurs when maximum output current becomes less than I_{LO} in magnitude. Float delay is not fully tested.
5. These inputs may be asynchronous to CLK2. The setup and hold specifications are given for testing purposes to ensure recognition within a specific CLK2 period.
6. These specifications are for information only and are not tested. They are intended to assist the designer in selecting memory speeds. For each wait state in the design add two CLK2 cycles to the specification.

Table 11. AC Characteristics (Sheet 3 of 5)

Symbol	Parameter	25 MHz 4.75 V to 5.25 V		Test Condition
		Min. (ns)	Max. (ns)	
t33	LBA# Valid Delay	4	32	
t34	CS6:0#, UCS# Valid Delay	7	32	
t41	A25:1, BHE#, BLE# Valid to WR# Low	0		
t41a	UCS#, CS6:0# Valid to WR# Low	0		
t42	A25:1, BHE#, BLE# Hold After WR# High	5		
t42a	UCS#, CS6:0# Hold after WR# High	5		
t43	D15:0 Output Valid to WR# High	3CLK2 –27		(Note 6)
t44	D15:0 Output Hold After WR# High	CLK2 –10		
t45	WR# High to D15:0 Float		CLK2 + 10	(Note 4)
t46	WR# Pulse Width	3CLK2 –15		
t47	A25:1, BHE#, BLE# Valid to D15:0 Valid		4CLK2 - 36	(Note 6)
t47a	UCS#, CS6:0# Valid to D15-D0 Valid		4CLK2 - 46	(Note 6)
t48	RD# Low to D15:0 Input Valid		3CLK2 – 36	(Note 6)
t49	D15:0 Hold After RD# High	2		
t50	RD# High to D15:0 Float		10	(Note 4)
t51	A25:1, BHE#, BLE# Hold After RD# High	0		
t51a	UCS#, CS6:0# Hold after RD# High	0		
t52	RD# Pulse Width	3CLK2 –15		

NOTES:

1. Tested at maximum operating frequency and guaranteed by design characterization at lower operating frequencies.
2. These are not tested. They are guaranteed by characterization.
3. Tested with C_L set at 50 pF. Timings are guaranteed with C_L set at 75 pF.
4. Float condition occurs when maximum output current becomes less than I_{LO} in magnitude. Float delay is not fully tested.
5. These inputs may be asynchronous to CLK2. The setup and hold specifications are given for testing purposes to ensure recognition within a specific CLK2 period.
6. These specifications are for information only and are not tested. They are intended to assist the designer in selecting memory speeds. For each wait state in the design add two CLK2 cycles to the specification.

Table 11. AC Characteristics (Sheet 4 of 5)

Symbol	Parameter	25 MHz 4.75 V to 5.25 V		Test Condition
		Min. (ns)	Max. (ns)	
Synchronous Serial I/O (SSIO) Unit				
t100	STXCLK, SRXCLK Frequency (Master Mode)		CLK2/8	(Unit is MHz)
t101	STXCLK, SRXCLK Frequency (Slave Mode)		CLK2/4	(Unit is MHz; CLK2/4 or 6.25 MHZ, whichever is less)
t102	STXCLK, SRXCLK Low Time	3CLK2/2		
t103	STXCLK, SRXCLK High Time	3CLK2/2		
t104	STXCLK Low to SSIOTX Delay		10	
t105	SSIORX to SRXCLK High Setup Time	10		
t106	SSIORX from SRXCLK Hold Time	10		
Timer Control Unit (TCU) Inputs				
t107	TMRCLK*n* Frequency		8	(Unit is MHz)
t108	TMRCLK*n* Low	60		
t109	TMRCLK*n* High	60		
t110	TMRGATE*n* High Width	50		
t111	TMRGATE*n* Low Width	50		
t112	TMRGATE*n* to TMRCLK Setup Time (external TMRCLK only)	10		
Timer Control Unit (TCU) Outputs				
t113	TMRGATE*n* Low to TMROUT Valid		36	
t114	TMRCLK*n* Low to TMROUT Valid		36	
Interrupt Control Unit (ICU) Inputs				
t115	D7:0 Setup Time (INTA# Cycle 2)	7		
t116	D7:0 Hold Time (INTA# Cycle 2)	5		

NOTES:

1. Tested at maximum operating frequency and guaranteed by design characterization at lower operating frequencies.
2. These are not tested. They are guaranteed by characterization.
3. Tested with C_L set at 50 pF. Timings are guaranteed with C_L set at 75 pF.
4. Float condition occurs when maximum output current becomes less than I_{LO} in magnitude. Float delay is not fully tested.
5. These inputs may be asynchronous to CLK2. The setup and hold specifications are given for testing purposes to ensure recognition within a specific CLK2 period.
6. These specifications are for information only and are not tested. They are intended to assist the designer in selecting memory speeds. For each wait state in the design add two CLK2 cycles to the specification.

Table 11. AC Characteristics (Sheet 5 of 5)

Symbol	Parameter	25 MHz 4.75 V to 5.25 V		Test Condition
		Min. (ns)	Max. (ns)	
Interrupt Control Unit (ICU) Outputs				
t117	CLK2 High to CAS2:0 Valid		34	
DMA Unit Inputs				
t118	DREQ Setup Time (Sync Mode)	17		
t119	DREQ Hold Time (Sync Mode)	4		
t120	DREQ Setup Time (Async Mode)	10		
t121	DREQ Hold Time (Async Mode)	10		
t122	EOP# Setup Time (Sync Mode)	13		
t123	EOP# Hold Time (Sync Mode)	4		
t124	EOP# Setup Time (Async Mode)	10		
t125	EOP# Hold Time (Async Mode)	11		
DMA Unit Outputs				
t126	DACK# Output Valid Delay	4	29	
t127	EOP# Active Delay	4	30	
t128	EOP# Float Delay	4	33	(Note 4)
JTAG Test-logic Unit				
t129	TCK Frequency		10	(Unit is MHz)

NOTES:

1. Tested at maximum operating frequency and guaranteed by design characterization at lower operating frequencies.
2. These are not tested. They are guaranteed by characterization.
3. Tested with C_L set at 50 pF. Timings are guaranteed with C_L set at 75 pF.
4. Float condition occurs when maximum output current becomes less than I_{LO} in magnitude. Float delay is not fully tested.
5. These inputs may be asynchronous to CLK2. The setup and hold specifications are given for testing purposes to ensure recognition within a specific CLK2 period.
6. These specifications are for information only and are not tested. They are intended to assist the designer in selecting memory speeds. For each wait state in the design add two CLK2 cycles to the specification.

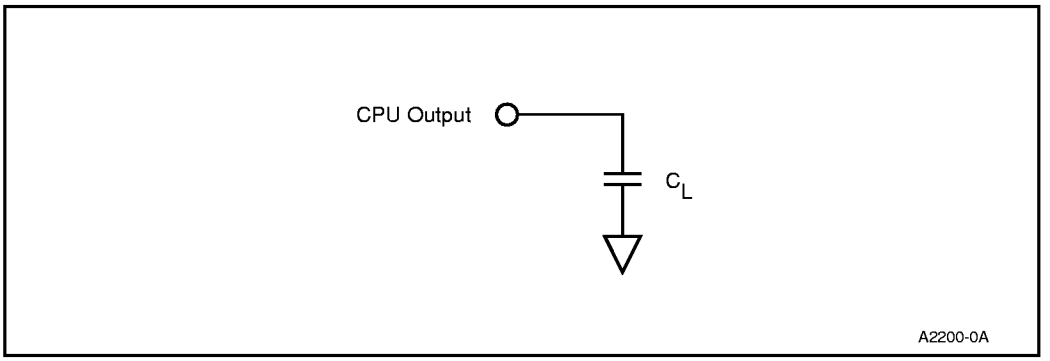


Figure 6. AC Test Loads

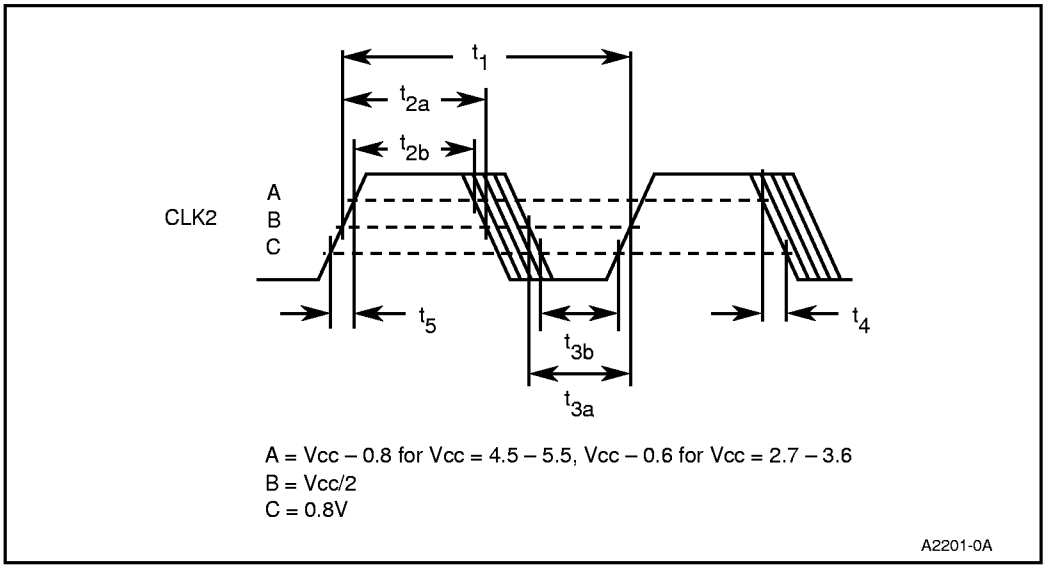


Figure 7. CLK2 Waveform

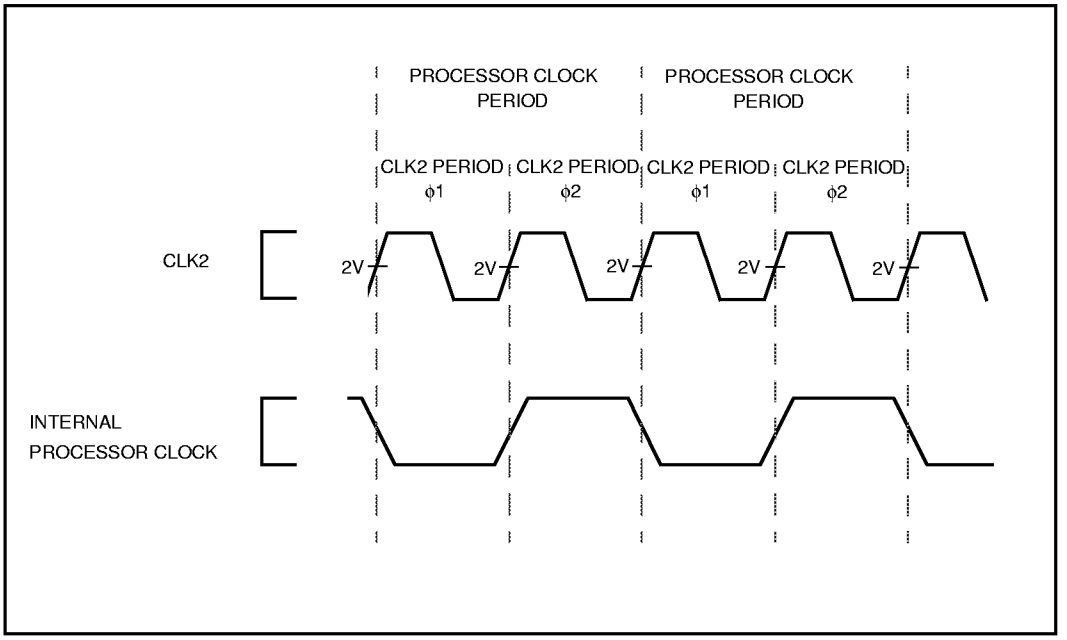


Figure 8. CLK2 Signal and Internal Processor Clock

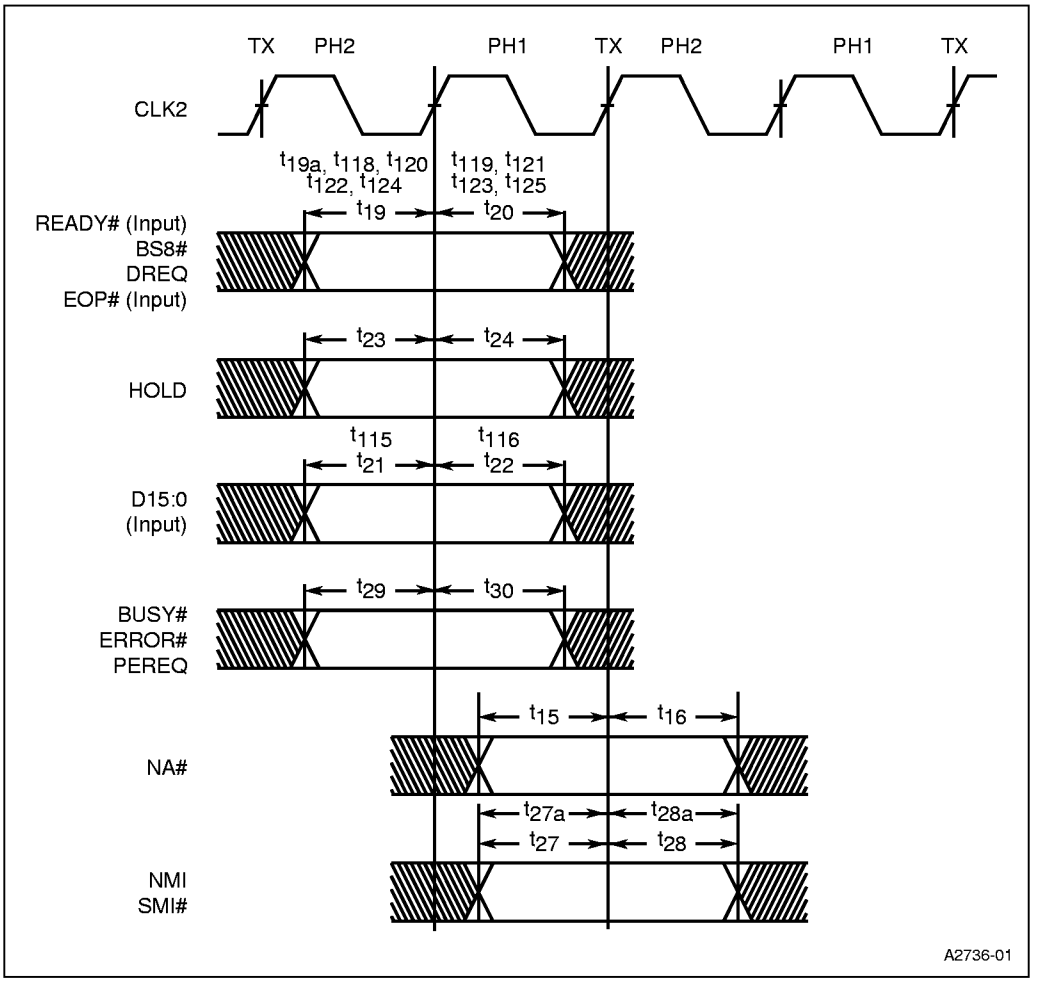


Figure 9. AC Timing Waveforms — Input Setup and Hold Timing

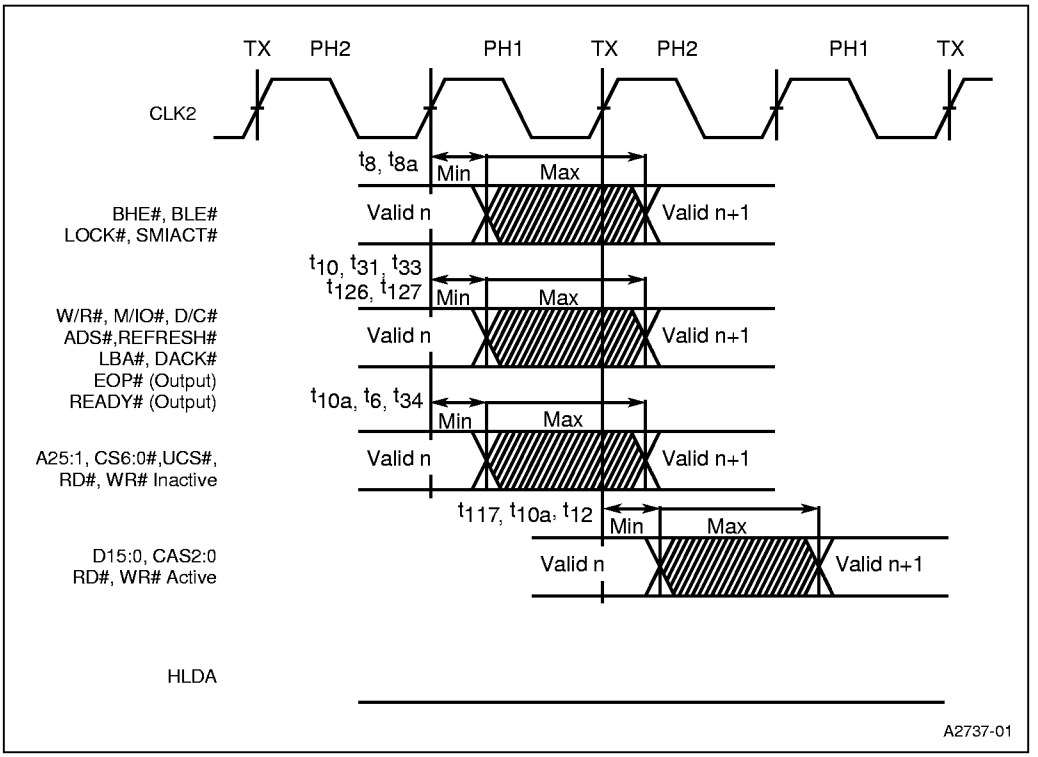


Figure 10. AC Timing Waveforms — Output Valid Delay Timing

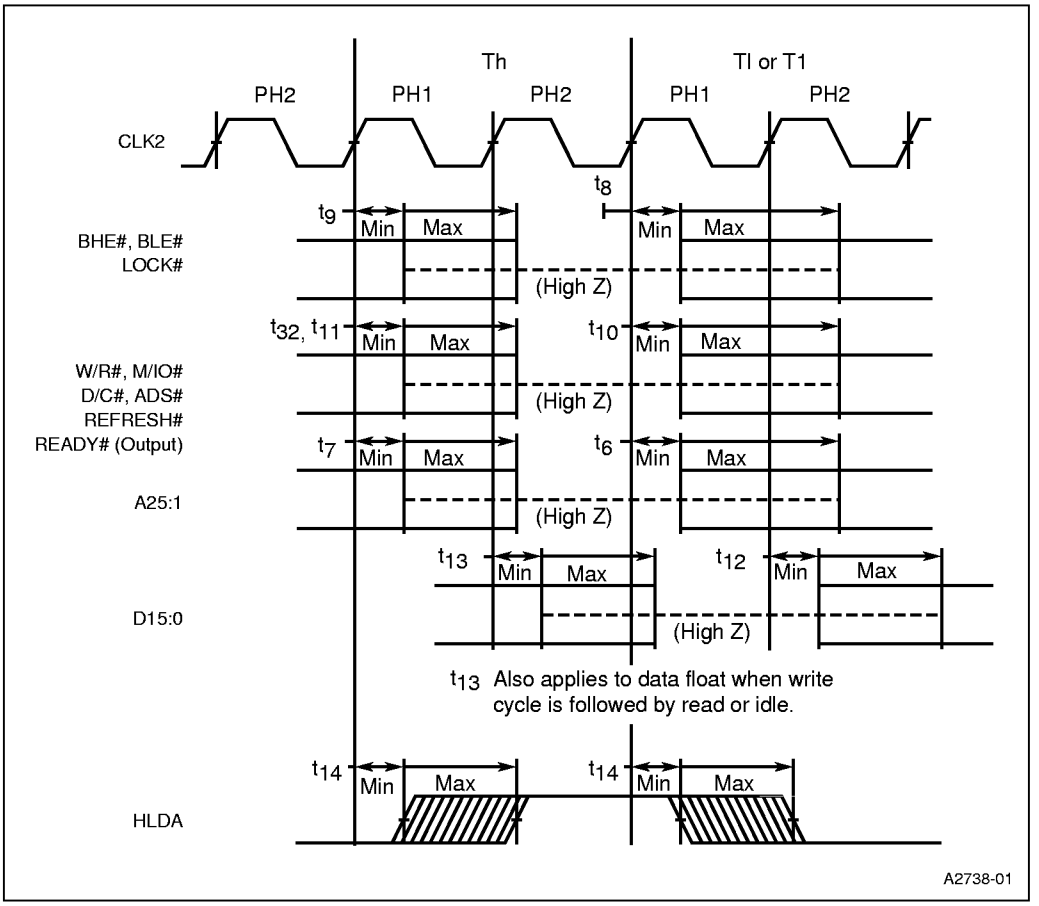


Figure 11. AC Timing Waveforms — Output Float Delay and HLDA Valid Delay Timing

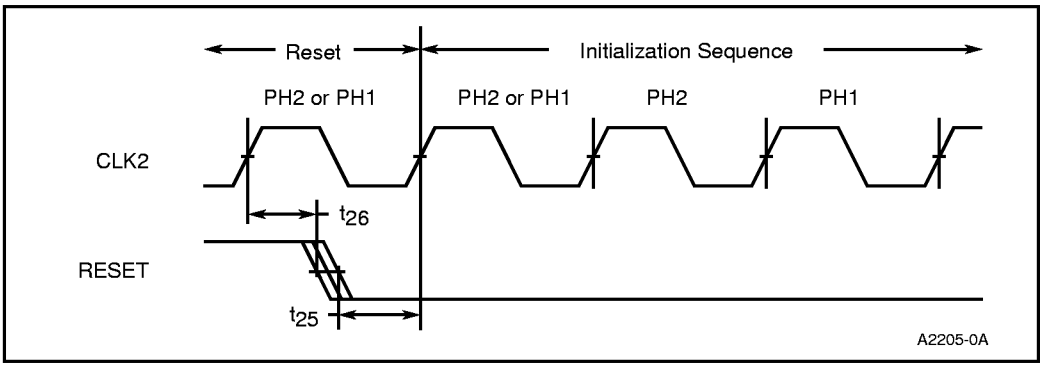


Figure 12. AC Timing Waveforms — RESET Setup and Hold Timing and Internal Phase

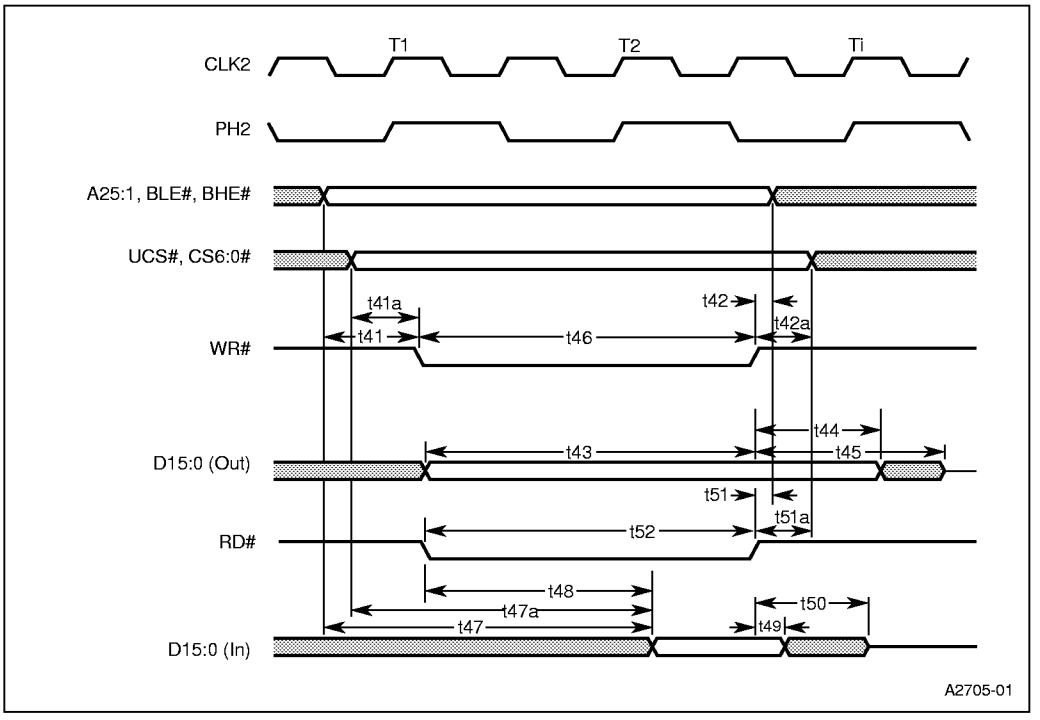


Figure 13. AC Timing Waveforms — Relative Signal Timing

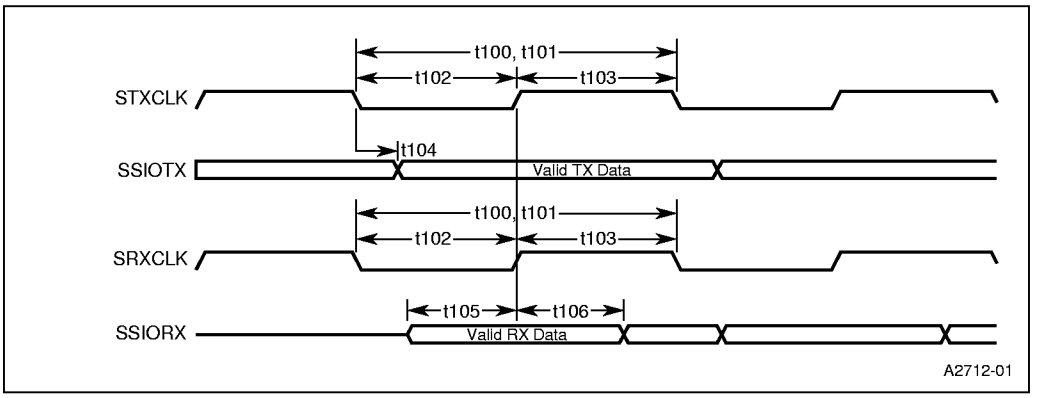


Figure 14. AC Timing Waveforms — SSIO Timing

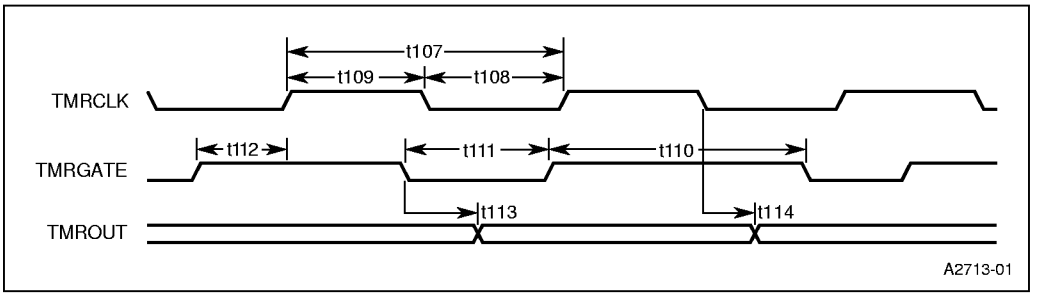
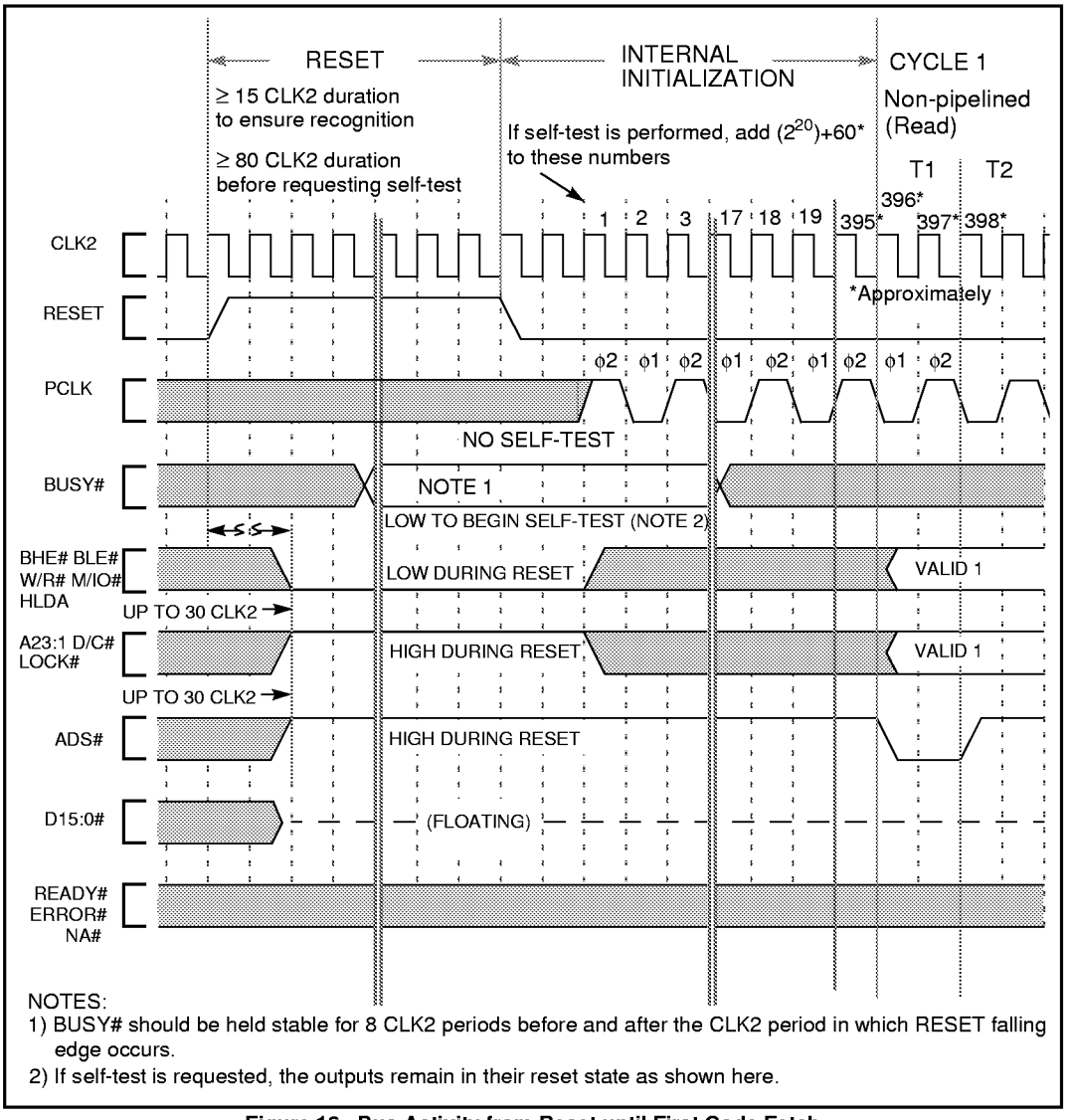


Figure 15. AC Timing Waveforms — Timer/Counter Timing

8.0 BUS CYCLE WAVEFORMS

Figures 16 through 24 present various bus cycles that are generated by the processor. What is shown in the figure is the relationship of the various bus signals to CLK2. These figures along with the information present in AC Specifications allow the user to determine critical timing analysis for a given application.



NOTES:
1) BUSY# should be held stable for 8 CLK2 periods before and after the CLK2 period in which RESET falling edge occurs.
2) If self-test is requested, the outputs remain in their reset state as shown here.

Figure 16. Bus Activity from Reset until First Code Fetch

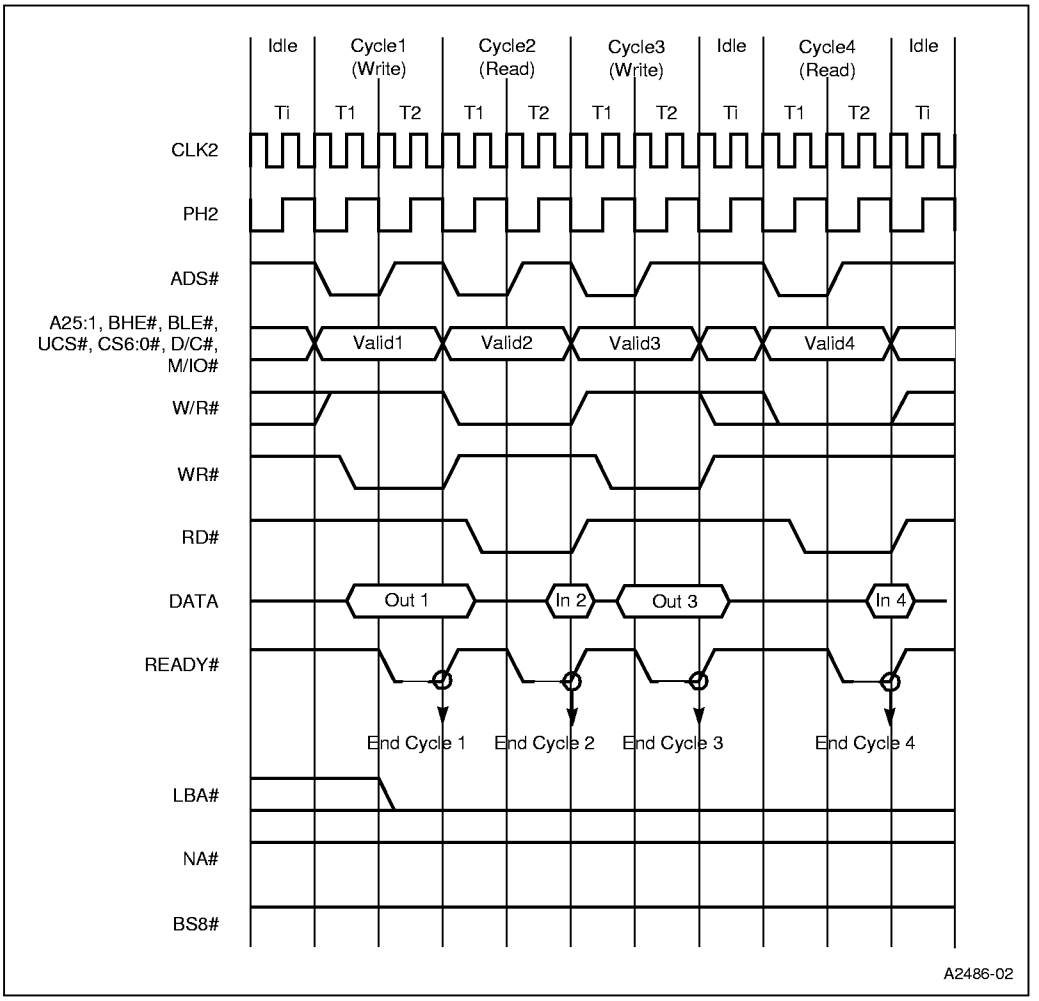


Figure 17. Local Bus Read and Write Cycles (Zero Wait States)

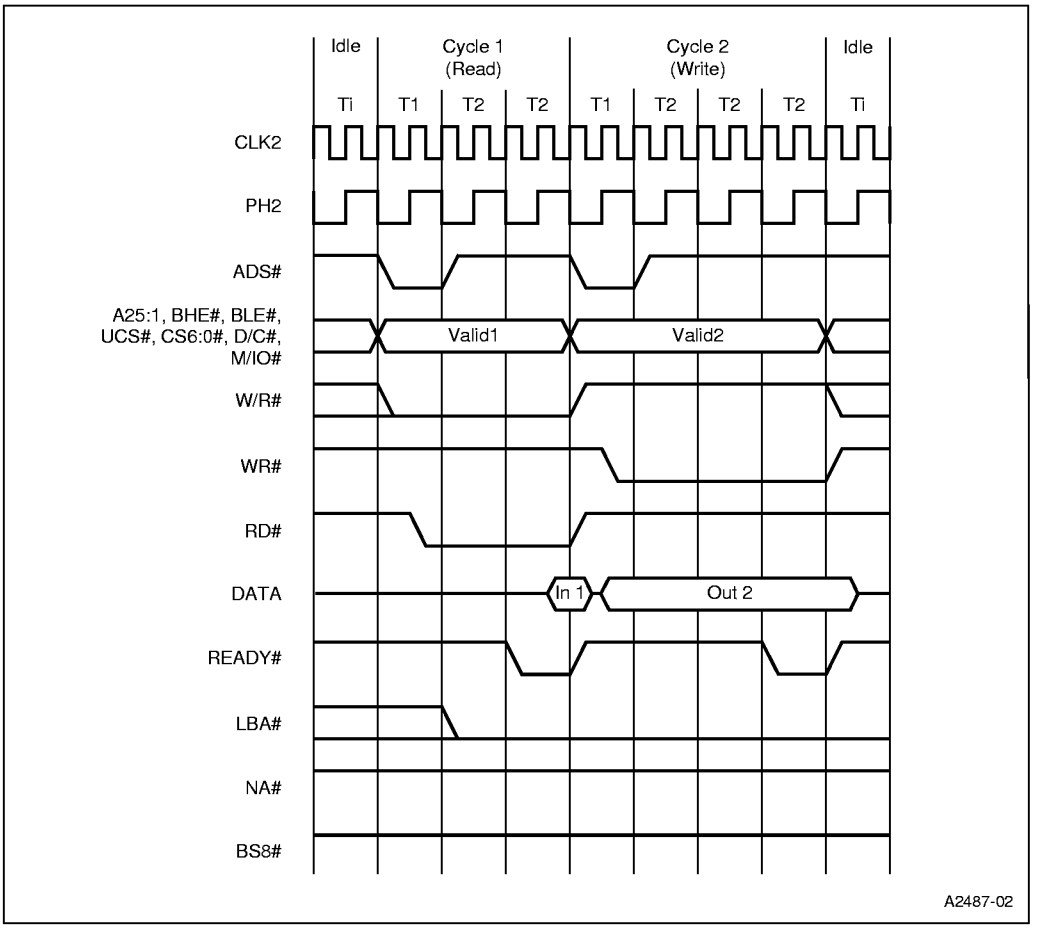


Figure 18. Local Bus Read and Write Cycles (With Wait States)

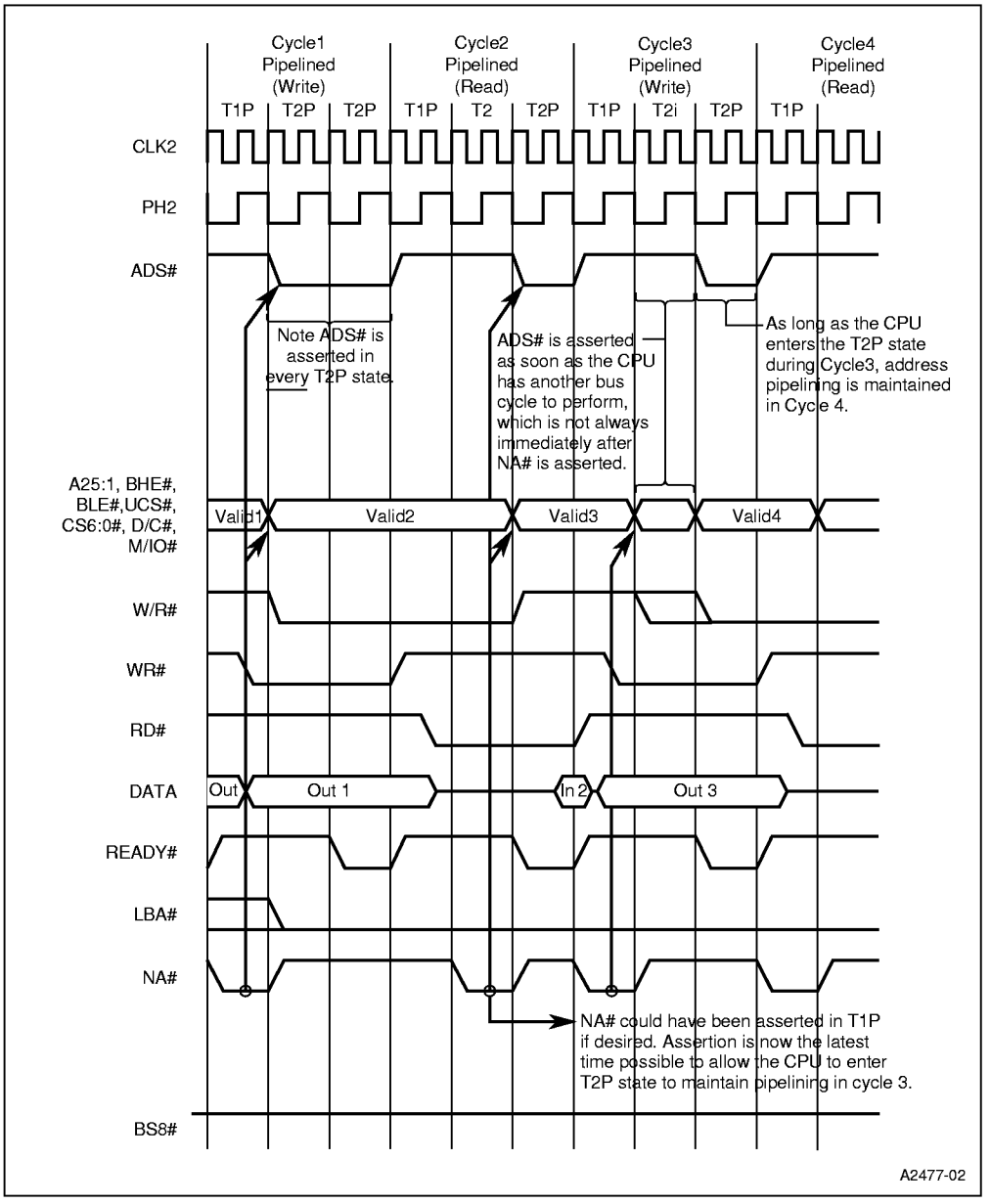


Figure 19. Pipelined Local Bus Read and Write Cycles (With Wait States)

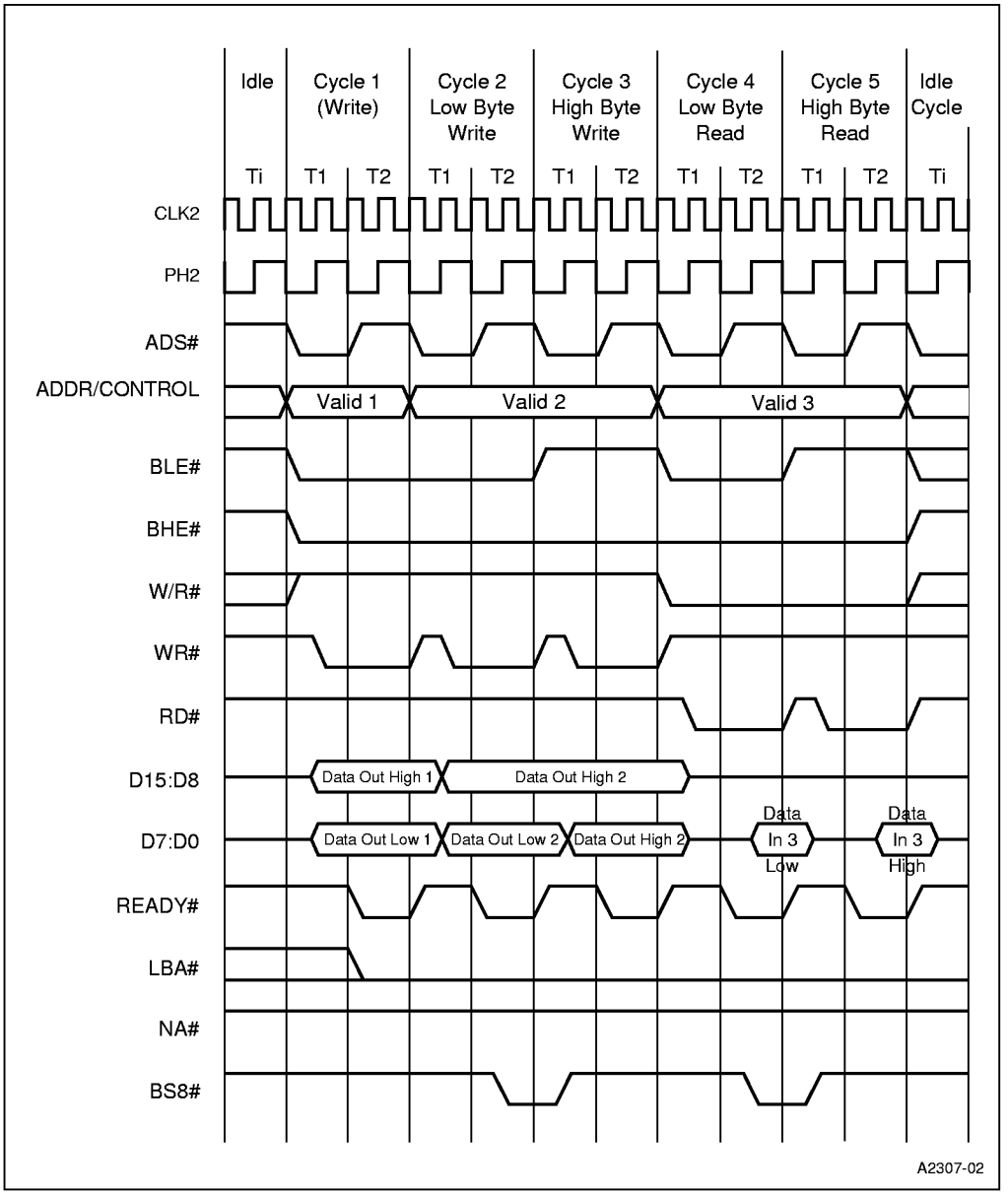


Figure 20. Local Bus Read and Write BS8# Cycles

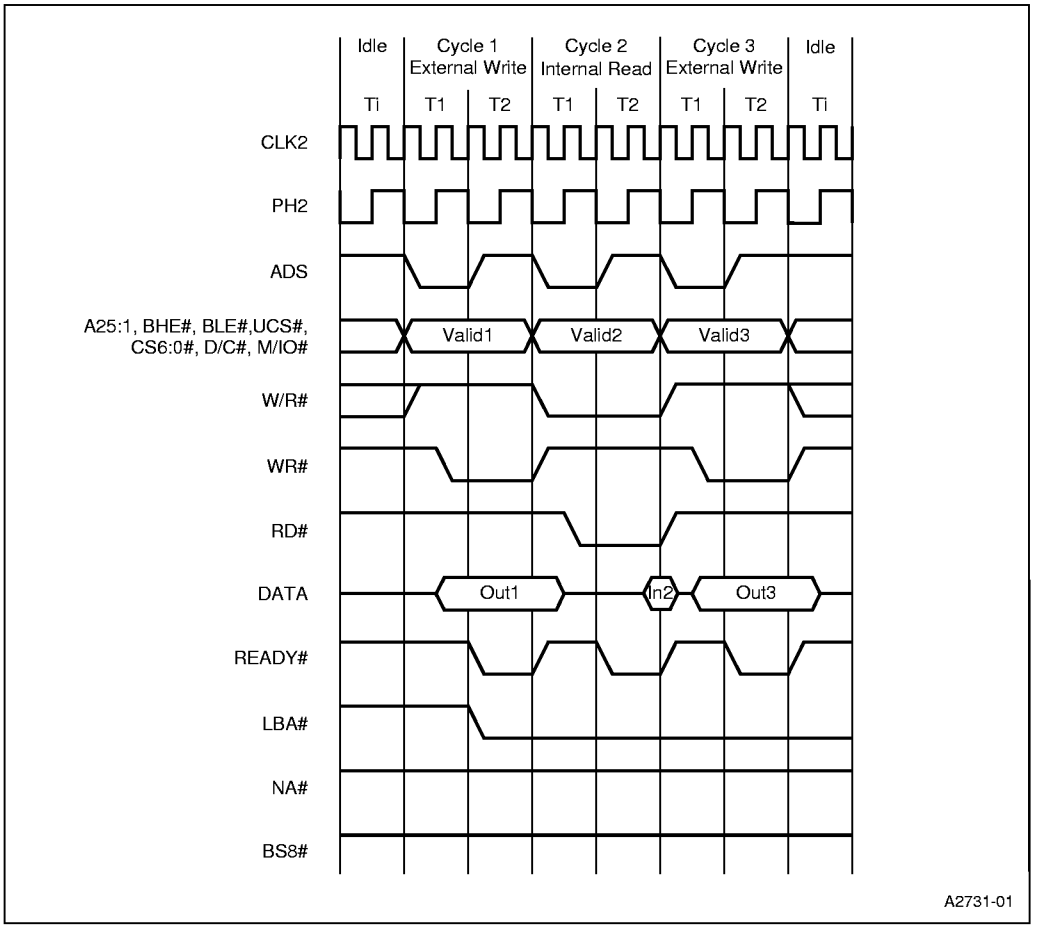


Figure 21. Local Bus Read and Write Cycles (Internal and External)

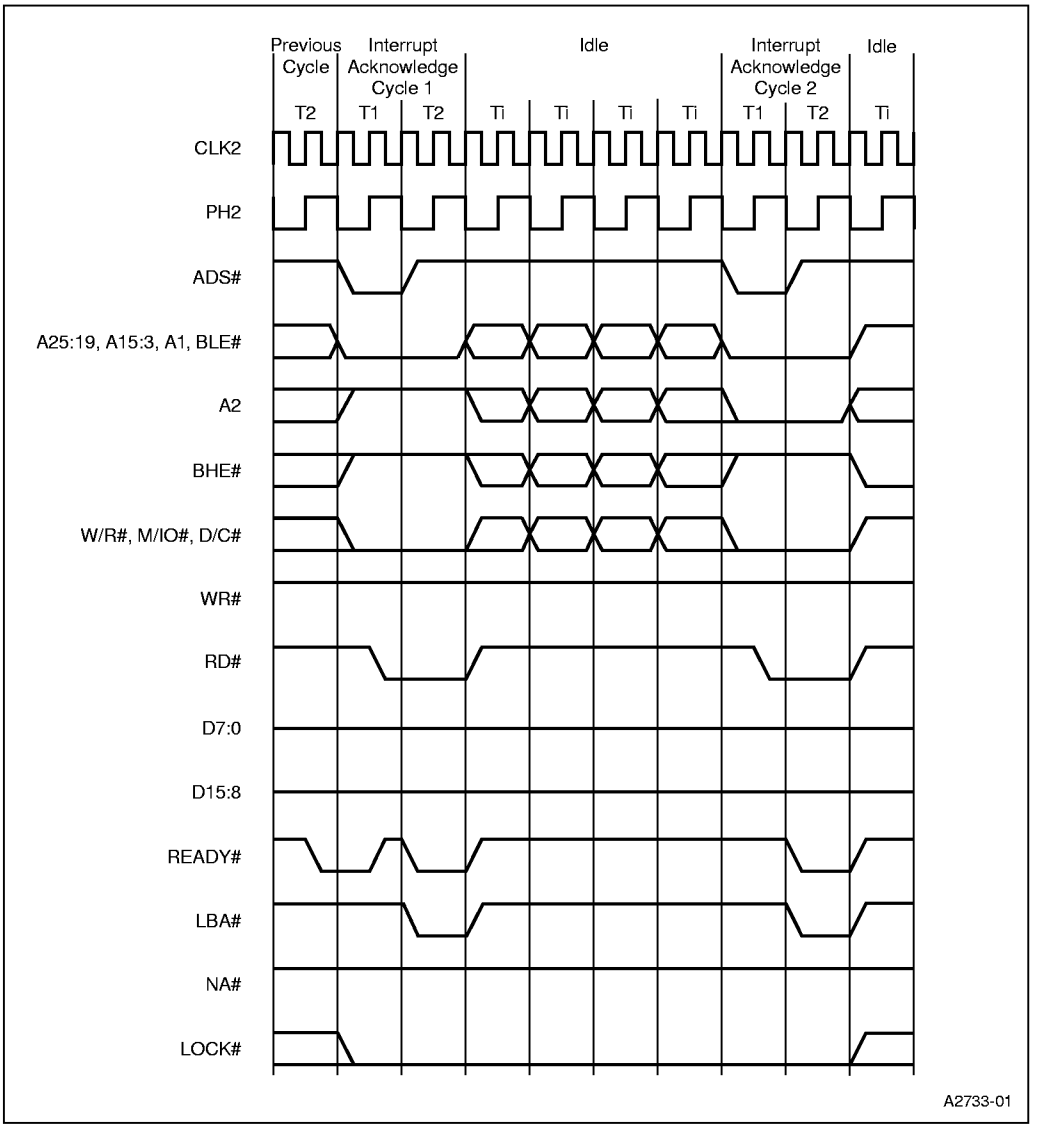


Figure 22. Local Bus Interrupt Acknowledge Cycle (Internal Cascade)

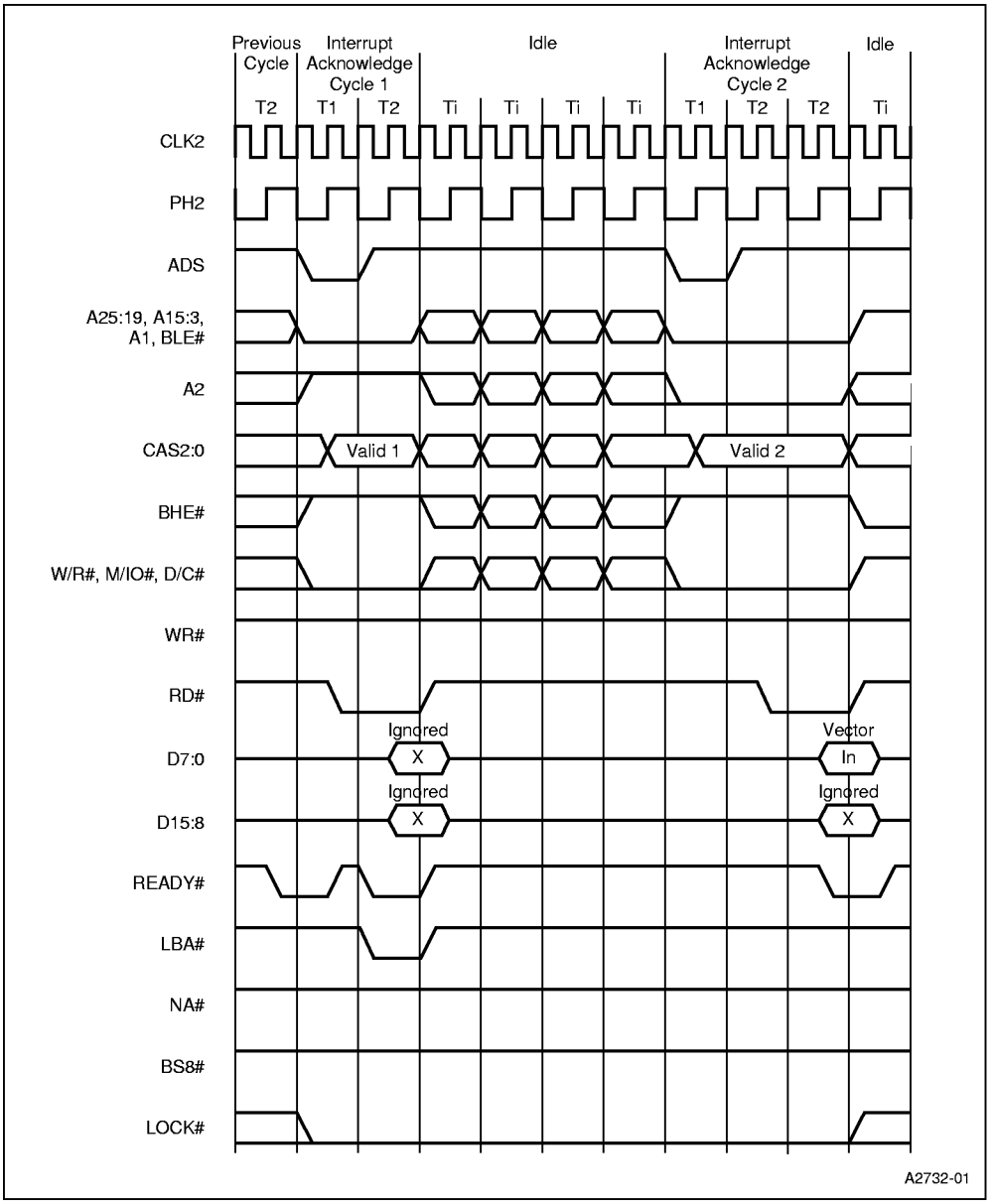


Figure 23. Local Bus Interrupt Acknowledge Cycle (External Cascade)

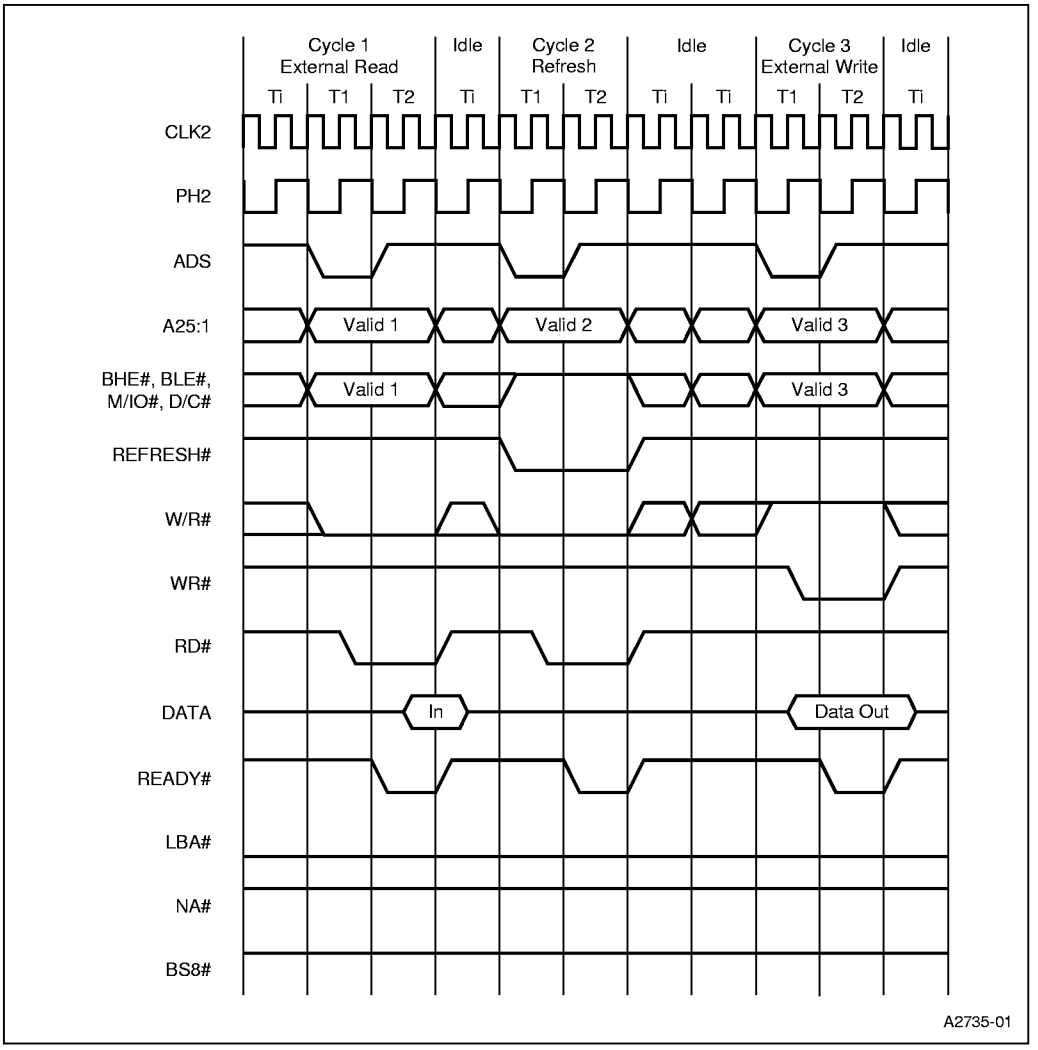


Figure 24. Local Bus Nonpipelined Refresh Cycle

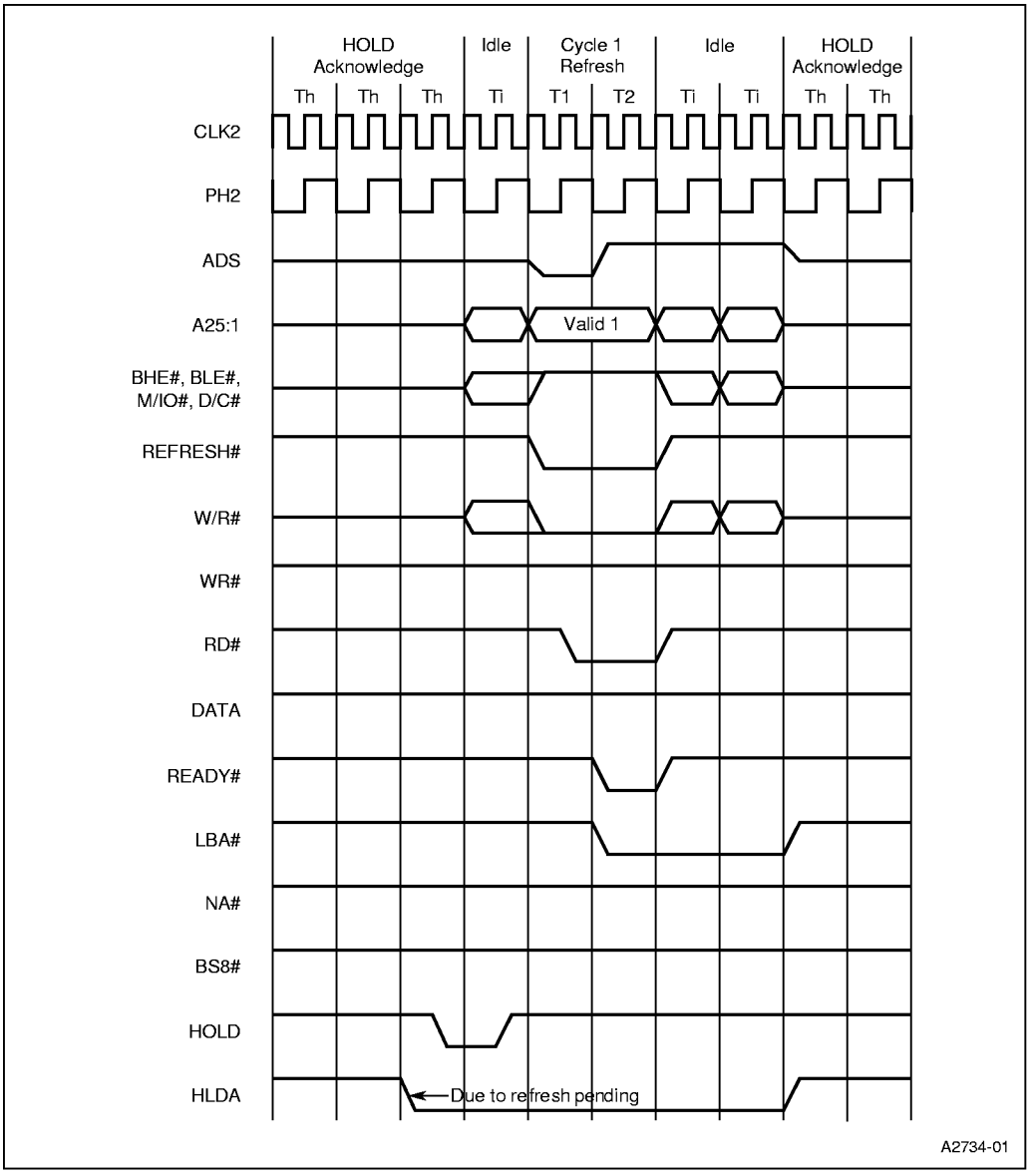


Figure 25. Local Bus Refresh Cycle During HOLD/HLDA

9.0 INTERFACE TO Intel387™ SX MATH COPROCESSOR

The Intel387 SX Math Coprocessor is an extension to the Intel386 EX embedded processor architecture. The combination of the Intel387 SX Math Coprocessor with the Intel386 EX embedded processor dramatically increases the processing speed of computer application software that uses high performance floating-point operations.

An internal Power Management Unit enables the Intel387 SX Math Coprocessor to perform floating-point operations while maintaining very low power consumption for portable and desktop applications. The internal Power Management Unit effectively reduces power consumption by 95% when the device is idle.

This section describes special considerations for interfacing the Intel387 SX Math Coprocessor with the Special Environment Intel386 EX Embedded Processor. For complete information, refer to *Military* Intel387™ SX Math Coprocessor datasheet (Order number 271166).

9.1 System Configuration

The Intel387 SX Math Coprocessor is designed to interface with the Special Environment Intel386™ EX embedded processor as shown in Figure 26.

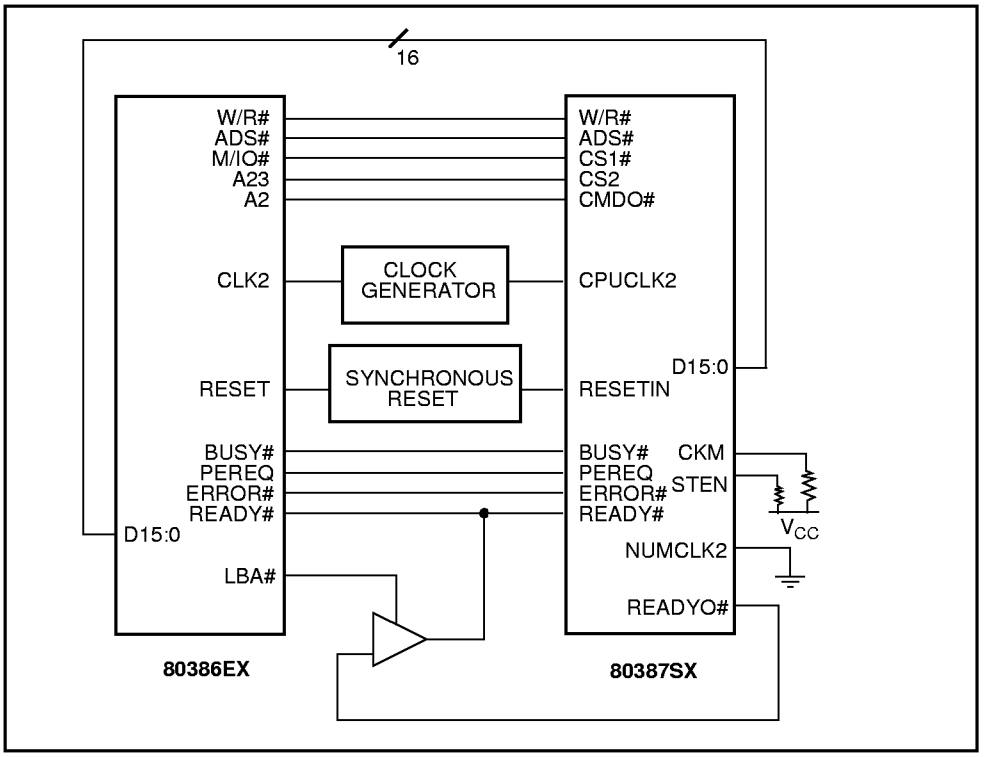


Figure 26. Intel386 EX processor and Intel387 SX Math Coprocessor System Configuration

A dedicated communication protocol makes possible high-speed transfer of opcodes and operands between the CPU and Math Coprocessor. Most Control Pins of the Math Coprocessor are connected directly to CPU pins.

The interface has these characteristics:

- The Math Coprocessor shares the local bus of the Intel386 EX embedded processor.
- The CPU and Math Coprocessor share the same reset signals. They may also share the same clock input.
- The corresponding BUSY#, ERROR#, and PEREQ# pins are connected together.
- The Status Enable (STEN) selects the math coprocessor. It causes the chip to recognize other chip select inputs. STEN must maintain the same setup and hold times as NPS1#, NPS2 and CMDO#.
- The Math Coprocessor NPS1# and NPS2 inputs are connected to the latched CPU M/IO# and A23 inputs respectively. For Math Coprocessor cycles, M/IO# is always LOW and A23 always HIGH.
- The Math Coprocessor input CMD0 is connected to the latched A2 output. The Intel386 EX embedded processor generates address 8000F8H when writing a command and address 8000FCH or 8000FEH (treated as 8000FCH by the Intel387 SX Math Coprocessor) when writing or reading data. It doe not generate any other addresses during Intel387 SX Math Coprocessor bus cycles.
- The READYO# pin of the coprocessor must be sent through a buffer to prevent the CPU and coprocessor from simultaneously driving the READY# pin. The buffer is enabled using the LBA# pin. During internal bus cycles, the LBA# pin is asserted and the CPU provides the READY# signal. In a coprocessor access, the LBA# is deasserted and the buffer is enabled and provides the READY# signal.

The Intel387 SX Math Coprocessor can operate in Synchronous or Asynchronous mode. When CKM is tied to V_{CC} (HIGH), the chip operates in Synchronous mode. When CKM is tied LOW, operation is Asynchronous. For Asynchronous operation, an external clock generator will be necessary to provide the NUMCLK2 input. CPUCLK2 must still be connected to CLK2 of the CPU.

10.0 REVISION HISTORY

Verify with your local Intel sales office that you have the latest version before finalizing a design or ordering devices.

Revision -004 was published on the Intel World Wide Web site only. The titles for figures 2 and 3 were corrected, and the “SMIACT#/EXCSIG” signal name was changed to “SMIACT#” in Figure 4 and Table 2.

Revision -003 was published for the Special Environment Databook; there were no changes from the -002 version.

Revision -002 contained the following changes from the previous version (-001).

- Updated AC Timings according to Intel386™ EX Embedded Processor Addendum.
- The following timing diagrams were added:
  - — CLK2 Signal and Internal Processor Clock
  - — Bus Activity from Reset until First Code Fetch
- The following figures were added:
  - — Top and Bottom 168-lead PGA
  - — 164-lead CQFP
  - — Intel386 EX processor and Intel387 SX Math Coprocessor System Configuration
- Added section 8.0 Interface to Intel387 SX Math Coprocessor