COS/MOS INTEGRATED CIRCUIT

HCC/HCF 4527B

BCD RATE MULTIPLIER

- CASCADABLE IN MULTIPLES OF 4-BITS
- SET TO 9 INPUT AND 9 DETECT OUTPUT
- QUIESCENT CURRENT SPECIFIED TO 20V FOR HCC DEVICE
- STANDARDIZED SYMMETRICAL OUTPUT CHARACTERISTICS
- 5V, 10V, AND 15V PARAMETRIC RATINGS
- INPUT CURRENT OF 100 nA AT 18V AND 25°C FOR HCC DEVICE
- 100% TESTED FOR QUIESCENT CURRENT
- MEETS ALL REQUIREMENTS OF JEDEC TENTATIVE STANDARD No. 13A, "STANDARD SPECIFICATIONS FOR DESCRIPTION OF "B" SERIES CMOS DEVICES"

The **HCC 4527B** (extended temperature range) and **HCF 4527B** (intermediate temperature range) are monolithic integrated circuit, available in 16-lead dual in-line plastic or ceramic package, and ceramic flat package.

The **HCC/HCF 4527** is a low-power 4-bit digital rate multiplier that provides an output-pulse rate which is the clock-input-pulse rate multiplied by 1/10 times the BCD input. For example, when the BCD input is 8, there will be 8 output pulses foe every 10 input pulses. This device may be used to perform arithmetic operations (add, subtract, divide, raise to a power), solve algebraic and differential equations, generate natural logarithms and trigonometric functions, A/D and D/A conversion, and frequency division.

ABSOLUTE MAXIMUM RATINGS

V_{DD}*	Supply voltage: **HCC** types	-0.5 to 20	V
	HCF types	-0.5 to 18	V
V_I	Input voltage	-0.5 to V_{DD} +0.5	V
I_I	DC input current (any one input)	± 10	mA
P_{tot}	Total power dissipation (per package)	200	mW
	Dissipation per output transistor for T_{op}= full package-temperature range	100	mW
T_{op}	Operating temperature: **HCC** types	-55 to 125	°C
	HCF types	-40 to 85	°C
T_{stg}	Storage temperature	-65 to 150	°C

* All voltage values are referred to V_{SS} pin voltage

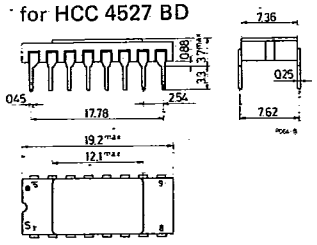
ORDERING NUMBERS:

HCC 4527	BD	for dual in-line ceramic package
HCC 4527	BF	for dual in-line ceramic package, frit seal
HCC 4527	BK	for ceramic flat package
HCF 4527	BE	for dual in-line plastic package
HCF 4527	BF	for dual in-line ceramic package, frit seal

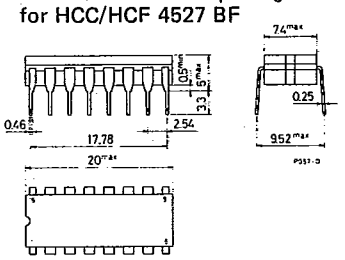
HCC/HCF 4527B

MECHANICAL DATA(dimensions in mm)

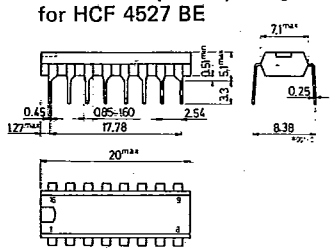
Dual in-line ceramic package for HCC 4527 BD



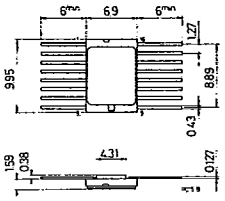
Dual in-line ceramic package for HCC/HCF 4527 BF



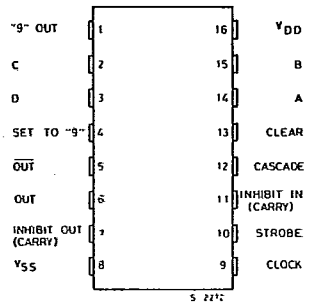
Dual in-line plastic package for HCF 4527 BE



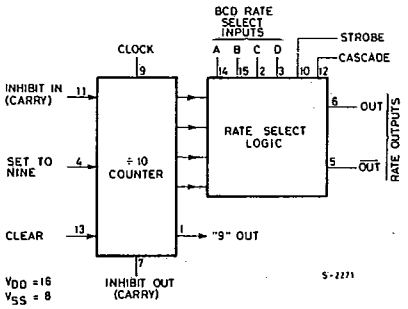
Ceramic flat package for HCC 4527 BK



CONNECTION DIAGRAM



FUNCTIONAL DIAGRAM

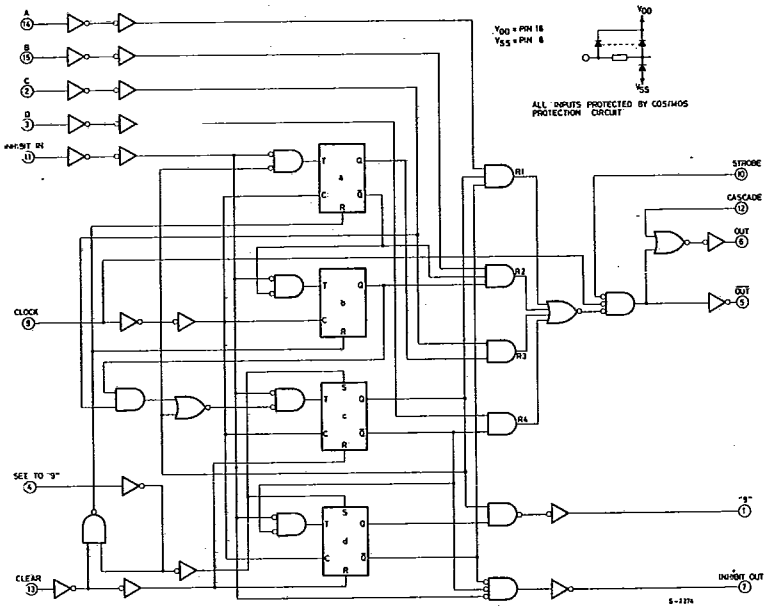


RECOMMENDED OPERATING CONDITIONS

V_{DD}	Supply voltage: **HCC** types	3 to 18	V
	HCF types	3 to 15	V
V_I	Input voltage	0 to V_{DD}	V
T_{op}	Operating temperature: **HCC** types	-55 to 125	°C
	HCF types	-40 to 85	°C

HCC/HCF 4527B

LOGIC DIAGRAM



TRUTH TABLE

INPUTS										OUTPUTS			
Number of Pulses or Input Logic Level (0 = Low; 1 = High; X = Don't Care)										Number of Pulses or Output Logic Level (L = Low; H = High)			
D	C	B	A	CLK	INH IN	STR	CAS	CLR	SET	OUT	$\overline{OUT}$	INH OUT	"9" OUT
0	0	0	0	10	0	0	0	0	0	L	H	1	1
0	0	0	1	10	0	0	0	0	0	1	1	1	1
0	0	1	0	10	0	0	0	0	0	2	2	1	1
0	0	1	1	10	0	0	0	0	0	3	3	1	1
0	1	0	0	10	0	0	0	0	0	4	4	1	1
0	1	0	1	10	0	0	0	0	0	5	5	1	1
0	1	1	0	10	0	0	0	0	0	6	6	1	1
0	1	1	1	10	0	0	0	0	0	7	7	1	1
1	0	0	0	10	0	0	0	0	0	8	8	1	1
1	0	0	1	10	0	0	0	0	0	9	9	1	1
1	0	1	0	10	0	0	0	0	0	8	8	1	1
1	0	1	1	10	0	0	0	0	0	9	9	1	1
1	1	0	0	10	0	0	0	0	0	8	8	1	1
1	1	0	1	10	0	0	0	0	0	9	9	1	1
1	1	1	0	10	0	0	0	0	0	8	8	1	1
1	1	1	1	10	0	0	0	0	0	9	9	1	1
X	X	X	X	10	1	0	0	0	0	▲	▲	H	▲
X	X	X	X	10	0	1	0	0	0	L	H	1	1
X	X	X	X	10	0	0	1	0	0	H	●	1	1
1	X	X	X	10	0	0	0	1	0	10	10	H	L
0	X	X	X	10	0	0	0	0	1	0	1	H	L
X	X	X	X	10	0	0	0	0	1	L	H	L	H

● Output same as the first 16 lines of this truth table (depending on values of A, B, C, D).
▲ Depends on internal state of counter.

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STATIC ELECTRICAL CHARACTERISTICS (over recommended operating conditions)

Parameter			Test conditions V_I (V)	V_O (V)	$\|I_O\|$ (μA)	V_{DD} (V)	Values T_{Low}* Min.	T_{Low}* Max.	25°C Min.	25°C Typ.	25°C Max.	T_{High}* Min.	T_{High}* Max.	Unit
I_L	Quiescent current	HCC types	0/ 5			5		5		0.04	5		150	μA
			0/10			10		10		0.04	10		300	
			0/15			15		20		0.04	20		600	
			0/20			20		100		0.08	100		3000	
		HCF types	0/ 5			5		20		0.04	20		150	
			0/10			10		40		0.04	40		300	
			0/15			15		80		0.04	80		600	
V_{OH}	Output high voltage		0/ 5		< 1	5	4.95		4.95			4.95		V
			0/10		< 1	10	9.95		9.95			9.95		
			0/15		< 1	15	14.95		14.95			14.95		
V_{OL}	Output low voltage		5/0		< 1	5		0.05			0.05		0.05	V
			10/0		< 1	10		0.05			0.05		0.05	
			15/0		< 1	15		0.05			0.05		0.05	
V_{IH}	Input high voltage			0.5/4.5	< 1	5	3.5		3.5			3.5		V
				1/9	< 1	10	7		7			7		
				1.5/13.5	< 1	15	11		11			11		
V_{IL}	Input low voltage			4.5/0.5	< 1	5		1.5			1.5		1.5	V
				9/1	< 1	10		3			3		3	
				13.5/1.5	< 1	15		4			4		4	
I_{OH}	Output drive current	HCC types	0/ 5	2.5		5	-2		-1.6	-3.2		-1.15		mA
			0/ 5	4.6		5	-0.64		-0.51	-1		-0.36		
			0/10	9.5		10	-1.6		-1.3	-2.6		-0.9		
			0/15	13.5		15	-4.2		-3.4	-6.8		-2.4		
		HCF types	0/ 5	2.5		5	-1.53		-1.36	-3.2		-1.1		
			0/ 5	4.6		5	-0.52		-0.44	-1		-0.36		
			0/10	9.5		10	-1.3		-1.1	-2.6		-0.9		
			0/15	13.5		15	-3.6		-3.0	-6.8		-2.4		
I_{OL}	Output sink current	HCC types	0/ 5	0.4		5	0.64		0.51	1		0.36		mA
			0/10	0.5		10	1.6		1.3	2.6		0.9		
			0/15	1.5		15	4.2		3.4	6.8		2.4		
		HCF types	0/ 5	0.4		5	0.52		0.44	1		0.36		
			0/10	0.5		10	1.3		1.1	2.6		0.9		
			0/15	1.5		15	3.6		3.0	6.8		2.4		
I_{IH}, I_{IL}	Input leakage current	HCC types	0/18	Any input		18		±0.1		$±10^{-5}$	±0.1		± 1	μA
		HCF types	0/15			15		±0.3		$±10^{-5}$	±0.3		± 1	
C_I	Input capacitance			Any input						5	7.5			pF

* T_{Low} = − 55°C for **HCC** device: −40°C for **HCF** device.
* T_{High} = +125°C for **HCC** device: +85°C for **HCF** device.
The Noise Margin for both "1" and "0" level is: 1V min. with V_{DD}= 5V
2V min. with V_{DD}= 10V
2,5V min. with V_{DD}= 15V

DYNAMIC ELECTRICAL CHARACTERISTICS (T_{amb}= 25°C, C_L= 50 pF, R_L= 200 kΩ, typical temperature coefficient for all V_{DD} values is 0.3%/°C, all input rise and fall times = 20 ns)

Parameter		Test conditions	Values			Unit
		V_{DD} (V)	Min.	Typ.	Max.	
t_{PHL}, t_{PLH} Propagation delay time	Clock to out	5		110	220	ns
		10		55	110	
		15		45	90	
	Clock or strobe to out	5		150	300	ns
		10		75	150	
		15		60	120	
	Clock to inhibit out high level to low level	5		320	640	ns
		10		145	290	
		15		100	200	
	Low level to high level	5		250	500	ns
		10		100	200	
		15		75	150	
	Clear to out	5		380	760	ns
		10		175	350	
		15		130	260	
	Clock to "9" or "1" out	5		300	600	ns
		10		125	250	
		15		90	180	
	Cascade to out	5		90	180	ns
		10		45	90	
		15		35	70	
	Inhibit input to inhibit out	5		130	260	ns
		10		60	120	
		15		45	90	
	Set to out	5		330	660	ns
		10		150	300	
		15		110	220	
t_{THL}, t_{TLH} Transition time		5		100	200	ns
		10		50	100	
		15		40	80	
f_{CL} Maximum clock frequency		5	1.2	2.4		MHz
		10	2.5	5		
		15	3.5	7		
t_W Clock pulse width		5	330	165		ns
		10	170	85		
		15	100	50		
t_r, t_f Clock rise or fall time		5			15	μs
		10			15	
		15			15	
t_W Set or clear pulse width		5	160	80		ns
		10	90	45		
		15	60	30		

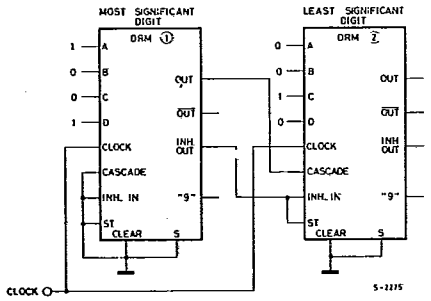
DYNAMIC ELECTRICAL CHARACTERISTICS (continued)

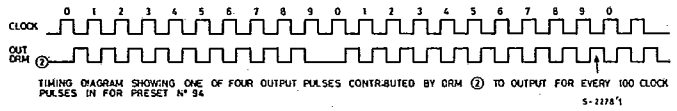
Parameter		Test conditions	Values			Unit
		V_{DD} (V)	Min.	Typ.	Max.	
t_{setup}	Inhibit input setup time	5	100	50		ns
		10	40	20		
		15	20	10		
t_R	Inhibit input removal time	5	240	120		ns
		10	130	65		
		15	110	55		
t_R	Set removal time	5	150	75		ns
		10	80	40		
		15	50	25		
t_R	Clear removal time	5	60	30		ns
		10	40	20		
		15	30	15		

APPLICATIONS NOTE

For fractional multipliers with more than one digit, **HCC/HCF 4527** devices may be cascaded in two different modes: the Add mode and the Multiply mode. See figs. 1 and 3.

Fig. 1 - Two **HCC/HCF 4527B** cascaded in the "Add" mode with a preset number





TIMING DIAGRAM SHOWING ONE OF FOUR OUTPUT PULSES CONTRIBUTED BY ORM ② TO OUTPUT FOR EVERY 100 CLOCK PULSES IN FOR PRESET N° 94

5-2276/1

When two units are cascaded in Add mode and programmed to 9 and 4 respectively, the more significant unit will have 9 output pulses for every 10 input pulses and the other unit will have 4 output pulses for every 100 input pulses for a total of $\frac{9}{10} + \frac{4}{100} = \frac{94}{100}$.

APPLICATIONS NOTE (continued)

The Addition of two variables, A and B is instead obtained with this application:

Fig. 2 - Addition of two variables, A and B

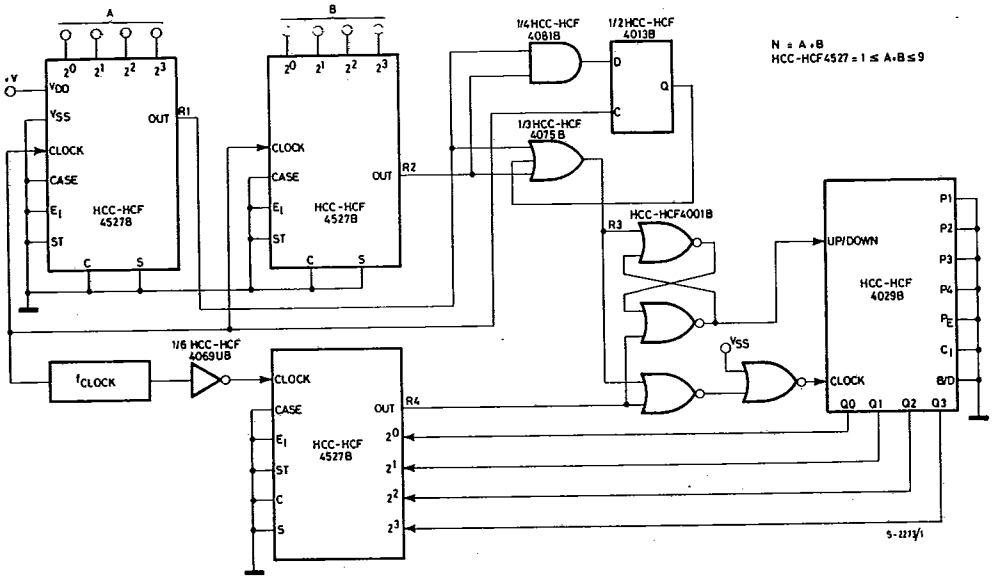
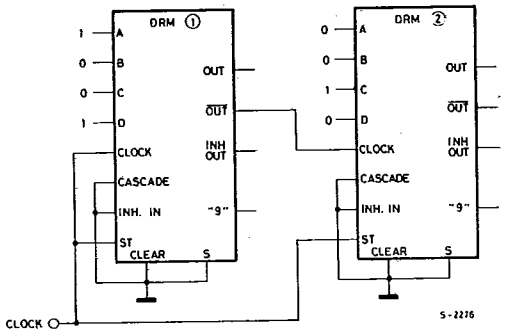


Fig. 3 - Two **HCC/HCF 4527B** cascaded in the "Multiply" mode with a preset number



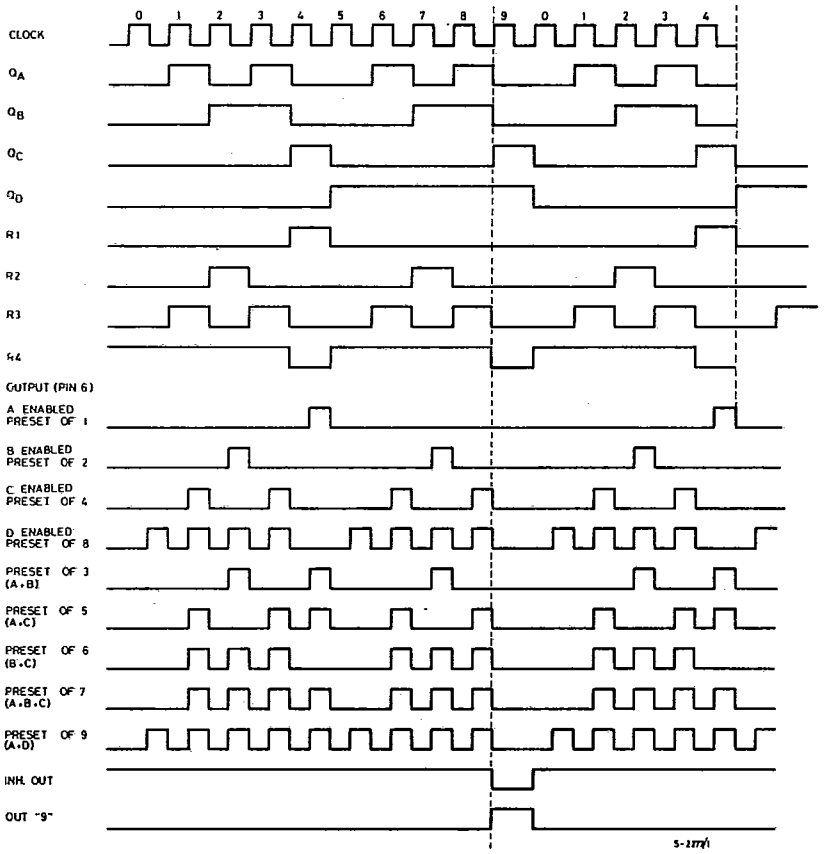
In the Multiply mode, the fraction programmed into the first rate multiplier is multiplied by the fraction programmed into the second one: If $N_1 = 9$ and $N_2 = 4$

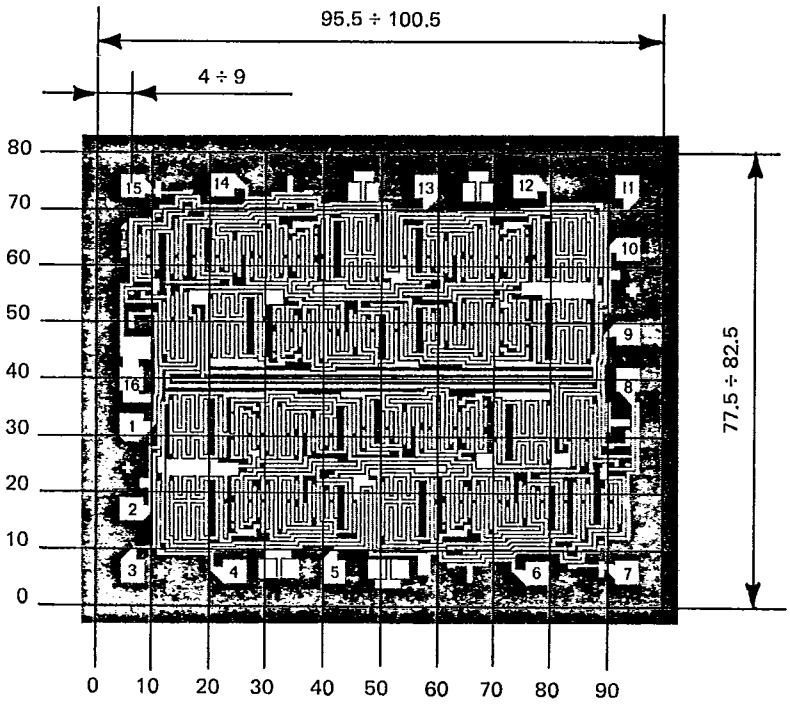
$f_{out2} = (\frac{4}{10}) \cdot f_{out1}$ $\quad f_{out1} = \frac{9}{10} f_{clock}$ $\quad f_{out2} = \frac{4}{10} \times (\frac{9}{10} f_{clock}) = \frac{36}{100} f_{clock}$

There fore 36 output pulses for every 100 clock input pulses.

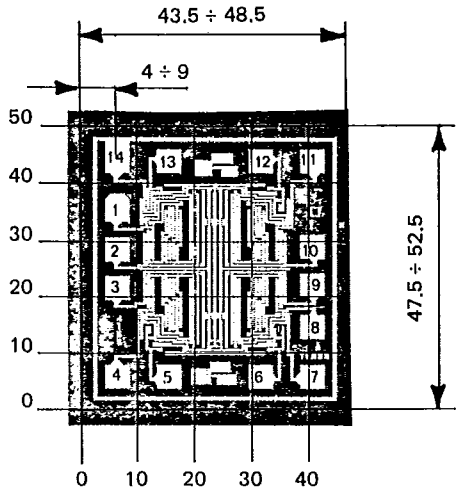
APPLICATIONS NOTE (continued)

Fig. 4 - Timing diagram (see Logic Diagram)




95.5 ÷ 100.5
4 ÷ 9
77.5 ÷ 82.5
80
70
60
50
40
30
20
10
0
0 10 20 30 40 50 60 70 80 90
15 14 13 12 11 10 9 8 16 1 2 3 4 5 6 7

4015B


43.5 ÷ 48.5
4 ÷ 9
47.5 ÷ 52.5
50
40
30
20
10
0
0 10 20 30 40
14 13 12 11 1 2 3 10 9 8 4 5 6 7

4016B