YAMAHA

YSS932

AC3D3B

96kHz DIR + Dolby Digital / Pro Logic II / DTS decoder + Sub DSP

■ OUTLINE

YSS932 is one chip LSI consisting of three built-in blocks : SPDIF receiver (DIR), Dolby Digital (AC-3) / Pro Logic II & DTS decoder (Main DSP) and programmable sound fields processing DSP (Sub DSP).

The Sub DSP is capable of realizing various sound fields, such as virtual surround by down-loading the program and coefficient from outside.

■ FEATURES

[DIR Block]

- Sampling frequency: Two ranges are available including;
  32k to 48kHz (normal rate) and 64k to 96kHz (double rate).
- Provides master clock, 256fs, to DAC, ADC and the other peripheral devices. The clock output can be controlled with various modes determined by register settings.
- Has a pin that indicates the double rate operation.
- Every channel status and user data can be read through the microprocessor interface.
- Has an output pin for interrupt that is activated by changing of the status information.
- Internal operation frequency: 25MHz

[Main DSP Block]

- Dolby Digital (AC-3) / Pro Logic II and DTS decode.
- High quality internal 24 bit DSP.
- No external memory is required. (Memory for the center and surround channel signal delay is included.)
- AC-3 Karaoke mode.
- Supports compression mode at AC-3 / DTS decoding.
- Included de-emphasis filter for the PCM signal.
- Pro Logic II decoding for Dolby Digital 2 channels decoded signal as well as ordinary PCM signal.
- Reads Dolby Digital / DTS decode information through the microprocessor interface.
- Internal operation frequency: 30MHz

[Sub DSP Block]

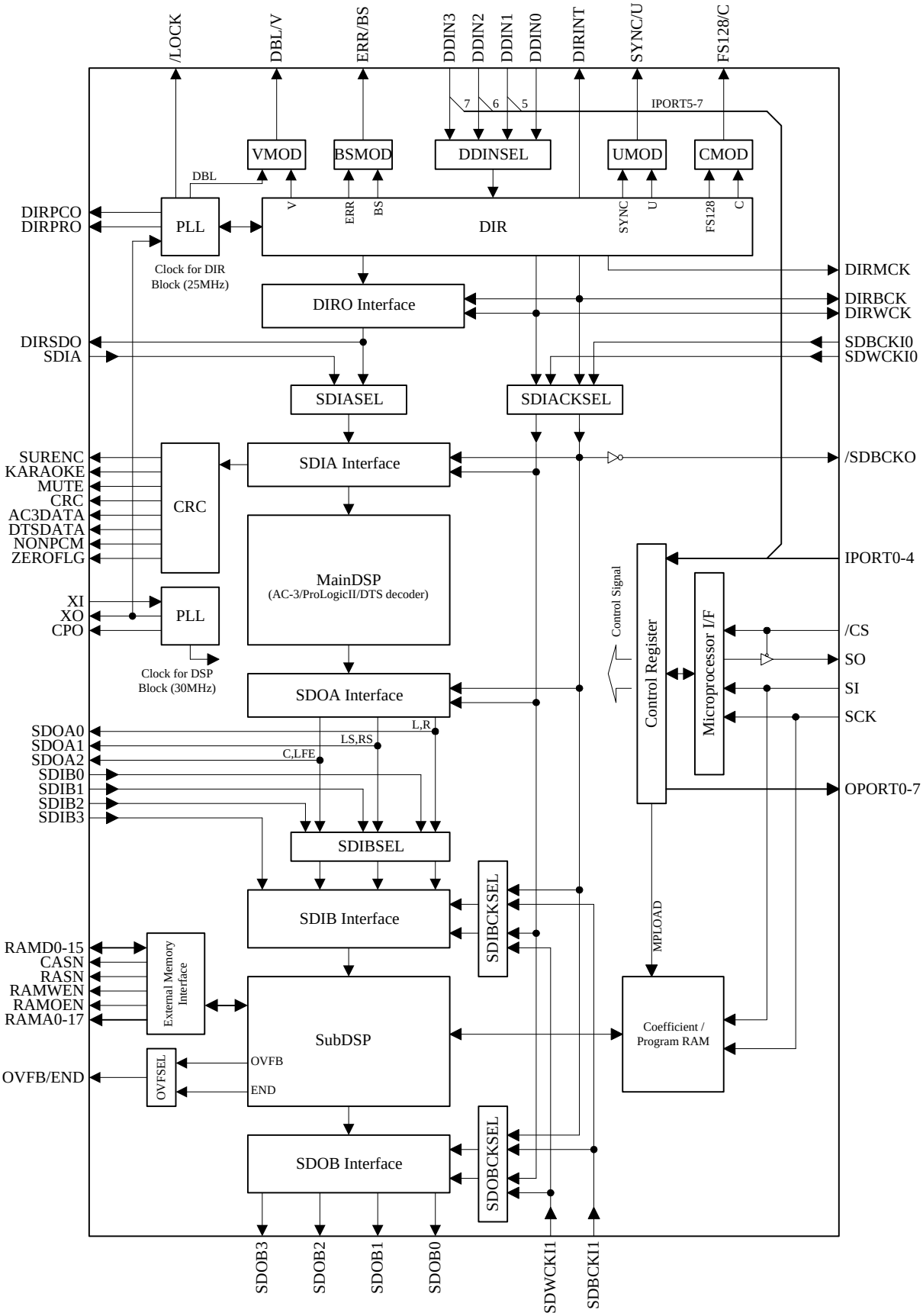
- Capable of realizing various sound fields, such as simulation surround, output configuration and virtual surround by downloading the programs from the microprocessor.
- Adoption of the 32 bit floating-point DSP assuring highly accurate processing.
- Up to 2.73 seconds delay at fs=48kHz achievable by adding DRAM or SRAM externally.
- Internal operation frequency: 30MHz

[Other Features]

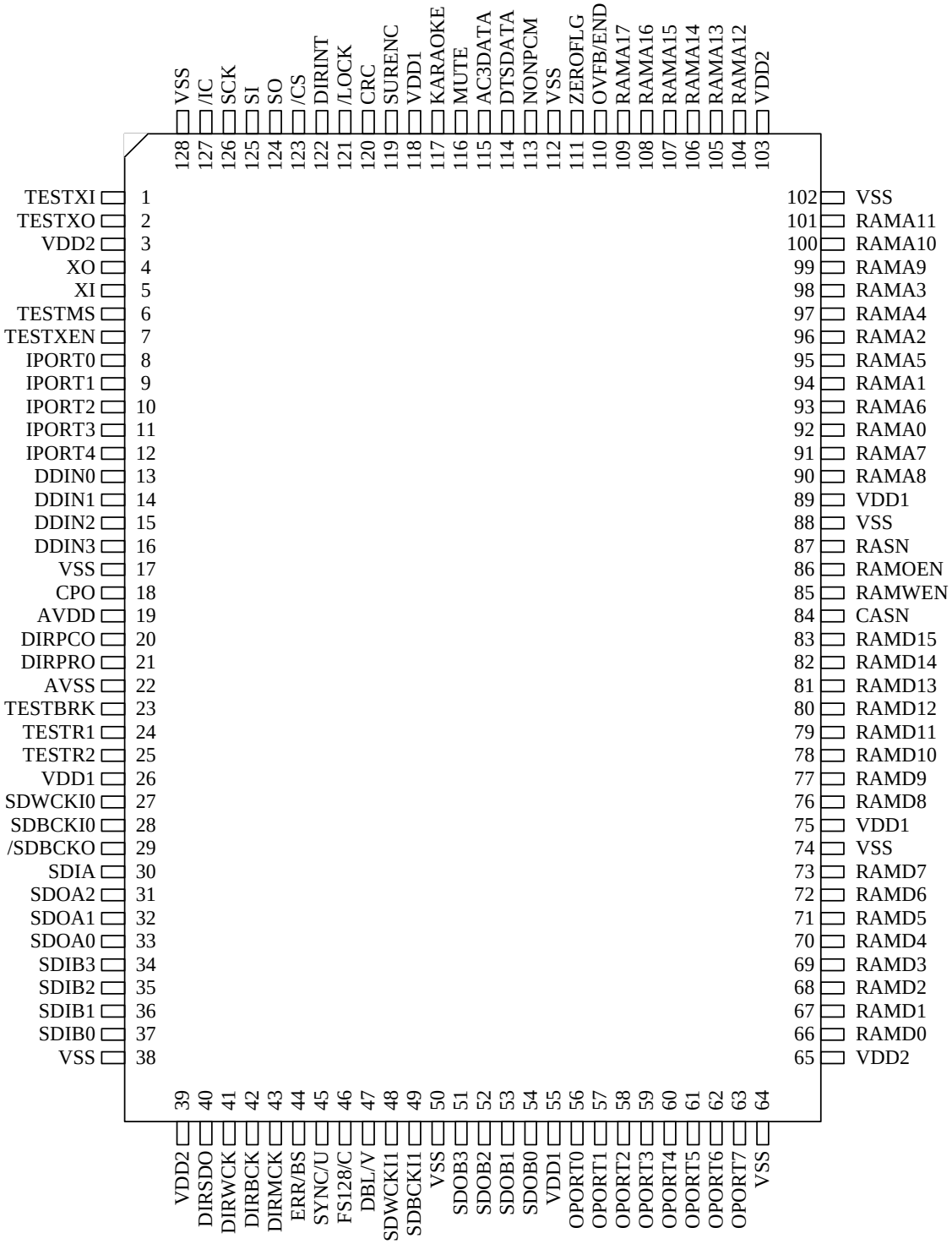
- Connectable to almost all ADC and DAC by making appropriate settings to the control register.
- Total of 16 general purpose input/output ports are provided.
- 2 built-in PLL circuits for generation of operation clocks for DIR block and DSP blocks.
- Power supply voltage: 2 power sources (2.5V for core logic section and 3.3V for I/O section)
- Si-gate CMOS process
- 128SQFP (YSS932-S)

Note: "AC-3" and "Pro Logic II" are registered trademarks of Dolby Laboratories Licensing corporation.
"DTS" is a registered trademark of DTS, Inc.
Use of this LSI must be licensed by both Dolby Laboratories Licensing Corporation and DTS, Inc.

■ BLOCK DIAGRAM



■ PIN CONFIGRATION



< 128SQFP TOP VIEW >

■ PIN FUNCTION

No.	Name	I/O	Function
1	TESTXI	I	LSI Test pin (must be connected to VSS)
2	TESTXO	O	LSI Test pin (to be open)
3	VDD2	-	+2.5V power supply (for internal core logic)
4	XO	O	Crystal oscillator connection
5	XI	I	Crystal oscillator connection (24.576MHz)
6	TESTMS	I+	LSI Test pin (to be open)
7	TESTXEN	I+	LSI Test pin (to be open)
8	IPORT0	I+	General purpose input port
9	IPORT1	I+	General purpose input port
10	IPORT2	I+	General purpose input port
11	IPORT3	I+	General purpose input port
12	IPORT4	I+	General purpose input port
13	DDIN0	Is	DIR: Digital audio interface data input 0
14	DDIN1	Is	DIR: Digital audio interface data input 1 / General purpose input port
15	DDIN2	Is	DIR: Digital audio interface data input 2 / General purpose input port
16	DDIN3	Is	DIR: Digital audio interface data input 3 / General purpose input port
17	VSS	-	Ground
18	CPO	A	PLL filter connection
19	AVDD	-	+3.3V power supply (for DIR block)
20	DIRPCO	A	DIR: PLL filter connection
21	DIRPRO	A	DIR: PLL filter connection
22	AVSS	-	Ground (for DIR block)
23	TESTBRK	I+	LSI Test pin (to be open)
24	TESTR1	I+	Initial Clear input for PLL in DSP block
25	TESTR2	I+	LSI Test pin (to be open)
26	VDD1	-	+3.3V power supply (for I/O)
27	SDWCKI0	I+	Word clock input for SDIA, SDOA, SDIB, SDOB
28	SDBCKI0	I+	Bit clock input for SDIA, SDOA, SDIB, SDOB
29	/SDBCKO	O	Reverse clock output of DIRBCK or SDBCKI0
30	SDIA	I	Input of bitstream or PCM data to Main DSP
31	SDOA2	O	PCM data output from Main DSP (C, LFE)
32	SDOA1	O	PCM data output from Main DSP (LS, RS)
33	SDOA0	O	PCM data output from Main DSP (L, R)
34	SDIB3	I+	PCM data input 3 to Sub DSP
35	SDIB2	I+	PCM data input 2 to Sub DSP
36	SDIB1	I+	PCM data input 1 to Sub DSP
37	SDIB0	I+	PCM data input 0 to Sub DSP
38	VSS	-	Ground
39	VDD2	-	+2.5V power supply (for internal core logic)
40	DIRSDO	O	Output of bitstream or PCM data from DIR
41	DIRWCK	O	DIR: Serial data word clock (fs) output
42	DIRBCK	O	DIR: Serial data bit clock (64fs) output
43	DIRMCK	O	DIR: Serial data master clock (256fs or 128fs) output
44	ERR/BS	O	DIR: Data error detect / Block start output
45	SYNC/U	O	DIR: Serial data synchronized timing / User data output
46	FS128/C	O	DIR: Serial data master clock 128fs / Channel status output
47	DBL/V	O	DIR: Double rate lock detect / Validity flag output
48	SDWCKI1	I+	Word clock input for SDIB, SDOB
49	SDBCKI1	I+	Bit clock input for SDIB, SDOB
50	VSS	-	Ground
51	SDOB3	O	PCM data output from Sub DSP
52	SDOB2	O	PCM data output from Sub DSP
53	SDOB1	O	PCM data output from Sub DSP
54	SDOB0	O	PCM data output from Sub DSP
55	VDD1	-	+3.3v power supply (for I/O)

No.	Name	I/O	Function
56	OPORT0	O	General purpose output port
57	OPORT1	O	General purpose output port
58	OPORT2	O	General purpose output port
59	OPORT3	O	General purpose output port
60	OPORT4	O	General purpose output port
61	OPORT5	O	General purpose output port
62	OPORT6	O	General purpose output port
63	OPORT7	O	General purpose output port
64	VSS	-	Ground
65	VDD2	-	+2.5V power supply (for internal core logic)
66	RAMD0	I+/O	Sub DSP: External memory interface Data 0
67	RAMD1	I+/O	Sub DSP: External memory interface Data 1
68	RAMD2	I+/O	Sub DSP: External memory interface Data 2
69	RAMD3	I+/O	Sub DSP: External memory interface Data 3
70	RAMD4	I+/O	Sub DSP: External memory interface Data 4
71	RAMD5	I+/O	Sub DSP: External memory interface Data 5
72	RAMD6	I+/O	Sub DSP: External memory interface Data 6
73	RAMD7	I+/O	Sub DSP: External memory interface Data 7
74	VSS	-	Ground
75	VDD1	-	+3.3V power supply (for I/O)
76	RAMD8	I+/O	Sub DSP: External memory interface Data 8
77	RAMD9	I+/O	Sub DSP: External memory interface Data 9
78	RAMD10	I+/O	Sub DSP: External memory interface Data 10
79	RAMD11	I+/O	Sub DSP: External memory interface Data 11
80	RAMD12	I+/O	Sub DSP: External memory interface Data 12
81	RAMD13	I+/O	Sub DSP: External memory interface Data 13
82	RAMD14	I+/O	Sub DSP: External memory interface Data 14
83	RAMD15	I+/O	Sub DSP: External memory interface Data 15
84	CASN	O	Sub DSP: External DRAM interface Column address strobe output
85	RAMWEN	O	Sub DSP: External memory interface Write enable output
86	RAMOEN	O	Sub DSP: External memory interface Output enable output
87	RASN	O	Sub DSP: External DRAM interface Row address strobe output
88	VSS	-	Ground
89	VDD1	-	+3.3V power supply (for I/O)
90	RAMA8	O	Sub DSP: External memory interface Address 8
91	RAMA7	O	Sub DSP: External memory interface Address 7
92	RAMA0	O	Sub DSP: External memory interface Address 0
93	RAMA6	O	Sub DSP: External memory interface Address 6
94	RAMA1	O	Sub DSP: External memory interface Address 1
95	RAMA5	O	Sub DSP: External memory interface Address 5
96	RAMA2	O	Sub DSP: External memory interface Address 2
97	RAMA4	O	Sub DSP: External memory interface Address 4
98	RAMA3	O	Sub DSP: External memory interface Address 3
99	RAMA9	O	Sub DSP: External memory interface Address 9
100	RAMA10	O	Sub DSP: External memory interface Address 10
101	RAMA11	O	Sub DSP: External memory interface Address 11
102	VSS	-	Ground
103	VDD2	-	+2.5V power supply (for internal core logic)
104	RAMA12	O	Sub DSP: External memory interface Address 12
105	RAMA13	O	Sub DSP: External memory interface Address 13
106	RAMA14	O	Sub DSP: External memory interface Address 14
107	RAMA15	O	Sub DSP: External memory interface Address 15
108	RAMA16	O	Sub DSP: External memory interface Address 16
109	RAMA17	O	Sub DSP: External memory interface Address 17
110	OVFB/END	O	Sub DSP: Overflow / Program end detect

No.	Name	I/O	Function
111	ZEROFLG	O	Main DSP: Zero flag output
112	VSS	-	Ground
113	NONPCM	O	Main DSP: non-PCM data detect
114	DTSDATA	O	Main DSP: DTS data detect
115	AC3DATA	O	Main DSP: AC-3 data detect
116	MUTE	O	Main DSP: Auto mute detect
117	KARAOKE	O	Main DSP: AC-3 Karaoke data detect
118	VDD1	-	+3.3V power supply (for I/O)
119	SURENC	O	Main DSP: AC-3 2/0 mode Dolby Surround Encode input detect
120	CRC	O	Main DSP: AC-3 CRC error detect
121	/LOCK	O	DIR: PLL lock detect
122	DIRINT	O	DIR: interrupt output
123	/CS	Is	Microprocessor interface Chip select input
124	SO	Ot	Microprocessor interface Data output
125	SI	Is	Microprocessor interface Data input
126	SCK	Is	Microprocessor interface Clock input
127	/IC	Is	Initial clear input
128	VSS	-	Ground

I : Input pin
Is : Schmitt trigger input pin
I+ : Input pin with a pull-up resistor
O : Output pin
Ot : Tri-state output pin
A : Analog pin

■ FUNCTION DESCRIPTION

YSS932 consists of three blocks; the Main DSP block where AC-3 / Pro Logic II / DTS decoding is executed, the Sub DSP block where various sound field effects are added and the SPDIF receiver (DIR) block.

The Sub DSP is a 8 channel input / 8 channel output programmable DSP exclusively for sound field processing. It can apply such effects as simulation surround, output configuration and virtual surround. In addition, with SRAM or DRAM connected, it can produce reverberation up to 2.73 seconds delay at fs=48kHz. By using this function, it is possible to simulate various sound fields such as a hall or a church.

The SPDIF receiver (DIR) can handle the digital audio interface format input signals of the sampling frequency 32kHz through 96kHz.

Note)
If adopting some technology owned by another company is desired for use in Sub DSP block, note that a separate contract may be required between the owner of that technology and the user with respect to adoption of the technology.

■ PIN DESCRIPTION

1) DIR Block

1-1) Digital audio interface signal input

- **DDIN0-3**

  Input digital audio interface format signal (DAIF signal) into these pins. Then the signal selected by control register DDINSEL0, 1 is input to the DIR block.
  As the pull-up resistors are not built in, connect the unnecessary pins to VSS.

  Also, DDIN1, 2, 3 are served as IPORT5, 6, 7. If they are not used as DDIN input pins, they are usable as general purpose input ports.

1-2) Clock

- **DIRMCK**

  The master clock for such peripheral devices as DAC and ADC is output.
  The operation mode of DIRMCK is selected according to the lock condition of PLL in the DIR block and settings for the control register. The DIRMCK output modes are as follows.

  - When PLL in the DIR block is not locked (/LOCK=H) ----- (1)
    DIRMCK outputs 12.288MHz.
  - When PLL in the DIR block is locked (/LOCK=L) and CKMOD=1 ----- (2)
    DIRMCK outputs 12.288MHz
  - When PLL in the DIR block is locked (/LOCK=L) and CKMOD=0
    DIRMCK outputs according to the setting of LOCKMOD1-0.

LOCKMOD1	LOCKMOD0	Normal rate	Double rate
0	0	256fs	256fs
0	1	256fs	128fs
1	*	256fs	12.288MHz -(3)

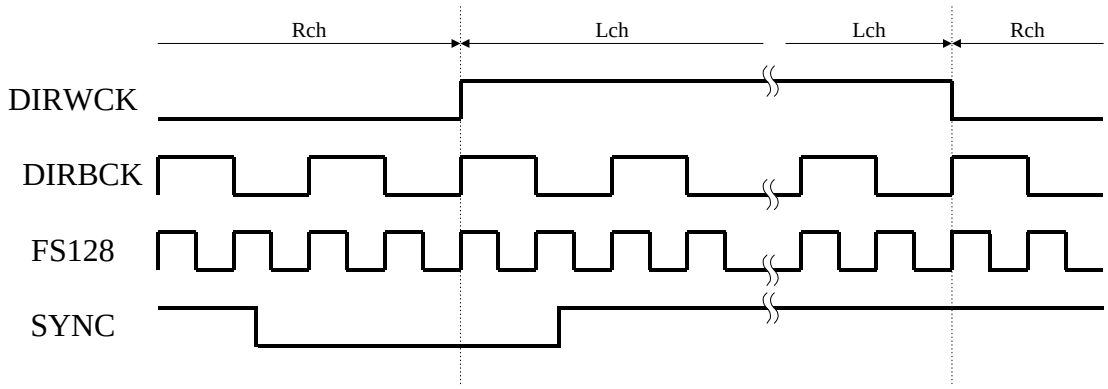
The mode like the above (1), (2) and (3) in which the XI's divided clock of 12.288 MHz is output from DIRMCK is referred to as "free-run mode".

● **DIRBCK, DIRWCK, FS128, SYNC**

The clock for such peripheral devices as DAC and ADC is output.
At CMOD=0 setting, FS128 is output from FS128/C pin and at UMOD=0 setting, SYNC is output from SYNC/U pin.
DIRBCK, DIRWCK and FS128 are obtained by dividing the clock of DIRMCK and the period of each clock is as follows.

DIRBCK	→	64fs
DIRWCK	→	fs
FS128	→	128fs

SYNC is output according to the following timing.
Note) At settings of DIROWP=0, DIROBP=0



1-3) Serial data output

● **DIRSDO**

The DAIF signal data is output. The output is always 24-bit width including audio auxiliary bit. The data is output from the DIRSDO pin as well as goes into the Main DSP block through the SDIA interface.

It must be noted that the data output from the DIRSDO pin is muted during the free-run mode or at SDOMUTE=1 setting, but the data output to the Main DSP is muted only during the free-run mode regardless of SDOMUTE setting.

The output format can be selected by setting the DIR SDO register. For the details of the format, refer to "Serial Data Interface Format".

1-4) Status data output

● **BS, V, U, C**

The data of block start, validity flag, user data and channel status obtained from the DAIF signals are output as described below.

The block start is output from the ERR/BS pin at BSMOD=1 setting.
The validity flag is output from the DBL/V pin at VMOD=1 setting.
The user data is output from the SYNC/U pin at UMOD=1 setting.
The channel status is output from the FS128/C pin at CMOD=1 setting.

BS, V, U, C are fixed to the "L" level during the free-run mode or at VUCMUTE=1 setting.

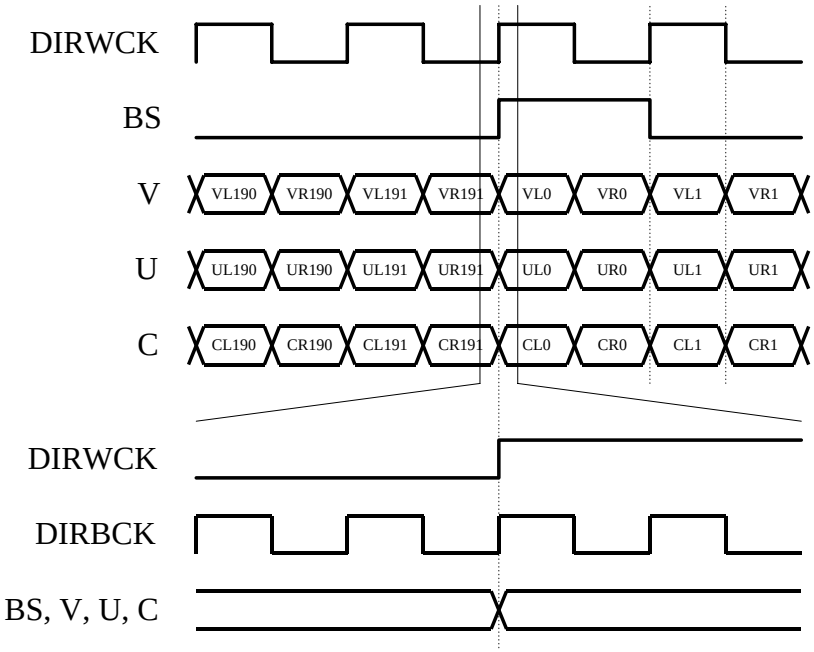
BS, V, U and C are output according to the format shown below.

Alphabet clusters in the figure represent:

VLn --- Validity flag of L-ch frame n VRn --- Validity flag of R-ch frame n
ULn --- User data of L-ch frame n URn --- User data of R-ch frame n
CLn --- Channel status of L-ch frame n CRn --- Channel status of R-ch frame n

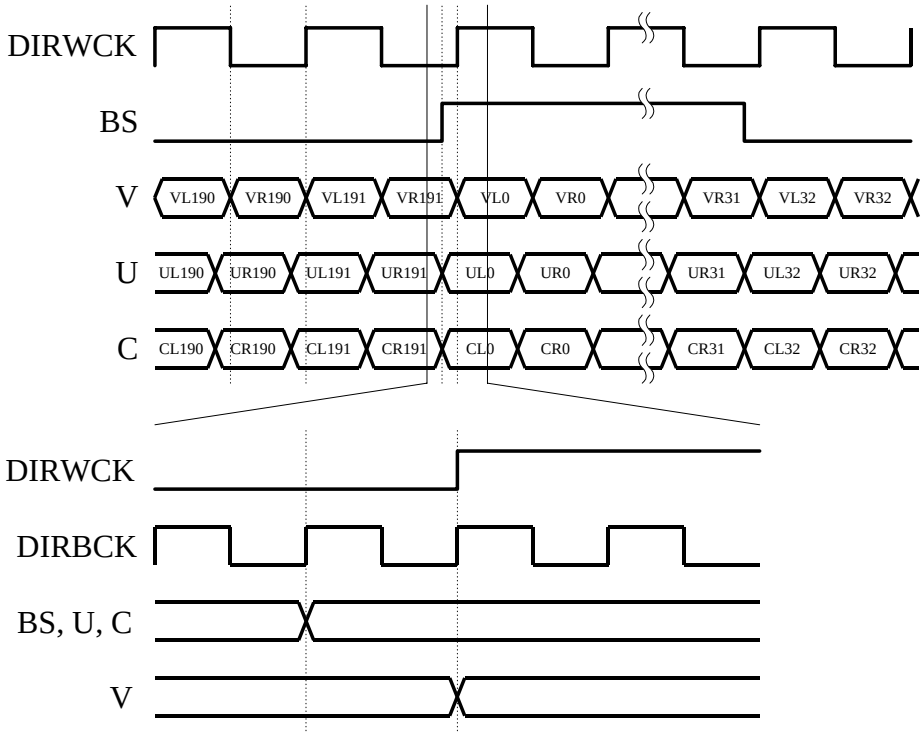
When in mode 0 (CTIMMOD=0)

Note) at settings of DIROWP=0, DIROBP=0



When in mode 1 (CTIMMOD=1)

Note) at settings of DIROWP=0, DIROBP=0



- **/LOCK, ERR, DIRINT**

  The same data as LOCKN, DIRERR, DIRINT of DIR STATUS Register are output from /LOCK, ERR/BS, DIRINT pins respectively.
  The DIRERR data is output from ERR/BS pin at BSMOD=0 setting.

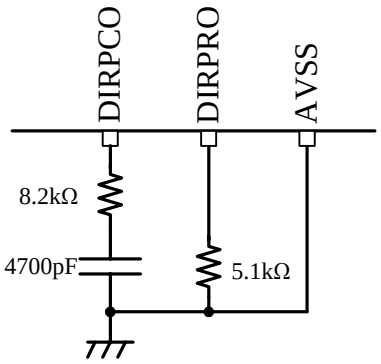
- **DBL**

  The information, whether the DDIN input signal is a double rate signal, is output from the DBL/V pin at VMOD=0 setting.
  If PLL in the DIR block is locked at double rate and the free-run mode is not used, "H" level is output.
  If PLL in the DIR block is locked at normal rate or the free-run mode is used, "L" level is output.

1-5) Analog circuit for PLL in DIR block

- **DIRPCO, DIRPRO**

  These are capacitor and resistor connection pins for PLL in DIR block. As shown below, connect a 4700pF capacitor and an 8.2kΩ resistor between DIRPCO and AVSS as close as physically possible to DIRPCO and a 5.1kΩ resistor between DIRPRO and AVSS as close as physically possible to DIRPRO.



2) Main DSP Block

2-1) Serial data input / output

- **SDIA**

  This is used to input PCM or bitstream into the Main DSP block. Normally, the PCM output of the external ADC is input.
  The input format can be selected by setting the SDIA register.
  For the format, refer to "Serial Data Interface Format".
  The SDIA pin input or DIRSDO output of the DIR block is selected by SDIASEL, and processed in the Main DSP block.

- **SDOA0-2**

  The PCM signal processed in the Main DSP block is output to these pins.
  L-ch, R-ch signals are output from SDOA0 pin, LS-ch, RS-ch signals from SDOA1 pin and C-ch, LFE-ch signals from SDOA2 pin.
  At the same time the signals are output from these pins, they are input to the Sub DSP block through the SDIB interface.
  The output format can be selected by setting the SDOA register.
  For the format, refer to "Serial Data Interface Format".

- **SDBCKI0, SDWCKI0, SDBCKI1, SDWCKI1**

  These are input clocks for the serial data. When the serial data is synchronized not to DIRBCK, DIRWCK from DIR included in this LSI but to the clocks from the outside, supply clocks to these pins.
  The clocks for the SDIA / SDOA interface will be DIRBCK / DIRWCK or SDBCKI0 / SDWCKI0 selected at SDIACKSEL.
  The clocks for the SDIB / SDOB interfaces will be the same clocks for the SDIA interface
  (DIRBCK / DIRWCK or SDBCKI0 / SDWCKI0 selected at SDIACKSEL)
  or
  SDBCKI1 / SDWCKI1
  (Refer to "Block Diagram".)
  When not using the external clock, keep these pins unconnected.

- **/SDBCKO**

  A reverse clock of DIRBCK or SDBCKI0 selected at SDIACKSEL is output. This clock can be utilized when the polarity of the clock for the peripheral devices such as ADC and DAC differs.
  Refer to "Block Diagram".

2-2) Status output

- **DTSDATA, AC3DATA, SURENC, KARAOKE, MUTE, CRC, NONPCM**

  These pins output the status data of the signals processed in the Main DSP block.
  The status, which is the same as the contents of the STATUS Register, is output from respective pins.

- **ZEROFLG**

  This pin indicates how long the input signal (SDIA or DIRSDO) for the Main DSP block is kept in the digital zero state. The same status as ZEROFLG of the ZERO Register is output.

3) Sub DSP Block

3-1) Serial data input / output

- **SDIB0-3**

  These are PCM input pins to the Sub DSP block.
  The data input to SDIB0-2 pins or the SDOA0-2 output from the Main DSP block are selected at SDIBSEL and processed in the Sub DSP block. The input data to the SDIB3 pin is always processed in the Sub DSP block regardless of SDIBSEL.
  Refer to "Block Diagram".

  The input format can be selected by setting the SDIB register.
  For the format, refer to "Serial Data Interface Format".

- **SDOB0-3**

  These are the output pins for the PCM signals processed in the Sub DSP block.
  The output format can be selected by setting the SDOB register.
  For the format, refer to "Serial Data Interface Format".

3-2) External memory interface

- **RAMA0-17, RAMD0-15, RAMWEN, RAMOEN, CASN, RASN**

  These pins are used to connect an external memory to the Sub DSP block for the data delay.

3-3) Status output

- **OVFB/END**

  The output varies depending on OVFSEL settings of ERAM register bit 7.
  This output is used when programming Sub DSP.

  OVFB at OVFSEL=0

  This pin becomes "H" level when a digital overflow occurs as a result of operation in the Sub DSP block. "H" level is kept from the moment an overflow occurs to the moment the next PCM sample is output from the SDOB interface. When the next PCM sample output starts, the pin is reset to "L" level.

  END at OVFSEL=1

  This pin becomes "H" level while the program counter of Sub DSP is operating, and "L" level when all the processing is completed and the program counter stops. While operating correctly, it becomes "L" level once during one sample time. If it fails to become "L" level even once during one sample time, it means that the program has not been completed correctly and fully.

4) Microprocessor Interface

- **/CS, SCK, SI, SO**

  The control registers are read / written via the four-wire serial microprocessor interface.
  For the interface format, refer to "Microprocessor Interface Format".

- **IPORT0-4, DDIN1-3**

  The signals input to these pins can be read via the IPORT register.
  By connecting the status output of other devices to these pins, it is possible to read the data of other devices via the microprocessor interface of this device. It should be noted that DDIN1-3 are also used as input signal pins of DIR block.
  IPORT0-4 pins may be left open when unused as pull-up resistors are built-in, but be sure to connect the unused DDIN1-3 pins to VSS as no pull-up resistors are built-in.

- **OPORT0-7**

  The data written in the OPORT register are output from these pins.
  By connecting the mode selection of other devices to these pins, the other device can be controlled via the microprocessor interface of this device.

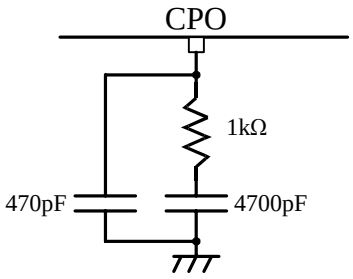
5) Clock

- **XI, XO**

  These are crystal oscillator (24.576MHz) connection pins. Use a crystal oscillator of fundamental mode.
  Use XI when inputting the external clock.

- **CPO**

  This is to connect external parts for PLL generating the operation clock of the DSP block. Connect a resistor and capacitors between CPO and AVSS as close as physically possible to CPO.



■ Control Register / Register Map

The decoding system is controlled by reading and writing the control registers as shown below through microprocessor interfaces (/CS, SCK, SI, SO).

All control registers are reset to "0" by initial clear (/IC=L).

Address	Name	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
0x00	AUTO/DSN	AUTOMOD				DSNIGN	DSN2-0		
0x01	MUTE	LMUTEN	CMUTEN	RMUTEN	RSMUTEN	LSMUTEN	LFEMUTEN	DSPMUTEN	AMOFF
0x02	SDIA	SDIACKSEL	SDIASEL	SDIAFMT1-0		SDIABIT1-0		SDIAWP	SDIABP
0x03	SDOA			SDOAFMT1-0		SDOABIT1-0		SDOAWP	SDOABP
0x04	OPORT	OPORT7-0							
0x05	IPORT	IPORT7-0							
0x06	(TEST)								
0x07	(TEST)								
0x08	PCM	PLDECMOD1-0		PCMDLY	LROUT				
0x09	NOISE LEVEL	NOISELEV7-0							
0x0A	CENTER DELAY						CDELAY2-0		
0x0B	SURROUND DELAY					SRDELAY3-0			
0x0C	NOISE	NOISE	PN/WN	IMPULSE	DIMCFG2-0				
0x0D	FS	CWCFG2-0			SRFIL1-0		FS2-0		
0x0E	L VOLUME	LVOL7-0							
0x0F	C VOLUME	CVOL7-0							
0x10	R VOLUME	RVOL7-0							
0x11	LS VOLUME	LSVOL7-0							
0x12	RS VOLUME	RSVOL7-0							
0x13	LFE VOLUME	LFEVOL7-0							
0x14	COMPRESSION	EMPON	AIBON	VOLON	DITHOFF	P11OFF	DIALOFF	COMPMOD1-0	
0x15	HDYNRNG	HDYNRNG7-0							
0x16	LDYNRNG	LDYNRNG7-0							
0x17	MODE	PCMMOD	PLDECON	RSINV	DUALMOD1-0		OUTMOD2-0		
0x18 | 0x2A	BITSTREAM	(described in the later section)							
0x2B	(Unused)	(Undefined)							
0x2C	(Unused)	(Undefined)							
0x2D	Pc	Pc7-0							
0x2E	DATA STREAM	STREAM7	STREAM6	STREAM5	STREAM4	STREAM3	STREAM2	STREAM1	STREAM0
0x2F	STATUS	DTSDATA	AC3DATA	2/0MODE	SURENC	KARAOKE	MUTE	CRC	NONPCM
0x30	ZERO	ZEROFLG	ZERO6-0						
0x31	(TEST)								
0x32	MPCNT_H	MPLOAD	MPCLEARN			MPCNT11-8			
0x33	MPCNT_L	MPCNT7-0							
0x34	SDIB	SDIBCKSEL	SDIBSEL	SDIBFMT1-0		SDIBBIT1-0		SDIBWP	SDIBBP
0x35	SDOB	SDOBCKSEL		SDOBFMT1-0		SDOBBIT1-0		SDOBWP	SDOBBP
0x36	ERAM	OVFSEL	JMPSEL			RASREF	ERAMMOD	ERAMSEL1-0	
0x37	(TEST)								

0x38	MI0	MI0REG7-0							
0x39	MI1	MI1REG7-0							
0x3A	MI2	MI2REG7-0							
0x3B	MI3	MI3REG7-0							
0x3C	MI4	MI4REG7-0							
0x3D	MI5	MI5REG7-0							
0x3E	MI6	MI6REG7-0							
0x3F	MI7	MI7REG7-0							
0x40	DIR CTRL	CKMOD	VUCMUTE	SDOMUTE				DDINSEL1-0	
0x41	DIR SDO	LOCKMOD1-0		DIROFMT1-0		DIROBIT1-0		DIROWP	DIROBP
0x42	DIR PIN	BSMOD	VMOD	UMOD	CMOD				CTIMMOD
0x43	DIR INTMOD		INTMOD6-1						
0x44	(TEST)								
0x45	DIR CUADR	DHLD	R/L	U/C	CUADR4-0				
0x46	DIR CUDAT	CUDAT7-0							
0x47	DIR STATUS	DIRINT	DIRERR	LOCKN	VFLAG	CSB1	CSCHG	BSFLAG	(Undefined)
0x48	DIR FS					CSB3	DIRFS2-0		
0x49 | 0x57	(TEST)								
0x58 | 0x7F	Invalid	The output at the SO pin becomes High-Z.							

Never write "1" into the shaded bits because the bits for testing are assigned there.

Never make an access to addresses 0x06, 0x07, 0x31, 0x37, 0x44, 0x49 to 0x57 because the registers for testing are assigned there.

The contents of the bitstream register (addresses 0x18 to 0x2A) vary depending on the input signal, i.e., the Main DSP input signal is AC-3 bitstream, DTS bitstream or PCM as shown below.

Only reading is allowed with the BITSTREAM register and not writing.

1) When the input signal is **AC-3 bitstream**

Address	Name	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
0x18	BITSTREAM 0	fscod		frmsizecod					
0x19	BITSTREAM 1	bsid					bsmod		
0x1A	BITSTREAM 2	acmod			cmixlev		surmixlev		lfeon
0x1B	BITSTREAM 3	dsurmod		copyrightb	origbs	0	0	0	0
0x1C	BITSTREAM 4	0	0	0	dialnorm				
0x1D	BITSTREAM 5	0	0	0	dialnorm2				
0x1E	BITSTREAM 6	audprodie	mixlevel					roomtyp	
0x1F	BITSTREAM 7	audprodi2e	mixlevel2					roomtyp2	
0x20	BITSTREAM 8 (when bsid=6)	timecod1e (xbsi1e)	0 (0)	timecod1 (dmixmod)		(ltrtcmixlev)			(ltrtsurmixlev)
0x21	BITSTREAM 9 (when bsid=6)	timecod1 (ltrtsurmixlev)		(lorocmixlev)			(lorosurmixlev)		
0x22	BITSTREAM 10 (when bsid=6)	timecod2e (xbsi2e)	0 (0)	timecod2 (dsurexmod)		(dheadphonmod)		(adconvtyp)	(xbsi2)
0x23	BITSTREAM 11 (when bsid=6)	timecod2 (xbsi2)							(encinfo)
0x24	BITSTREAM 12	langcode	langcod2e	compre	compr2e	0	0	0	0
0x25	BITSTREAM 13	langcod							
0x26	BITSTREAM 14	langcod2							
0x27	BITSTREAM 15	compr							
0x28	BITSTREAM 16	compr2							
0x29	BITSTREAM 17	dynrng							
0x2A	BITSTREAM 18	dynrng2							

2) When the input signal is **DTS bitstream**

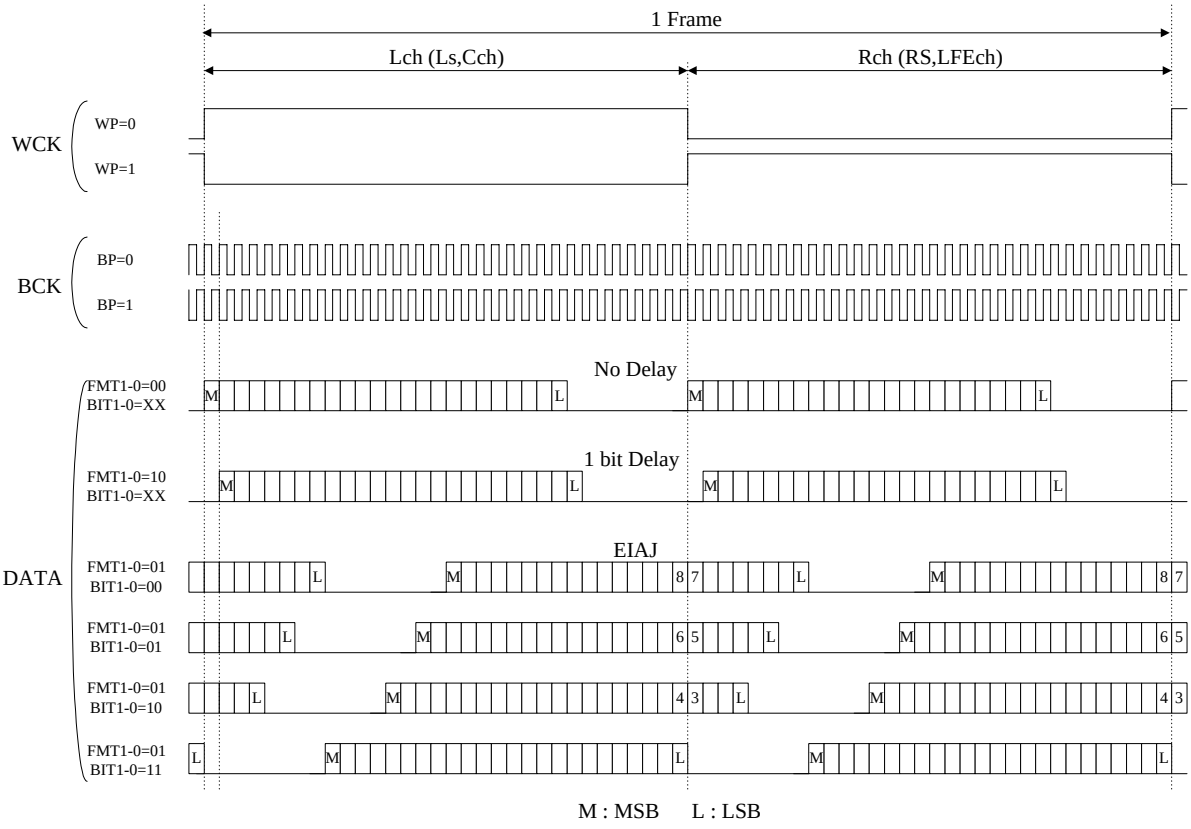
Address	Name	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
0x18	BITSTREAM 0	fscod		(Undefined)	RATE				
0x19	BITSTREAM 1	(Undefined)			HDCD	EXT_AUDIO_ID			EXT_AUDIO
0x1A	BITSTREAM 2	AMODE						(Undefined)	lfeon
0x1B	BITSTREAM 3	(Undefined)					PCMR		
0x1C | 0x23	BITSTREAM 4 | BITSTREAM 11	(Undefined)							
0x24	BITSTREAM 12	(Undefined)		DYNF	(Undefined)				
0x25	BITSTREAM 13	(Undefined)							
0x26	BITSTREAM 14	(Undefined)							
0x27	BITSTREAM 15	RANGE							
0x28	BITSTREAM 16	(Undefined)							
0x29	BITSTREAM 17	(Undefined)							
0x2A	BITSTREAM 18	(Undefined)							

3) When the input signal is **PCM**

The contents of BITSTREAM register (addresses 0x18 to 0x2A) are all undefined.

■ Serial Data Interface Format

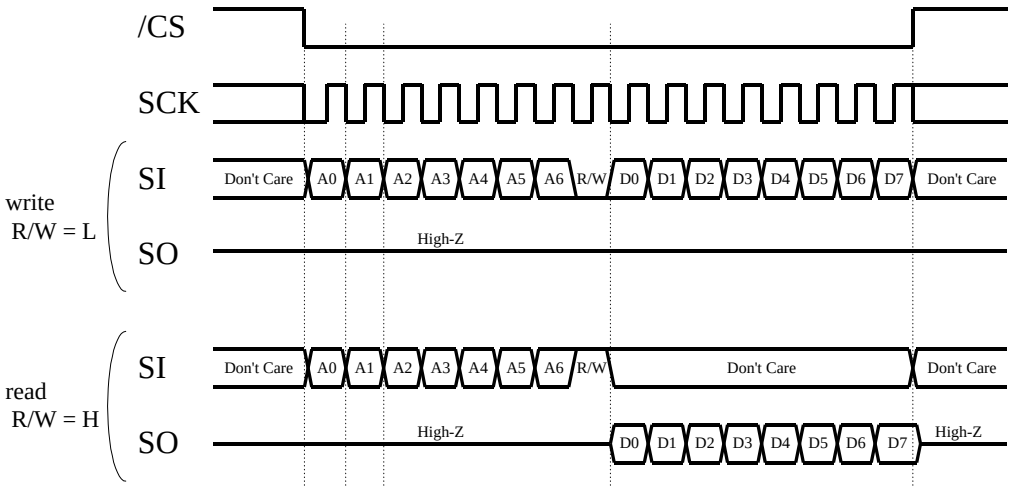
Shown below are interface formats obtained by setting SDIA Register, SDOA Register, SDIB Register, SDOB Register and DIR SDO Register.



M : MSB L : LSB

■ Microprocessor Interface Format

A four-wire serial interface is used to read and write the control registers.



SO becomes an output pin only when all of the following conditions are met.

- /CS=L
- When reading the valid addresses
- Timing of 8 bits data output

If any of the above conditions is not met, SO outputs High-Z. Thus SO, SI and SCK can be used jointly with other devices that have similar interfaces.

[CAUTION]

Set /CS=H during /IC=L.

■ ELECTRICAL CHARACTERISTICS

1. Absolute Maximum Ratings

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Power Supply Voltage	$V_{DD}1$		Vss-0.5		4.6	V
	AV_{DD}		Vss-0.5		4.6	V
	$V_{DD}2$		Vss-0.5		3.6	V
Input Voltage	VI	except XI pin *1	-0.5		5.75	V
		XI pin	-0.5		$V_{DD}1$+0.5	V
Storage Temperature	Tstg		-50		125	°C

*1: 5V tolerant input terminal is used.

2. Recommended Operating Conditions

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Power Supply Voltage	$V_{DD}1$		3.0	3.3	3.6	V
	AV_{DD}		3.0	3.3	3.6	V
	$V_{DD}2$		2.3	2.5	2.7	V
Operating Temperature	Top		0	25	70	°C

2. DC Characteristics

Conditions: Under recommended operating conditions

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Input Voltage "H" level 1	$V_{IH}1$	*1	0.7$V_{DD}1$			V
Input Voltage "L" level 1	$V_{IL}1$	*1			0.3$V_{DD}1$	V
Input Voltage "H" level 2	$V_{IH}2$	*2	2.4			V
Input Voltage "L" level 2	$V_{IL}2$	*2			0.8	V
Input Voltage "H" level 3	$V_{IH}3$	*3	2.2			V
Input Voltage "L" level 3	$V_{IL}3$	*3			0.8	V
Output Voltage "H" level	V_{OH}	I_{OH} = -80 µA	$V_{DD}1$-0.4			V
Output Voltage "L" level	V_{OL}	I_{OL} = 1.0 mA			0.4	V
Input Leakage Current	I_{LI}	no pull-up resistor pin	-10		10	µA
Pull-up Resistor	R_U		40		160	kΩ
Power Consumption	P_D1	$V_{DD}1$		60	120	mW
	P_D2	$V_{DD}2$		220	260	mW

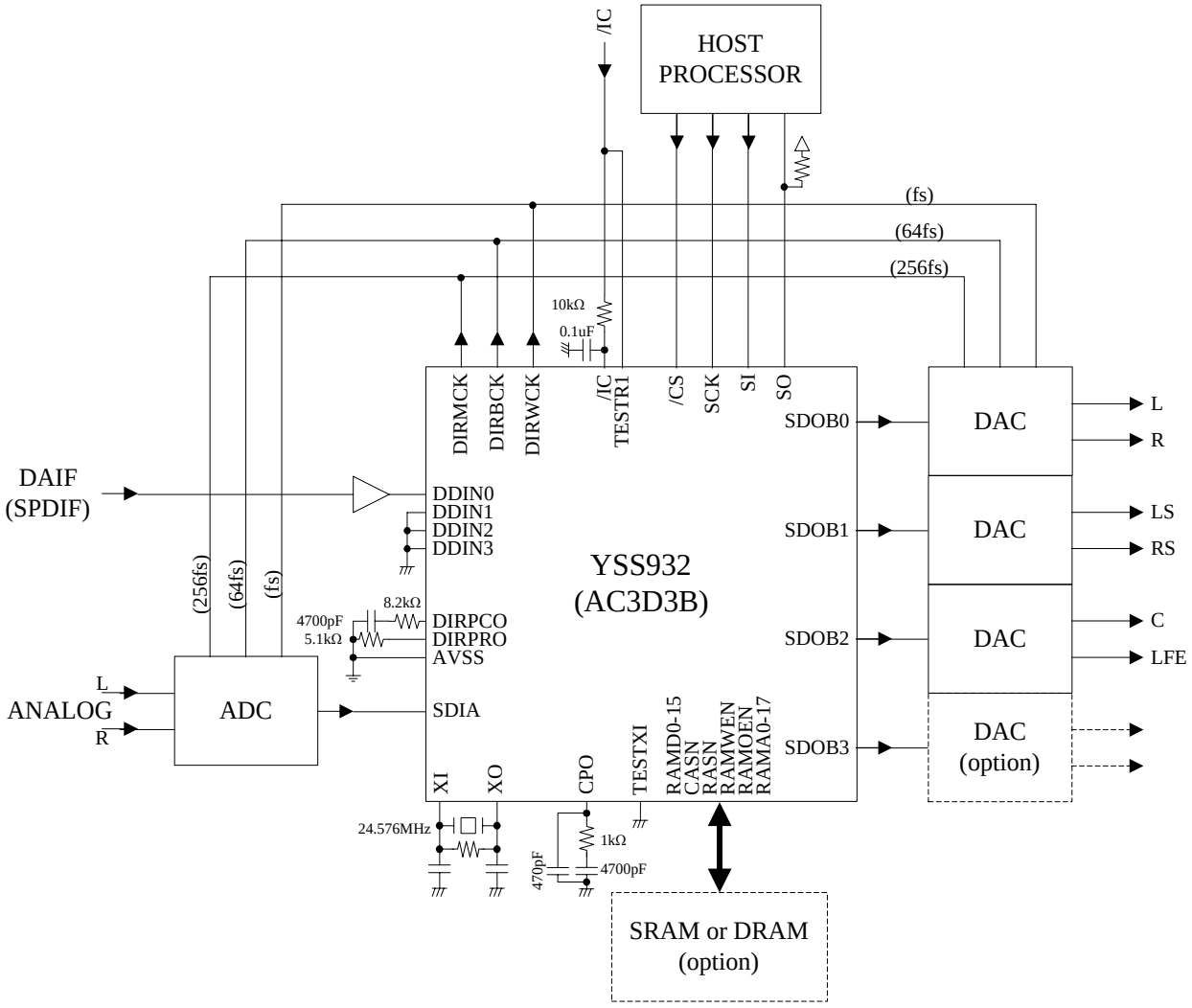
*1: Applicable to XI pin.

*2: Applicable to /IC and DDIN0-3 pins.

*3: Applicable to input pins except the above pins.

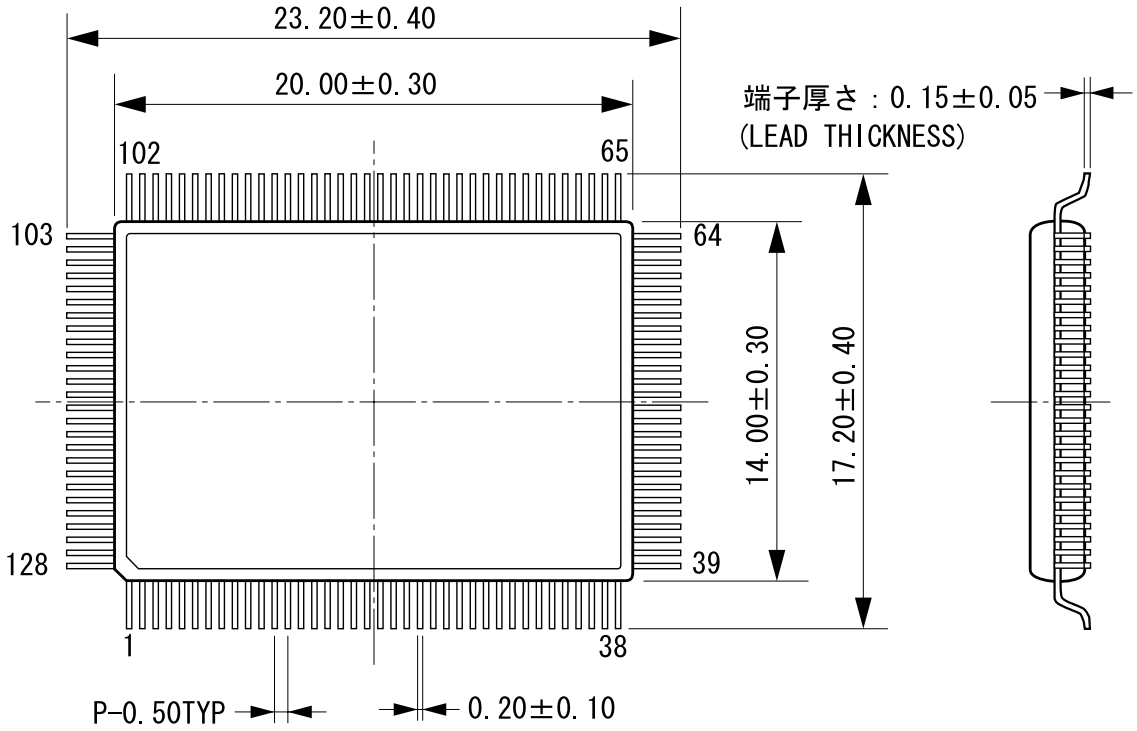
■ SYSTEM CONNECTION DIAGRAM

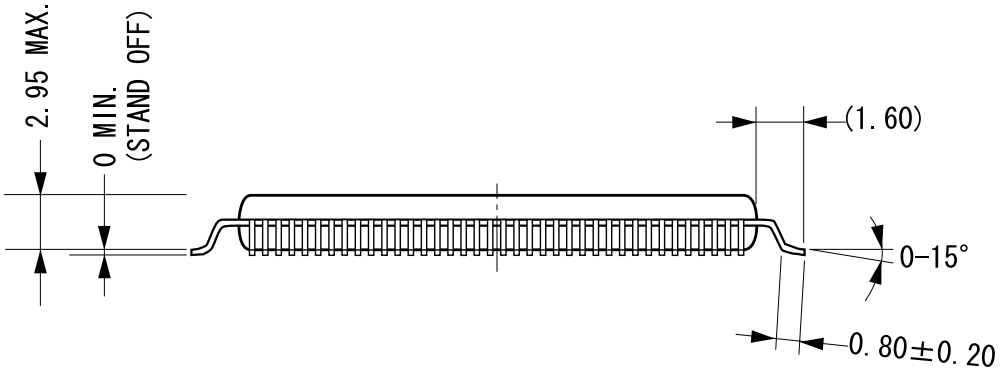
Shown below is an example of basic connection of YSS932 (AC3D3B) and the peripheral circuits.



■ EXTERNAL DIMENSIONS

C-PK128SP-1





モールドコーナー形状は、この図面と若干異なるタイプのものもあります。
カッコ内の寸法値は参考値とする。
モールド外形寸法はバリを含まない。
単位(UNIT) : mm (millimeters)

The shape of the molded corner may slightly different from the shape in this diagram.
The figure in the parenthesis ( ) should be used as a reference.
Plastic body dimensions do not include burr of resin.
UNIT: mm

注) 表面実装LSIは保管条件及び、半田付けについての特別な配慮が必要です。
詳しくはヤマハ代理店までお問い合わせ下さい。
Note: The LSIs for surface mount need special consideration on storage and soldering conditions.
For detailed information, Please contact your nearest Yamaha agent.

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