

YAMAHA LSI

YM3012

2-Channel Serial Input Floating D/A Converter (DAC-MS)

■ OUTLINE

YM3012: DAC-MS (hereinafter referred to as DAC) is a floating D/A converter with serial input for two channels. It can generate analog output (dynamic range 16 bits) of 10-bit mantissa section and 3-bit exponent section on the basis of input digital signal.

■ FEATURES

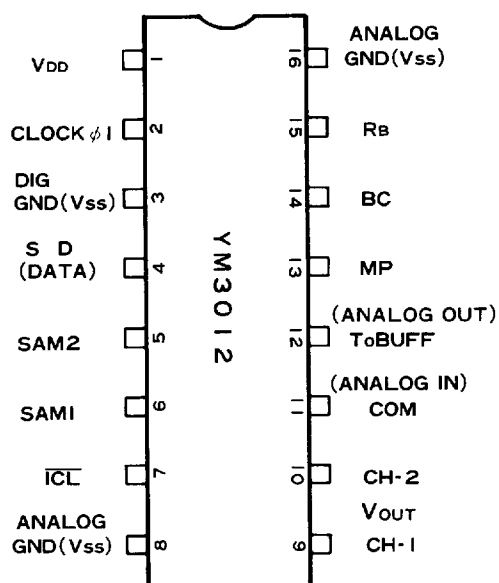
- An external buffer operational amplifier is provided to obtain analog output easily.
- A wide dynamic range with 16 bits.
- Compatible with PCM audio sources of up to 2 channels
- Built-in sample hold analog switches
- It is possible to obtain low noise, low harmonic distortion and good temperature characteristics.
- Monolithic chip with high precision thin film resistor and CMOS and contained in a 16 pin plastic DIL package.

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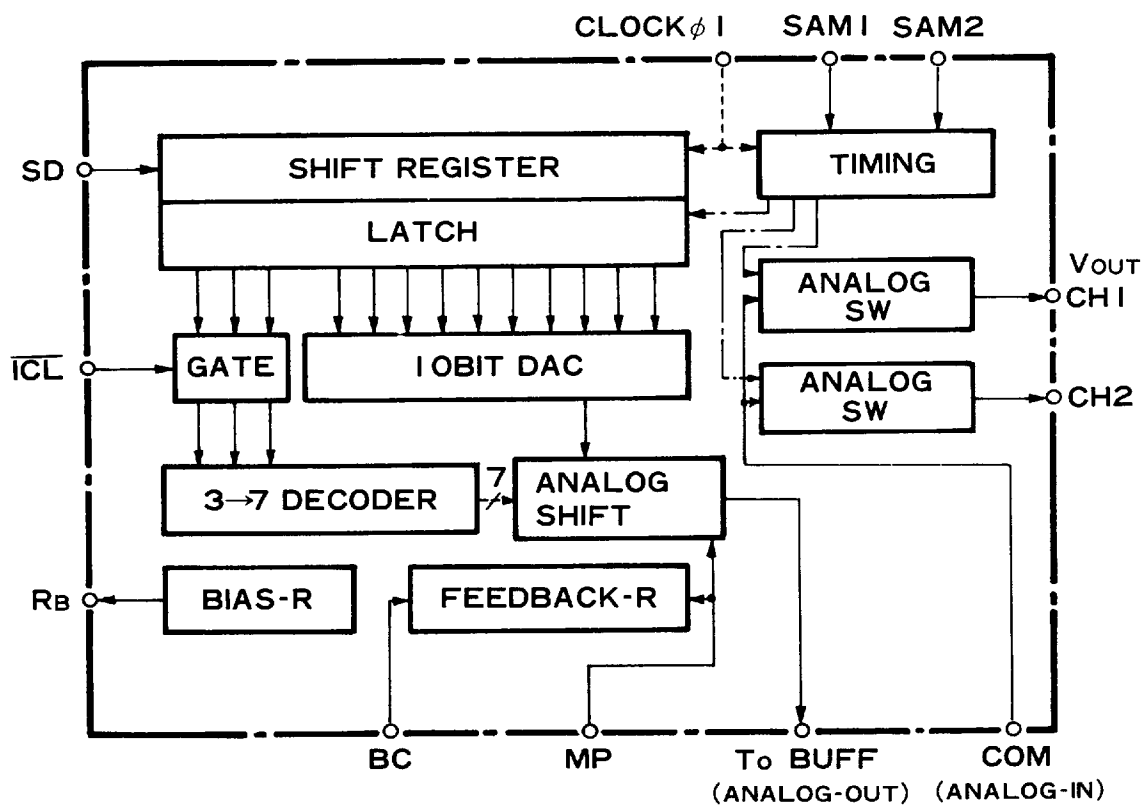
YM3012 CATALOG
CATALOG No.: LSI-2130123
1992. 4



■ PIN DIAGRAM



■ BLOCK DIAGRAM



■ PIN DISIGNATION

Pin No.	Symbol	Function
1	VDD	Reference power source on high potential side
2	CLOCK	Clock (ϕ 1) for operation of shift register and timing generator
3	DIG-Vss	Digital section power source on low potential side (GND)
4	SD	Serial input of converted digital signal
5	SAM2	"1" section becomes CH2 sampling period
6	SAM1	"1" section becomes CH1 sampling period, Trailing edge of SAM1 and SAM2 are used to generate internal signal for latching serial data
7	ICL	"1" -normal operation; "0" - analog output becomes equal ($S_2 = S_1 = 0, S_0 = 1$), regardless of SD signal
8	ANALOG Vss	Analog section power source on low potential side (GND)
9	Vout CH1	CH1 sample hold analog switch output
10	Vout CH2	CH2 sample hold analog switch output
11	COM	Analog switch common input for CH1 and CH2
12	To BUFF	Analog output from DAC, input to buffer operational amplifier
13	MP	Normally biased to $1/2 V_{DD}$, exponential analog output obtained on the base of MP potential by S signal
14	BC	Resistance eliminating error due to buffer operational amplifier input bias current, present between this pin and 13 pin. It is recommended to externally connect a CC capacitor for phase compensation
15	RB	High precision $1/2 V_{DD}$ voltage generated internally, outputs from this pin. Applied to 8 pin through buffer operational amplifier
16	ANALOG Vss	Low potential side power source (GND) for generating $1/2 V_{DD}$ voltage of 15 pin

■ DESCRIPTION OF FUNCTIONS

1. Relationship between Digital Input Data and Analog Output Voltage

To perform one conversion at 16-bit time by YM3012, the first 3-bit data in the 16-bit serial data is treated as invalid data in the DAC. The next 10 bit data (D₀ through D₉) is input into the 10-bit DAC section as the data of MSB to LSB to constitute the manissa section of analog output. The remaining 3-bit data (S₀ through S₂) is input into the 2^{-N} analog shift section to constitute the exponent section of analog output. For example, when the basic circuit is used, output voltage is as follows.

$$V_{OUT} = 1/2 V_{DD} + 1/4 V_{DD} (-1 + D_9 + D_8 2^{-1} + \dots + D_0 2^{-9} + 2^{-10}) 2^{-N}$$

$$N = \bar{S}_2 2^2 + \bar{S}_1 2^1 + \bar{S}_0$$

$S_2 = S_1 = S_0 = 0$: not allowed.

That is, it has the maximum amplitude of $1/2 V_{DD}$ and the minimum amplitude of $1/2 V_{DD} 2^{-16}$ with $1/2 V_{DD}$ potential as a center.

2. Operation in the DAC

Digital input data is taken into the shift register through the SD pin, synchronized with the clock rise. The latch signal is generated in the timing circuit using the trailing edge of SAM1 and SAM2. By this latch signal, the D₀ through D₉ and S₀ through S₂ serial data is latched, driving the 10-bit DAC section and the analog shift section, respectively, to start conversion. The analog output is output from the “To BUFF” pin. When this analog output is input to the COM pin through the proper buffer operational amplifier and resistor, it is output from the CH1 and CH2 pins for the period during which SAM1 and SAM2 are “1”. When SAM1 and SAM2 are “0”, the analog output for each channel is held in a proper electrostatic capacity.

3. Summary of Operation

- As shown in Fig. 3, make the trailing edge timing of SAM1 and SAM2 coincide with the S₂ rear end timing of SD signal.
- The SAM1 and SAM2 sampling period can also be set to be other timing than 8-bit shown in Fig.3.
- When using channel 1 only, set SAM2 to VSS, and make the S₂ rear end timing of SD coincide with the SAM1 trailing edge timing.
- Conversion cycles with a different bit timing are possible by increasing or decreasing the invalid bit data.

4. Initial Clear Function

When ICL is made "0", $S_2 = S_1 = 0$ and $S_0 = 1$, that is, the mantissa does not change, and output with the exponential section reduced to 2^{-6} is output from each channel output regardless of the digital input data value.

2. Recommended Operation Conditions

ITEM	SYMBOL	MIN.	TYP.	MAX.	UNIT
Supply voltage	V _{DD}	+4.75	5.0	10.0	V
	V _{SS}	0	0	0	V
Input signal voltage	CLOCK SD SAM1,2 ICL	0	—	V _{DD}	V
Ambient operation temperature	T _a	0	—	70	°C

3. D.C. Characteristics

ITEM	SYMBOL	MEASUREMENT CONDITIONS	MIN.	TYP.	MAX.	UNIT
High level input voltage	V _{IH}	V _{DD} = 5.0V	3.3	—	—	V
Low level input voltage	V _{IL}	V _{DD} = 5.0V	—	—	1.0	V
Input current	I _{IN}	V _{DD} = 10.0V	—	—	10 ⁻³	μA
Power current	I _{DD}	V _{DD} = 5.0V	—	—	6	mA

4. AC Characteristics

ITEM	SYMBOL	CONDITIONS	MIN.	TYP.	MAX.	UNIT
• Clock Frequency	f _c		0.65	1.6	3.2	MHz
High level time	t _H		100			ns
Rise time	t _r				50	ns
Fall time	t _f				50	ns
• Data Set-up time	t _{DS}	SD SAM1	100			ns
Rise time	t _r	SAM2			50	ns
Fall time	t _f				50	ns

5. Capacity

ITEM	SYMBOL	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Input capacity	C _{IN}		—	—	5	pF



6. DAC Characteristics

ITEM	SYMBOL	CONDITIONS	MIN.	STD.	MAX.	UNIT
Max.out put amplitude	VOA			1/2VDD		V
Resolution				16		Bit
Settling time	t_s			2.5	5.0	μs
Total harmonic distortion	THD1	VDD = 5V, 110Hz		0.05	0.10	%
(Analysis mode)	THD6	level 0 dB -36 dB			0.15	%
Noise				-92	-80	dBm
Crosstalk				-72		dB
Temperature characteristics		Output voltage Total harmonic distortion		5		ppm/°C

7. Timing Diagram

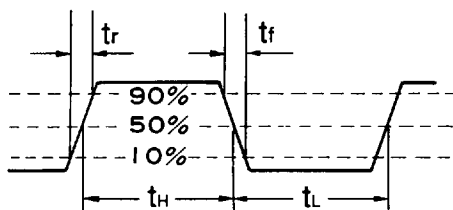


Fig. 1 Data timing

SD, SAM1, SAM2

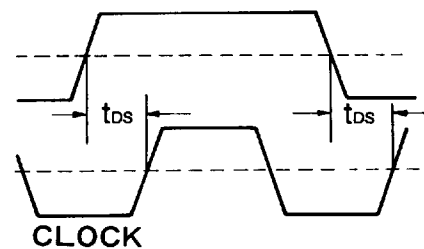


Fig. 2 Input data-clock timing

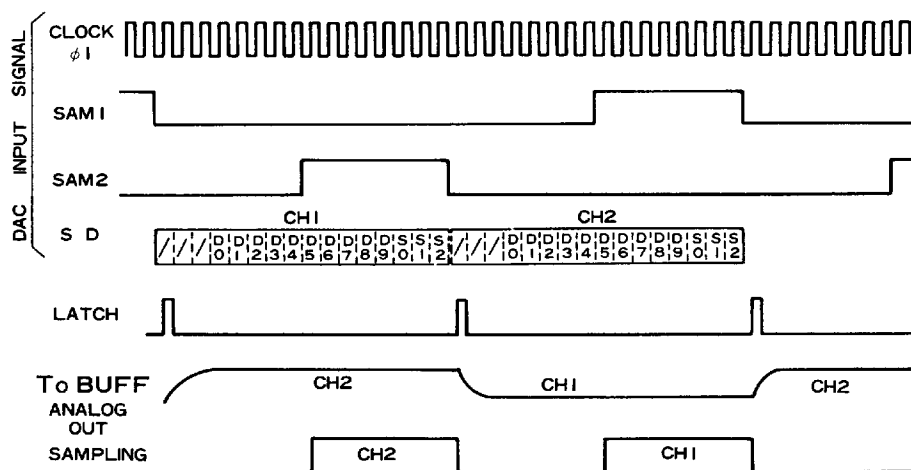
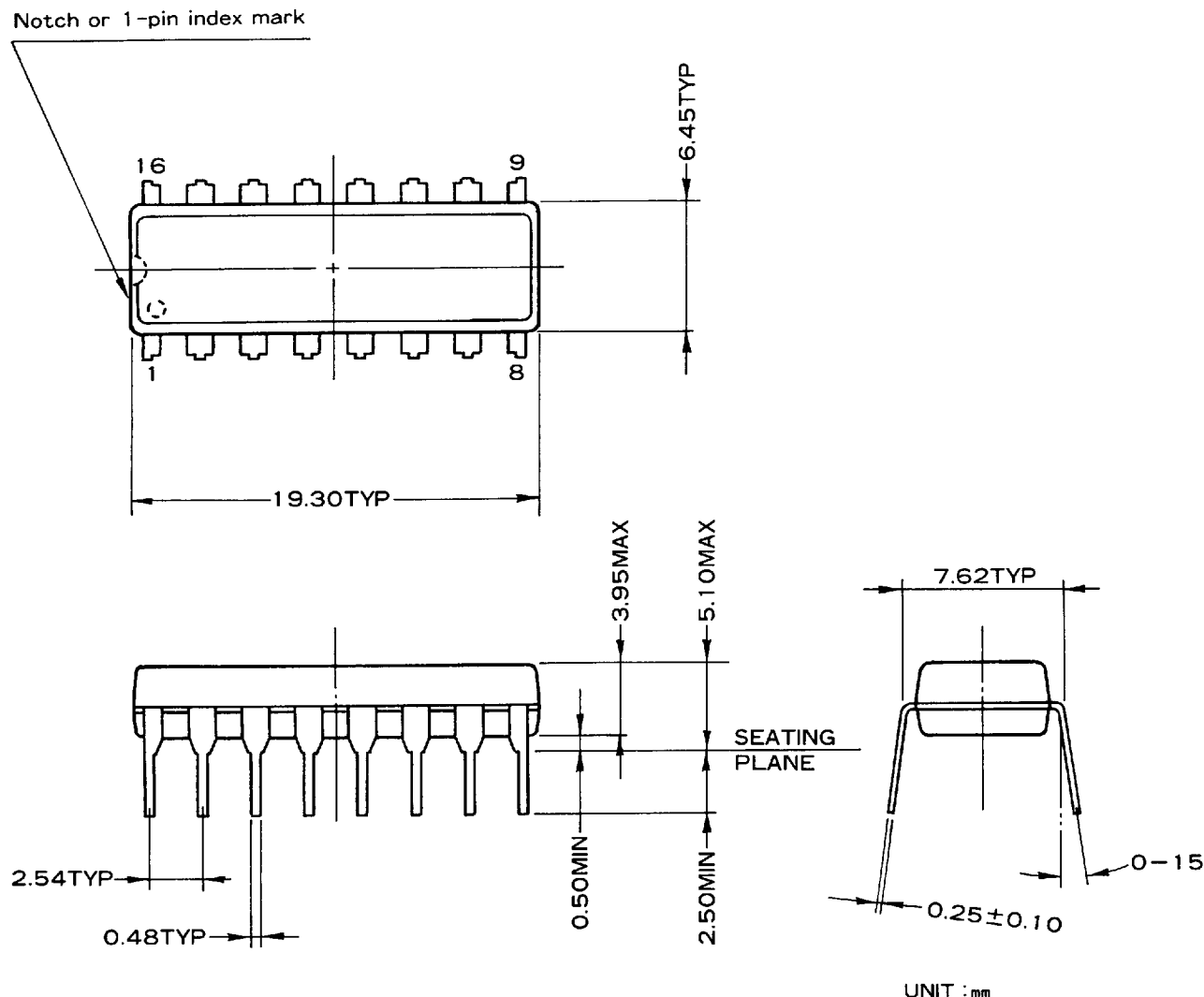


Fig. 3 TIMING

■ OUTLINE DIMENSIONS



The specifications of this product are subject to improvement changes without prior notice.

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