IC Plus Corp.
九暘電子股份有限公司

IP101
Single port 10/100 Fast Ethernet Transceiver

1.0 Features

- 10/100Mbps TX/FX
- Full-duplex or half-duplex
- Supports Auto MDI/MDIX function
- Fully compliant with IEEE 802.3/802.3u
- Supports IEEE 802.3u auto-negotiation
- Supports MII / RMII / SNI interface
- IEEE 802.3 full duplex control specification
- Supports Automatic Power Saving mode
- Supports BaseLine Wander (BLW) compensation
- Supports Interrupt function
- Supports repeater mode
- Single 3.3V power supply with built-in 2.5V regulator
- DSP-based PHY Transceiver technology
- Using either 25MHz crystal or 50MHz REF_CLK as clock source
- Flexible LED display for speed, duplex, link, activity and collision
- Supports flow control to communicate with other MAC through MDC and MDIO
- 0.25u, CMOS technology
- 48-pin LQFP

2.0 General Description

IP101 is an IEEE 802.3/802.3u compliant single-port Fast Ethernet Transceiver for both 100Mbps and 10Mbps operations. It supports Auto MDI/MDIX function to simplify the network installation and reduce the system maintenance cost. To improve the system performance, IP101 provides a hardware interrupt pin to indicate the link, speed and duplex status change. IP101 also provides Media Independent Interface (MII) / Serial Network Interface (SNI) or Reduced Media Independent Interface (RMII) to connect with different types of 10/100Mb Media Access Controller (MAC). IP101 is designed to use category 5 unshielded twisted-pair cable or Fiber-Optic cables connecting to other LAN devices. A PECL interface is supported to connect with an external 100Base-FX fiber optical transceiver.

IP101 Transceiver is fabricated with advanced CMOS technology, which the chip only requires 3.3V as power supply and consumes very low power in the Auto Power Saving mode. IP101 can be implemented as Network Interface Adapter with RJ-45 for twisted-pair connection or MAU for Fiber Connection. It can also be easily implemented into HUB, Switch, Router, Access Point, Advanced Communication Riser (ACR) and Communication and Networking Riser (CNR).

3.0 Transmit and Receive Data Path Block Diagram

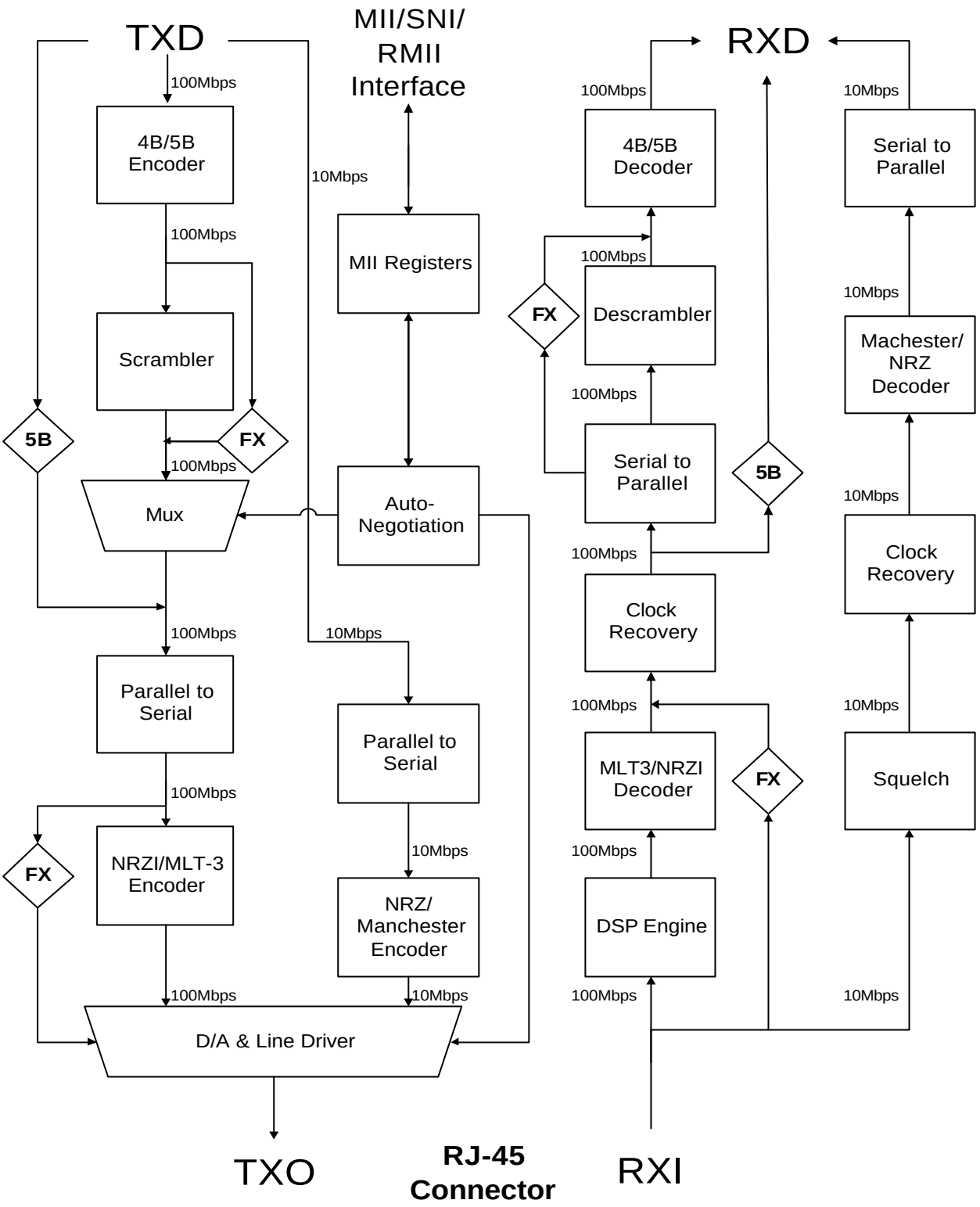


Figure 1: Flow chart of IP101

4.0 Pin Assignments

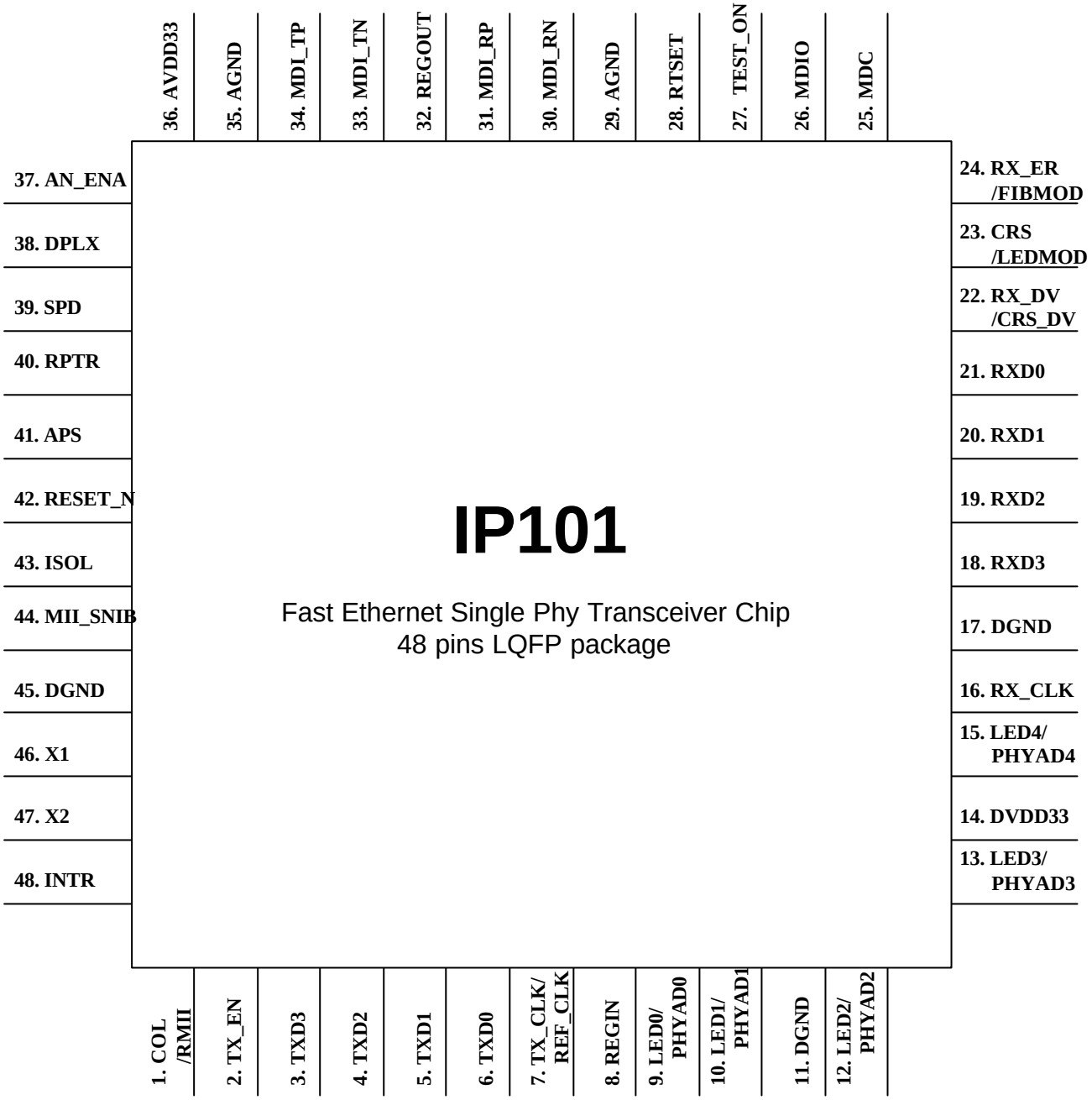


Figure 2 : IP101 pins assignment

5.0 Pin Descriptions

Type	Description
LI	Latched Input in power up or reset
I/O	Bi-directional input and output
I	Input
O	Output

Type	Description
PD	Internal Pull-Down
PU	Internal Pull-Up
P	Power
OD	Open Drain

Pin no.	Label	Type	Description
MII and PCS Interface - Management Interface Pins			
25	MDC	I	**Management Data Interface Clock:** This pin provides a clock reference to MDIO. The clock rate can be up to 10MHz.
26	MDIO	I/O	**Management Data interface Input/Output:** The function of this pin is to transfer management information between PHY and MAC.
MII and PCS Interface – Media Independent Interface (MII) Pins			
2	TX_EN	I (PD)	**Transmit Enable:** This pin is an active high input. At high status, it indicates the nibble data in TXD[3:0] is valid.
7	TX_CLK	O	**Transmit Clock:** This pin provides a continuous 25MHz clock at 100Mbps and 2.5Mbps as timing reference for TXD[3:0] and TX_EN when the chip operates under MII and SNI modes. This pin is an input pin operates as RMII reference clock (REF_CLK) under RMII mode.
3, 4, 5, 6	TXD[3:0]	I	**Transmit Data:** When TX_EN is set low, MAC will transmit data through these 4 lines to PHY which the transmission is synchronizing with TX_CLK.
22	RX_DV	O	**Receive Data Valid:** At high status stands for data flow is present within RXD[0:3] lines and low means no data exchange occurred.
16	RX_CLK	O	**Receive Clock:** This pin provides 25MHz for 100Mbps transmission or 2.5Mhz for 10Mbps transmission and RX_DV pin uses this pin as its reference under MII or SNI mode. While under RMII mode this pin is driven low.
18, 19, 20, 21	RXD[3:0]	O	**Receive Data:** These 4 data lines are transmission path for PHY to send data to MAC and they are synchronizing with RX_CLK.

5.0 Pin Descriptions (continued)

Pin no.	Label	Type	Description
MII and PCS Interface – Media Independent Interface (MII) Pins			
24	RX_ER/ FIBMOD	O/LI (PD)	**Receive error:** This pin outputs a high status when errors occurred in the decoded data in the transmission. **Fiber Mode:** During power on reset, this pin status is latched to determine at which media mode to operate: 1: Fiber mode 0: UTP mode An internal weak pull low resistor sets this to the default of UTP mode. It is possible to use an external 5.1KΩpull high resistor to enable fiber mode. After power on, the pin operates as the Receive Error pin.
1	COL/RMII	O/LI (PD)	**Collision Detected:** When this pin outputs a high status signal it means collision is detected. **RMII Mode:** During power on reset, this pin status is latched and arranged with MII/SNIB (pin44) to determine MAC interface **RMII MII/SNIB** 1 X RMII Interface 0 1 MII Interface 0 0 SNII Interface (**Notice:** This pin is pulled down internally)
23	CRS/LEDMOD	O (PD)	**Carrier Sense:** When signal output from this pin is high indicates the transmission is in process and at low status means the line is in idle state. **LEDMOD:** During power on reset, this pin status is latched to determine at which LED mode to operate, please refer to the LED pins description. (**Notice:** This pin is pulled down internally)
RMII (Reduced MII)			
7	REF_CLK	I	**Reference Clock:** This pin is an input pin operates as RMII reference clock (REF_CLK) under RMII mode. 25MHz Crystal Input and Output, X1 & X2, should be disconnected when REF_CLK is used as the clock source of IP108.
2	TX_EN	I (PD)	**Transmit Enable:** For MAC to indicate transmit operation
5,6	TXD[1:0]	I	**Transmit two-bit Data**
24	RX_ER	I/O	**Receive Error**
22	CRS_DV	O	**Carrier Sense and Receive Data Valid**
20, 21	RXD[1:0]	O	**Received two-bit Data**

5.0 Pin Descriptions (continued)

Pin no.	Label	Type	Description
SNI (Serial Network Interface): 10Mbps only			
2	TX_EN	I (PD)	**Transmit Enable:** Indicate transmit operation to MAC
7	TX_CLK	O	**Transmit Clock:** 10MHz, generate either by PHY or by external
6	TXD0	I	**Transmit Serial Data**
16	RX_CLK	O	**Receive Clock:** 10MHz, clock recovery from received data
21	RXD0	O	**Received Serial Data**
1	COL	O	**Collision Detect**
23	CRS	O	**Carrier Sense**
Cable Transmission Interface			
34 33	MDI_TP MDI_TN	O O	**Transmit Output Pair:** Differential pair shared by 100Base-TX, 100Base-FX and 10Base-T modes. When configured as 100Base-TX, output is an MLT-3 encoded waveform. When configured as 100Base-FX, the output is pseudo-ECL level.
31 30	MDI_RP MDI_RN	I I	**Receive Input Pair:** Differential pair shared by 100Base-TX, 100Base-FX, and 10Base-T modes.
IC Configuration Options			
43	ISOL	I (PD)	Set high to this pin will isolate IP101 from other MAC. This action will also isolate the MDC/MDIO management interface. The power usage is at minimum when this pin is activated. This pin can be directly connected to GND or VCC. (An internal weak pulled-down is used to be inactive as a default)
40	RPTR	I (PD)	Enable this pin to high will put the IP101 into repeater mode. This pin can be directly connected to GND or VCC. (An internal weak pulled-down is used to be inactive as a default)
39	SPD	LI/O (PU)	This pin is latched to input during a power on or reset condition. Set high to put the IP101 into 100Mbps operation. This pin can be directly connected to GND or VCC. (An internal weak pulled-up is used to set 100Mbps as a default)
38	DPLX	LI/O (PU)	This pin is latched to input during a power on or reset condition. Set high to enable full duplex. This pin can be directly connected to GND or VCC. (An internal weak pulled-up is used to set full duplex as a default)
37	AN_ENA	LI/O (PU)	This pin is latched to input during a power on or reset condition. Set high to enable auto-negotiation mode, set low to force mode. This pin can be directly connected to GND or VCC. (An internal weak pulled-up is used to enable N-WAY as a default)
41	APS	I (PU)	Set high to put the IP101 into APS mode. This pin can be directly connected to GND or VCC. Refer to Section 7.7 for more information. (An internal weak pulled-up is used to enable APS mode as a default)
44	MII_SNIB	LI/O (PU)	This pin is latched to input during a power on or reset condition. Pull high to set the IP101 into MII mode operation. Set low for SNI mode. This pin can be directly connected to GND or VCC. (An internal weak pulled-up is used to set MII mode as a default)

5.0 Pin Descriptions (continued)

Pin no.	Label	Type	Description
LED and PHY Address Configuration			
These five pins are latched into the IP101 during power up reset to configure PHY address [0:4] used for MII management register interface. And then, in normal operation after initial reset, they are used as driving pins for status indication LED. The driving polarity, active low or active high, is determined by each latched status of the PHY address [4:0] during power-up reset. If latched status is high then it will be active low, and if latched status is Low then it will be active high. Moreover, IP101 provides 2 LED modes. If 2nd LED mode is selected by pulling up pin CRS, only 3 LEDs are needed for status indication. Default is first LED mode.			
9	PHYAD0/ LED0	LI/O	**PHY Address [0]** **Status:** Mode1: Active when linked. Mode2: Active when linked and blinking when transmitting or receiving data.
10	PHYAD1/ LED1	LI/O	**PHY Address [1]** **Status:** Mode1: Active when in Full Duplex operation. Mode2: Active when in Full Duplex operation and blinking when collisions occur.
12	PHYAD2/ LED2	LI/O	**PHY Address [2]** **Status:** Mode1: Active when linked in 10Base-T mode, and blinking when transmitting or receiving data. Mode2: Active when linked in 10Base-T mode.
13	PHYAD3/ LED3	LI/O	**PHY Address [3]** **Status:** Mode1: Active when linked in 100Base-TX and blinking when transmitting or receiving data. Mode2: Active when linked in 100Base-TX mode.
15	PHYAD4/ LED4	LI/O	**PHY Address [4]** **Status:** Mode1: Active when collisions occur. Mode2: Reserved.
Clock and Miscellaneous - Crystal Input/Output Pins			
47	X2	O	**25MHz Crystal Output:** Connects to crystal to provide the 25MHz output. It must be left open when X1 is driven with an external 25MHz oscillator. It must be left open when X1 is driven with an external 25MHz oscillator or set to low with a pull down resistor.
46	X1	I	**25MHz Crystal Input:** Connects to crystal to provide the 25MHz crystal input. If a 25MHz oscillator is used, connect X1 to the oscillator' s output. If X1 is set to low with a pull down resistor, a 50MHz clock could be applied to pin7 as clock source.

IP101-DS-R0.02 *Feb. 24, 2003*	7 / 33	*Copyright©2003, IC Plus Corp.* *Confidential, All rights reserved.* *Advanced, Specification subject to change without notice.*

5.0 Pin Descriptions (continued)

Pin no.	Label	Type	Description
Clock and Miscellaneous - Miscellaneous Pins			
42	RESET_N	I	**RESET_N:** Enable a low status signal will reset the chip. For a complete reset function, this pin must be asserted low for at least 10ms.
48	INTR	I/O (OD)	**Interrupt Pin:** When the MII register 17:<15> is set to high, this pin is used as an interrupt pin (Notice: this is an open drain output, so an external pulled-up resistor is needed)
27	TEST_ON	(PD)	**Test Enable:** Set this pin to high to enable test mode, while for normal operation, this pin does not need to be connected. (An internal weak pulled-down is used to disable test mode as a default)
28	ISET	I	**Transmit Bias Resistor Connection:** This pin should be connected to GND via a 6.2KO (1%) resistor to define driving current for transmit DAC. The resistance value may be changed, depending on experimental results of the IP101.
Power and Ground			
32	REGOUT	P	**Regulator Power Output:** This is a regulator power output for IP101 digital circuitry.
36	AVDD33	P	**3.3V Analog power input:** This is a 3.3V power supply for analog circuitry, and it should be decoupled carefully.
29,35	AGND	P	**Analog Ground:** These 2 pins should connect to motherboard's GND.
8	REGIN	P	**Regulator Power Input:** This is a regulator power input from Pin32. No external regulator needed.
14	DVDD33	P	**3.3V Digital Power input:** This is a 3.3V power supply for digital circuitry.
11,17,45	DGND	P	**Digital Ground:** These 3 pins should connect to motherboard's GND.

6.0 Register Descriptions

This section will explain the meaning and usage for each of the registers available in the IP101.
The first 7 registers, i.e., Register 0 to Register 6, are defined according to IEEE 802.3 standard, while the rest registers are defined by IC Plus Corp. and they are for internal use or reserved for other usage.
The first 2 registers contain the basic control and status register defined by IEEE standard.
Each register has its own default value, and it is placed in the right block of each register title.

Register 0 : MII Control Register			
Address	**Name**	**Description/Usage**	**Default value (h): 3100**
15	Reset	When set, this action will bring both status and control registers of the PHY to default state. This bit is self-clearing. 1 = Software reset 0 = Normal operation	0, RW
14	Loop-back	This bit enables loop-back of transmit data to the receive data path, i.e., TXD to RXD. 1 = enable loop-back 0 = normal operation	0, RW
13	Speed Selection	This bit sets the speed of transmission. 1 = 100Mbps 0 = 10Mbps During 100Base-FX mode, and when this bit = 1, it indicates read only.	1, RW
12	Auto-Negotiation Enable	This bit determines the auto-negotiation function. 1 = enable auto-negotiation; bits 13 and 8 will be ignored. 0 = disable auto-negotiation; bits 13 and 0:<8> will determine the link speed and the data transfer mode, under this condition. When 100Base-FX mode is enabled, and this bit=0, it indicates read only.	1, RW
11	Power Down	This bit will turn down the power of the PHY chip and the internal crystal oscillator circuit if this bit is enabled. The MDC and MDIO are still activated for accessing to the MAC. 1 = power down 0 = normal operation	0, RW
10	Isolate	1=electrically Isolate PHY from MII but not isolate MDC and MDIO 0=normal operation	0,RW
9	Restart Auto-Negotiation	This bit allows the Nway auto-negotiation function to be reset. 1 = restart auto-negotiation 0 = normal operation	0, RW
8	Duplex Mode	This bit sets the duplex mode if auto-negotiation is disabled (bit 12=0) 1 = full duplex 0 = half duplex After completing auto-negotiation, this bit will reflect the duplex status.(1: Full duplex, 0: Half duplex) When 100Base-FX mode is enabled, this bit can be set through the MDC/MDIO SMI interface or DUPLEX pin.	1, RW
7	Collision Test	1=enable COL signal test 0=disable COL signal test	0,RW
6:0	Reserved		

6.0 Register Descriptions (continued)

Register 1 : MII Status Register			
Address	**Name**	**Description/Usage**	**Default value (h): 7849**
15	100Base-T4	1 = enable 100Base-T4 support 0 = suppress 100Base-T4 support	0, RO
14	100Base-TX Full Duplex	1 = enable 100Base-TX full duplex support 0 = suppress 100Base-TX full duplex support	1, RO
13	100BASE-TX Half Duplex	1 = enable 100Base-TX half duplex support 0 = suppress 100Base-TX half duplex support	1, RO
12	10Base-T Full Duplex	1 = enable 10Base-T full duplex support 0 = suppress 10Base-T full duplex support	1, RO
11	10_Base-T Half Duplex	1 = enable 10Base-T half duplex support 0 = suppress 10Base-T half duplex support	1, RO
10:7	Reserved		0, RO
6	MF Preamble Suppression	The IP101 will accept management frames with preamble suppressed. The IP101 accepts management frames without preamble. A Minimum of 32 preamble bits are required for the first SMI read/write transaction after reset. One idle bit is required between any two management transactions as per IEEE802.3u specifications	1, RO
5	Auto-Negotiation Complete	1 = auto-negotiation process completed 0 = auto-negotiation process not completed	0, RO
4	Remote Fault	1 = remote fault condition detected (cleared on read) 0 = no remote fault condition detected When in 100Base-FX mode, this bit means an in-band signal Far-End-Fault is detected.	0, RO/LH
3	Auto-Negotiation	1 = Link had not been experienced fail state 0 = Link had been experienced fail state	1, RO
2	Link Status	1 = valid link established 0 = no valid link established	0, RO/LL
1	Jabber Detect	1 = jabber condition detected 0 = no jabber condition detected	0, RO/LH
0	Extended Capability	1 = extended register capability 0 = basic register capability only	1, RO

6.0 Register Descriptions (continued)

Register 2 : PHY Identifier Register 1			
Address	**Name**	**Description/Usage**	**Default value (h): 0243**
15:0	PHYID1	PHY identifier ID for software recognize IP101	0X0243, RO

Register 3 : PHY Identifier Register 2			
Address	**Name**	**Description/Usage**	**Default value (h): 0C50**
15:0	PHYID2	PHY identifier ID for software recognize	0X0C50, RO

Note : Register 2 and register 3 identifier registers altogether consist of Vender model, model revision number and Organizationally Unique identifier (OUI) information. Total of 32 bits allocate in these 2 registers and they can return all zeroes in all bits if desired. Register 2 contains OUI's most significant bits and OUI's lest significant bits, Vender model, Model revision number are allocated in register 3.

6.0 Register Descriptions (continued)

Register 4 lists the advertised abilities during auto-negotiation for what will be transmitted to IP101's Link Partner.

Register 4 : Auto-Negotiation Advertisement Register			
Address	**Name**	**Description/Usage**	**Default value (h): 0001**
15	NP	Next Page bit. 0 = transmitting the primary capability data page 1 = transmitting the protocol specific data page	0, RO
14	Reserved		0, RO
13	RF	1 = advertise remote fault detection capability 0 = do not advertise remote fault detection capability	0, RW
12	Reserved		0, RO
11	Asymmetric. Pause	1 = asymmetric flow control is supported by local node 0 = asymmetric flow control is NOT supported by local node	0, RW
10	Pause	1 = flow control is supported by local node 0 = flow control is NOT supported by local node	0, RW
9	T4	1 = 100Base-T4 is supported by local node 0 = 100Base-T4 not supported by local node	0, RO
8	TX Full Duplex	1 = 100Base-TX full duplex is supported by local node 0 = 100Base-TX full duplex not supported by local node	1, RW
7	TX	1 = 100Base-TX is supported by local node 0 = 100Base-TX not supported by local node	1, RW
6	10 Full Duplex	1 = 10Base-T full duplex supported by local node 0 = 10Base-T full duplex not supported by local node	1, RW
5	10	1 = 10Base-T is supported by local node 0 = 10Base-T not supported by local node	1, RW
4:0	Selector	Binary encoded selector supported by this node. Currently only CSMA/CD <00001> is specified. No other protocols are supported.	<00001>, RO

6.0 Register Descriptions (continued)

Register 5 describes the advertised abilities of the Link Partner's PHY when it is receiving data during the process of auto-negotiation. If next-pages are supported, this register may change after the auto-negotiation has established.

Register 5 : Auto-Negotiation Link Partner Ability Register			
Address	**Name**	**Description/Usage**	**Default value (h): 0080**
15	Next Page	Next Page bit. 0 = transmitting the primary capability data page 1 = transmitting the protocol specific data page	0, RO
14	Acknowledge	1 = link partner acknowledges reception of local node' s capability data word 0 = no acknowledgement	0, RO
13	Remote Fault	1 = link partner is indicating a remote fault 0 = link partner does not indicate a remote fault	0, RO
12	Reserved		0, RO
11	Asymmetric. Pause	1 = asymmetric flow control is supported by local node 0 = asymmetric flow control is NOT supported by local node	0, RO
10	Pause	1 = flow control is supported by Link partner 0 = flow control is NOT supported by Link partner	0, RO
9	T4	1 = 100Base-T4 is supported by link partner 0 = 100Base-T4 not supported by link partner	0, RO
8	TXFD	1 = 100Base-TX full duplex is supported by link partner 0 = 100Base-TX full duplex not supported by link partner	0, RO
7	100BASE-TX	1 = 100Base-TX is supported by link partner 0 = 100Base-TX not supported by link partner This bit will also be set after the link in 100Base is established by parallel detection.	1, RO
6	10FD	1 = 10Base-T full duplex is supported by link partner 0 = 10Base-T full duplex not supported by link partner	0, RO
5	10Base-T	1 = 10Base-T is supported by link partner 0 = 10Base-T not supported by link partner This bit will also be set after the link in 10Base is established by parallel detection.	0, RO
4:0	Selector	Link Partner' s binary encoded node selector Currently only CSMA/CD <00001> is specified	<00000>, RO

6.0 Register Descriptions (continued)

Register 6 defines more auto-negotiation registers to meet the requirement.

Register 6 : Auto-Negotiation Expansion Register			
Address	**Name**	**Description/Usage**	**Default value (h): 0000**
15:5	Reserved	This bit is always set to 0.	
4	MLF	This status indicates if a multiple link fault has occurred. 1 = fault occurred 0 = no fault occurred	0, RO
3	LP_NP_ABLE	This status indicates if the link partner supports Next Page negotiation. 1 = supported 0 = not supported	0, RO
2	NP_ABLE	This bit indicates if the device is able to send additional Next Pages.	0, RO
1	PAGE_RX	This bit will be set if a new link code word page has been received. It is cleared automatically after the auto-negotiation link partner' s ability register (register 5) is read by the management.	0, RO
0	LP_NW_ABLE	1 = link partner supports Nway auto-negotiation.	0, RO

6.0 Register Descriptions (continued)

Register 16 and register 17 are defined by IC Plus Corp. and it is for internal testing purpose.

Register 16 : PHY Spec. Control Register			
Address	**Name**	**Description/Usage**	**Default value (h): 0000**
15	Debug Mode	0 = IP101 operates at normal mode 1 = IP101 operates at debug mode (Notice the functionalities of bit 16:<14>, 16:<13>, 16:<12>, and 16:<4:0> depend on the setting of this bit 16:<15>	0, R/W
14:12	Reserved		
11	MDI disable	Set high to disable the automatic switch of MDI and MDI-X modes	0, R/W
10	Heart Beat Enable	Heart beat function enable at 10Base-T	0, R/W
9	Jabber Enable	Jabber function enable at 10Base-T	0, R/W
8	Far-End Fault Enable/Disable	To enable or disable the functionality of Far-End Fault Mode Enable Disable 100Base-TX 1 0 100Base-FX 0 1	0, R/W
7	Analog Power Saving Disable	Set high to disable the power saving during auto-negotiation	0, R/W
6	Reserved		0, R/W
5	Bypass DSP reset	Set high to bypass the reset DSP mechanism in PCS sub-layer	0, R/W
4:3	Reserved		
2	Repeater Mode	Set high to put IP101 into repeater mode	0, R/W
1	APS Mode	Set high to enable Auto Power Saving mode	0, R/W
0	Analog Off	Set high to power down analog transceiver	0, R/W

6.0 Register Descriptions (continued)

Register 17 : PHY Interrupt Ctrl/Status Register			
Address	**Name**	**Description/Usage**	**Default value (h): 0E00**
15	INTR pin used	Set high to enable pin48 as an interrupt pin, or high impedance is presented at this pin	0, R/W
14:12	Reserved		
11	All Mask	When this bit is set high, changes in all events will not cause an interrupt	1, R/W
10	Speed Mask	When this bit is set high, changes in speed mode will not cause an interrupt	1, R/W
9	Duplex Mask	When this bit is set high, changes in duplex mode will not cause an interrupt	1, R/W
8	Link Mask	When this bit is set high, changes in link status will not cause an interrupt	1, R/W
7	Arbiter State Enable	When this bit is set high, changes in N-WAY arbiter state machine will cause an interrupt	0, R/W
6	Arbiter State Change	Flag to indicate N-WAY arbiter change interrupt	0, R/W
5:3	Reserved		0, R/W
2	Link Status Change	Flag to indicate link status change interrupt	0, R/W
1	Speed Change	Flag to indicate speed change interrupt	0, R/W
0	Duplex Change	Flag to indicate duplex change interrupt	0, R/W

7.0 Functional Description

IP101 10/100Mbps Ethernet PHY Transceiver integrates 100 Base-TX, 100 Base-FX and 10 Base-T modules into a single chip. IP101 acts as an interface between physical signaling and Media Access Controller (MAC).

IP101 has several major functions:

1. **PCS layer (Physical Coding Sub-Layer)**: This function contains transmit, receive and carrier sense functional circuitries.
2. **Management interface**: Media Independent Interface (MII) or Reduced Management Interface (RMII) registers contains information for communication with other MAC.
3. **Auto-Negotiation**: Communication conditions between 2 PHY transceivers. IP101 advertise its own ability and also detects corresponding operational mode from the other party, eventually both sides will come to an agreement for their optimized transmission mode.

IP101's major features included:

1. Flow Control ability
2. LED configuration access
3. Operation modes for both full and half duplex
4. APS (Auto Power Saving) mode
5. Base Line Wander (BLW) compensation
6. Auto MDI/MDIX function
7. Interrupt function
8. Repeater Mode

Major Functional Block Description

The functional blocks diagram is referred to Figure 1:

1. **4B/5B encoder:** 100 Base-X transmissions require converting 4-bit nibble data into 5-bit wide data code-word format. Transmitting data is packaged by J/K codes at the start of packet and by T/R codes at the end of packet in the 4B/5B block. When transmit error has occurred during a transmitting process, the H error code will be sent. The idle code is sent between two packets.

2. **4B/5B Decoder:** The decoder performs the 5B/4B decoding from the received code-groups. The 5 bits (5B) data is decoded into four bits nibble data. The decoded 4 bit (4B) data is then forwarded through MII to the repeater, switch or MAC device. The SSD is then converted into 4B 5 nibbles and the ESD and IDLE Codes are replaced by 4B 0 nibbles data. The decoded data is driven onto the corresponding MII port or shared MII port. Receiving an invalid code group will cause PHY to assert the MII RXER signal.

3. **Scrambler/Descrambler:** Repetitive patterns exist in 4B/5B encoded data which result in large RF spectrum peaks and keep the system from being approved by regulatory agencies. The peak in the radiated signal is reduced significantly by scrambling the transmitted signal. Scrambler adds a random generator to the data signal output. The resulting signal is with fewer repetitive data patterns. The scrambled data stream is descrambled at the receiver by adding another random generator to the output. The receiver's random generator has the same function as the transmitter's random generator. Scrambler operation is dictated by the 100Base-X and TP_FDDI standards.

4. **NRZI/MLT-3(Manchester) Encoder and Decoder:** 100 Base-TX Transmission requires to encode the data into NRZ format and again converted into MLT-3 signal, while 10 Base-T will convert into Manchester form after NRZ coding. This helps to remove the high frequency noise generated by the twisted pair cables. At receiving end, the coding is reversed from MLT-3 (Manchester) signal back to NRZ format.

5. **Clock Recovery:** The receiver circuit recovers data from the input stream by regenerating clocking information embedded in the serial stream. The clock recovery block extracts the RXCLK from the transition of received

6. **DSP Engine:** This block includes Adaptive equalizer and Base Line Wander correction function.

Transmission Description

10Mbps Transmit flow path:

TXD → Parallel to Serial → NRZI/Manchester Encoder → D/A & line driver → TXO

After MAC passes data to PHY via 4 bits nibbles, the data are serialized in the parallel to serial converter. The converter outputs NRZI coded data which the data are then mapped to Manchester code within the Manchester Encoder. Before transmitting to the physical medium, the Manchester coded data are shaped by D/A converter to fit the physical medium.

10Mbps Receive:

RXI → Squelch → Clock Recovery → Manchester/NRZ Decoder → Serial to Parallel → RXD

The squelch block determines valid data from both AC timing and DC amplitude measurement. When a valid data is present in the medium, squelch block will generate a signal to indicate the data has received. The data receive are coded in Manchester form, and are decoded in the Manchester to NRZ Decoder. Then the data are mapped to 4 bits nibbles and transmitted onto MAC interface.

100Mbps TX Transmit:

TXD → 4B/5B Encoder → Scrambler → NRZI/MLT-3 Encoder → D/A & line driver → TXO

The major differences between 10Mbps transmission and 100Mbps transmission are that 100Mbps transmission requires to be coded from 4-bit wide nibbles to 5 bits wide data coding, and after that the data are scrambled through scrambler to reduce the radiated energy generated by the 4B/5B conversion.
Then the data is converted into NRZI form and again from NRZI coded form into MLT-3 form. The MLT-3 data form is fed into D/A converter and shaped to fit the physical medium transmission.

100Mbps TX Receive:

RXI → DSP → Serial to Parallel → Descrambler → 4B/5B Decoder → RXD

The received data first go through DSP engines which includes adaptive equalizer and base-line wander correction mechanism. The adaptive equalizer will compensate the loss of signals during the transmission, while base-line wander monitors and corrects the equalization process. If a valid data is detected then the data are parallelized in Serial to Parallel block, which it converts NRZI coded data form back to scrambled data. The scrambled data are descrambled and converted back to 4 bits–wide format data and then feed into MAC.

100Mbps FX Transmit:

TXD → 4B/5B Encoder → Parallel to Serial → D/A & line driver → TXO

Fiber transmission first encodes the data into 5bits wide data format. The data are then serialized and then converted to fit the physical medium transmission.

100Mbps FX Receive:

RXI → DSP (Clock Recovery) → Serial to Parallel → 4B/5B Decoder → RXD

The received data contains the information periodically, and for Fiber Receive, the Clock recovery extracts the data from the clock cycle. The extracted data is parallelized into 5-bits wide data, which are then converted back to nibble-formed information.

MII and Management Control Interface

Media Independent Interface (MII) is described in clause 22 in the IEEE 802.3u standard. The main function of this interface is to provide a communication path between PHY and MAC/Repeater. It can operate either in 10Mb or 100Mb environment, and operate at 2.5MHz frequency for 10Mb clock data rate or 25MHz frequency for 100Mb data rate transmission. MII consists of 4 bit wide data path for both transmit and receive. The transmission pins consists of TXD[3:0], TX_EN and TXC, and at receiving MII pins have RXD[3:0], RXER, RX_DV and RXC. The Management control pins include MDC and MDIO. MDC, Management Data Clock, provides management data clock at maximum of 10MHz as a reference for MDIO, Management Data Input/Output. CRS, Carrier Sense, is used for signaling data transmission is in process while COL, Collision, is used for signaling the occurrence of collision during transmission.

Transmitting a packet, MAC will first assert TX_EN and convert the information into 4 bit wide data and then pass the data to IP101. IP101 will sample the data according to TX_CLK until TX_EN is low.
While receiving a packet, IP101 asserts RX_DV high when data present in the medium through RXD[3:0] bus lines. IP101 samples received data according to RX_CLK until the medium is back to idle state.

RMII Interface

Reduced Media Independent Interface (RMII) is defined to provide a fewer pins data transmission condition. The management interface, MDC and MDIO, are identical to the MII defined in IEEE 802.3. RMII supports 10/100Mb data rates and the clock source is provided by a single 50MHz clock from either external or within IP101. This clock is used as reference for transmit, receive and control. RMII provides independent 2 bit wide transmit and receive data path, i.e., TXD[1:0] and RXD[1:0]. CRS_DV is asserted when the receive medium is not idle and de-asserted when the medium is idle.

Before any transmission occurs, CRS_DV should be de-asserted and value "00" should be present in both TXD[1:0] and RXD[1:0]. When transmission begins, IP101 will send "01" (TXD[1:0] = 01) for preamble to indicate SFD, and also assert TX_EN synchronous with first nibble of the preamble. TX_EN should be de-asserted until the end of the data transmission. At receiving mechanism, by receiving "01" means a valid data is available. If False carrier is detected, RXD[1:0] shall be "10" until the end of the transmission.

At 10Mbps mode, every 10^{th} cycle of REF_CLK will be sampled in RXD[1:0] and TXD[1:], because the REF_CLK frequency is 10 times faster than the data rate of the 10Mbps.

SNI Interface

The IP101 also provides serial-network interface for legacy MACs, when the chip operates at 10BASE-T either by NWAY resolved result or by forced mode. To setup for this mode of operation, pull both the MII/SNIB and the COL/RMII pins to low.
The transaction protocol of SNI interface is almost identical to that of MII interface, except of data bit width and clock rate. This interface consists of 10Mbps transmit and receive clock generated by PHY's digital phase-locked loop (DPLL), 10Mbps transmit and receive serial data, transmit enable, collision detect, and carry sense signals.

Auto-Negotiation and Related Information

IP101 supports clause 28 in the IEEE 802.3u standard. IP101 can be operated either in 10Mbps/100Mbps or half/full duplex transmission mode. IP101 also supports flow control mechanism to prevent any collision in the network. If the other end does not support N-Way function, IP101 will link at half duplex mode and enter parallel detection.
At beginning of auto-negotiation, IP101 will advertise its own ability by sending FLP waveform out to the other end and also listening signals from the other end. IP101 will place itself into correct connection speed depends on the received signals. If NLP signal is replied from the other end, IP101 will enter 10Mbps, while active idle pulses (unique 100Mbps pattern) IP101 will go to 100Mbps mode instead.

Once the negotiation has completed with the other party, IP101 will configure itself to the desired connection mode, i.e., 10/100Mbps or Half/Full duplex modes. If there is no detection of link pulses within 1200ms~1500mS, IP101 will enter Link Fail State and restart auto-negotiation procedure.

The auto-negotiation information is stored in the IP101's MII registers. These registers can be modified and monitor the IP101's N-Way status. The reset auto-negotiation in register 0 of MII registers can be set at any time to restart auto-negotiation.

The flow control ability is also included in the IP101 chip. If MAC supports flow control condition, then flow control will be enabled by setting bit 10 (Pause) of the Register 4.

Pin 37 (AN_ENA), 38 (DLPX), 39 (SPD) can be configured manually to set IP101's transmission ability.

1. Enabling Pin 37 (set high) will put IP101 to N-Way mode, if set low to pin 37, it will put IP101 into forced mode.
2. Pin 38 will configure Duplex ability of IP101, at high, IP101 is set to Full-Duplex and low will let IP101 enter half duplex mode.
3. Pin 39 determines the speed of connection. If the pin is pulled high, IP101 is set at 100Mbps, while at low will make IP101 to connect at 10Mbps speed.

LED Configuration

Various Link indications are displayed by LEDs.

LED	Function
LED0	Link status: Active indicates the link has established
LED1	Duplex operation: Active indicates duplex operation is on
LED2	10Mbps Transmission: Active indicates 10Mbps connection has established
LED3	100Mbps Transmission: Active indicates 100Mbps connection has established
LED4	Collision detect: Active indicates Collision has occurred

Table 4-1: LED Configuration

LED pins also include the information of PHY address, the default PHY address is set at 00001b (01h). The PHY address can be modified by changing the LED circuitry. The modification can be arranged as follow:

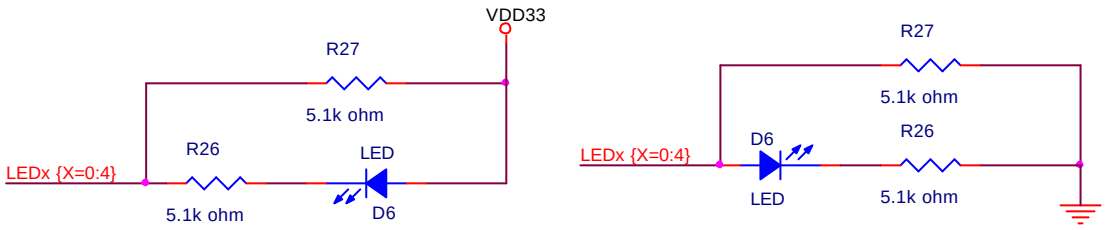


Figure 3: PHY address Configuration

The left diagram will enable the specific PHY address to 1, if it is connected to VDD33. The diagram on the right shows the configuration for setting PHY address to 0, when the circuit is connected to ground.
By setting either one of the bits according to the diagram will allow one to modify PHY addresses from PHYAD0 to PHYAD4.

Power-Down Modes

IP101 can be power-down by 4 methods. These 4 methods are as follow:

1. Power Down in bit 11 of Register 0: Enable this bit will disconnect the power to IP101 and also internal clock, but MDC and MDIO are still activated.
2. APS mode in bit 1 of Register 16: Set high to this bit will let PHY into power saving mode
3. Analog off in bit 0 of Register 16: Enable this bit will put IP101 in analog off state. This will power down all analog functions but not internal 25MHz oscillator.
4. ISOL pin (pin 43): Set high will isolate IP101 from MAC and disable management interface (MDC and MDIO). The power usage is at minimum when this pin is activated.

Repeater Modes

To enter Repeater mode, one can either set pin 40 (RPTR) to high or set 1 to bit 2 of Register 16 will allow IP101 to enter Repeater mode. If IP101 is used in repeater, CRS will be high if IC is in process of receiving packets, while IP101 is used in a network interface card, CRS will be generated in both transmitting and receiving packets.

Miscellaneous

ISET (pin 28) should be connected to GND via a 6.2k ohm resistor with 1% accuracy to ensure a correct driving current for transmit DAC.

Set low to pin 42, REST_N, for at least 10ms will reset all functions available in IP101. The bit 15 of Register 0 will put PHY into its default status.

8.0 Electrical Characteristics (D.C. Characteristic)

Absolute Maximum Rating

Symbol	Conditions	Minimum	Typical	Maximum
Supply Voltage		3.0 V	3.3V	3.6V
Storage Temp		-55°C		125°C

Power Dissipation

Symbol	IP101
Auto Power Saving Mode	27mA
Analog off Mode	8mA
Power Down Mode	4mA
Isolate Mode	3mA
100 Full	136mA
100 Half	140mA
10 Full	149mA
10 Half	149mA
10 Transmit	149mA
10 Receive	149mA
10 IDLE	73mA

Operating Condition

Symbol	Conditions	Minimum	Typical	Maximum
Vcc	3.3V Supply voltage	3.0 V	3.3V	3.6V
TA	Operating Temperature	0°C		70°C

Supply Voltage

Symbol	Specific Name	Condition	Min	Max
V_{IH}	Input High Vol.		0.5*Vcc	Vcc+0.5V
V_{IL}	Input Low Vol.		-0.5V	0.3*Vcc
V_{OH}	Output High Vol.		0.9*Vcc	Vcc
V_{OL}	Output Low Vol.			0.1*Vcc
I_{OZ}	Tri-state Leakage	Vout=Vcc or GND		
I_{IN}	Input Current	Vin=Vcc or GND		
Icc	Average Operating Supply Current	Iout=0mA		200mA
PECL V_{IH}	PECL Input High Vol		Vdd-1.16V	Vdd-0.88V
PECL V_{IL}	PECL Input Low Vol.		Vdd-1.81V	Vdd-1.47V
PECL V_{OH}	PECL Output High Vol.		Vdd-1.02V	
PECL V_{OL}	PECL Output Low Vol.			Vdd-1.62V

9.0 Layout Guideline

General Layout Guideline

Best performance depends on good layout. The following recommendation steps will help customer to gain maximum performance.

Create good power source to minimize noise from switching power source.

- All components are qualified, especially high noise component, such as clock component.
- Use bulk capacitors between power plane and ground plane for 4 layers board, signals trace on component and bottom side, power plane on third layer, and ground layer on second layer.
- Use decoupling capacitors to decouple high frequency noise between chip' s power and ground, must be as close as possible to IP101.
- The clock trace length to IP101 must be equal the clock trace length to MAC.
- Use guard traces to protect clock traces if possible
- Avoid signals path parallel to clock signals path, because clock signals will interference with other parallel signals, degrading signal quality, such as MDC and X1signals.
- The clock must be low jitter with less than 0.5ns for 25/50/125Mhz 100ppm.
- Avoid highly speed signal across ground gap to prevent large EMI effect.
- Keep ground region as one continuous and unbroken plane.
- Place a gap between the system and chassis grounds.
- No any ground loop exists on the chassis ground.

Twisted Pair recommendation

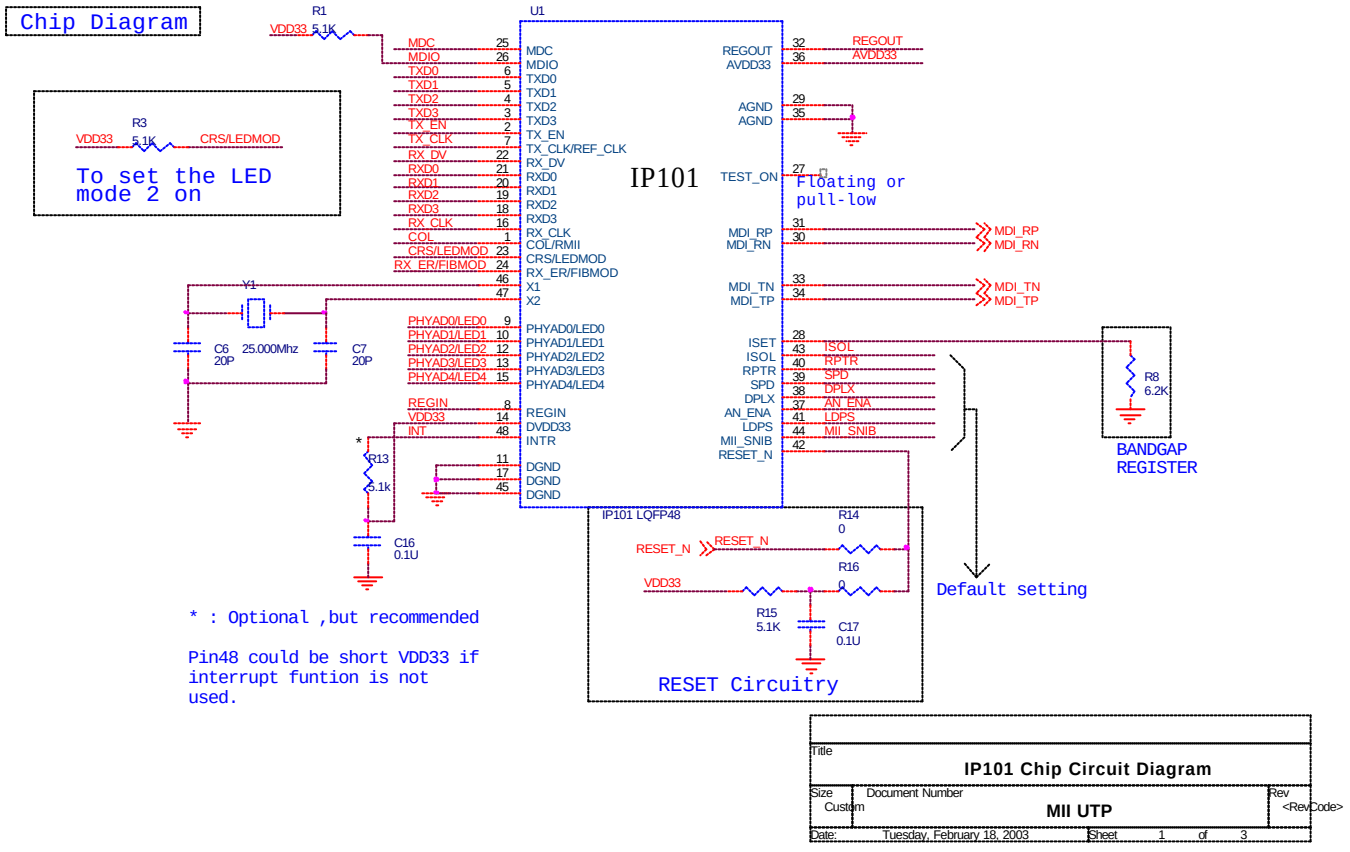
When routing the TD+/- signal traces from IP101 to transformer, the traces should be as short as possible, the termination resistors should be as close as possible to the output of the TD+/- pair of IP101. Center tap of primary winding of these transformers must be connected to analog 2.5V respectively. It is recommended that RD+/- trace pair be route such that the space between it and others is three times space, which can separate individual traces from one another.

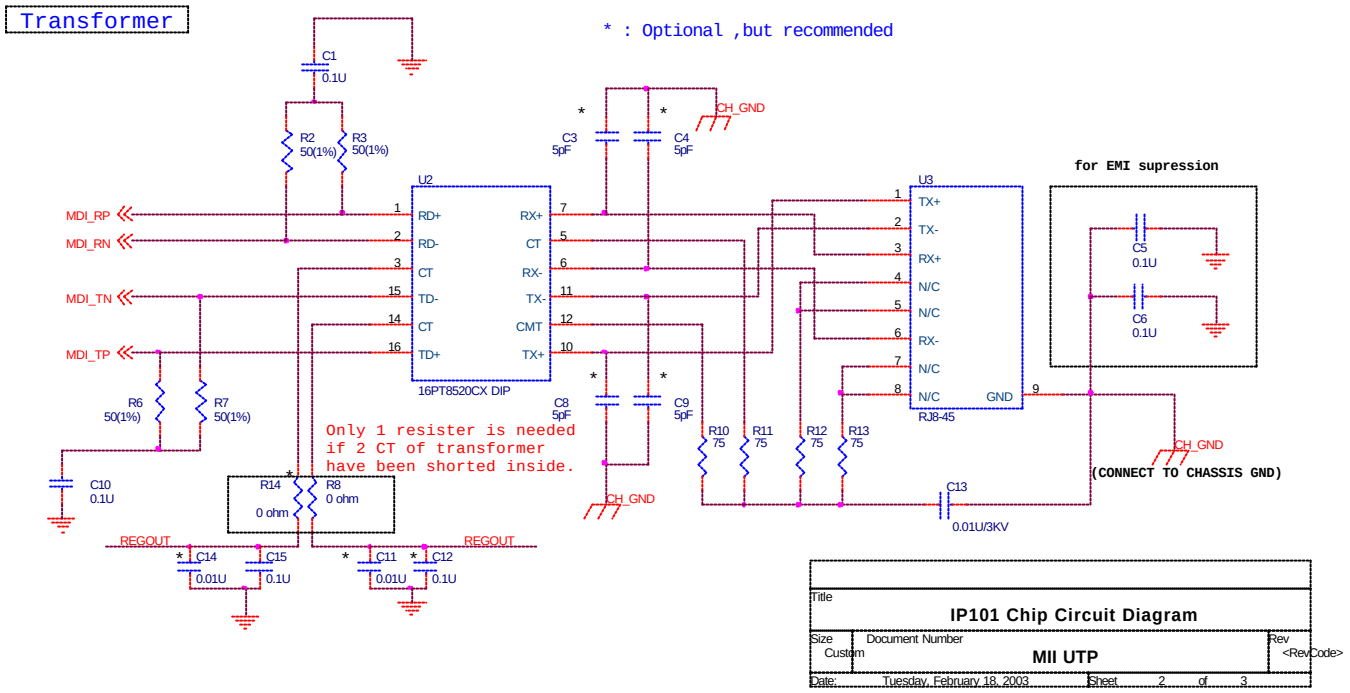
It is recommended that offers chassis ground in the area between transformer and media connector (RJ-45 port), this isolates the analog signals from external noise sources and reduces EMI effect. Note the usage of the vias, it is best not use via to place anywhere other than in close proximity to device, in order to minimize impedance variations in a given signal trace.

10.0 Circuit Diagram

There are 3 suggested circuit diagrams for IP101.

10.1 MII interface with UTP

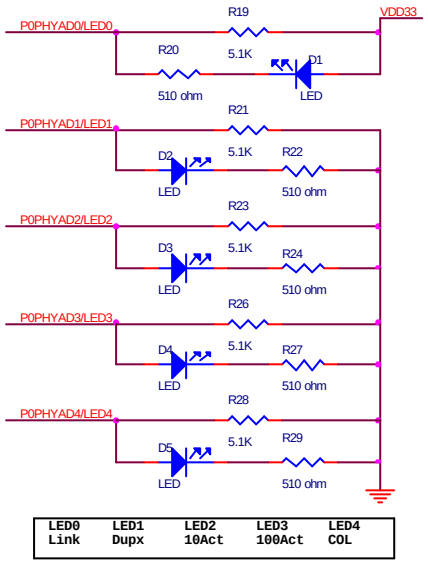




10.1 MII interface with UTP (continued)

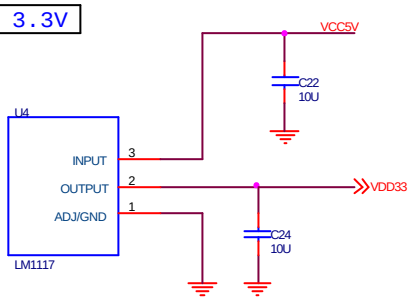
LED and PHY address Configuration

This schematic sets PHY address to 00001b.

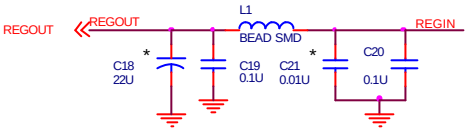


LED0	LED1	LED2	LED3	LED4
Link	Dupx	10Act	100Act	COL

Power: 5V ~ 3.3V



REGOUT and REGIN connection

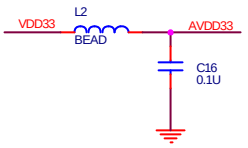


* : Optional ,but recommended

Hardwire Configuration network:

1. This configuration shows
   Enable: Auto negotiation, Full duplex, 100Mbps,
   Link Down Power Saving, MII interface
   Disable: Isolate, Repeater mode
2. These senven configuration pins could be connected to VDD or GND directly.

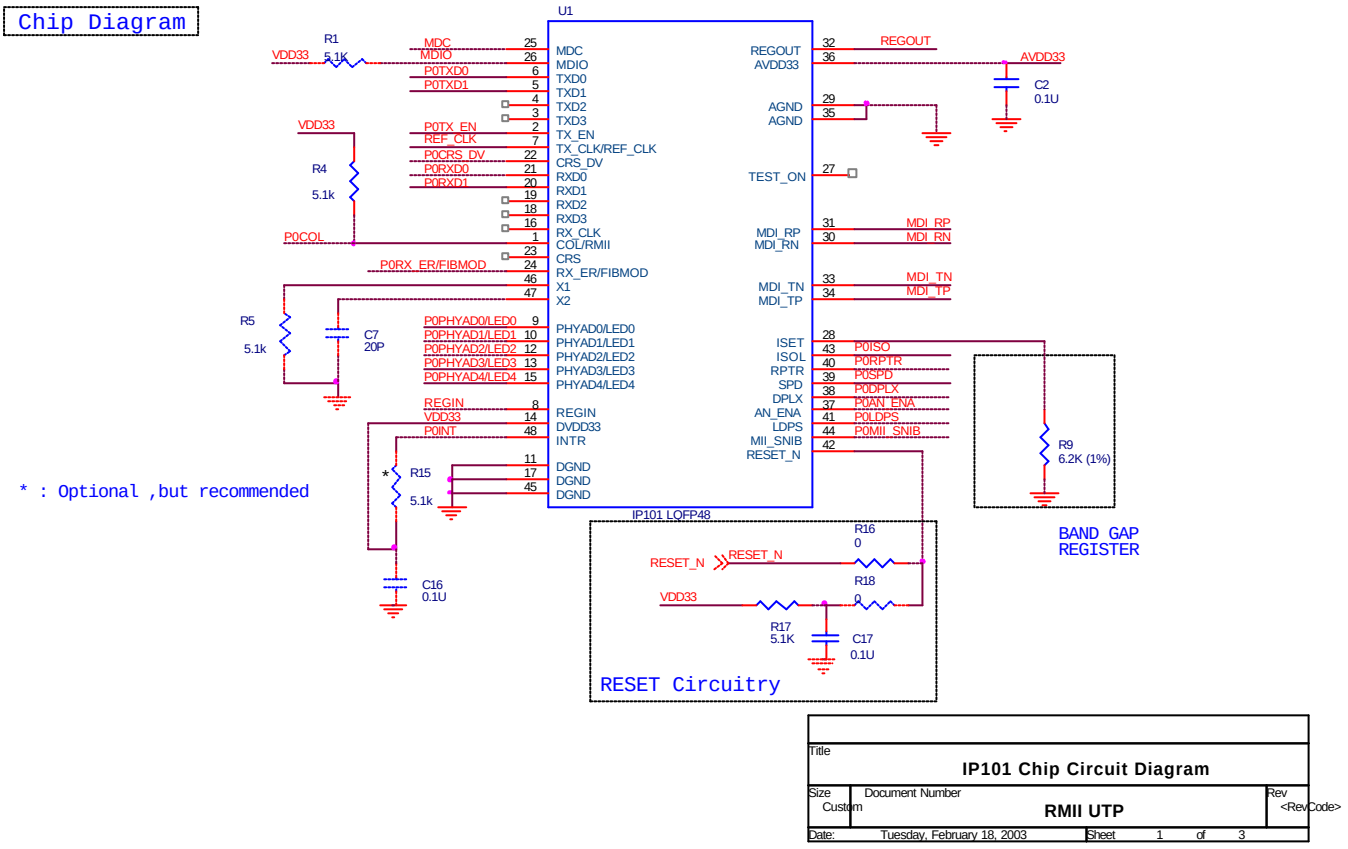
Analog and Digital 3.3V connection



Title	IP101 Chip Circuit Diagram	
Size: A	Document Number: MII UTP	Rev: <RevCode>
Date: Tuesday, February 18, 2003	Sheet 3 of 3	

10.2 RMII interface with UTP connection

Chip Diagram



Title	IP101 Chip Circuit Diagram		
Size: Custom	Document Number: RMII UTP		Rev: <RevCode>
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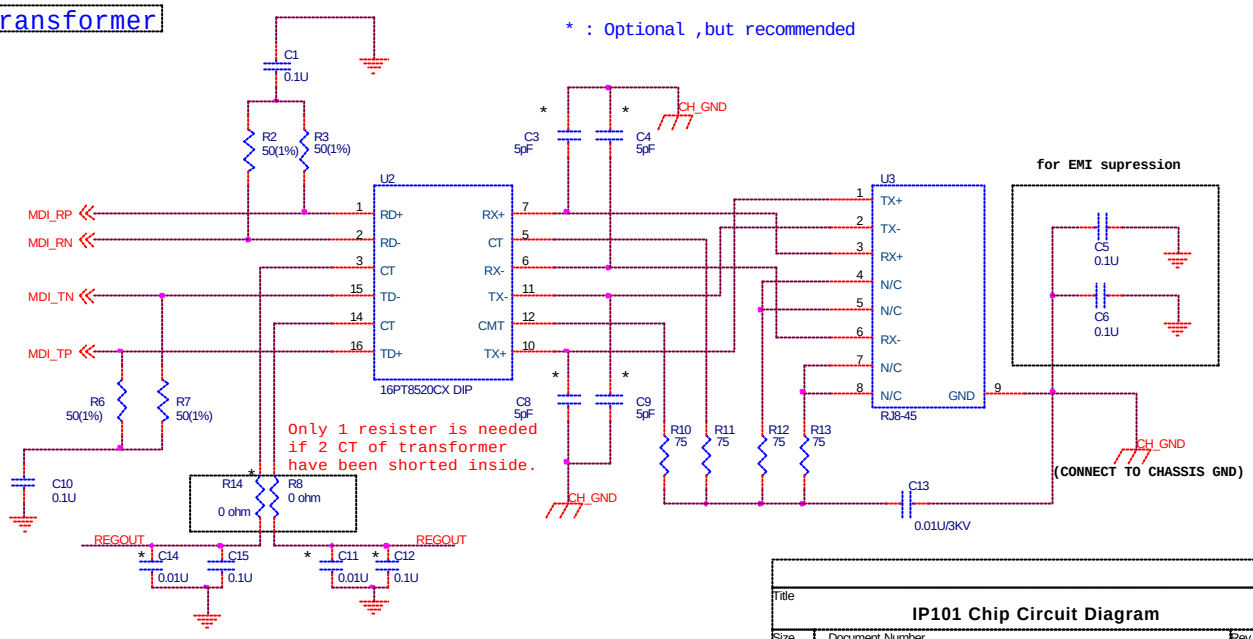
Transformer

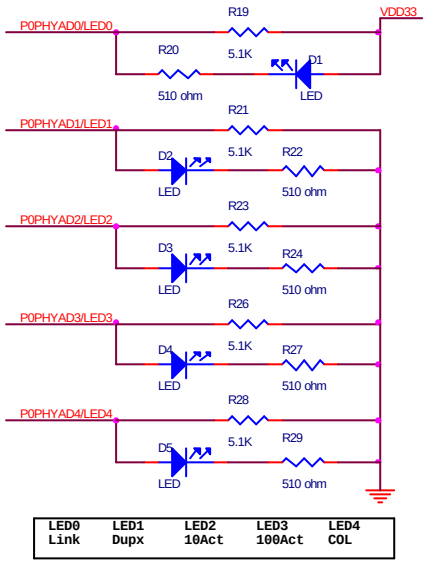


Title	IP101 Chip Circuit Diagram		
Size: Custom	Document Number: RMII UTP		Rev: <RevCode>
Date: Tuesday, February 18, 2003	Sheet 2 of 3		

10.2 RMII interface with UTP connection (continued)

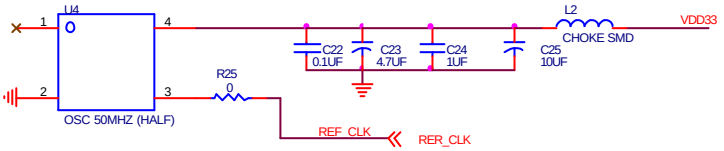
LED and PHY address Configuration

This schematic sets PHY address to 00001b.



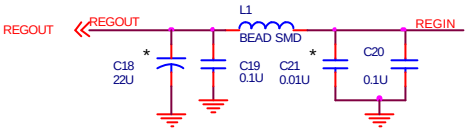
LED0	LED1	LED2	LED3	LED4
Link	Dupx	10Act	100Act	COL

CLOCK



Oscillator's clock MUST be at same distance from all chipsets.

REGOUT and REGIN connection

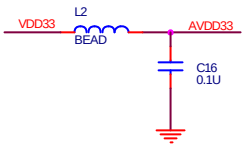


* : Optional ,but recommended

Hardwire Configuration network:

1. This configuration shows
   Enable: Auto negotiation, Full duplex, 100Mbps,
   Link Down Power Saving, MII interface
   Disable: Isolate, Repeater mode
2. These senven configuration pins could be connected to VDD or GND directly.

Analog and Digital 3.3V connection



Title	IP101 Chip Circuit Diagram	
Size A	Document Number RMII UTP	Rev <RevCode>
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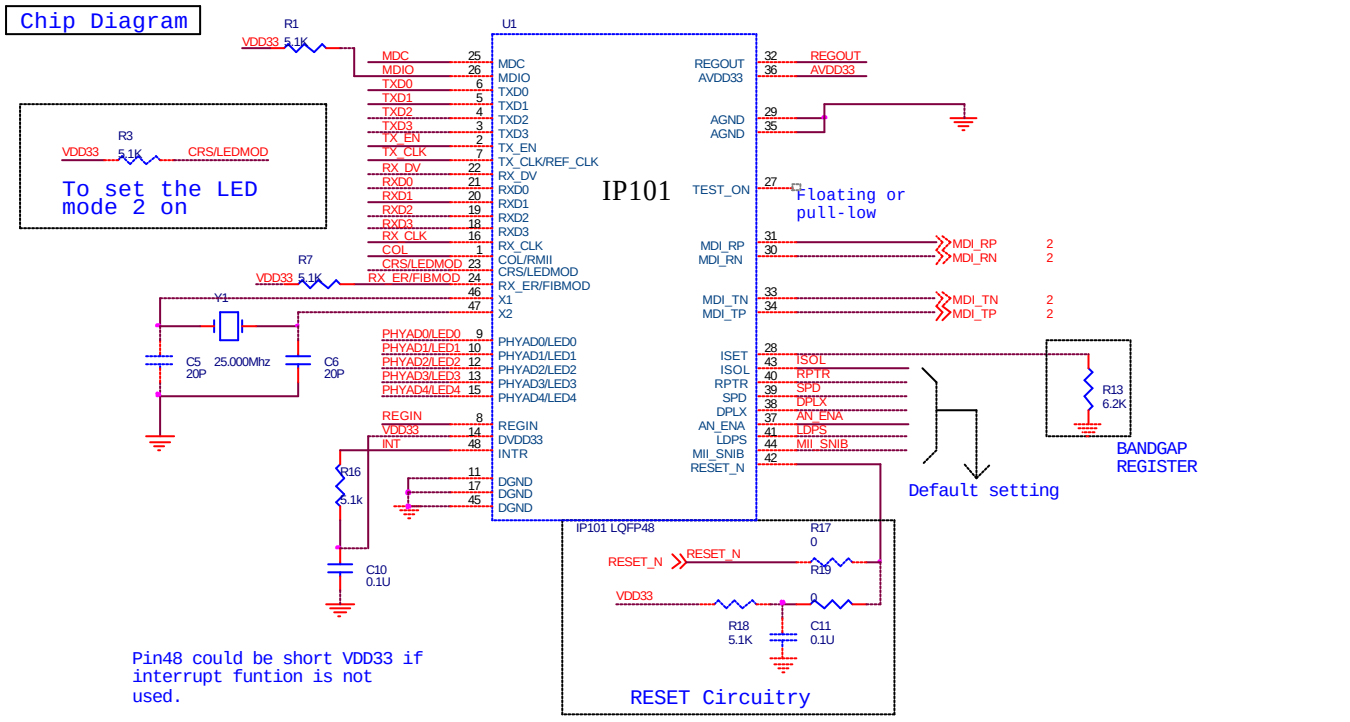
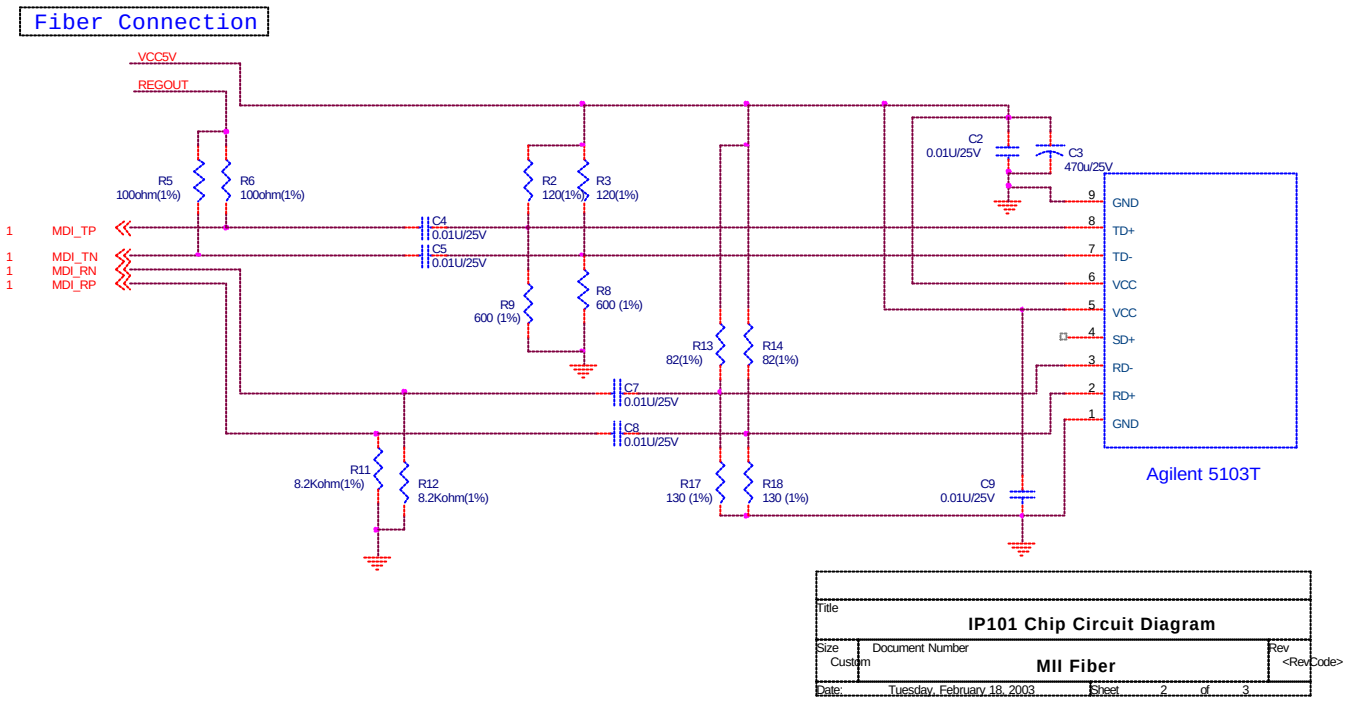
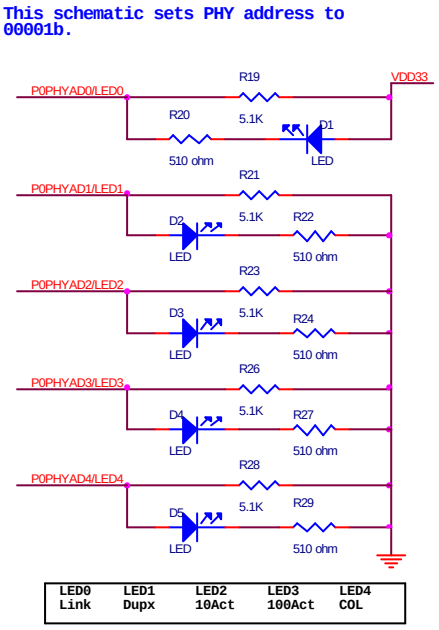
10.3 Fiber connection for both MII and RMII circuits



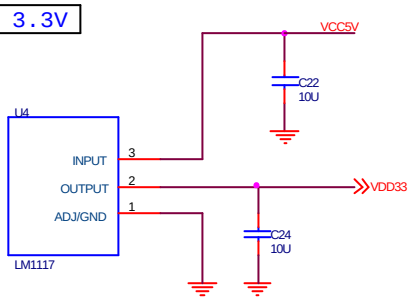


10.3 Fiber connection for both MII and RMII circuits (continued)

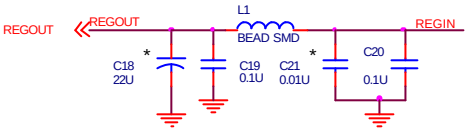
LED and PHY address Configuration



Power: 5V ~ 3.3V



REGOUT and REGIN connection

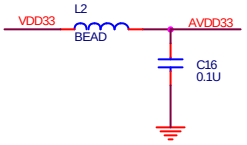


* : Optional ,but recommended

Hardwire Configuration network:

1. This configuration shows
   Enable: Auto negotiation, Full duplex, 100Mbps,
   Link Down Power Saving, MII interface
   Disable: Isolate, Repeater mode
2. These senven configuration pins could be connected to VDD or GND directly.

Analog and Digital 3.3V connection



Title	IP101 Chip Circuit Diagram		
Size A	Document Number MII Fiber		Rev <RevCode>
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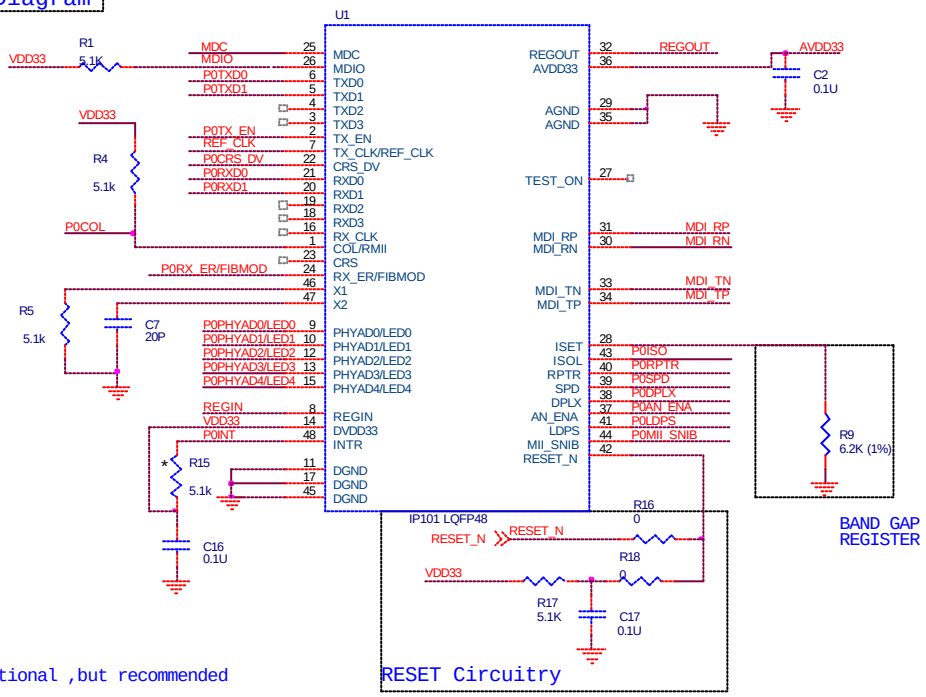
10.3 Fiber connection for both MII and RMII circuits (continued)

Chip Diagram



Title	IP101 Chip Circuit Diagram	
Size: Custom	Document Number: RMII Fiber	Rev: <RevCode>
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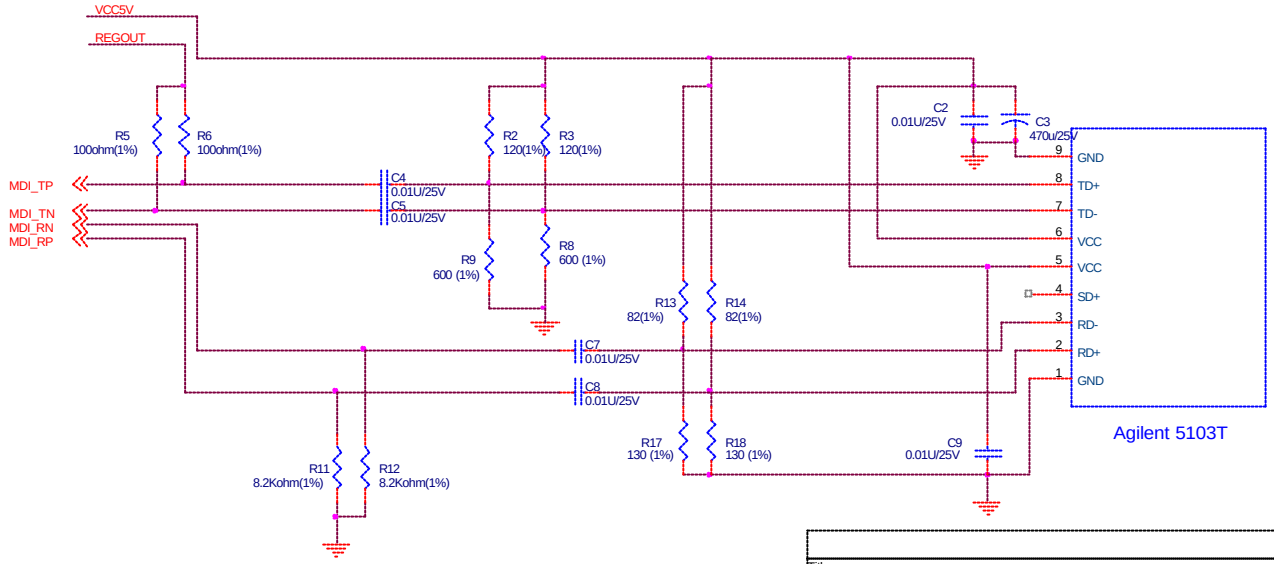
Fiber Connection



Title	IP101 Chip Circuit Diagram	
Size: Custom	Document Number: RMII Fiber	Rev: <RevCode>
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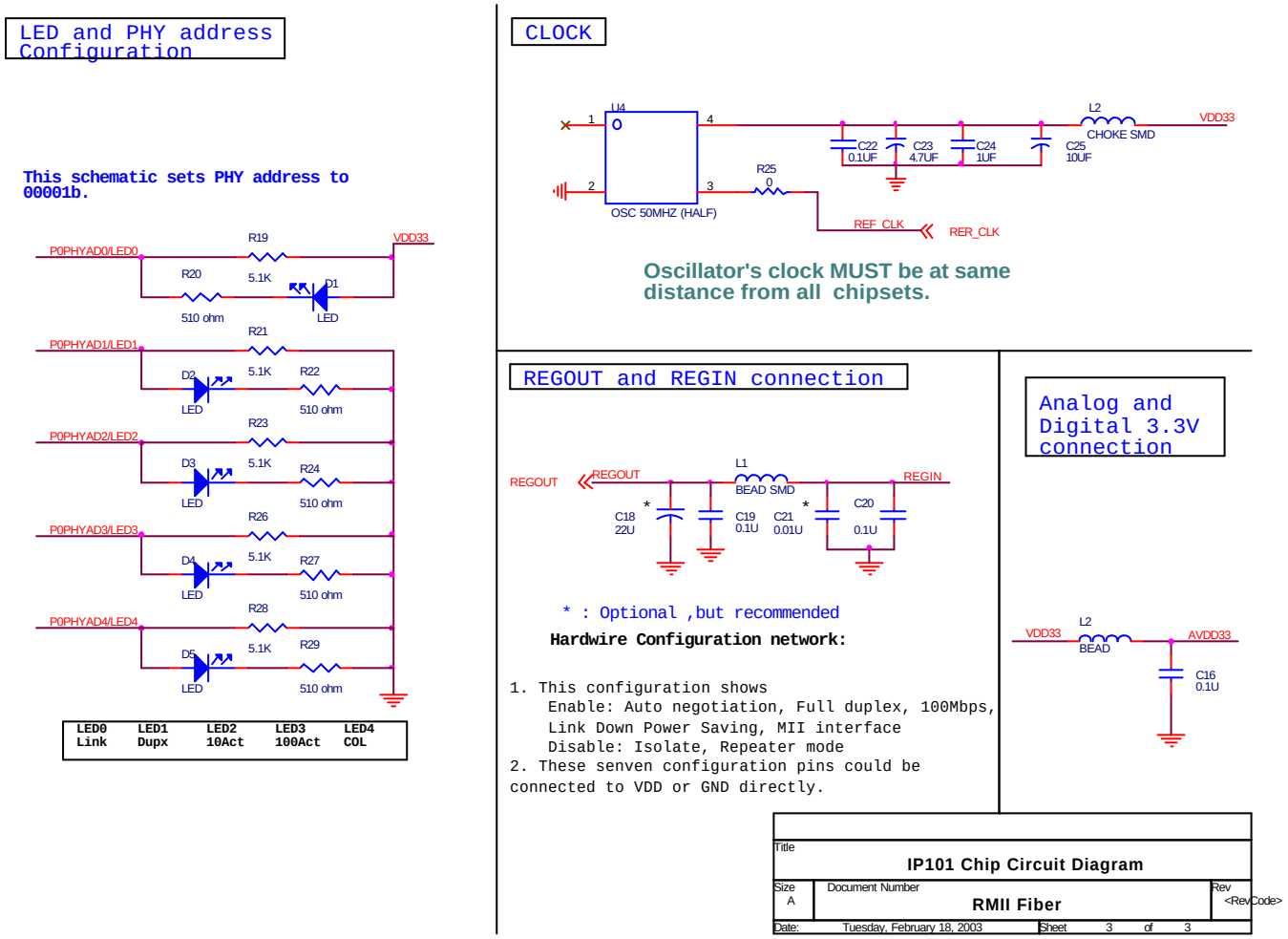
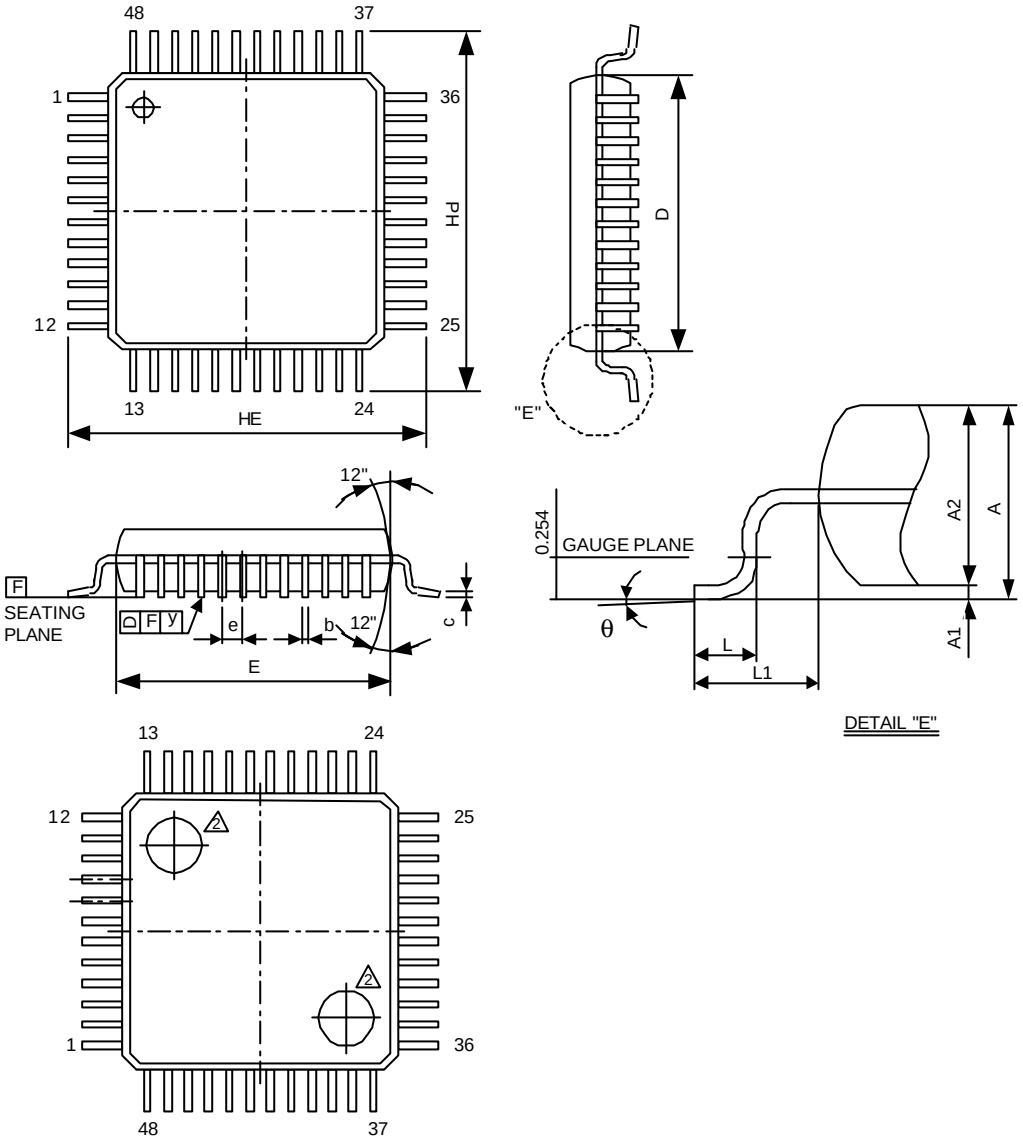
10.3 Fiber connection for both MII and RMII circuits (continued)



11.0 Order Information

Part No.	PIN	Notice
IP101	48 PIN LQFP	-

12.0 Package and Mechanical Specification



unit / Symbol	mm	inch
A	1.600MAX.	0.0630MAX.
A1	0.050~0.150	0.0020~0.0059
A2	1.400±0.05	0.0551±0.0020
b	0.200TYP	0.0078TYP
c	0.127TYP	0.0050TYP
D	7.000±0.100	0.2756±0.0039
E	7.000±0.100	0.2756±0.0039
e	0.500TYP	0.0196TYP
Hd	9.000±0.250	0.3543±0.0098
He	9.000±0.250	0.3543±0.0098
L	0.600±0.150	0.0236±0.006
L1	1.000REF	0.0393REF
y	0.100MAX.	0.0039MAX.
e	0”~7”	0”~7”

Notes:
1. DIMENSION D & E DO NOT INCLUDE MOLD FLASH OR PROTRUSION.
2. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION / INTRUSION.
3. MAX. END FLASH IS 0.15MM.
4. MAX. DAMBAR PROTRUSION IS 0.13MM.
5. GENERAL APPEARANCE SPEC SHOULD BE BASED ON FINAL VISUAL INSPECTION SPEC.

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