IC PLUS CORP.
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IP175
5 Port 10/100 Ethernet Integrated Switch

Feature

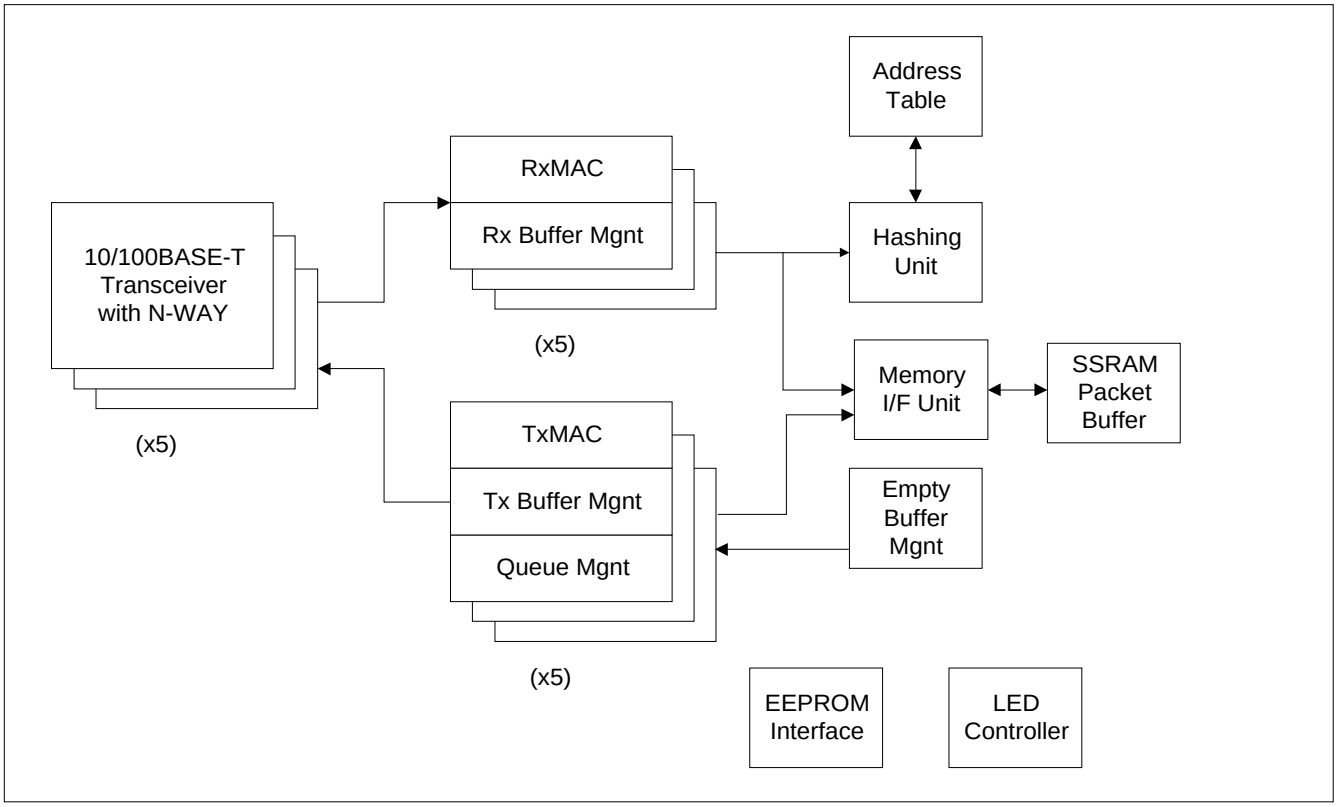
- 5 port 10/100 Ethernet switch with built in transceivers and memory
- Build in SSRAM for frame buffer
- Built in storage of 1K MAC address
- Support flow control
  - Support IEEE802.3x for flow control on full duplex mode operation
  - Support back pressure for flow control in half duplex mode operation
- A 5 port switching fabric
  - Support two-level hashing algorithm to solve address collision
  - Support address aging
  - Store and forward mode
  - Broadcast storm protection
  - Full line speed capability of 148800 (14880) packets/sec for 100M (10M)
  - Support 1536 byte data transfer for VLAN traffic
- Integrate 5 ports transceiver
  - Auto negotiation
  - Fully digital adaptive equalizer and timing recovery module
  - Base line Wander correction
  - 10BaseTX, 100BaseTX, and 100BaseFX operation
- Support one MII port for router application
- LED status of Link, activity, Full/half duplex, and speed
- LED with power on diagnostic function
- Initial parameter setting by pin configuration or EEPROM
- Utilize single clock source only (25Mhz)
- Utilize single power (2.5v)
- 0.25um technology
- Packaged in 128 pin PQFP

General Description

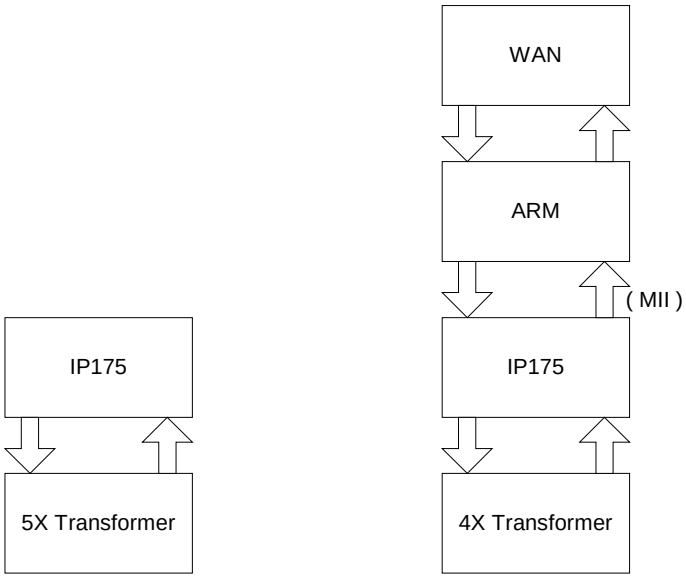
IP175 is a 5 port 10/100 Ethernet integrated switch. It consists of a 5-port switch controller and five Fast Ethernet transceivers. Each of the transceivers complies with the IEEE802.3, IEEE802.3u, and IEEE802.3x specifications. The transceivers in IP175 are designed in DSP approach with advance 0.25um technology; this results in high noise immunity and robust performance.

The IP175 operates in store and forward mode. It stores the incoming packet to the internal SSRAM and learns the SA (source address) automatically if the packet is error free. The SA is stored in the internal address table. IP175 forwards a packet according to DA destination address and address table. When the segments of destination ports are free, it reads the packet from the internal SSRAM and forwards it to the appropriate ports according to the address table. The incoming packets with errors are dropped. IP175 supports IEEE802.3x, optional backpressure, and various LED functions, etc. These functions can be configured to fit the different requirements by feeding operation parameters via EEPROM interface or pull up/down resistors on specified pins.

Block Diagram



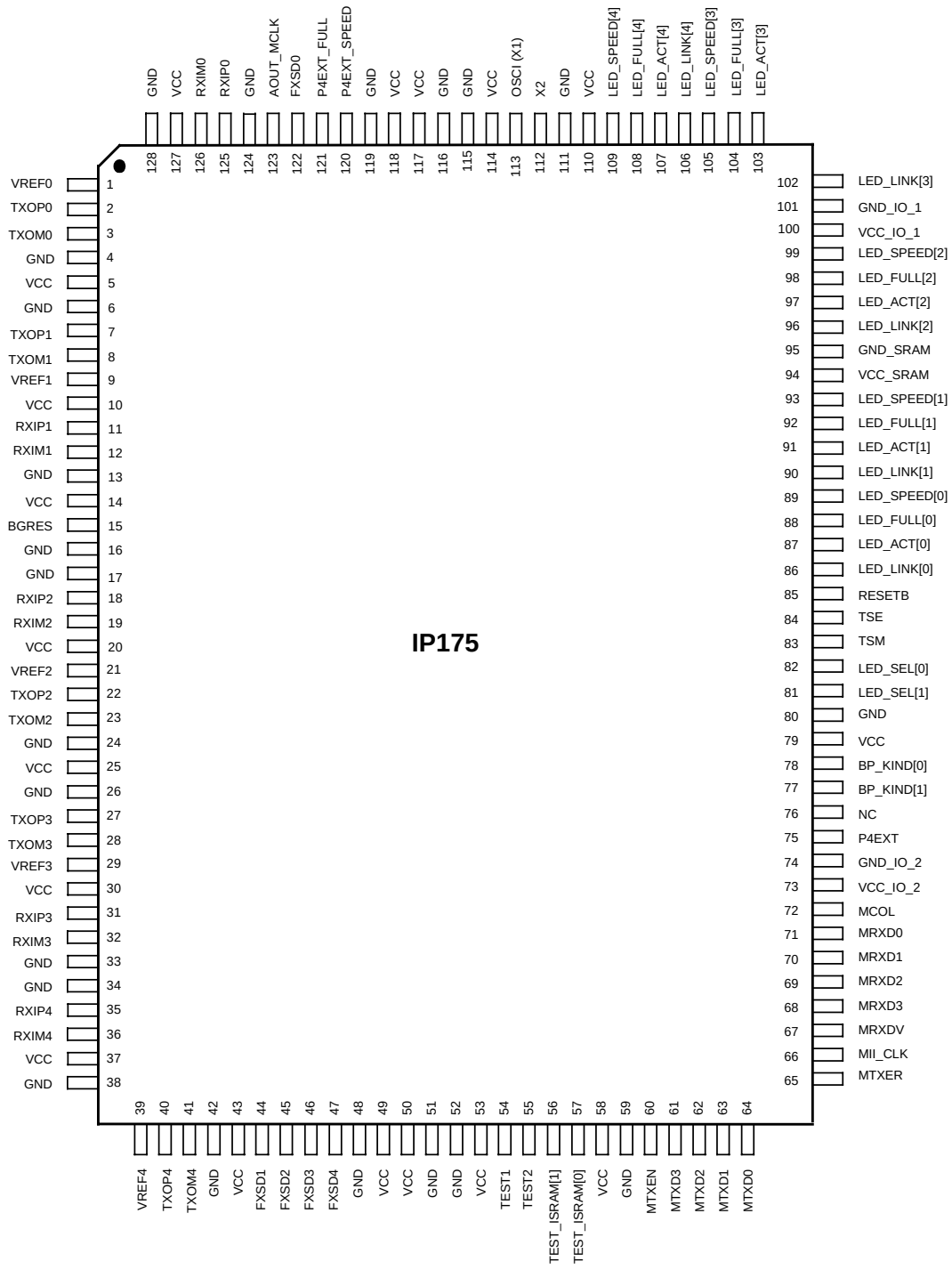
Two Applications of IP175



A 5 port SOHO Ethernet Switch port

A 4 port Ethernet Switch + One WAN

PIN Assignments



PIN Description

Type	Description
I	Used as Input pin
O	Used as Output pin
O	Used as Output with Open Drain
IPL	Input pin with pull-low resistor

Pin no.	Label	Type	Description
MLT3 Signals			
1,9,21,29,39	VREF0~4	O	**Reference voltage for transmit transformer center tap**
2,7,22,27,40, 3,8,23,28,41	TXOP0~4 TXOM0~4	O	**TP transmit**
15	BGRES	O	**Band gap resister** It is connected to GND through a 6.19k (1%) resistor in application circuit
122,44-47	FXSD0~4	I	**100Base-FX signal detect** It must be connected to ground to select TX mode.
125,11,18,31,35, 126,12,19,32,36	RXIP0~4 RXIM0~4	I	**TP receive**
LED Normal Output Mode			
81,82	LED_SEL[1:0]	IPH	**LED output mode selection** They are latched at the end of reset to select the LED output mode LED_SEL[1:0]=2'b00: LED mode 0, LED_SEL[1:0]=2'b01: LED mode 1, LED_SEL[1:0]=2'b10: LED mode 2, LED_SEL[1:0]=2'b11: LED mode 3 (default) After reset, IP175 reads EEPROM with LED_SEL[1:0], which works as EECS and EESK. These two pins are output signals during reading EEPROM. After finishing reading EEPROM, these two pins becomes input signal to isolate IP175 from EEPROM

PIN Description (continued)

Pin no.	Label	Type	Description
LED Normal Output Mode (continued)			
106,102, 96 90,86	LED_LINK[4:0]	O	**Link, Activity (output after reset)** LED mode0: Link+Activity (off: Link fail, on:Link ok and no activity, flash: Link ok and TX/RX activity) LED mode1: Receive activity (off: not receiving, flash: receiving) LED mode2: Tx/Rx Activity (off: no activity, flash: TX or RX activity) LED mode3: Link+Activity (off: Link fail, on:Link ok and no activity, flash: Link ok and TX/RX activity)
107,103,97,91,87	LED_ACT[4:0]	O	**Full/half, Collision, Tx activity (output after reset)** LED mode0: Collision (off: no collision, flash: when collision happens) LED mode1: Tx activity (1: no TX activity, flash: when TX activity happens) LED mode2, 3: Full+collision (1: half without collision, 0: full, flash: collision)
108,104,98,92,88	LED_FULL[4:0]	O	**Full/half, Link (output after reset)** LED mode0, Full/half: (off: half, on: full) LED mode1, Link: (off: Link fail, on: Link ok) LED mode2, Link: (off: Link fail, on: Link ok) LED mode3: same as mode 0
109,105,99,93,89	LED_SPEED[4:0]	O	**Speed (output after reset)** LED mode0: (off: speed=10M, on: speed=100M) LED mode1: (off: speed=10M, on: speed=100M) LED mode2: (off: speed=10M, on: speed=100M) LED mode3: (off: speed=10M, on: speed=100M)
Note: Please refer to the paragraph of “LED display” for information about Flash and ON			
LED pins used as initial setting mode during reset			
Note: Please refer to the paragraph of Initial Value Set Via Pins for detail information about pull high/ low setting.			
86	LED_LINK[0]	IPH	**IEEE 802.3X enable (X_en) on all ports** 1: enable (default), 0: disable It is internally pulled high.
92	LED_FULL[1]	IPH	**Backpressure enable (BK_EN)** 1: enable (default), 0: disable This pin doesn’t set the flow control of external MII port It is internally pulled high.

PIN Description (continued)

<table>
<tr><th>Pin no.</th><th>Label</th><th>Type</th><th>Description</th></tr>
<tr><td colspan="4">LED pins used as initial setting mode during reset (continued)</td></tr>
<tr><td>90</td><td>LED_LINK[1]</td><td>IPH</td><td>Address aging enable
1: enable, aging time 300s (default),
0: disable

It is internally pulled high.</td></tr>
<tr><td>88</td><td>LED_FULL[0]</td><td>IPL</td><td>Change capability enable (Update_r4_en)
A full duplex port will change its capability to half duplex, if the remote full duplex port does not support IEEE802.3x and this function is enabled.
1: enable, 0: disable (default)

This pin doesn’t control the flow control of external MII port.
It is internally pulled low.</td></tr>
<tr><td>98
99
102
103
104</td><td>LED_FULL[2]
LED_SPEED[2]
LED_LINK[3]
LED_ACT[3]
LED_FULL[3]</td><td>IPL</td><td>OP mode setting
It decides a port to work with nway or in force mode

force_mode = LED_FULL[2],
op1[1:0] = { LED_SPEED[2], LED_LINK[3] },
op0[1:0] = {LED_ACT [3], LED_FULL[3]}
The default value is 5’b0
They are internally pulled low.
<table>
<tr><th colspan="4">Summary</th></tr>
<tr><th>op1 [1:0]</th><th>op0 [1:0]</th><th>force_ mode</th><th>Description</th></tr>
<tr><td>0 0</td><td>x</td><td>0</td><td>Port1,3 nway with all capability</td></tr>
<tr><td>0 1</td><td>x</td><td>0</td><td>Port1,3 half duplex only</td></tr>
<tr><td>1 0</td><td>x</td><td>0</td><td>Port1,3 nway with all capability</td></tr>
<tr><td>1 1</td><td>x</td><td>0</td><td>Port1,3 nway with all capability</td></tr>
<tr><td>0 0</td><td>x</td><td>1</td><td>Port1,3 force 100M full duplex</td></tr>
<tr><td>0 1</td><td>x</td><td>1</td><td>Port1,3 force 100M half duplex</td></tr>
<tr><td>1 0</td><td>x</td><td>1</td><td>Port1,3 force 10M full duplex</td></tr>
<tr><td>1 1</td><td>x</td><td>1</td><td>Port1,3 force 10M half duplex</td></tr>
<tr><td>x</td><td>0 0</td><td>0</td><td>Port0,2,4 nway with all capability</td></tr>
<tr><td>x</td><td>0 1</td><td>0</td><td>Port0,2,4 half duplex only</td></tr>
<tr><td>x</td><td>1 0</td><td>0</td><td>Port0,2,4 nway with all capability</td></tr>
<tr><td>x</td><td>1 1</td><td>0</td><td>Port0, 2 nway, Port 4 FX</td></tr>
<tr><td>x</td><td>0 0</td><td>1</td><td>Port0,2,4 force 100M full duplex</td></tr>
<tr><td>x</td><td>0 1</td><td>1</td><td>Port0,2,4 force 100M half duplex</td></tr>
<tr><td>x</td><td>1 0</td><td>1</td><td>Port0,2,4 force 10M full duplex</td></tr>
<tr><td>x</td><td>1 1</td><td>1</td><td>Port0,2,4 force 10M half duplex</td></tr>
</table></td></tr>
<tr><td></td><td></td><td></td><td></td></tr>
</table>

PIN Description (continued)

Pin no.	Label	Type	Description
LED pins used as initial setting mode during reset (continued)			
77,78	BP_KIND[1:0]	IPL	**Backpressure type selection** Bp_kind[1:0] are valid only if Bk_en is set to high. 00: carrier base backpressure (default) 01: collision base backpressure with hashing 10: collision base backpressure without hashing After reset, IP175 reads EEPROM with BP_KIND[1:0], which works as EEDO and EEDI. BP_KIND[1] is an input signal and BP_KIND[0] is an output signal during reading EEPROM. After finishing reading EEPROM, these two pins becomes input signal to isolate IP175 from EEPROM They are internally pulled low.
105	LED_SPEED[3]	IPH	**Turn on twopartD (Twopart)** IP175 examine the carrier for 64 bits only during its back off period if this function is enabled. It makes IP175 have higher priority in a collision event. 1: enable (default), 0: disable It is internally pulled high.
93	LED_SPEED[1]	IPH	**Aggressive back off enable (MODBCK)** IP175 uses modified (aggressive) back off algorithm if this function is enabled. The maximum back off period is limited to 8-slot time. It makes IP175 have higher priority in a collision event. 1: aggressive mode enable (default), 0: standard back off This pin doesn't affect the external MII port. It is internally pulled high.
106	LED_LINK[4]	IPL	**Bypass scrambler (BPSCR_MODE)** 1: bypass, 0: not bypass (default) The default value must be adopted for normal operation. It is internally pulled low.
96	LED_LINK[2]	IPH	**Nodrop16 (Drop16*)** 1: do not drop after 16 collisions, (default) 0: drop after 16 collision This pin doesn't affect the external MII port. It is internally pulled high.

PIN Description (continued)

Pin no.	Label	Type	Description
LED pins used as initial setting mode during reset (continued)			
97	LED_ACT[2]	IPL	**Broadcast storm protection enable (BF_STM_EN)** 1: enable, 0: disable (default) It is internally pulled low.
108	LED_FULL[4]	IPL	**FIBER_HALF** 1: all fiber port works at half duplex, 0: all fiber port works at full duplex (default) It is internally pulled low.
External MII control signals			
75	P4EXT	I	**Port4 external MII enable** 1: IP175 works as a 4-TP + 1 MII port switch MII interface is enabled and is connected to external MAC device. The MAC data is fed to port4 MII interface of switch core directly and bypass the internal port4 transceiver 0: IP175 works as a 5-TP port switch If external MII is enabled, IP175 generates MCOL to external MAC device when both MRXDV and MTXEN are active and P4EXT_FULL is set to logic low.
120	P4EXT_SPEED	IPL	**Port4 external MII interface speed selection** 1: 10M 0: 100M (default) It is valid only if P4EXT is set to logic high.
121	P4EXT_FULL	IPL	**Port4 external MII interface full/half duplex selection** 0: half (default) 1: full It is valid only if P4EXT is set to logic high.
87	LED_ACT[0]	IPL	**MII_FC_EN, Flow control enable for MII port** 1: enable, 0: disable (default)
89	LED_SPEED[0]	IPH	**UTPdet** It is a power saving mode for TP port. TP port will be power down when the cable is unplugged and the function is enabled. 1: enable (default), 0: disable It is internally pulled high.

PIN Description (continued)

Pin no.	Label	Type	Description
Test Pin			
54,55	TEST1, TEST2	IPL	**Test mode selection** They are internally pulled low. They are recommended to be connected to GND for normal operation
56,57	TEST_ISRAM[1:0]	IPL	**Test internal SRAM** It is valid to test internal SRAM only if both TEST1 and TEST0 are set to logic high. They are internally pulled low.
83	TSM	I	**Scan mode** It is connected to GND in application circuit.
84	TSE	I	**Scan enable** It is connected to GND in application circuit.
123	AOUT_MCLK	IPL	**It is used as scan clock.** It is left open in application circuit.
Misc.			
85	RESETB	I	**Reset, low active**
112	X2	O	**Crystal pin**
113	OSCI(X1)	I	**25M system clock input**

PIN Description (continued)

Pin no.	Label	Type	Description
External MII interface			
60	MTXEN	I	MTXEN is used to frame NRZ data from external MII device
61-64	MTXD[3:0]	I	MTXD is NRZ data from external MAC controller
65	MTXER	I	**MTXER is transmit error**
66	MII_CLK	O	**MII_CLK is MII interface clock** It is the MIITxclk of switch core and is used as MIITxclk and MIIRxclk for the external MAC device
67	MRXDV	O	MRXDV is used to frame MRXD, which is sent to external MAC device
68-71	MRXD[3:0]	O	MRXD is NRZ data to external MAC device
72	MCOL	O	MCOL is active, only if both MRXDV and MTXEN are both active and the MII interface is set to be half-duplex
Power			
5,25,43	VCC	I	**Tx VCC of Analog circuit** It is connected to 2.5v.
10,20,30,37,127	VCC	I	**Rx VCC of Analog circuit** It is connected to 2.5v.
14	VCC	I	**Band gap VCC of Analog circuit** It is connected to 2.5v.
49,50,53,58,79, 110,117,118	VCC	I	**VCC of digital core** It is connected to 2.5v.
114	VCC	I	**VCC of crystal** It is connected to 2.5v.
73	VCC_IO_2	I	**VCC of digital I/O buffer** It is connected to 2.5v for a dumb switch. It should be connected to 3.3v if external MII interface is active.
94	VCC_SRAM	I	**VCC of SRAM** It is connected to 2.5v.
100	VCC_IO_1	I	**VCC of digital I/O buffer** It is connected to 2.5v for a dumb switch. It should be connected to 3.3v if external MII interface is active.
4,6,24,26,42	GND	I	**Tx GND of Analog circuit**
13,17,33,34,38,12 4,128	GND	I	**Rx GND of Analog circuit**
16	GND	I	**Band gap GND of Analog circuit**
48,51,52,59,80,11 5, 116,119	GND	I	**GND of digital core**
111	GND	I	**GND of crystal**
74	GND_IO_2	I	**GND of digital I/O buffer**
95	GND_SRAM	I	**GND of SRAM**
101	GND_IO_1	I	**GND of digital I/O buffer**

PIN Description (continued)

A Summary of Multi-Function Pins

Pin no.	Label	Default	PCB	Normal
121	P4EXT_FULL	0	R1/0	P4EXT_FULL
120	P4EXT_SPEED	0	R1/0	P4EXT_SPEED
77	BP_KIND[1]	0	0	EEDO
78	BP_KIND[0]	0	0	EEDI
81	LED_SEL[1]	1		EECS
82	LED_SEL[0]	1		EESK
89	LED_SPEED[0]	1	R0	UTPDET
88	LED_FULL [0]	0	R0	UPDATE_R4_EN
87	LED_ACT[0]	0		MII_FC_EN
86	LED_LINK[0]	1	R1	X_EN
93	LED_SPEED[1]	1	R1	MODBCK
92	LED_FULL[1]	1	R1	BK_EN
91	LED_ACT[1]	0		
90	LED_LINK[1]	1	R1	AGING
99	LED_SPEED[2]	0		OP1[1]
98	LED_FULL[2]	0		FORCE_MODE
97	LED_ACT[2]	0		BF_STM_EN
96	LED_LINK[2]	1		NODROP16
105	LED_SPEED[3]	1		TWOPART
104	LED_FULL[3]	0		OP0[0]
103	LED_ACT[3]	0		OP0[1]
102	LED_LINK[3]	0		OP1[0]
109	LED_SPEED[4]	0		NA
108	LED_FULL[4]	0		FIBER_HALF
107	LED_ACT [4]	0		
106	LED_LINK[4]	0		BPSCR
72	MCOL			
71	MRXD0			
70	MRXD1			
69	MRXD2			
68	MRXD3			
67	MRXDV			
123	AOUT_MCLK			
65	MTXER		0	
64	MTXD0		0	
63	MTXD1		0	
62	MTXD2		0	
61	MTXD3		0	
60	MTXEN		0	
75	P4EXT		0	
76	NC		0	
56	TSET_ISRAM1	-	R0	

Functional Description

Basic Operation

IP175 consists of five switching ports. Full/half duplex and speed of each port depends on the result of auto negotiation of its corresponding transceiver. It is not necessary to use an external memory to buffer packets.

Each port of IP175 has its own receive buffer management, transmit buffer management, transmit queue management, transmit MAC and receive MAC. All ports share a hashing unit, a memory interface unit, an empty buffer management, and an address table.

An incoming packet is stored in the internal memory if the packet is error free. A packet is error free if its CRC field is correct and its length is between 64 and 1536 byte. At the same time, IP175 examines the address field of the packet. By the way, switch learns the locations of every station (source address) and records them on the address table. IP175 then reads the packet from the internal memory and sends it to the appropriate ports according to the address table. Eventually, IP175 supports the switching function by dropping or forwarding the incoming packets.

Block Description

The basic function of each block in the block diagram is illustrated in the following context. Hashing unit is responsible to learn and to recognize address. Transmit buffer management and receive buffer management are responsible to store data to or to read data from the internal memory through memory interface unit. Transmit MAC and receive MAC interface to transceivers and implement Ethernet protocol.

Receive MAC receives the incoming data from transceiver and converts nibble data into double word data. As a 32 bit data is ready, it feeds the data into receive FIFO and requests receive buffer management for data transfer. When receive buffer management receives the request, it gets a empty block from empty buffer management and writes the double word data to the buffer, which is located in the internal SSRAM, through memory interface unit. The incoming packet is fed to hashing unit at the same time. Hashing unit extracts the source address of incoming packet to set up an address table. An incoming packet is dropped or forwarded according to the table. The address table is built in the SSRAM of IP175.

All ports share an empty buffer management. After reset, the empty buffer management provides 5 addresses of empty blocks. When a packet comes in, it searches for a new empty block. After a packet is forwarded, the corresponding blocks are released. Empty buffer management treats the block as an empty block and provides its address to desired receive buffer management. Five addresses are always ready for receive buffer management.

Back off Algorithm

IP175 provides three parameters to modify its back off algorithm. They are Modbck, Twopart and NoDrop16. IP175 implements the IEEE802.3 standard binary exponential back off algorithm (Modbck=0) and modified back off algorithm (Modbck=1) when it works at half duplex mode. If Modbck is set, the maximum back off time is limited to eight-slot time. The minimum defer time is separated into the two periods. The first period consists of the first 64-bit time and the 2nd period consists of the rest 32 bit-time. In the case of minimum defer time IP175 transmits a packet after 96-bit time immediately in spite of the status of cable on the 2nd period if Twopart is set. After 16 consecutive collisions, the transmitting packet is dropped if NoDrop16 is reset.

Operation Parameter

IP175 supports many optional functions. They can be configured to fit different requirements by setting appropriate parameters. These parameters can be fed into IP175 through EEPROM interface or through pins.

Flow Control

IP175 provides two mode of flow control. Backpressure is for half duplex mode and IEEE802.3x flow control is for full duplex.

Backpressure

The backpressure is used for flow control in half duplex mode if Bk_en is turned on. When the buffer of a port is full, it will start to send jam signals. The remote station will defer transmission after detecting the jam signals. IP175 support two types of backpresure, collision base (Bp_kind =2'b10) and carrier base (Bp_kind=2'b00).

Collision based backpressure is sent by IP175, only when the buffer of a port is full and it receives a packet. IP175 stops sending backpressure packet when the remote station is idle. The definition of buffer full for collision base backpressure is there is no empty buffer for incoming packets.

Carrier based backpressure is sent by IP175, when the buffer of a port is full. IP175 sends jam packets continuously to defer the remote station. The length of jam packet is 1518 byte and the IPG is equal to 96-bit time. If the port has packets to transmit during this period, it transmits the queuing packet instead of the jam packets. After the queuing packets are transmitted, IP175 resumes to jam the segment by sending jam packets if the buffer of a port is full. If a collision occurs, the back off algorithm is skipped and the jam packets are generated immediately. The definition of buffer full for carrier base backpressure is there is only one empty buffer for a port.

IEEE 802.3x

The IEEE 802.3x is used for flow control in full duplex mode if both IP175 (X_en=1) and the remote station have IEEE802.3x capability. When the level of occupied buffer of a port is over set threshold, it will send a PAUSE frame with maximum delay FFFF. The remote station will stop to transmit the next packet after receiving the PAUSE frame. After level of the occupied buffer is below release threshold, the port sends out a PAUSE frame with zero delay to resume receiving the incoming packets. The remote station is re-enable to transmit packets after receiving the PAUSE frame with zero delay. While level of the occupied buffer of a port is over set threshold, IP175 re-transmits the PAUSE frame with maximum delay to ensure the pause timer of the remote station does not expire and begins transmission. The IPG between PAUSE frames is 42ms(100M) or 420ms(10M).

When an incoming PAUSE frame with non-zero delay is received, the port stops the next frame transmission and starts its pause timer. It is re-enabled transmission function either the pause timer is expired or a PAUSE frame with zero delay is received. If another pause frame is received before the timer expires, the timer will be updated with the new value. During this period, only PAUSE frame from IP175 will be transmitted.

PAUSE Frame Format

Destination	Source	Type	Opcode	Pause Timer	Pad	CRC
01-80-C2-00-00-01	SA	8808	0001	FFFF(0000)	PAD with zero	CRC
6 bytes	6 bytes	2 bytes	2bytes	2 bytes	42 bytes	4 bytes

Capability Changing

If the remote station does not support IEEE802.3x and has full duplex capability, IP175 supports a private mechanism to handle flow control to prevent packet loss. It is called capability changing and is controlled by the parameter Update_r4_en.

When the remote station does not support IEEE802.3x and has full duplex capability and Update_r4_en is turned on, the port changes its ability to half duplex to make the remote station link at half duplex after Nway. IP175 handles the data flow of segment by backpressure. To do this, the port keeps silence to force the remote node link failure and changes its capability to half duplex then restarts Nway. Both side of the segment will be link at half duplex.

When the remote station does not support IEEE802.3x and has full duplex capability and Update_r4_en is turned off, the port turns off its IEEE802.3x capability and is link at full duplex after Nway. There is no flow control between these two nodes in this application. The detail operation is illustrated in the following table.

Conditions						Result			
X_EN	REMOTE_IEEE 802.3X	UPDATE_ R4_E	BK_EN	Remote site	My site	Remote site	My site	My 802.3x	My back pressure
x	x	x	0	half	X	half	half	off	off
x	x	x	1	half	X	half	half	off	on
1	1	0	x	full/half	full/half	full	full	on	off
0	1	0	x	full/half	full/half	full	full	off	off
1	0	0	x	full/half	full/half	full	full	off	off
0	0	0	x	full/half	full/half	full	full	off	off
1	1	1	x	full/half	full/half	full	full	on	off
0	1	1	x	full/half	full/half	half	half	off	on
1	0	1	x	full/half	full/half	half	half	off	on
0	0	1	x	full/half	full/half	half	half	off	on

Aging

IP175 support address aging and buffer aging. If the address aging is enabled, the learned SA will be cleared if it is not refreshed within the aging time (300 seconds). The aging time is not adjustable in IP175.

Broadcast Storm Protection

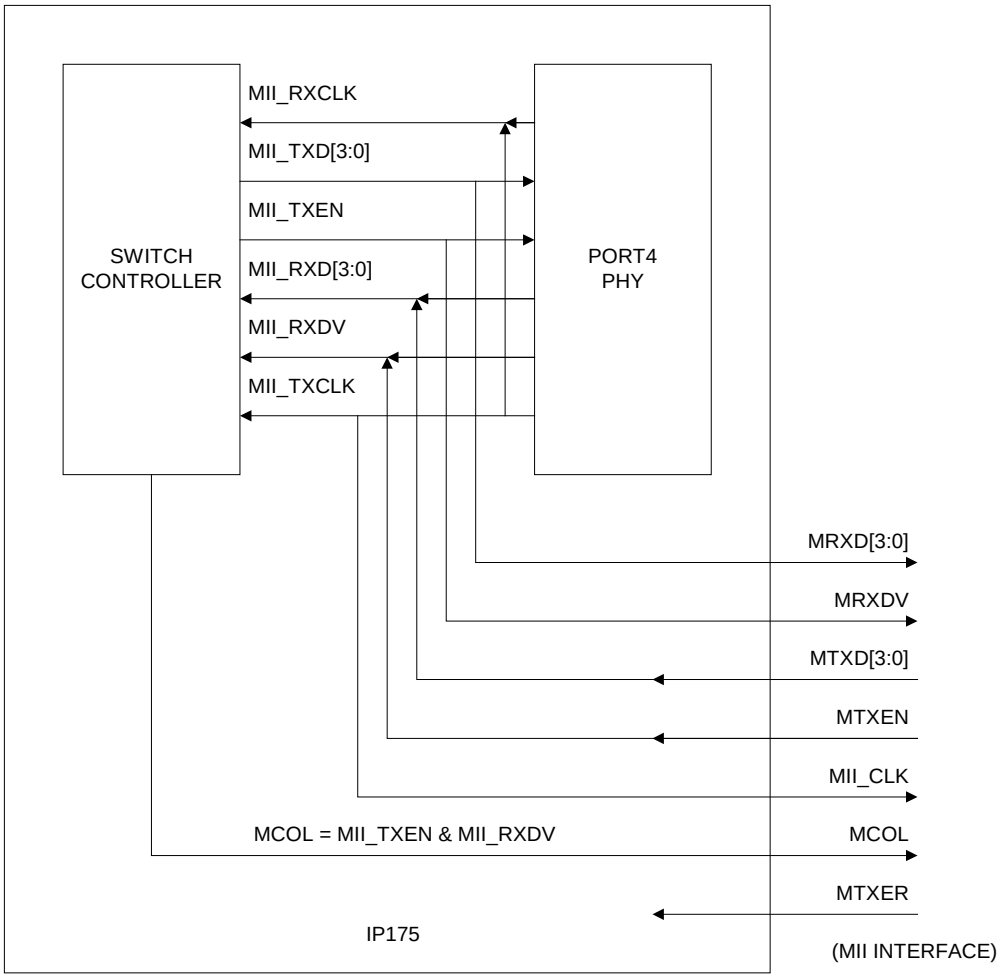
IP175 is able to prevent receiving too many broadcast packets to waste the switch resource. IP175 discards the incoming broadcast packets depending on the setting of Bf_stm_en if the number of broadcast packets from a port exceeds threshold. The threshold can be set by writing Bq_hwm_0_sel[1:0] in EEPROM register.

MII port

IP175 supports one MII port. When the interface is active, the transceiver of port4 is disabled and the switch core interfaces the MII interface directly. This makes IP175 can behave like a Fast Ethernet transceiver.

The major difference between the IP175 MII and IEEE standard MII are clock and RXER signal. There is only one clock and there is no RXER signal on the interface. For half duplex operation, MCOL is used as a collision during transmission. The following diagram shows the interface in the IP175.

Pin 73 (VCC_IO_2) and pin 100 (VCC_IO_1) should be connected to 3.3v in this application.



A System Block of Mac Interface

Power on Diagnostic of LED

(Link, Act, Fdx and Speed LED are all the same during this period)

(0) T = 0 sec

(1) T = 0.25 sec

(2) T = 0.50 sec

(3) T = 0.75 sec

(4) T = 1.00 sec

(5) T = 1.25 sec

(6) T = 1.50 sec

(7) T = 1.75 sec

(8) T = 2.00 sec

(9) T = 2.25 sec

(10) After T = 2.5 sec, LED becomes normal operation

LED_SPEED
LED_FULL
LED_ACT
LED_LINK

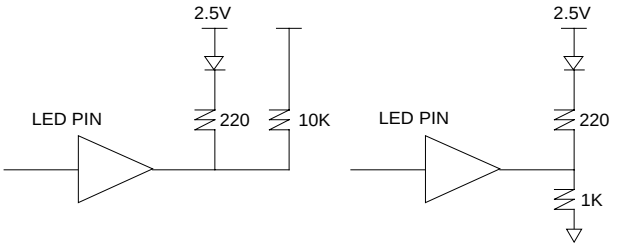
LED and Initial Value Setting

IP175 supports two ways to modify its initial values of operation parameters to fit different applications. It read the initial value via pins or EPROM interface.

Initial Value Set Via Pins

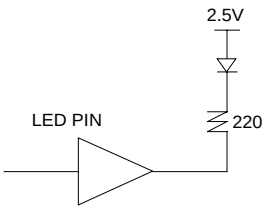
To set the parameter via pins, connect them to vcc or ground through resistors. IP175 reads initial value via pins during the period of reset. An initial value is set to 1'b1 (1'b0) by connecting a pin to vcc (gnd) through a 10kΩ (1kΩ) resistor as shown on the following figure. The function begins after the internal PLL clock active. To make sure the proper operation of PLL, the duration of reset must be no less than 1 ms. If there is no setting resistor, IP175 uses the default value.

IP175 reads initial setting via pins during the period of reset. At reset, these pins are input signals and IP175 reads the initial value. After reset, LED pins become output signals and show LED functions at normal mode. The application circuit is shown below.



To set initial value = 1
with pull up 10K ohm resister

To set initial value = 0
with pull down 1K ohm resister



To use default value
(use no resistor to leave it open)

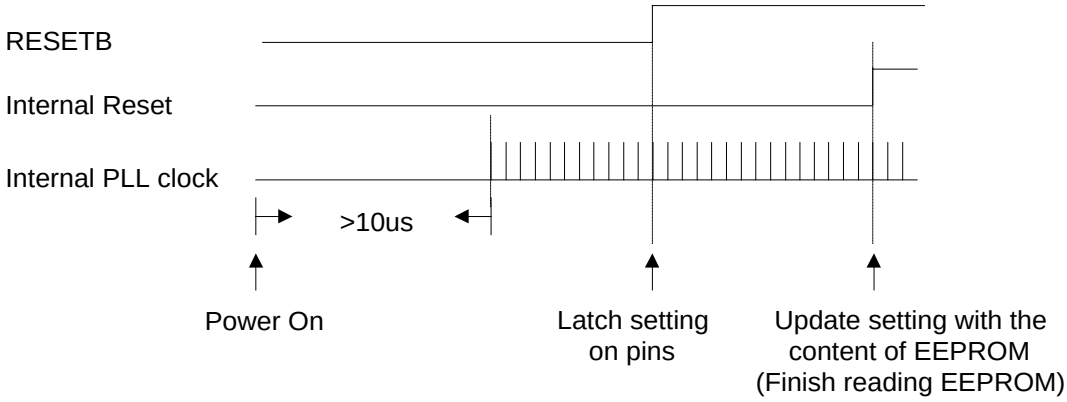
EEPROM Interface

During reset, IP175 sets the default value for each bit. After reset, IP175 latches the setting on pins at the end of reset and begins to read the content in the EEPROM. The data in EEPROM is valid only if there is a specific pattern 55AA read in the register 0. If there is no EEPROM, IP175 keeps the value read from resistors setting. IP175 is still in reset state before finishing EEPROM reading.

IP175 will stop reading the content of an EEPROM if there is no specific pattern 55AA read in the register 0. After IP175 read the EEPROM, the EEPROM pins (BP_KIND and LED_SEL) are kept in input mode.

All fields in EEPROM corresponding to the registers of IP175 should be filled with correct value if an EEPROM is used. Because the default value in IP175 will be replaced with the content in EEPROM if it is valid.

IP175 uses a 93C46 EEPROM device. The detail operation is illustrated in the following figure.



EEPROM Register Description

Offset	Default Value	Corresponding Pin	Description
00H[15:0]	55AA	-	**EEEPROM enable register** This register should be filled with 55AA. IP175 will check the specified pattern to confirm a valid EEPROM exists. The initial setting is updated after power on reset only if the specified pattern 55AA is found.
LED output selection register			
01H[15:2]	14'b0	-	**Reserved**
01H[1:0]	11	LED_SEL[1:0]	**LED_SEL, LED mode selection** LED_SEL[1:0]=2'b00: LED mode 0, LED_SEL[1:0]=2'b01: LED mode 1, LED_SEL[1:0]=2'b10: LED mode 2, LED_SEL[1:0]=2'b11: LED mode 3 Please refer to pin description for detail LED definition.
Switch control register 1			
02H[15:13]	3'b0	-	**Reserved**
02H[12:11]	00	BP_KIND[1:0]	**BP_KIND, Backpressure type selection** It is valid only if Bk_en (02H[4]) is set to 1'b1. 00: carrier base backpressure 01: collision base backpressure with hashing 10: collision base backpressure without hashing
02H[10]	0	-	**Reserved**
02H[8]	0	-	**Reserved**
02H[7]	1	X_EN (LED_LINK[0])	**X_EN, IEEE 802.3x flow control enable** 1: enable 0:disable
02H[6:5]	2'b0	-	**Reserved**
02H[4]	1	BK_EN (LED_FULL[1])	**BK_EN, Backpressure enable** 1: enable, 0: disable
02H[3]	0	(LED_ACT[0])	**MII_FC_EN, External MII port flow control enable** 1: enable, 0:disable
02H[2]	0	BF_STM_EN (LED_ACT[2])	**Broadcast storm enable** 1: enable Drop the incoming packet if the number of queued broadcast packet is over the threshold. The threshold is defined in register 0AH[14:13]. 0: disable
02H[1:0]	2'b0	-	**Reserved**

EEPROM Register Description (continued)

Offset	Default Value	Corresponding Pin	Description
Switch control register 2			
03H[15:10]	6'b0	-	**Reserved**
03H[8]	0	-	**Reserved**
03H[7]	1	Nodrop16 (LED_LINK[2])	**No drop16,** A port will drop the transmitting packet after 16 consecutive collisions if this function is turned on. 1: do not drop 0: drop
03H[4]	1	AGETIME (LED_LINK[2])	**AGETIME, enable aging of address table** An address tag in hashing table will be dropped if this function is turned on and its aging timer expires (300 seconds).
03H[2]	1	TWOPART (LED_SPEED[3])	**TWOPART, Turn on twopartD** IP175 examine the carrier for 64 bits only during its back off period if this function is enabled. It makes IP175 have higher priority in a collision event. 1: turn on 0: turn off
03H[1]	1	MODBCK (LED_SPEED[1])	**MODBCK, Turn on modified back off algorithm** IP175 uses modified (aggressive) back off algorithm if this function is enabled. The maximum back off period is limited to 8-slot time. It makes IP175 have higher priority in a collision event. 1: turn on 0: turn off
03H[0]	0	-	**Reserved**

EEPROM Register Description (continued)

Offset	Default Value	Corresponding Pin	Description
Transceiver control register			
04H[15:14]	00	**OP1[1:0]** (LED_SPEED[2]) (LED_LINK[3])	**OP1,** Bit[15:14] are corresponding to op1[1:0]. The default value must be adopted for normal operation.
04H[13:11]	000	OP0[1:0], FORCE_ MODE (LED_ACT[3]) (LED_FULL[3]) (LED_FULL[2])	**OP0 and FORCE_MODE,** Bit[13:11] are corresponding to op0[1:0] and force_mode. The default value must be adopted for normal operation.
Summary			

04H[15:11]	OP1[1:0]	OP0[1:0]	FORCE_MODE	Description
	0 0	x	0	Port1, 3 nway with all capability
	0 1	x	0	Port1, 3 half duplex only
	1 0	x	0	Port1, 3 nway with all capability
	1 1	x	0	Port1, 3 nway with all capability
	0 0	x	1	Port1, 3 force 100M full duplex
	0 1	x	1	Port1, 3 force 100M half duplex
	1 0	x	1	Port1, 3 force 10M full duplex
	1 1	x	1	Port1, 3 force 10M half duplex
	x	0 0	0	Port0, 2, 4 nway with all capability
	x	0 1	0	Port0, 2, 4 half duplex only
	x	1 0	0	Port0, 2, 4 nway with all capability
	x	1 1	0	Port0, 2 nway with all capability, Port 4 FX
	x	0 0	1	Port0, 2, 4 force 100M full duplex
	x	0 1	1	Port0, 2, 4 force 100M half duplex
	x	1 0	1	Port0, 2, 4 force 10M full duplex
	x	1 1	1	Port0, 2, 4 force 10M half duplex

04H[9]	1	-	The default value must be adopted for normal operation.
04H[8]	0	-	The default value must be adopted for normal operation.
04H[7:0]	0000 0000	-	The default value must be adopted for normal operation.

EEPROM Register Description (continued)

Offset	Default Value	Corresponding Pin	Description
Transceiver verification register			
05H[15:14]	2'b0	-	**Reserved**
05H[13]	0	-	The default value must be adopted for normal operation.
05H[12]	0	UPDATE_R4_EN (LED_FULL[0])	**UPDATE_R4_EN, Change capability enable** A full duplex port will change its capability to half duplex, if the remote full duplex port does not support 802.3x and this function is enable. 1: enable 0: disable
05H[11]	0	-	The default value must be adopted for normal operation.
05H[10]	0	-	The default value must be adopted for normal operation.
05H[9]	0	-	The default value must be adopted for normal operation.
05H[8]	0	-	The default value must be adopted for normal operation.
05H[7:6]	00	-	The default value must be adopted for normal operation.
05H[5]	0	-	The default value must be adopted for normal operation.
05H[4]	0	-	The default value must be adopted for normal operation.
05H[3]	0	-	The default value must be adopted for normal operation.
05H[2]	0	-	
05H[1]	0	BPSCR (LED_LINK[4])	**BYSCR_MODE, Bypass scrambler** 1: bypass 0: not bypass The default value must be adopted for normal operation.
05H[0]	0	-	The default value must be adopted for normal operation.
Testing & verify mode register			
06H[15:7]	9'b0	-	**Reserved**
06H[6]	0	-	The default value must be adopted for normal operation.
06H[5:0]	6'b0	-	The default value must be adopted for normal operation.
07H[15:14]	2'b0	-	The default value must be adopted for normal operation.
07H[13:10]	4'b0	-	**Reserved**
07H[7:0]	8'h77	-	**MAX_USE_THR, Input queue threshold** An incoming packet will be dropped if the number of packet queued in a port is over the input queue threshold. This function is always active in spite of if there is flow control or not. It is usually higher than the threshold for flow control. It is recommended to adopt the default value.
08H[15]	0	-	**Reserved**
08H[14:8]	7'h30	-	**BCKP_THR_RLS, Backpressure off threshold**
08H[7]	0	-	**Reserved**
08H[6:0]	7'h60	-	**BCKP_THR, Backpressure on threshold**
09H[15]	0	-	**Reserved**
09H[14:8]	7'h30	-	**X802_3_THR_RLS, 802.3x off threshold**
09H[7]	0	-	**Reserved**
09H[6:0]	7'h50	-	**X802_3_THR, 802.3x on threshold**

EEPROM Register Description (continued)

Offset	Default Value	Corresponding Pin	Description
Testing & verify mode register (continued)			
0AH[15]	0	-	**Reserved**

0AH[14:13]	11	-	**BQ_HWM_0_SEL**,
			Broadcast Queue high water mark threshold selection. IP175 will drop the incoming broadcast packet if the broadcast packet count exceeds the threshold.
			If (register 02H[2]: bf_stm_en==1), its corresponding threshold is 00:1024, 01:256, 10:128, 11:48,
			
			If (register 02H[2]: bf_stm_en==0), the function is disabled.

0AH[12:11]	2'b0	-	**Reserved**
0AH[10:0]	11'd128	-	**OQ_THR, Output Queue threshold** An incoming packet will be dropped if the number of packet queued in destination port is over the output queue threshold. IP175 enables this function automatically only if there is no flow control.
0BH[14:10]	5'b0	-	The default value must be adopted for normal operation.
0BH[9:5]	5'b0	-	The default value must be adopted for normal operation.
0BH[4:0]	5'b0	-	The default value must be adopted for normal operation.
NA	0	-	The default value must be adopted for normal operation.
NA	0	-	The default value must be adopted for normal operation.

A summary of EEPROM Registers and Their Corresponding Pins

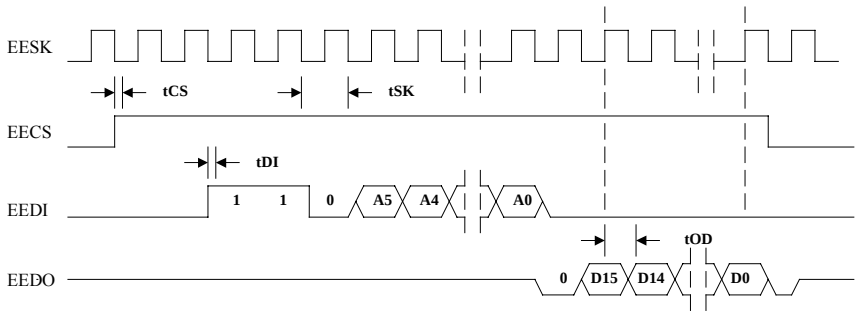
Offset	Default Value	Corresponding Pin	Normal	Register Content
00H[15:0]	55AA	-	-	PROM ENABLE
01H[1:0]	11	LED_SEL		LED_SEL
02H[12:11]	00	BP_KIND		BP_KINK
02H[7]	1	LED_LINK[0]	X_EN	X_EN
02H[4]	1	LED_FULL[1]	BK_EN	BK_EN
02H[3]	0	LED_ACT[0]	MII_FC_EN	MII_FC_EN
02H[2]	0	LED_ACT[2]	BF_STM_EN	BF_STM_EN
03H[7]	1	LED_LINK[2]	NODROP16	NO DROP16
03H[4]	1	LED_LINK[1]	AGING	AGETIME
03H[2]	1	LED_SPEED[3]	TWOPART	TWOPART
03H[1]	1	LED_SPEED[1]	MODBCK	MODBCK
04H[15]	0	LED_SPEED[2]	OP1[1]	OP1[1]
04H[14]	0	LED_LINK[3]	OP1[0]	OP1[0]
04H[13]	0	LED_ACT[3]	OP0[1]	OP0[1]
04H[12]	0	LED_FULL[3]	OP0[0]	OP0[0]
04H[11]	0	LED_FULL[2]	FORCE_ MODE	FORCE_ MODE
04H[10]	0	LED_FULL[4]	FIBER_HALF	FIBER_HALF
04H[9]	1	-	-	
04H[8]	0	-	-	
04H[7:0]	8'b0	-	-	
05H[13]	0	BP_KIND[1]		
05H[12]	0	LED_FULL[0]	UPDATE_R4_EN	UPDATE_R4_EN
05H[11]	0	AOUT_MCLK		
05H[10]	0	MTXER		
05H[9]	0	MTXD0		
05H[8]	0	BP_KIND[0]		
05H[7:6]	11	LED_SEL		
05H[5]	0	MTXD1		
05H[4]	0	MRXDV		
05H[3]	0	LED_SPEED[0]		
05H[2]	0	-	-	
05H[1]	0	LED_LINK[4]	BPSCR	BYSCR_MODE
05H[0]	0	LED_ACT[4]		
06H[6]	0	LED_ACT[1]		
06H[5]	0	MCOL		
06H[4]	0	MRXD0		
06H[3]	0	MTXD3		
06H[2]	0	MTXEN		
06H[1]	0	MRXD2		
06H[0]	0	MTXD2		

A summary of EEPROM Registers and Their Corresponding Pins (continued)

Offset	Default Value	Corresponding Pin	Normal	Register Content
07H[15:14]	2'b0	-	-	
07H[7:0]	8'h77	-	-	MAX_USE_THR
08H[14:8]	7'h30	-	-	BCKP_THR_RLS
08H[6:0]	7'h60	-	-	BCKP_THR
09H[14:8]	7'h30	-	-	X802_3_THR_RLS
09H[6:0]	7'h50	-	-	X802_3_THR
0AH[14:13]	11	-	-	BQ_HWM_0_SEL
0AH[10:0]	11'd128	-	-	OQ_THR
0BH[14:10]	5'b0	-	-	
0BH[9:5]	5'b0	-	-	
0BH[4:0]	5'b0	-	-	
0CH[15]	0	-	-	
0CH[14]	0	-	-	
0CH[11:10]	00	-	-	
0DH[15]	0	-	-	
0DH[14]	0	-	-	
0DH[13]	0	-	-	
0DH[12]	0	-	-	
0DH[11]	0	-	-	
0DH[10]	0	-	-	
0DH[7]	0	-	-	
0DH[6]	0	-	-	
0DH[5]	0	-	-	
0DH[4]	0	-	-	
0DH[3]	0	-	-	
0DH[2]	0	-	-	
0DH[1]	0	-	-	
0DH[0]	0	-	-	
NA	0	MRXD3		
NA	0	MRXD1		

AC Characteristic

Read EEPROM



Parameter	Description	Min	Typical	Max	Units
TSK	Clock period		5.12		us
TCS	Chip select delay			2	ns
TDI	Data input delay			2	ns
TOD	Output delay			2000	ns

Absolute Maximum Rating

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. Functional performance and device reliability are not guaranteed under these conditions. All voltages are specified with respect to GND.

Supply Voltage	–0.3V to 4.0V
Input Voltage	–0.3V to 5.0V
Output Voltage	–0.3V to 5.0V
Storage Temperature	-65°C to 150°C
Ambient Operating Temperature (Ta)	0°C to 70°C

DC Characteristic

■ Operating Conditions

Parameter	Sym.	Min.	Typ.	Max.	Unit	Conditions
Supply Voltage	VCC2.5	2.375	2.5	2.625	V	
	TXVCC	2.375	2.5	2.625	V	
Junction Operation Temperature	Tj	0	25	125	℃	
Power Consumption			2.0		W	

■ Input Clock

Parameter	Sym.	Min.	Typ.	Max.	Unit	Conditions
Frequency			25		MHz	
Frequency Tolerance		-50		+50	PPM	

■ I/O Electrical Characteristics

Parameter	Sym.	Min.	Typ.	Max.	Unit	Conditions
Input Low Voltage	VIL			0.8	V	
Input High Voltage	VIH	2.0			V	
Output Low Voltage	VOL			0.4	V	IOH=4mA, VCC=3.3V
Output High Voltage	VOH	2.4			V	IOL=4mA, VCC=3.3V

■ TX Transceiver Electrical Characteristics

Parameter	Sym.	Min.	Typ.	Max.	Unit	Conditions
Peak Differential Output Voltage	VP	0.95	1.0	1.05	V	
Signal Amplitude Symmetry	-	98	100	102	%	
Signal Rise/Fall Time	TRF	3	4	5	ns	
Rise/Fall Time Symmetry	TRFS			0.5	ns	
Duty Cycle Distortion	-			0.5	ns	
Overshoot	VO			5	%	

Thermal Data

Parameter	Symbol	Conditions	Min	Typical	Max	Units
Thermal resistance: junction to ambient 0 m/sec air flow	θ_{ja}	4 layer PCB, ambient temperature 70℃		20.8		℃/W
Thermal resistance: junction to ambient 0 m/sec air flow	θ_{jc}	4 layer PCB, ambient temperature 70℃		9.0		℃/W

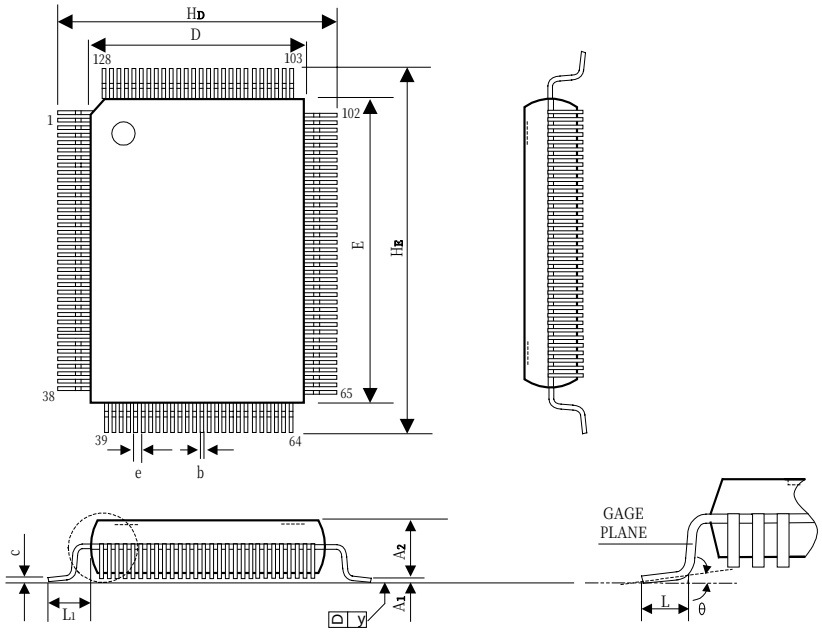
Order Information

Part No.	PIN	Notice
IP175	128 PIN PQFP	-

Package Detail

QFP 128L Outline Dimensions

Unit: Inches/mm



Symbol	Dimensions In Inches			Dimensions In mm		
	Min.	Nom.	Max.	Min.	Nom.	Max.
A_1	0.010	0.014	0.018	0.25	0.35	0.45
A_2	0.107	0.112	0.117	2.73	2.85	2.97
b	0.007	0.009	0.011	0.17	0.22	0.27
c	0.004	0.006	0.008	0.09	0.15	0.20
H_D	0.669	0.677	0.685	17.00	17.20	17.40
D	0.547	0.551	0.555	13.90	14.00	14.10
H_E	0.906	0.913	0.921	23.00	23.20	23.40
E	0.783	0.787	0.791	19.90	20.00	20.10
e	-	0.020	-	-	0.50	-
L	0.025	0.035	0.041	0.65	0.88	1.03
L_1	-	0.063	-	-	1.60	-
y	-	-	0.004	-	-	0.10
θ	0°	-	12°	0°	-	12°

Note:
1. Dimension D & E do not include mold protrusion.
2. Dimension B does not include dambar protrusion.
   Total in excess of the B dimension at maximum material condition.
   Dambar cannot be located on the lower radius of the foot.