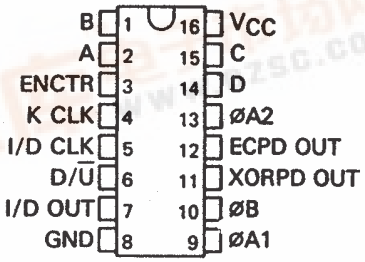
查询SN54LS297供应商 捷多邦，专业PCB打样工厂，24小时在线

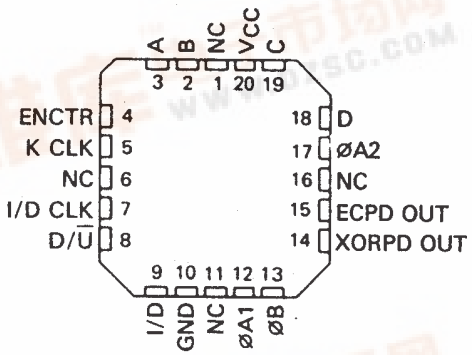


- **Digital Design Avoids Analog Compensation Errors**
- **Easily Cascadable for Higher Order Loops**
- **Useful Frequency from DC to:**
  **50 MHz Typical (K Clock)**
  **35 MHz Typical (I/D Clock)**

**SN54LS297 . . . J OR W PACKAGE**
**SN74LS297 . . . N PACKAGE**
**(TOP VIEW)**




**SN54LS297 . . . FK PACKAGE**
**(TOP VIEW)**




NC-No internal connection

## description

The SN54LS297 and SN74LS297 devices are designed to provide a simple, cost-effective solution to high-accuracy, digital, phase-locked-loop applications. These devices contain all the necessary circuits, with the exception of the divide-by-N counter, to build first order phase-locked loops as described in Figure 1.

Both exclusive-OR (XORPD) and edge-controlled (ECPD) phase detectors are provided for maximum flexibility.

Proper partitioning of the loop function, with many of the building blocks external to the package, makes it easy for the designer to incorporate ripple cancellation or to cascade to higher order phase-locked loops.

The length of the up/down K counter is digitally programmable according to the K counter function table. With A, B, C, and D all low, the K counter is disabled. With A high and B, C, and D low, the K counter is only three stages long, which widens the bandwidth or capture range and shortens the lock time of the loop. When A, B, C, and D are all programmed high, the K counter becomes seventeen stages long, which narrows the bandwidth or capture range and lengthens the lock time. Real-time control of loop bandwidth by manipulating the A through D inputs can maximize the overall performance of the digital phase-locked loop.

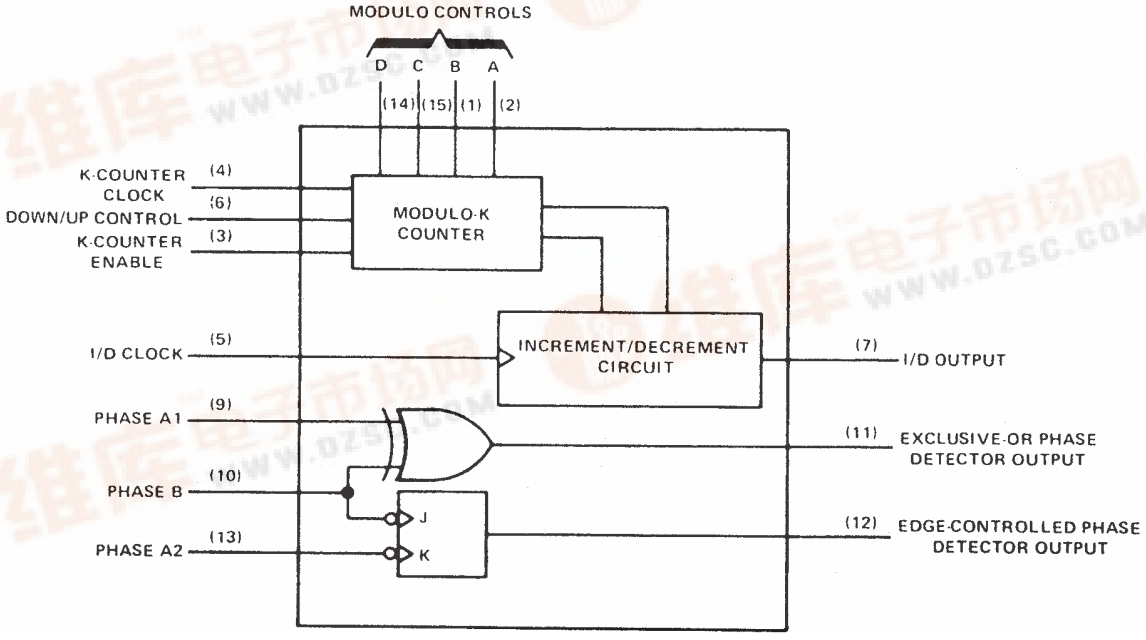



**FIGURE 1–SIMPLIFIED BLOCK DIAGRAM**

Pin numbers shown are for J, N and W packages.

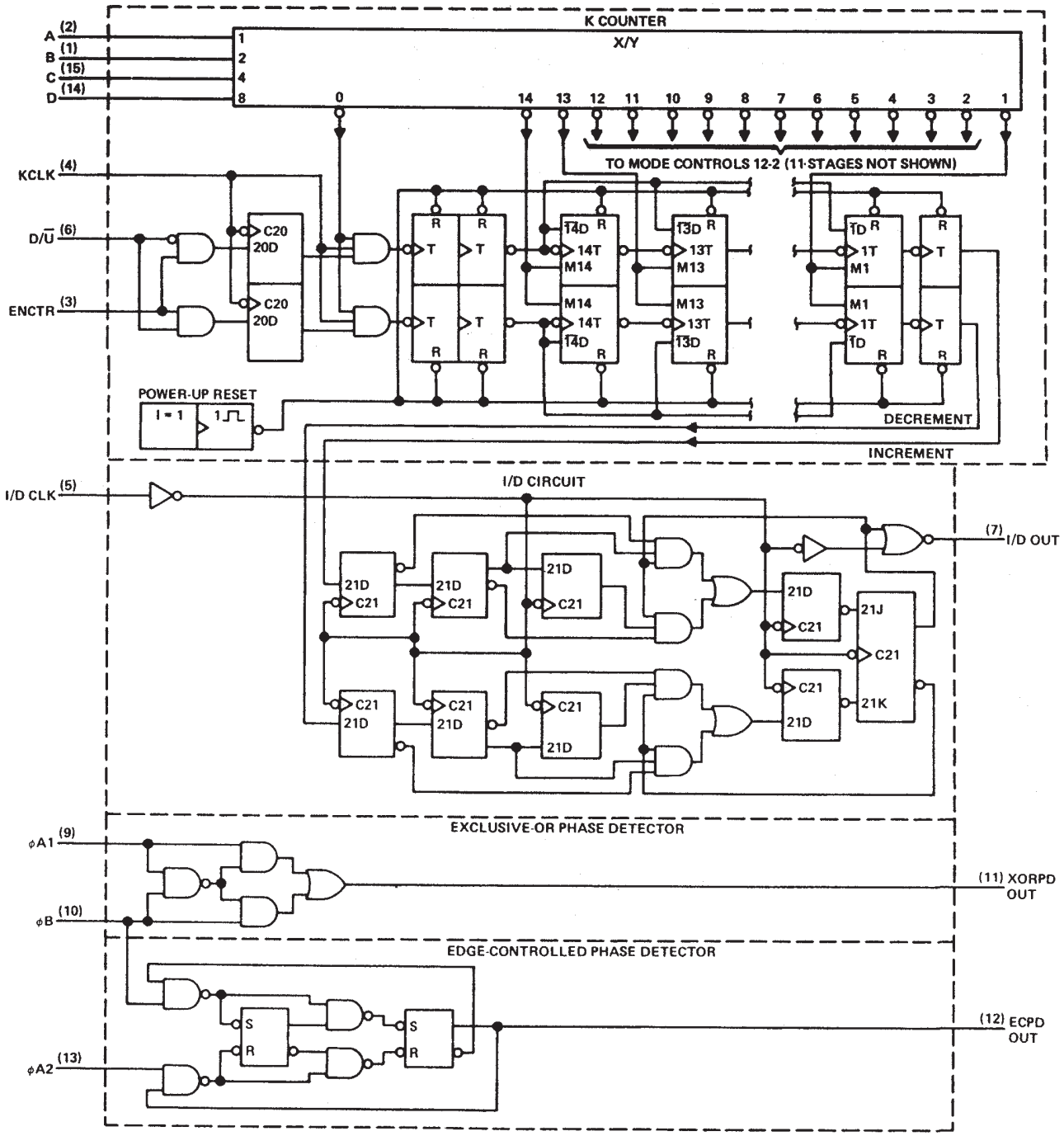
PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include

Copyright © 1988, Texas Instruments Incorporated

## description (continued)

The 'LS297 can perform the classic first-order phase-locked loop function without using analog components. The accuracy of the digital phase-locked loop (DPLL) is not affected by $V_{CC}$ and temperature variations, but depends solely on accuracies of the K clock, I/D clock, and loop propagation delays. The I/D clock frequency and the divide-by-N modulos will determine the center frequency of the DPLL. The center frequency is defined by the relationship $f_c$ = I/D Clock/2N (Hz).

## logic diagram (positive logic)




Pin numbers shown are for J, N, and W packages.

**K COUNTER FUNCTION TABLE**
**(DIGITAL CONTROL)**

| D | C | B | A | MODULO (K) |
|---|---|---|---|---|
| L | L | L | L | Inhibited |
| L | L | L | H | $2^3$ |
| L | L | H | L | $2^4$ |
| L | L | H | H | $2^5$ |
| L | H | L | L | $2^6$ |
| L | H | L | H | $2^7$ |
| L | H | H | L | $2^8$ |
| L | H | H | H | $2^9$ |
| H | L | L | L | $2^{10}$ |
| H | L | L | H | $2^{11}$ |
| H | L | H | L | $2^{12}$ |
| H | L | H | H | $2^{13}$ |
| H | H | L | L | $2^{14}$ |
| H | H | L | H | $2^{15}$ |
| H | H | H | L | $2^{16}$ |
| H | H | H | H | $2^{17}$ |

**FUNCTION TABLE**
**EXCLUSIVE-OR PHASE DETECTOR**

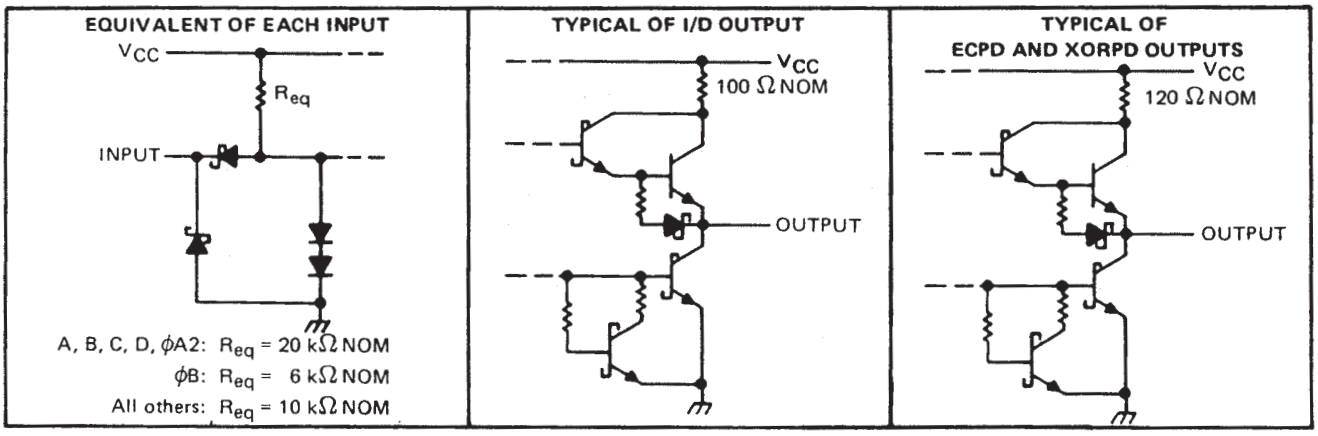
| $\phi$A1 | $\phi$B | XORPD OUT |
|---|---|---|
| L | L | L |
| L | H | H |
| H | L | H |
| H | H | L |

**FUNCTION TABLE**
**EDGE-CONTROLLED PHASE DETECTOR**

| $\phi$A2 | $\phi$B | ECPD OUT |
|---|---|---|
| H or L | ↓ | H |
| ↓ | H or L | L |
| H or L | ↑ | No change |
| ↑ | H or L | No change |

H = steady-state high level
L = steady-state low level
↓ = transition from high to low
↑ = transition from low to high

## schematics of inputs and outputs




## operation

The phase detector generates an error signal waveform that, at zero phase error, is a 50% duty cycle square wave. At the limits of linear operation, the phase detector output will be either high or low all of the time, depending on the direction of the phase error ($\phi_{in} - \phi_{out}$). Within these limits, the phase detector output varies linearly with the input phase error according to the gain $k_d$, which is expressed in terms of phase detector output per cycle of phase error. The phase detector output can be defined to vary between ±1 according to the relation:

$$\text{PD Output} = \frac{\%\ \text{high} - \%\ \text{low}}{100} \qquad (1)$$

The output of the phase detector will be $k_d\ \phi_e$, where the phase error $\phi_e = \phi_{in} - \phi_{out}$.

Exclusive-OR phase detectors (XORPD) and edge-controlled phase detectors (ECPD) are commonly used digital types. The ECPD is more complex than the XORPD logic function, but can be described generally as a circuit that changes states on one of the transitions of its inputs. $k_d$ for an XORPD is 4 because its output remains high (PD output = 1) for a phase error of 1/4 cycle. Similarly, $k_d$ for the ECPD is 2 since its output remains high for a phase error of 1/2 cycle. The type of phase detector will determine the zero-phase-error point, i.e., the phase separation of the phase detector inputs for $\phi_e$ defined to be zero. For the basic DPLL system of Figure 2, $\phi_e = 0$ when the phase detector output is a square wave. The XORPD inputs are 1/4 cycle out of phase for zero phase error. For the ECPD, $\phi_e = 0$ when the inputs are 1/2 cycle out of phase.

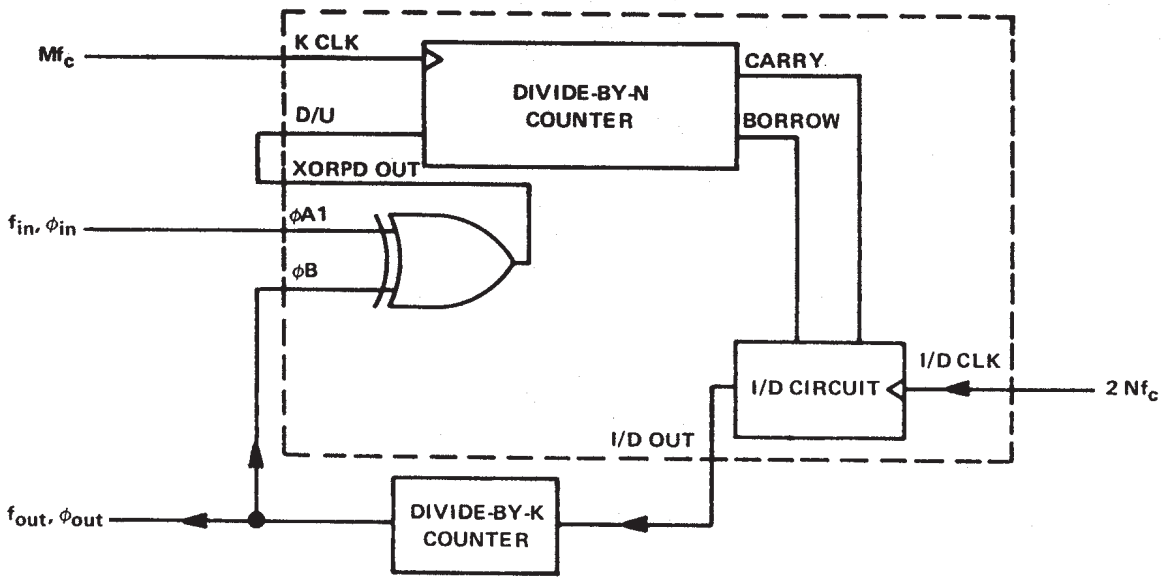



**FIGURE 2–DPLL USING EXCLUSIVE-OR PHASE DETECTION**

The phase detector output controls the up/down input to the K counter. The counter is clocked by input frequency $Mf_C$, which is a multiple M of the loop center frequency $f_C$. When the K counter recycles up, it generates a carry pulse. Recycling while counting down generates a borrow pulse. If the carry and borrow outputs are conceptually combined into one output that is positive for a carry and negative for a borrow, and if the K counter is considered as a frequency divider with the ratio $Mf_C/K$, the output of the K counter will equal the input frequency multiplied by the division ratio. Thus the output from the K counter is $(k_d \phi_e Mf_C)/K$.

The carry and borrow pulses go to the increment/decrement (I/D) circuit, which, in the absence of any carry or borrow pulse, has an output that is 1/2 of the input clock I/D CLK. The input clock is just a multiple, 2N, of the loop center frequency. In response to a carry or borrow pulse, the I/D circuit will either add or delete a pulse at I/D OUT. Thus the output of the I/D circuit will be $Nf_C + (k_d \phi_e Mf_C)/2K$.

The output of the N counter (or the output of the phase-locked loop) is thus:

$$f_O = f_C + (k_d \phi_e Mf_C)/2KN$$

If this result is compared to the equation for a first-order analog phase-locked loop, the digital equivalent of the gain of the VCO is just $Mf_C/2KN$ or $f_C/K$ for $M = 2N$.

Thus the simple first-order phase-locked loop with an adjustable K counter is the equivalent of an analog phase-locked loop with a programmable VCO gain.

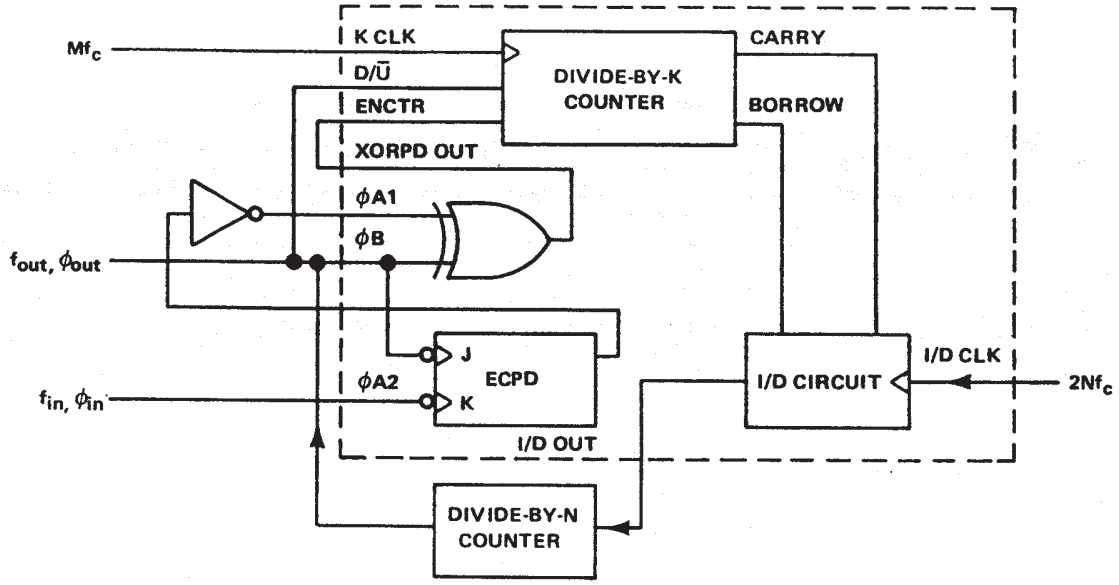



FIGURE 3–DPLL USING BOTH PHASE DETECTORS IN A RIPPLE-CANCELLATION SCHEME

## absolute maximum rating over operating free-air temperature range (unless otherwise noted)

Supply voltage, $V_{CC}$ (see Note 1) . . . . . 7 V
Input voltage . . . . . 7 V
Operating free-air temperature range: SN54LS297 . . . . . – 55° C to 125° C
SN74LS297 . . . . . 0° C to 70° C
Storage temperature range . . . . . – 65° C to 150° C

NOTE 1: Voltage values are with respect to network ground terminal.

## recommended operating conditions

| | | | SN54LS297 | | | SN74LS297 | | | UNIT |
|---|---|---|---|---|---|---|---|---|---|
| | | | MIN | NOM | MAX | MIN | NOM | MAX | |
| $V_{CC}$ | Supply voltage | | 4.5 | 5 | 5.5 | 4.75 | 5 | 5.25 | V |
| $I_{OH}$ | High-level output current | I/D OUT | | | – 1.2 | | | – 1.2 | mA |
| | | EXOR, ECPD | | | – 400 | | | – 400 | μA |
| $I_{OL}$ | Low-level output current | I/D OUT | | | 12 | | | 24 | mA |
| | | XOR, ECPD | | | 4 | | | 8 | mA |
| $f_{clock}$ | Clock frequency | K Clock | 0 | | 32 | 0 | | 32 | MHz |
| | | I/D Clock | 0 | | 16 | 0 | | 16 | MHz |
| $t_w$ | Width of clock input pulse | K Clock | 16 | | | 16 | | | ns |
| | | I/D Clock | 33 | | | 33 | | | ns |
| $t_{su}$, to K | Setup time to K Clock ↑ | U/$\overline{D}$, ENCTR | 30 | | | 30 | | | ns |
| $t_h$ | Hold time from K Clock ↑ | U/$\overline{D}$, ENCTR | 0 | | | 0 | | | ns |
| $T_A$ | Operating free-air temperature | | – 55 | | 125 | 0 | | 70 | °C |

## electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

| PARAMETER | | | TEST CONDITIONS† | | SN54LS297 MIN | SN54LS297 TYP‡ | SN54LS297 MAX | SN74LS297 MIN | SN74LS297 TYP‡ | SN74LS297 MAX | UNIT |
|---|---|---|---|---|---|---|---|---|---|---|---|
| $V_{IH}$ | High-level input voltage | | | | 2 | | | 2 | | | V |
| $V_{IL}$ | Low-level input voltage | | | | | | 0.7 | | | 0.8 | V |
| $V_{IK}$ | Input clamp voltage | | $V_{CC}$ = MIN, $I_I$ = −18 mA | | | | −1.5 | | | −1.5 | V |
| $V_{OH}$ | High-level output voltage | I/D OUT | $V_{CC}$ = MIN, $V_{IH}$ = 2 V, $V_{IL}$ = $V_{IL}$ max | $I_{OH}$ = MAX | 2.4 | | | 2.4 | | | V |
| | | Others | | $I_{OH}$ = MAX | 2.5 | | | 2.7 | | | |
| $V_{OL}$ | Low-level output voltage | I/D OUT | $V_{CC}$ = MIN, $V_{IH}$ = 2 V, $V_{IL}$ = $V_{IL}$ max | $I_{OL}$ = 12 mA | | 0.25 | 0.4 | | 0.25 | 0.4 | V |
| | | | | $I_{OL}$ = 24 mA | | | | | 0.35 | 0.5 | |
| | | Others | | $I_{OL}$ = 4 mA | | 0.25 | 0.4 | | 0.25 | 0.4 | |
| | | | | $I_{OL}$ = 8 mA | | | | | 0.35 | 0.5 | |
| $I_I$ | Input current at maximum input voltage | | $V_{CC}$ = MAX, $V_I$ = 7 V | | | | 0.1 | | | 0.1 | mA |
| $I_{IH}$ | High-level input current | U/$\overline{D}$, EN, $\phi$A1 | $V_{CC}$ = MAX, $V_I$ = 2.7 V | | | | 40 | | | 40 | μA |
| | | $\phi$B | | | | | 60 | | | 60 | |
| | | All others | | | | | 20 | | | 20 | |
| $I_{IL}$ | Low-level input current | U/$\overline{D}$, EN, $\phi$A1 | $V_{CC}$ = MAX, $V_I$ = 0.4 V | | | | −0.8 | | | −0.8 | mA |
| | | $\phi$B | | | | | −1.2 | | | −1.2 | |
| | | All others | $V_I$ = 0.4 V | | | | −0.4 | | | −0.4 | |
| $I_{OS}$ | Short-circuit output current § | I/D OUT | $V_{CC}$ = MAX | | −30 | | −130 | −30 | | −130 | mA |
| | | Others | | | −20 | | −100 | −20 | | −100 | |
| $I_{CC}$ | Supply current | | $V_{CC}$ = MAX, All inputs grounded, All outputs open | | | 75 | 120 | | 75 | 120 | mA |

†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
‡All typical values are of $V_{CC}$ = 5 V, $T_A$ = 25°C.
§Not more than one output should be shorted at a time and the duration of the short-circuit should not exceed one second.

## switching characteristics, $V_{CC}$ = 5 V, $T_A$ = 25°C

| PARAMETER¶ | FROM (INPUT) | | TO (OUTPUT) | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|---|---|
| $f_{max}$ | KCLK | | I/D OUT | $R_L$ = 667 Ω, $C_L$ = 45 pF, See Note 2 | 32 | 50 | | MHz |
| | I/D CLK | | I/D OUT | | 16 | 35 | | |
| $t_{PLH}$ | I/D CLK ↑ | | I/D OUT | | | 15 | 25 | ns |
| $t_{PHL}$ | I/D CLK ↑ | | I/D OUT | | | 22 | 35 | ns |
| $t_{PLH}$ | $\phi$A1 or $\phi$B | Other input low | XOR OUT | $R_L$ = 2 kΩ, $C_L$ = 45 pF, See Note 2 | | 10 | 15 | ns |
| | $\phi$A1 or $\phi$B | Other input high | XOR OUT | | | 17 | 25 | |
| $t_{PHL}$ | $\phi$A1 or $\phi$B | Other input low | XOR OUT | | | 15 | 25 | ns |
| | $\phi$A1 or $\phi$B | Other input high | XOR OUT | | | 17 | 25 | |
| $t_{PLH}$ | $\phi$B ↓ | | ECPD OUT | | | 20 | 30 | ns |
| $t_{PHL}$ | $\phi$A2↓ | | ECPD OUT | | | 20 | 30 | ns |

¶$t_{PLH}$ = propagation delay time, low-to-high-level output
$t_{PHL}$ = propagation delay time, high-to-low-level output
NOTE 2: Load circuits and voltage waveforms are shown in Section 1.

## IMPORTANT NOTICE

Texas Instruments and its subsidiaries (TI) reserve the right to make changes to their products or to discontinue any product or service without notice, and advise customers to obtain the latest version of relevant information to verify, before placing orders, that information being relied on is current and complete. All products are sold subject to the terms and conditions of sale supplied at the time of order acknowledgement, including those pertaining to warranty, patent infringement, and limitation of liability.

TI warrants performance of its semiconductor products to the specifications applicable at the time of sale in accordance with TI's standard warranty. Testing and other quality control techniques are utilized to the extent TI deems necessary to support this warranty. Specific testing of all parameters of each device is not necessarily performed, except those mandated by government requirements.

CERTAIN APPLICATIONS USING SEMICONDUCTOR PRODUCTS MAY INVOLVE POTENTIAL RISKS OF DEATH, PERSONAL INJURY, OR SEVERE PROPERTY OR ENVIRONMENTAL DAMAGE ("CRITICAL APPLICATIONS"). TI SEMICONDUCTOR PRODUCTS ARE NOT DESIGNED, AUTHORIZED, OR WARRANTED TO BE SUITABLE FOR USE IN LIFE-SUPPORT DEVICES OR SYSTEMS OR OTHER CRITICAL APPLICATIONS. INCLUSION OF TI PRODUCTS IN SUCH APPLICATIONS IS UNDERSTOOD TO BE FULLY AT THE CUSTOMER'S RISK.

In order to minimize risks associated with the customer's applications, adequate design and operating safeguards must be provided by the customer to minimize inherent or procedural hazards.

TI assumes no liability for applications assistance or customer product design. TI does not warrant or represent that any license, either express or implied, is granted under any patent right, copyright, mask work right, or other intellectual property right of TI covering or relating to any combination, machine, or process in which such semiconductor products or services might be or are used. TI's publication of information regarding any third party's products or services does not constitute TI's approval, warranty or endorsement thereof.

Copyright © 1999, Texas Instruments Incorporated