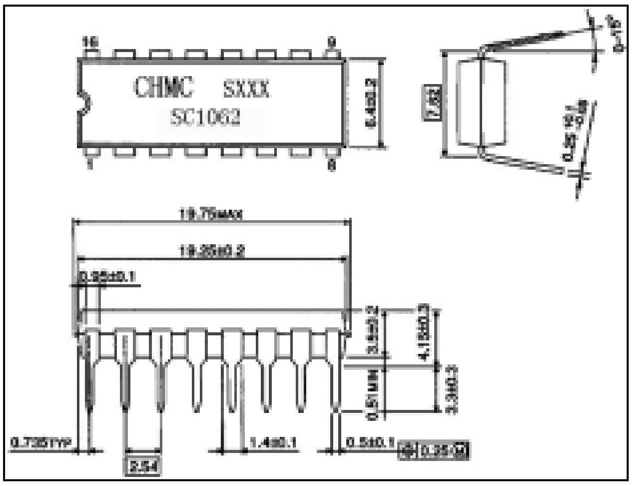
Silicore

LOW VOLTAGE TRANSMISSION CIRCUITS WITH DIALLER INTERFACE SC1062/SC1062A

GENERAL DESCRIPTION

The SC1062/SC1062A are integrated circuits that perform all speech and line interface functions required in fully electronic telephone sets. They perform electronic switching between dialing and speech. The ICs operate at line voltage down to 1.6V DC (with reduced performance) to facilitate the use of more telephone sets connected in parallel.

Outline Drawing

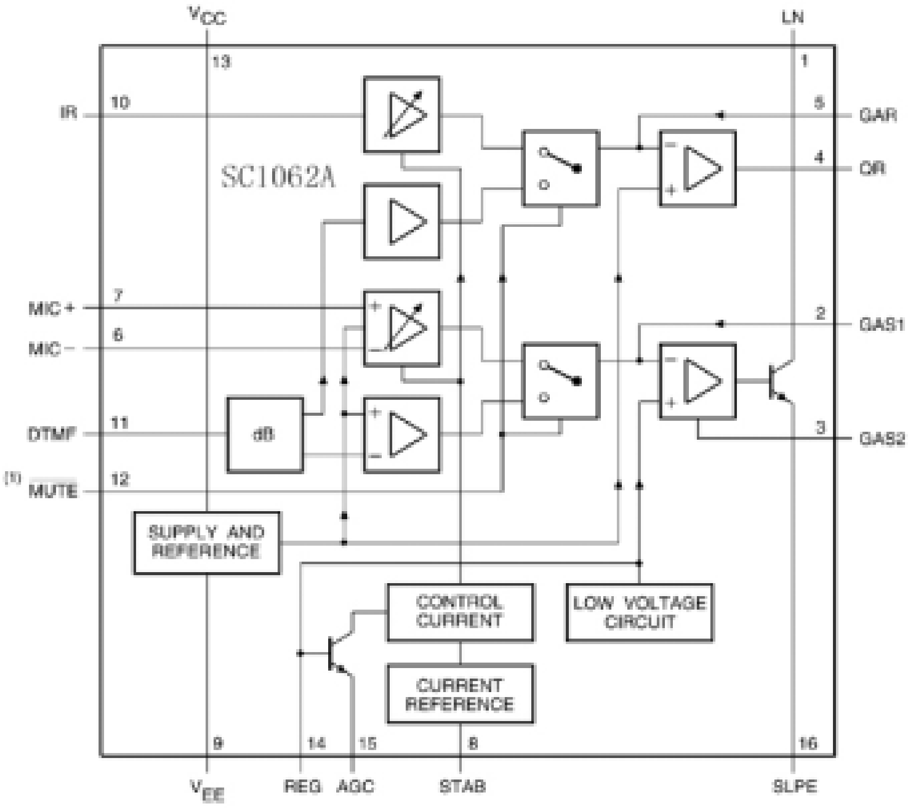


All statements and values refer to all versions unless otherwise specified.

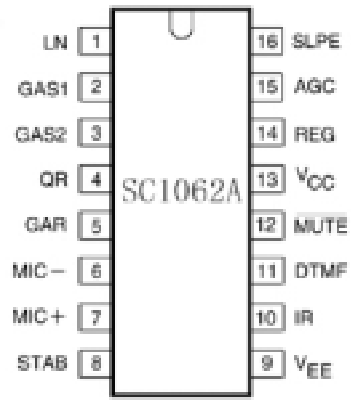
FEATURES

- Low DC line voltage: operates down to 1.6V (excluding polarity guard)
- Voltage regulator with adjustable static resistance
- Provides a supply for external circuits
- Symmetrical high-impedance inputs (64kΩ) for dynamic, magnetic or piezoelectric microphones
- Asymmetrical high-impedance input (32kΩ) for electret microphones
- DTMF signal input with confidence tone
- Mute input for pulse or DTMF dialing
  - SC1062: active HIGH (MUTE)
  - SC1062A: active LOW ($\overline{\text{MUTE}}$)
- Receiving amplifier for dynamic, magnetic or piezoelectric earpieces
- Large gain setting ranges on microphone and earpiece amplifiers
- Line loss compensation (line current dependent) for microphone and earpiece amplifiers
- Gain control curve adaptable to exchange supply
- DC line voltage adjustment facility

BLOCK DIAGRAM



PIN CONNECTION



Note: pin 12 is active HIGH (MUTE) for SC1062

PIN DESCRIPTION

PIN	SYMBOL	DESCRIPTION	PIN	SYMBOL	DESCRIPTION
1	LN	Positive line terminal	9	VEE	Negative line terminal
2	GAS1	Gain adjustment; transmitting amplifier	10	IR	Receiving amplifier input
3	GAS2	Gain adjustment; transmitting amplifier	11	DTMF	Dual-tone multi-frequency input
4	QR	Non-inverting output; receiving amplifier	12	$\overline{\text{MUTE}}$	Mute input (see note)
5	GAR	Gain adjustment; receiving amplifier	13	Vcc	Positive supply decoupling
6	MIC-	Inverting microphone input	14	REG	Voltage regulator decoupling
7	MIC+	Non- inverting microphone input	15	AGC	Automatic gain control input
8	STAB	Current stabilizer	16	SLPE	Slope (DC resistance) adjustment

Note: pin 12 is active HIGH(MUTE) for SC1062

MAXIMUM VALUES

PARAMETER	SYMBOL	CONDITIONS	MIN	MAX.	UNIT
Positive continuous line voltage	V_{LN}			12	V
Repetitive line voltage during switch-on or line interruption	$V_{LN(R)}$			13.2	V
Repetitive peak line voltage for a 1ms pulse per 5s	$V_{LN(RM)}$	R9=20Ω;R10=13Ω		28	V
Line current	Iline	R9=20Ω;note 1		140	mA
Input voltage on all other pins	V_I	Positive input voltage		Vcc+0.7	V
		Negative input voltage		-0.7	V
Total power dissipation	P_D	R9=20Ω;note 2		666	mW
Operating ambient temperature	Tamb		-25	+75	°C
Storage temperature	Tstg		-40	+125	°C
Junction temperature	Tj			125	°C

Notes:

1. Mostly dependent on the maximum required Tamb and on the voltage between LN and SLPE
2. Calculated for the maximum ambient temperature specified (Tamb=75°C) and a maximum junction temperature of 125°C

ELECTRIC CHARACTERISTICS

Unless otherwise specified: Iline=11 to 140mA; V_{EE}=0V; f=800Hz; Tamb=25°C.

Characteristic	Symbol	Condition	Min.	Typ.	Max.	Unit
Microphone inputs MIC- and MIC+(Pins 6 and 7)						
Input impedance differential	|Zis|	Between MIC- and MIC+		64		kΩ
Input impedance single-ended	|Zis|	MIC- or MIC+ to V_{EE}		32		kΩ
Common mode rejection ratio	CMRR			82		dB
Voltage gain MIC+ or MIC- to LN	Gv	Iline=15mA;R7=68 kΩ	50	52	54	dB
Gain variation with frequency referenced to 800Hz	Δ Gvf	f=300~ 3400Hz		±0.2		dB
Gain variation with temperature referenced to 25°C	Δ Gvt	Without R6;Iline=50mA Tamb=-25~+75°C		±0.2		dB
Gain adjustment inputs GAS1 and GAS2 (pins 2 and 3)						
Transmitting amplifier gain variation by adjustment of R7 between GAS1 and GAS2	Δ Gv		-8		0	dB

ELECTRIC CHARACTERISTICS continue

Characteristic	Symbol	Condition	Min.	Typ.	Max	Unit
Supplies LN and Vcc (pins 1 and 13)						
Voltage drop over circuit between LN and V_{EE}	V_{LN}	MIC inputs open-circuit; Iline=1mA		1.6		V
		MIC inputs open-circuit; Iline=4mA		1.9		V
		MIC inputs open-circuit; Iline=15mA	3.55	4.0	4.25	V
		MIC inputs open-circuit; Iline=100mA	4.9	5.7	6.5	V
		MIC inputs open-circuit; Iline=140mA			7.5	V
Variation with temperature	$\Delta V_{LN}/\Delta T$	Iline=15mA		-0.3		mV/K
Voltage drop over circuit between LN and V_{EE} with external resistor R_{VA}	V_{LN}	Iline=15mA; R_{VA}(LN to REG)=68kΩ		3.5		V
		Iline=15mA; R_{VA}(REG to SLPE)=39kΩ		4.5		V
Supply current	Icc	Vcc=2.8V		0.9	1.35	mA
Supply voltage available for peripheral circuitry SC1062	Vcc	Iline=15mA MUTE=HIGH; Ip=1.2mA	2.2	2.7		V
		Iline=15mA MUTE=HIGH; Ip=0mA		3.4		V
Supply voltage available for peripheral circuitry SC1062A	Vcc	Iline=15mA MUTE=LOW; Ip=1.2mA	2.2	2.7		V
		Iline=15mA MUTE=LOW; Ip=0mA		3.4		V
DTMF input (pin 11)						
Input impedance	|Zis|			20.7		kΩ
Voltage gain from DTMF to LN	Gv	Iline=15mA;R7=68kΩ	24	25.5	27	dB
Gain variation with frequency referenced to 800Hz	Δ Gvf	f=300~ 3400Hz		±0.2		dB
Gain variation with temperature referenced to 25°C	Δ Gvt	Iline=50mA Tamb=-25~+75°C		±0.2		dB
Sending amplifier output LN (pin 1)						
Output voltage (RMS value)	V_{LN}(rms)	THD=10%; Iline=4mA		0.8		V
		THD=10%; Iline=15mA	1.7	2.3		V
Noise Output voltage (RMS value)	Vno(rms)	Iline=15mA;R7=68kΩ; 200Ω between MIC- and MIC+		-69		dBmp
Receiving amplifier input IR (pin 10)						
Input impedance	|Zis|			20		kΩ
Gain adjustment input GAR (pin 5)						
Receiving amplifier gain variation by adjustment of R4 between GAR and QR	Δ Gv		-11		0	dB

ELECTRIC CHARACTERISTICS continue

Characteristic	Symbol	Condition	Min.	Typ.	Max.	Unit
Receiving amplifier output QR (pin 4)						
Output impedance	|Zos|			4		Ω
Voltage gain from IR to QR	Gv	Iline=15mA;R_L=300Ω (from pin9 to pin4)	29.5	31	32.5	dB
Gain variation with frequency referenced to 800Hz	Δ Gvf	f=300~ 3400Hz		±0.2		dB
Gain variation with temperature referenced to 25°C	Δ Gvt	Without R6;Iline=50mA Tamb=-25~+75°C		±0.2		dB
Output voltage (RMS value)	Vo(rms)	THD=2%; since wave drive; R4=100kΩ Iline=50mA; Ip=0mA; R_L=150Ω	0.22	0.33		V
		THD=2%; since wave drive; R4=100kΩ Iline=50mA; Ip=0mA; R_L=450Ω	0.3	0.48		V
Output voltage (RMS value)	Vo(rms)	THD=10%; R4=100kΩ; R_L=150Ω; Iline=4mA		15		mV
Noise Output voltage (RMS value)	Vno(rms)	Iline=15mA; R4=100kΩ IR open-circuit R_L=300Ω		50		μV
Mute input (pin 2)						
HIGH level input voltage	V_{IH}		1.5		Vcc	V
LOW level input voltage	V_{IL}				0.3	V
Input current	I_{MUTE}			8	15	μA
Reduction of gain						
MIC+ or MIC- to LN	Δ Gv	SC1062 MUTE=HIGH		70		dB
		SC1062A $\overline{\text{MUTE}}$=LOW		70		dB
Voltage gain from DTMF to QR	Gv	SC1062 MUTE=HIGH R4=100 kΩ; R_L=300Ω		-17		dB
		SC1062A $\overline{\text{MUTE}}$=LOW R4=100kΩ; R_L=300Ω		-17		dB
Automatic gain control input AGC (pin 5)						
Controlling the gain from IR to QR and the gain from MIC+, MIC- to LN gain control range	Δ Gv	R6=110kΩ (between AGC and V_{EE}) Iline=70mA		-5.8		dB
Highest line current for maximum gain	I_{lineH}			23		mA
Lowest line current for maximum gain	I_{lineL}			61		mA

FUNCTION DESCRIPTION

Supply: Vcc, LN, SLPE, REG and STAB

Power for the SC1062 and its peripheral circuits is usually obtained from the telephone line. The IC supply voltage is derived from the line via a dropping resistor and regulated by the SC1062, The supply voltage Vcc may also be used to supply external circuits e.g. dialing and control circuits. Decoupling of the supply voltage is performed by a capacitor between Vcc and V_{EE} while the internal voltage regulator is decoupled by a capacitor between REG and V_{EE}.

The DC current drawn by the device will vary in accordance with varying values of the exchange voltage(Vexch), the feeding bridge resistance(Rexch) and the DC resistance of the telephone line(Rline).

The SC1062 has an internal current stabilizer operating at a level determined by a 3.6kΩ resistor connected between STAB and V_{EE}(see Fig.8). When the line current (Iline) is more than 0.5 mA greater than the sum of the IC supply current (Icc) and the current drawn by the peripheral circuitry connected to Vcc (lp) the excess current is shunted to V_{EE} via LN.

The regulated voltage on the line terminal(V_{LN}) can be calculated as:

V_{LN}=Vref+I_{SLPE}*R9 or;

V_{LN}=Vref+[(Iline – Icc- 0.5*10^{-3} A)- Ip]*R9

where: Vref is an internally generated temperature compensated reference voltage of 3.7V and R9 is an external resistor connected between SLPE and V_{EE}. In normal use the value of R9 would be 20Ω. Changing the value of R9 will also affect microphone gain, DTMF gain, in control characteristics, ide-tone level, maximum output swing on LN and the dc characteristics(especially at the lower voltages).

Under normal conditions, when I_{SLPE} >= Icc+0.5mA +Ip, the static behavior of the circuit is that of a 3.7V regulator diode with an internal resistance equal to that of R9.In the audio frequency range the dynamic impedance is largely determined by R1.Fig.3 shows the equivalent impedance of the circuit.

Microphone inputs (MIC+ and MIC-) and gain pins (GAS1 and GAS2)

The SC1062 has symmetrical inputs. Its input impedance is 64kΩ (2*32kΩ) and its voltage gain is typically 52dB (when R7=68kΩ. see Fig.13). Dynamic, magnetic, piezoelectric or electret (with built-in FET source followers) can be used. Microphone arrangements are illustrated in Fig.10. The gain of the microphone amplifier can be adjusted between 44dB and 52dB to suit the sensitivity of the transducer in use. The gain is proportional to the value of R7 which is connected between GAS1 and GAS2. Stability is ensured by the external capacitors, C6 connected between GAS1 and SLPE and C8 connected between GAS1 and V_{EE}. The value of C6 is 100pF but this may be increased to obtain a first-order low-pass filter. The value of C8 is 10 times the value of C6. The cut-off frequency corresponds to the time constant R7*C6.

Mute input (MUTE)

A HIGH level at MUTE enables DTMF input and inhabits the microphone inputs and the receiving amplifier inputs; a LOW level or an open circuit does the reverse. Switching the mute input will cause negligible click is at the telephone outputs and on the line. In case the line current drops below 6mA(parallel operation of more sets) the circuit is always in speech condition independent of the DC level applied to the MUTE input. (SC1062A pin12 is $\overline{\text{MUTE}}$)

Dual-tone multi-frequency input (DTMF)

When the DTMF input is enabled dialing tones may be sent onto the line. The voltage gain from DTMF to LN is typically 25.5dB(when R7=68kΩ) and varies with R7 in the same way as the microphone gain. The signaling tones can be heard in the ear piece at a low level (confidence tone).

Receiving Amplifier (IR, OR and GAR)

The receiving amplifier has one input (IR) and a non-inverting output (OR). Ear piece arrangements are illustrated in Fig.11. The IR to OR gain is typically 31dB (when R4=100kΩ). It can be adjusted between 20 and 31dB to match the sensitivity of the transducer in use. The gain is set with the value of R4 which is connected between GAR and OR. The overall receive gain, between LN and OR, is calculated substracting the anti-sidetone network attenuation (32dB) from the amplifier gain. Two external capacitors, C4 and C7, ensure stability. C4 is normally 100pF and C7 is 10 times the value of C4. The value of C4 may be increased to obtain a first-order low-pass filter. The cut-off frequency will depend on the time constant R4*C4.

The output voltage of the receiving amplifier is specified for continuous-wave drive. The maximum output voltage will be higher under speech conditions where the peak to RMS ratio is higher.

Automatic gain control input AGC)

Automatic line loss compensation is achieved by connecting a resistor (R6) between AGC and VEE. The automatic gain control varies the gain of the microphone amplifier and the receiving amplifier in accordance with the DC line current. The control range is 5.8dB which corresponds to a line length of 5km for a 0.5mm diameter twisted pair copper cable with a DC resistance of 176Ω/km and average attenuation of 1.2dB/km. Resistor R6 should be chosen in accordance with the exchange supply voltage and its feeding bridge resistance (see Fig.12 and Table 1). The ratio of start and stop currents of the AGC curve is independent of the value of R6. If no automatic line loss compensation is required the AGC may be left open-circuit. The amplifier, in this condition, will give their maximum specified gain.

Side-tone suppression

The anti-sidetone network, R1//Zline, R2, R3, R8, R9 and Zbal, (see Fig.4) suppresses the transmitted signal in the ear piece. Compensation is maximum when the following conditions are fulfilled:

(a) R9*R2=R1[R3+(R8//Zbal)];

(b) [Zbal/(Zbal+R8)]=[Zline/(Zline+R1)];

If fixed values are chosen for R1, R2, R3 and R9 then condition (a) will always be fulfilled when R8/Zball << R3. To obtain optimum side-tone suppression condition (b) has to be fulfilled which results in: Zbal=(R8/R1) Zline=k*Zline where k is a scale factor; k=(R8/R1). The scale factor (k), dependent on the value of R8, is chosen to meet following criteria:

(a) Compatibility with a standard capacitor from the E6 or E12 range for Zbal,

(b) |Zbal//R8| << R3 fulfilling condition (a) and thus ensuring correct anti-sidetone bridge operation,

(c) | Zbal+R8| >>R9 to avoid influencing the transmitter gain.

In practice Zline varies considerably with the type and length. The value chosen for Zbal should therefore be for an average line length thus giving optimum setting for short or long lines.

Example

The balance impedance Zbal at which the optimum suppression is present can be calculated by: Suppose Zline =210Ω+(1265Ω//140nF) representing a 5km line of 0.5mm diameter, copper, twisted pair cable matched to 600 Ω (176Ω/km; 38nF/km). When k=0.64 then R8=390Ω, Zbal=130Ω+(820Ω//220nF).

At line currents below 9mA the internal reference voltage is automatically adjusted to a lower value (typically 1.6V at 1mA). This means that more sets can be operated in parallel with DC line voltages (excluding the polarity guard) down to an absolute minimum voltage of 1.6V. With line currents below 9mA the circuit has limited sending and receiving levels. The internal reference voltage can be adjusted by means of an external resistor (R_{VA}). This resistor when connected between LN and REG will decrease the internal reference voltage and when connected between REG and SLPE will increase the internal reference voltage.

Current (Ip) available from Vcc for peripheral circuits depends on the external components used. Fig.9 shows this current for Vcc > 2.2V. If MUTE is LOW when the receiving amplifier is driven the available current is further reduced. Current availability can be increased by connecting the supply IC (1081) in parallel with R1, as shown in Fig.16(c), or, by increasing the DC line voltage by means of an external resistor (R_{VA}) connected between REG and SLPE.

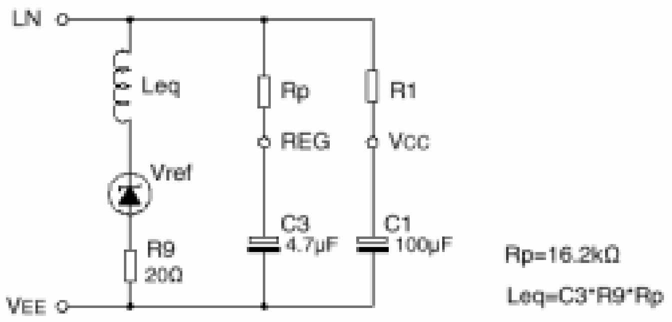


Fig.3 Equivalent impedance circuit

The anti-sidetone network for the SC1062 family shown in Fig.4 attenuates the signal received from the line by 32dB before it enters the receiving amplifier. The attenuation is almost constant over the whole audio frequency range. Fig.5 shows a conventional Wheat stone bridge anti-sidetone circuit that can be used as an alternative. Both bridge types can be used with either resistive or complex set impedance.

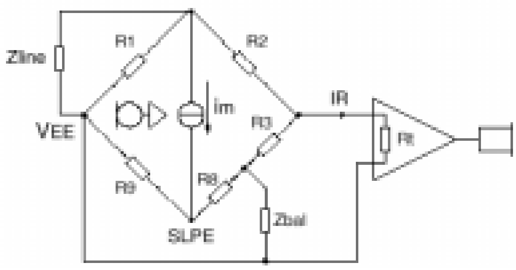


Fig.4 Equivalent circuit of SC1062 Anti-sidetone bridge

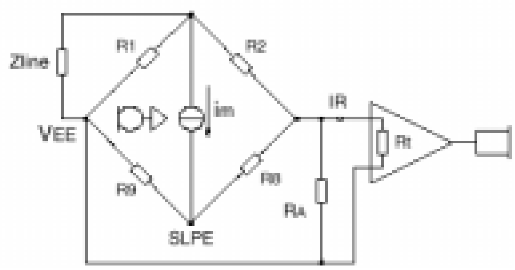


Fig.5 Equivalent circuit of an anti-sidetone network in a wheat stone bridge configuration

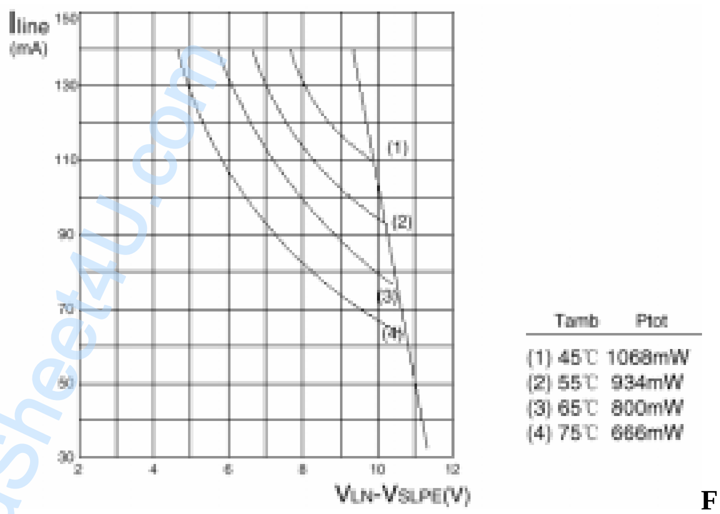


Fig.6 SC1062 safe operating area

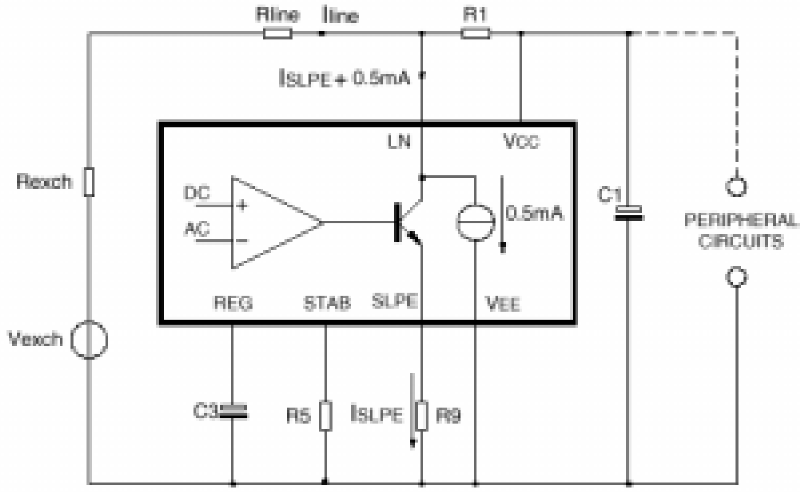


Fig.8 Supply arrangement

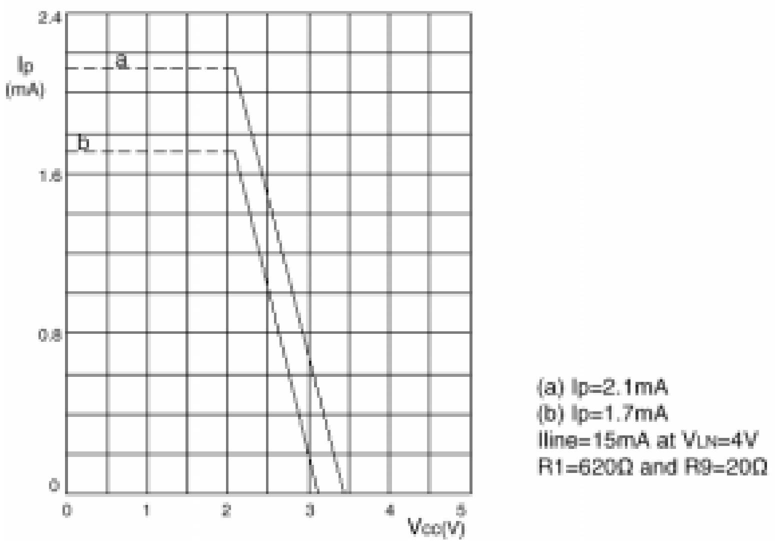
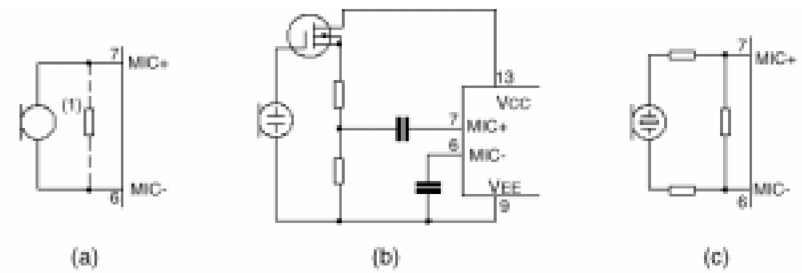


Fig.9 Typical current Ip available from Vcc peripheral circuitry with Vcc>=2.2V.

curve (a) is valid when the receiving amplifier is not driven or when MUTE =HIGH .curve(b) is valid when MUTE=LOW and the receiving amplifier is driven; Vo(rms)=150mV,R_L=150Ω. The supply possibilities can be increased simply by setting the voltage drop over the circuit V_{LN} to a high value by means of resistor R_{VA} connected between REG and SLPE.

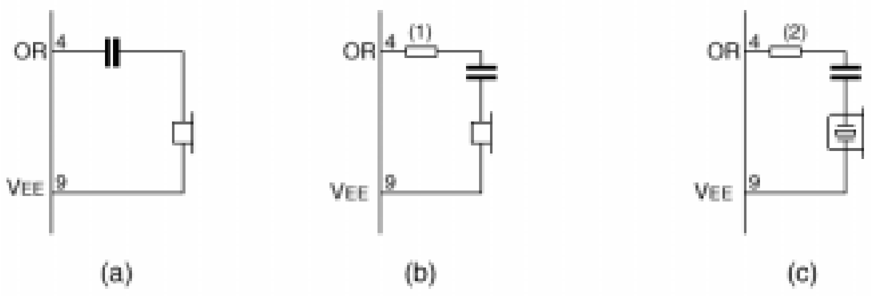


(a) Magnetic or dynamic microphone. The resistor marked (1) may be connected to decrease the terminating impedance.

(b) Electret microphone.

(c) Piezoelectric microphone.

Fig. 10 Alternative microphone arrangement



(a) Dynamic ear piece.

(b) Magnetic ear piece. The resistor marked (1) may be connected to prevent distortion (inductive load)

(c) Piezoelectric ear piece. The ear piece marked (2) is required to increase the phase margin (capacitive load)

Fig.11 Alternative receiver arrangement

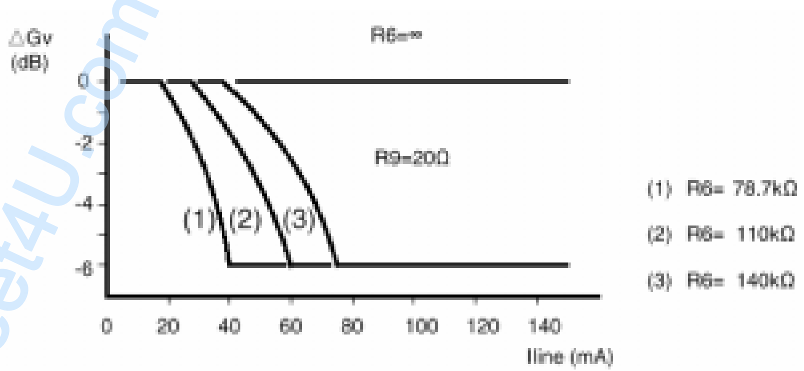


Fig.12 Variation of gain with line current, with R6 as a parameter

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		Rexch (Ω)			
		400	600	800	1000
		R6 (kΩ)			
Vexch (V)	36	100	78.7	×	×
	48	140	110	93.1	82
	60	×	×	120	102

Table 1 Values of resistor R6 for optimum line loss compensation, for various usual values of exchange supply voltage (Vexch) and exchange feeding bridge resistance (Rexch);R9=20Ω

TEST CIRCUIT

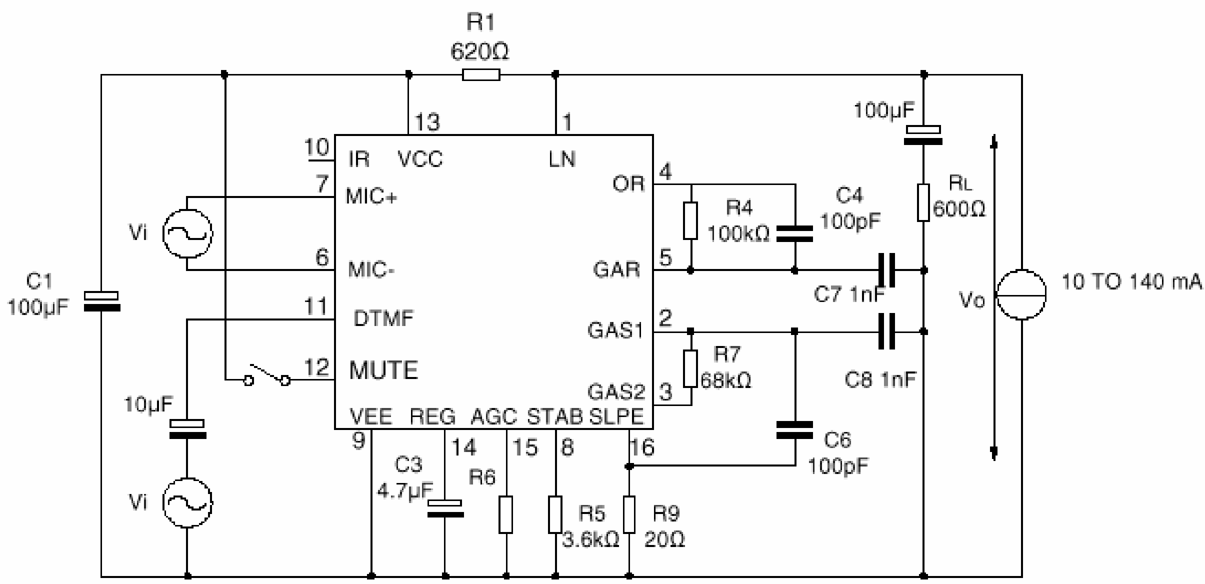

Fig.13 Test circuit defining voltage gain of MIC+, MIC- and DTMF inputs. Voltage gain is defined as: Gv=20*log (|VO/Vi|). For measuring the gain from MIC+ and MIC- the MUTE input should be LOW or open-circuit, for measuring the DTMF input MUTE should be HIGH .Inputs not under test should be open-circuit.

SC1062A pin12 is $\overline{\text{MUTE}}$

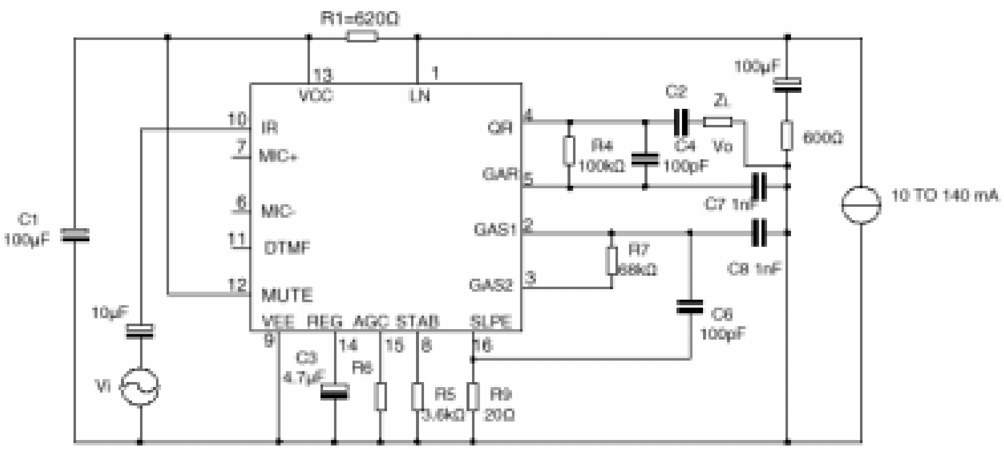

Fig.14 Test circuit for defining voltage gain of the receiving amplifier. Voltage gain is defined as: Gv=20*log(|VO/Vi|). SC1062A pin12 is MUTE

APPLICATION CIRCUIT

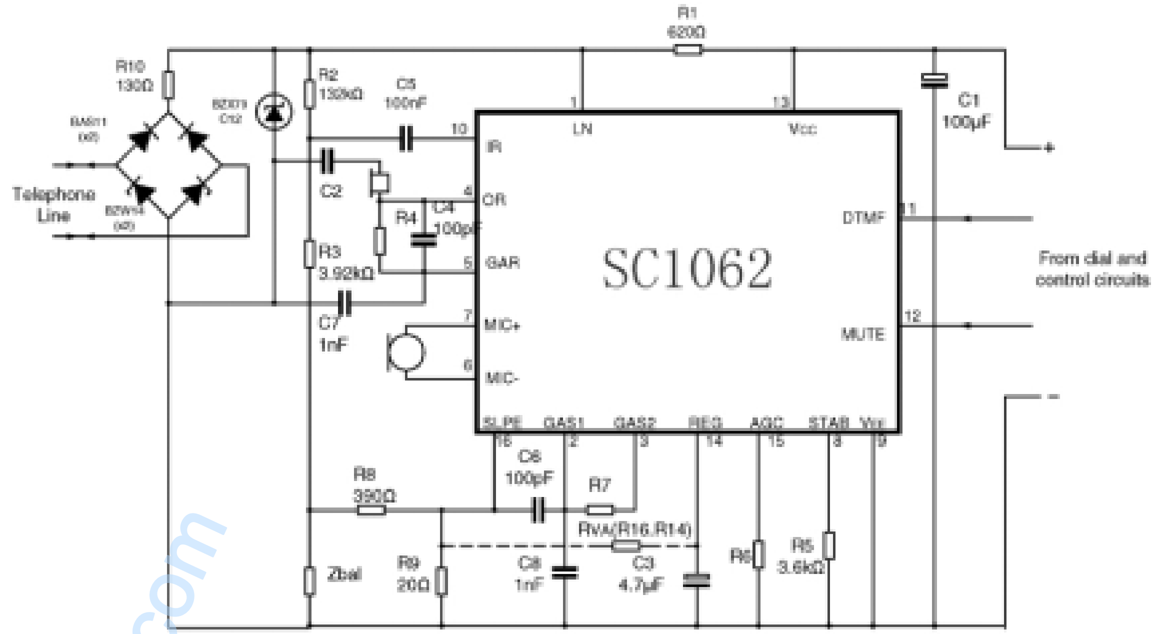

Fig.15 Typical application of the SC1062, shown here with a piezoelectric ear piece and DTMF dialing. The bridge to the left, the Zener diode and R10 limit the current into the circuit and the voltage across the circuit during line transients. Pulse dialing or register recall required a different protection arrangement. The DC line voltage can be set to a higher value by resistor R_{VA} (REG to SLPE).

SC1062A pin12 is MUTE

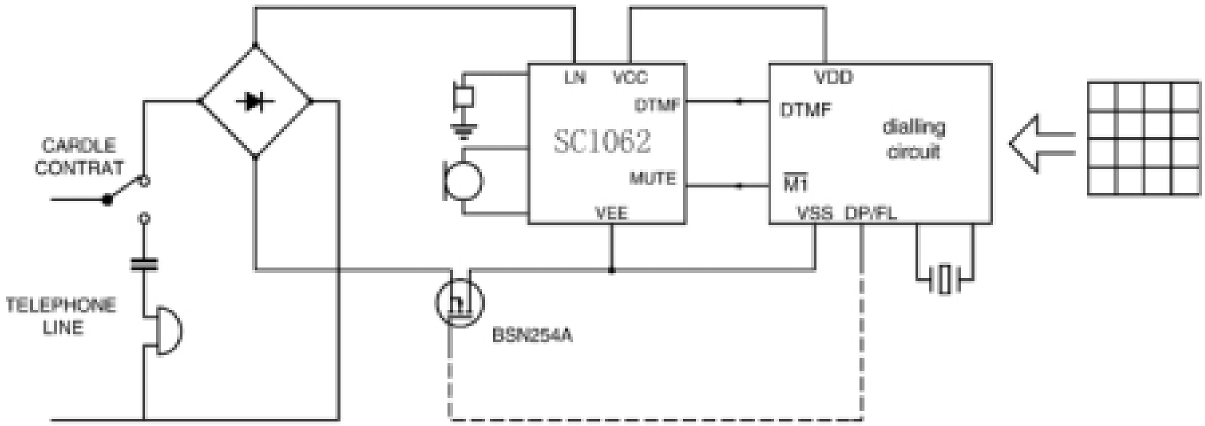

Fig.16 Typical applications of the SC1062 (simplified)

The dashed lines show an optional flash (register recall by timed loop break).

SC1062A pin12 is $\overline{\text{MUTE}}$