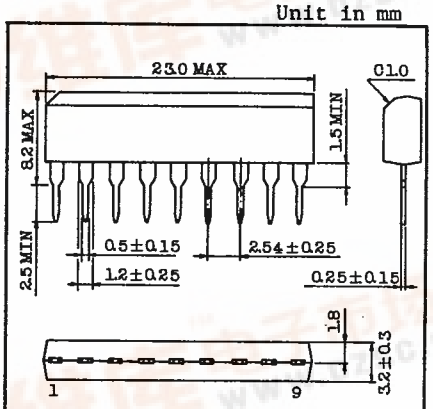
TA7324P

MUTING IC

TA7324P is developed for muting the popping sound made at power of one-off receivers, pre-amplifiers, main amplifiers, and other electric audio equipment as well as the noise made at changeover of switches.

- To mute the popping noise made in the case of receiving frequency or changeover of signal source of tuners.
- Delay muting at power ON.
- Instant muting at power OFF.
- Only a single timing capacitor and a very few external parts are provided.
- Either positive or negative pulse is applicable to the input trigger. The terminals consist of the high sensitive input terminal (sensitive level of 120mV) and the low sensitive input terminal (sensitive level of ±700mV)
- The operating power supply current is 5mA (Min.) available for portable sets.

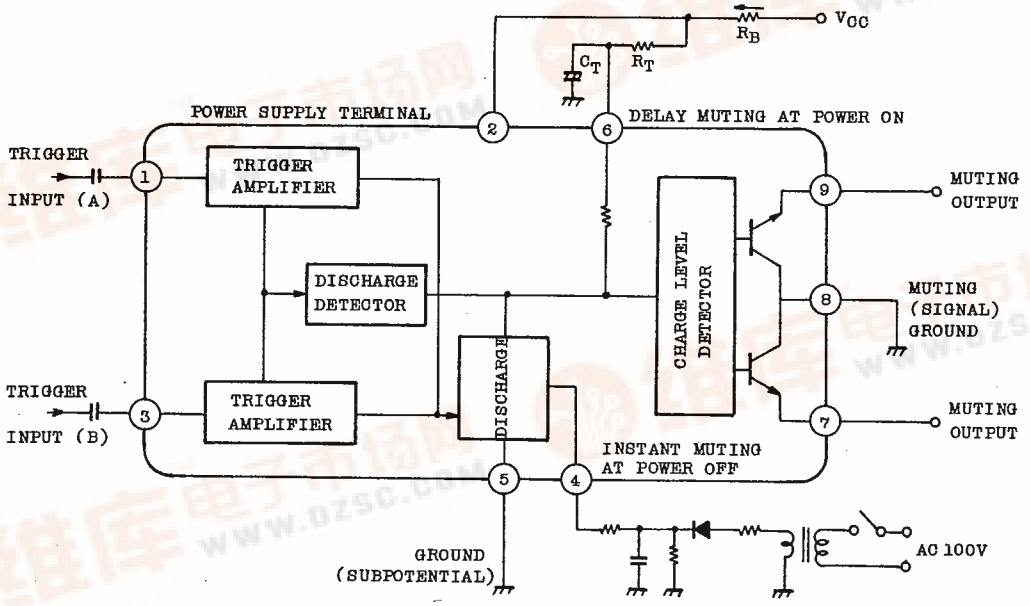
Unit in mm



Lead pitch is 2.54 and tolerance is ±0.25 against theoretical center of each lead that is obtained on the basis of No.1 lead.

JEDEC	—
TOSHIBA	S9A-P

BLOCK DIAGRAM



TA7324P

MAXIMUM RATINGS (Ta=25°C)

CHARACTERISTIC	SYMBOL	RATING	UNIT
Supply Voltage (V_{2-5}) (Note1)	V_{2-5}	3.4	V
Supply Current (I_2) (Note2)	I_2	20	mA
Power Dissipation (Note 3)	P_D	500	mW
Operating Temperature	T_{opr}	-20 ∿ 75	°C
Storage Temperature	Tstg	-55 ∿ 150	°C

Note 1. In case of constant voltage source.

Note 2. In case of constant current source.

Note 3. Derated above Ta=25°C in the proportion of 4mW/°C

The input voltage at the trigger terminal is GND-V_{BE}(≅0.7V)<input voltage ≤ V_{2-5}+V_{BE}.

When trigger terminals A and B are applied, must be set the operating supply current value from 5mA to 15mA.

ELECTRICAL CHARACTERISTICS (Ta=25°C, V_{CC}=18V, R_B=1.5kΩ)

CHARACTERISTEC	SYMBOL	TEST CIR-CUIT	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
Supply Terminal Voltage	V_{2-5}	1	Note 4 I_{CC}=20mA(CONST)	3.4	3.6	3.8	V
Trigger Sensitivity(A) V_1	±TRIGA	1	Note 6	±0.5	±0.7	±0.9	V
Trigger Sencitivity(B) V_3	±TRIGB	1	Note 7	±0.09	±0.12	±0.15	V
Trigger Sensitivity(A) I_1	±(I TRIG-A)	1	Note 6	-	±20	±60	uA
Trigger Sensitivity(B) I_3	±(I TRIG-B)	1	Note 7	-	±10	±30	uA
Detecting sensitivity at power OFF V_4	V_4 OFF	1	Note 8	-	0.75	1.0	V
Detecting current at power OFF	I_4 OFF	1	Note 8	-	6	-	uA
Output Saturation Voltage at muting ON V_7, V_9	V_{CE}(sat)	-	Note 9	-	18	40	mV
Max. Sink Current I_7, I_9	Imax			1.4	1.6	-	mA
Terminal Voltage (Pin 1)	V_1	1	Note 5	-	1.5	-	V
Terminal Voltage (Pin 2)	V_2			3.2	3.5	3.6	V
Terminal Voltage (Pin 3)	V_3				1.4	-	V
Terminal Voltage (Pin 6)			Muting OFF	2.6	2.7	2.8	V
Muting Attenuation	ATT	2	Note 10	45	50		dB
Muting Time at Power ON	M.T			-	1.8	-	sec

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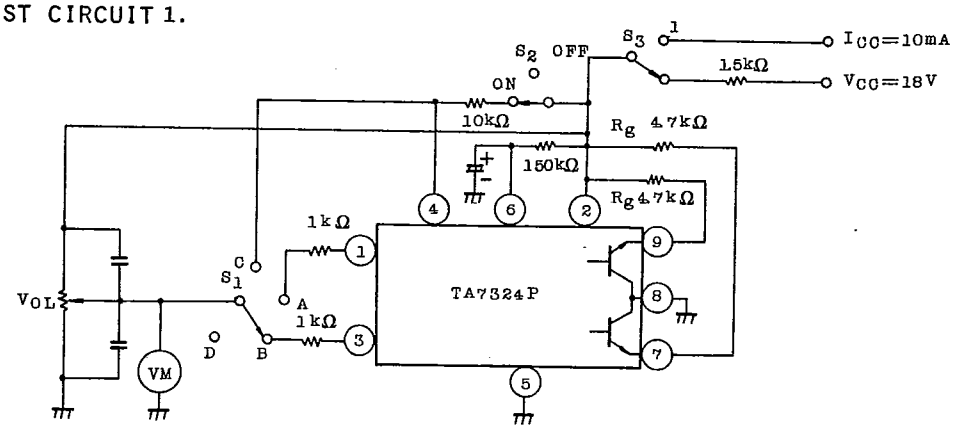
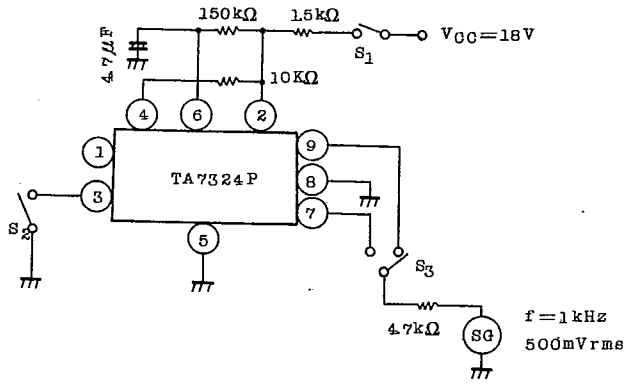
TEST CIRCUIT 1.



TEST CIRCUIT 2.



Note 4) Supply terminal Voltage (V_{2-5})

$S_1 \rightarrow$ D, $S_2 \rightarrow$ ON, $S_3 \rightarrow$ 1 (SW positions)

Read the voltage of pin 2 at I_{CC}=20mA.

Note 5) Terminal voltage (V_1, V_2, V_3, V_6)

$S_1 \rightarrow$ D, $S_2 \rightarrow$ ON, $S_3 \rightarrow$ V (SW positions)

Read each terminal voltage at the above SW position.

Note 6) Trigger sensitivity (A), Trigger current (A) <±TRIG-A, ±(I-TRIG-A)>

$S_1 \rightarrow A$, $S_2 \rightarrow ON$, $S_3 \rightarrow V$ (SW position)

Turn VOL gradually to increase the indication of VM from OV. In this case, pin 9 and pin 7 of the muting output terminal are at L level (about OV when output transistor is ON.). As the value of VM is increased, pin 9 and pin 7 are turned from "L" level to "H" level at a certain point (about 3.5mA when output transistor is OFF. In this case, if the value of VM is $V_{ML(A)}$ the negative trigger sensitivity (A) is given by the following equation:

Negative trigger sensitivity (A), $-TRIG-A=V_1-V_{MH(A)}$

If, after obtaining of the negative trigger sensitivity, the value of VM is further increased, pin 9 and pin 7 are re-turned from "H" level to "L" level.

In this case, if the indicating value of VM is $V_{MH(A)}$, the positive trigger sentivitity (A) is given as follows:

$+TRIG-A=V_{MH(A)}-V_1$

To measure the trigger current ±(I-TRIG-A), read the current of pin 1 at the measuring time of the $V_{ML(A)}$ and $V_{MH(A)}$ described above.

Note 7) Trigger sensitivity (B), trigger current (B) <±TRIG-B, ±(I-TRIG-B)>

$S_1 \rightarrow B$, $S_2 \rightarrow ON$, $S_3 \rightarrow V$ (SW position)

Measuring method is the same as mentioned in Note 5.

Negative trigger sensitivity, $-TRIG-B=V_3-V_{ML(B)}$

Positive trigger sensitivity, $-TRIG-B=V_{MH(B)}-V_3$

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Note 8) Detection sensitivity and current at power OFF (V_4OFF, I_4OFF)

$S_1 \rightarrow$ C, $S_2 \rightarrow$ OFF, $S_3 \rightarrow$ V (SW position)

Turn VOL gradually to increase the indicating value of VM from OV. When pin 9 and pin 7 of the muting output are turned from "L" level to "H" level, the value of VM comes to V_4. In this case, the current of pin 4 is I_4 OFF.

Note 9) Saturation voltage and maximum sink current at muting ON ($V_{CE(sat)}$, I_{Cmax})

$S_1 \rightarrow$ A or B, $S_2 \rightarrow$ ON, $S_3 \rightarrow$ V (SW position)

Measure the voltage and current of pin 9 and pin 7 when indicating value of VM is set to OV. (Set R_g=0 at measuring the current.)

Note 10) Muting attenuation and muting time at power ON (ATT, MT)

In the measuring circuit 2, the time from the instant when S_1 is ON (while S_2 remains OFF) and V_{CC} is applied to the circuit, to the moment when pin 9 and pin 7 are turned from "L" level to "H" level is taken as the muting time MT.

Measure the AC voltage at pin 9 or pin 7 with S_1 remains ON. In addition, turn S_2 ON, and measure the AC voltage at pin 9 or pin 7.

Muting attenuation $ATT = 20 \log \frac{\text{AC voltage at pin 7 (9) at } S_2 \text{ OFF}}{\text{AC voltage at pin 7 (9) at } S_2 \text{ ON}}$

TA7324P

CHARGE AND DISCHARGE LEVEL DETECTION

A built-in trigger amplifier is included in TA7324P for responding either to positive or negative pulse. In the trigger amplifier, two amplifiers are mounted in parallel; one is responding at a small level, while the other is responding at a large level. Both amplifiers are coupled to the discharge level detector circuit as shown Fig. 1 respectively.

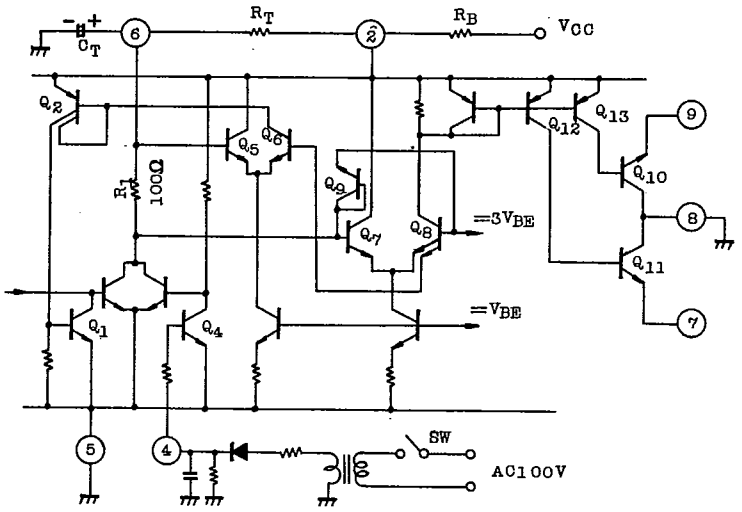

Fig.1 Charge and Discharge Level Equivalent Circuit

The discharge level detector circuit forms a flip-flop discharge circuit. The circuit is designed so that the trigger pulse width to discharge circuit may be maintained beyond constant width to discharge fully the charge of CT (Capacitor for muting and charging operation) even when the smaller width pulse is given to the trigger amplifier.

Charge operation and muting operation are described as follows:

1. OPERATION AT POWER (V_{CC}) ON (REFER TO FIG.2)

As soon as the power supply (V_{CC}) is ON, C_T starts to be charged through R_T and the potential V_6 on pin 6 rises gradually, in this case, Q_8 remains conductive till the base potential of Q_7 becomes equal to or more than the base potential (3 $V_{BE} \cong 2.1V$) of Q_8 and the muting operation is carried on by putting the muting output T_R Q_{10} and Q_{11} to ON position.

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When the base potential of Q_7 rises higher than that of Q_8, the Q_8, Q_{10} and Q_{11} are OFF to release the muting operation. CT charge stops at such a level as the base potential of Q_7 is V_{BE} (≅0.7V) higher than that of Q_8.

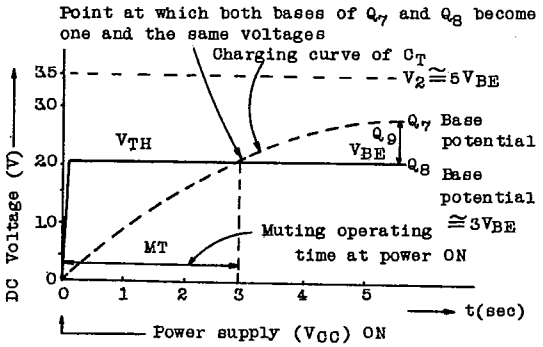

Fig. 2 Operating Potential of Each Part at Power ON

Q_1 : For discharge stop

Q_2 : For Q_1 drive

Q_3 and Q_3' : For discharge

Q_4 : For muting operation at power OFF

Q_5 and Q_6 : Discharge level detecting differenctial

Q_7 and Q_8 : For charge level detection and muting output stage drive

Q_9 : For charge level limit

Q_{10} and Q_{11} : Output T_R for muting

2. MUTING OPERATION BY TRIGGER A OR B (REFER TO FIG.3)

When a pulse from the trigger amplifier comes in Q_3 base, Q_3 is ON to discharge the charge from C_T through R_1(=100Ω). When the discharge level of C_T(Q_7 base potential) drops lower than the base potential of Q_8 ($3V_{BE}$≅2.1V), the Q_8, Q_{10}, and Q_{11} are turned ON to start the muting operation in which R_1 is designed for accelerating the speed to start muting operation.

When more discharge is carried on from C_T, if Q_5 base potential drops lower than Q_6 base potential ($2V_{BE}$≅1.4V), the Q_6, Q_2, and Q_1 are turned ON to stop discharging by shortening Q_3 base. (Q_1 acts also as a flip-flop operating reverse potential.)

When discharging stops, charging to C_T starts through R_T. When the base potential of Q_5 rises higher than that of Q_6, the Q_6, Q_2, and Q_1 are turned OFF.

When C_T is more charged, the base potential of Q_7 rises higher than that of Q_8, and the Q_8, Q_{10}, and Q_{11} are turned OFF to release the muting.

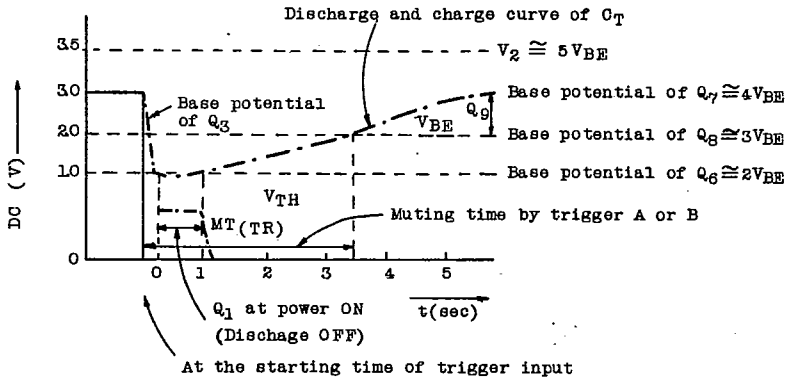

Fig. 3 Respective Operating Potentials at Muting by Trigger (A) or (B)

3. MUTING AT POWER OFF

When the power supply is ON, rectification from AC makes Q_4 ON and Q_3 OFF.

When AC is OFF, Q_4 is OFF and Q_3' is ON to dischage C_T for stating muting operation.

TA7324P

APPLICATION

1 SUPPLY VOLTAGE (V_{2-5}) AND SUPPLY CURRENT (I_2)

TA7324P contains a regulated power supply. Therefore, as shown in Fig. 4, the voltage is applied to pin 2 through the resistor R_B. The supply current I_2 is, in this case, adjusted to about 10mA by difining the value of R_B.

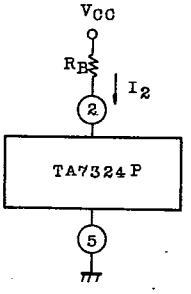

Fig. 4 Adding bias to Pin 2

According to V_{2-5} to I_2 characteristics shown in Fig. 1, when I_2 = 10mA, $V_{2-5} \cong 3.5V$ is given.

Thus, $R_B \cong \frac{V_{CC} - V_{2-5}}{10}$ (kΩ)

For muting operation $V_{2-5} \gtrsim 2.8V$ is required. As shown in Fig.1 if the current of $I_2 \gtrsim 3mA$ is flown, the muting function starts operating.

2. TRIGGER SENSITIVITY

Trigger sensitivity means the absolute value in the difference between the trigger terminal voltage at the start and the open voltage of trigger terminal. (Refer to Fig. 5.)

Trigger current is the value of current flowing into or from the trigger terminal at start of triggering.

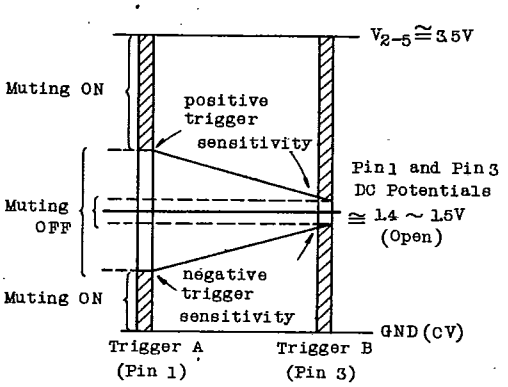

Fig. 5 Trigger Level

In TA7324P, the circuit is designed for discharging securely the timing capacitor even if a trigger of extremely narrow width is applied to the trigger input terminal. Consequently, the trigger is applied to even the input of pulse width less than 1ms, so that an erroneous operation may be caused when by a hair-like pulse is applied

to the trigger input terminal from the power supply or other sources. To prevent such erroneous operation, an integrated circuit of CR may be required to be provided to the input. In addition, trigger snesitivity varies according to temperature and voltage of V_{2-5}; therefore, such variation should be considered before designing. Trigger terminal impedance is 15kΩ∿25kΩ at start of triggering. I_2=5∿15mA is recommended for pin 1 or pin 3 because muting may not be restored after triggering to mute if I_2=15mA or more is applied.

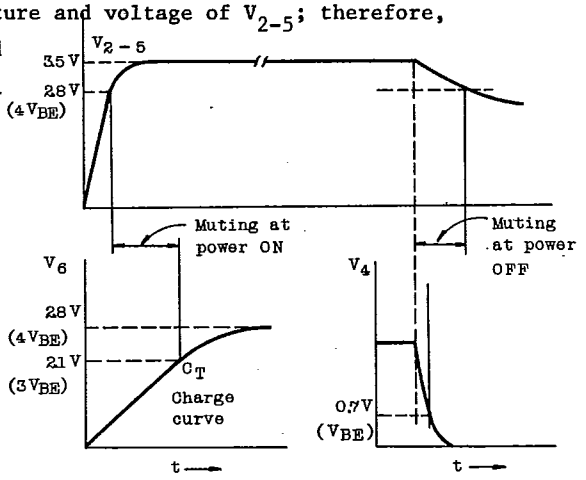

Fig. 6 Muting Operation at Power ON - OFF

3. MUTING AT POWER ON/OFF

(Refer to Fig. 6)

3.1 MUTING AT POWER ON

Muting at power ON continues till V_{2-5} is over about. 2.8V ($4V_{BE}$), Q_{12} and Q_{13} are turned ON, the timing capacitor C_T is charged, and the base potential of Q_7 rises to about 2.1V ($5V_{BE}$). Therefore, early rise is recommended for V_{2-5} potential.

3.2 MUTING AT POWER OFF

Muting at power OFF starts operating by decreasing the detecting terminal (pin 4) at OFF to about 0.7V or less (making Q_4 OFF.) Therefore, such a signal as is more than 0.7V in normal operation but turned to less than 0.7V instantly at power OFF, is required to be made.

Muting at power OFF starts operating at the time when pin 4 potential becomes less than 0.7V and continues till V_{2-5} becomes 2.8V or less. Therefore, the slow falling of V_{2-5} is more effective.

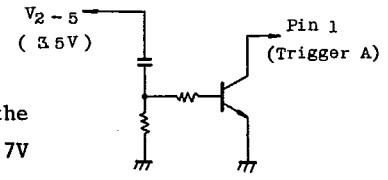

Fig. 7 Lengthening Way of Muting Time

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The detecting terminal at power OFF (pin 4) is available for trigger input; however, it is recommended that this terminal be linearly triggered as much as possible, because a narrower width pulse may miss ample discharge from the timing capacitor.

4. MUTING TIME

Muting time at power ON and casused by trigger is decided by the timing C_T and R_T. With the consideration for Q_5 and Q_7 base currents, the following are roughly given:

Muting time at power ON : $MT_{(ON)} \cong 1.3R_TC_T$

Muting time by trigger : $MT_{(TR)} \cong 0.45R_TC_T$

Here, if muting time is lengthened by setting R_TC_T time constant larger, distorted waves asymmetrical with respect to top and bottom may be originated by the slow speed of wave rise at muting OFF. Experiment tells that $MT_{(ON)} \cong 1.4$sec (R_T=220kΩ and C_T=4.7μF) or less has brought a good result.

When $MT_{(ON)}$ is required especially to be made longer, a method of applying the trigger terminal as shown in Fig. 7 and another method of giving a signal of slow rise to the detecting terminal at power OFF (pin 4) are considered. To activate a continuous muting, the DC voltage to make muting ON should be applied to trigger A or B, or the voltage of the detecting terminal at power OFF (pin 4) should be decreased to make Q_4 OFF.

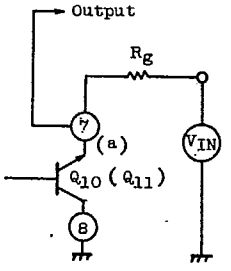

Fig. 8 Muting Output

5. SINGNAL LEVEL FOR MUTING AND ATTENUATION

Since peak value (half wave) and attenuation of signal for muting are decided according to the following conditions, the value of R_g is properly required for operation.

- o At muting ON, $V_{IN(peak)} \fallingdotseq R_g \cdot I_{max}$

  I_{max} is minimum value of maximum sink current.

- o At muting OFF, peak value and attenuation are decided by emitter-base reverse voltage of $Q_{10(Q11)}$, and the equation, $V_{IN(peak)} \leqq 5V$, is given.

- o Let $Q_{10(Q11)}$ saturating resistance be R_S, muting attenuation is given by

  Muting attenuation: $ATT = -20\log R_S/R_g$ $R_S \fallingdotseq (V_{CE(sat)}/I_{max})$

6. EXAMPLE OF APPLICATION (APPLIED TO A PRESET TUNER)

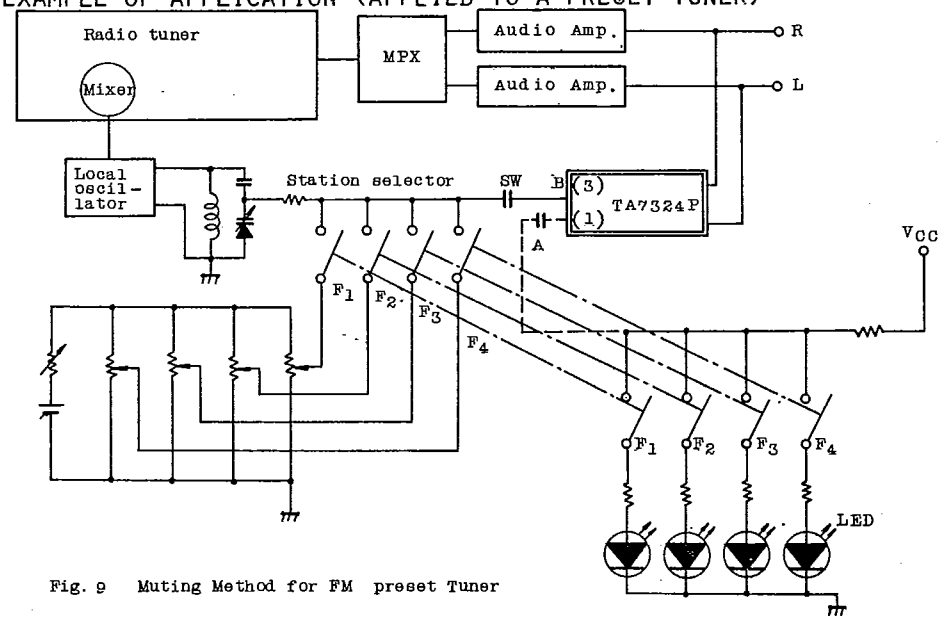

Fig. 9 Muting Method for FM preset Tuner

(1) Utilization of voltage variation added to the variable capacitance diode
(2) Utilization of voltage variation caused by station indicator LED

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In case of an FM preset tuner as shown in Fig. 9, station selection from F_1 to F_2 by the preset station selector switch provides a drastic variation to the voltage applied to variable capacitance diode.

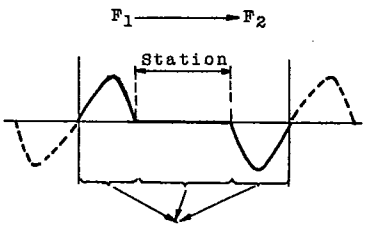


Fig. 10 'Buzz' Sound in Present Type

Accordingly, all of the detector DC voltage variation traced in and out the FM"S"curve and noise between stations as shown in Fig. 10 come out as "buzz" sound.

- In case of the above FM preset tuner equipped with a non-shorting type switch for station selection and the station indicator LED (or an indicator lamp), only LED voltage detection can operate muting securely by using the terminal 1 of TA7324P, that is, the trigger A, as shown by the dotted line in Fig. 9.

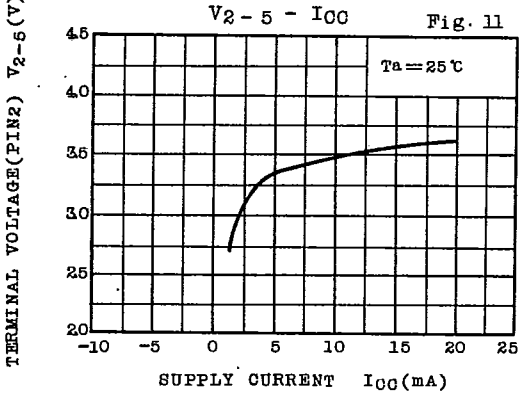
  For example, in case of presetting from F_1 to F_2, after SW of F_1 turned OFF, SW of F_2 becomes ON; therefore, detection of switch OFF of F_1 permits the muting operation to be performed.

- Even in case of using a shorting type switch, if the contact of indicator SW linked with the preset SW is securely ON several milli second ahead, the muting operation can be performed by voltage variation originated at LED ON. If the shorting type switch cannot securely make the other switch ON, the muting starts operating by detecting the voltage variation of variable capacitance by applying the terminal 3 of TA7324P, the trigger B, as shown by the solid line in Fig. 9.

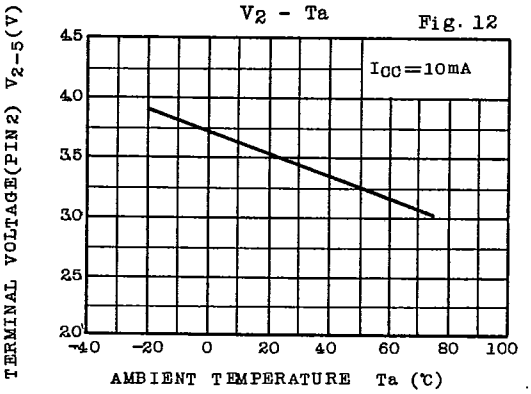
  However, in case where F_1 and F_2 are the same station or close stations at reception each other, no muting can be operated. (Variation is within several mV of variable capacitance diode voltage.)

TA7324P

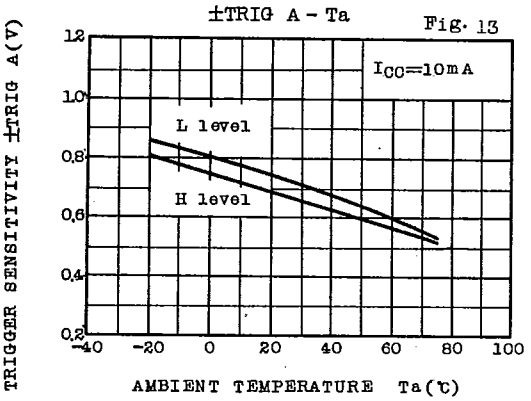
V_{2-5} - I_{CC} Fig. 11



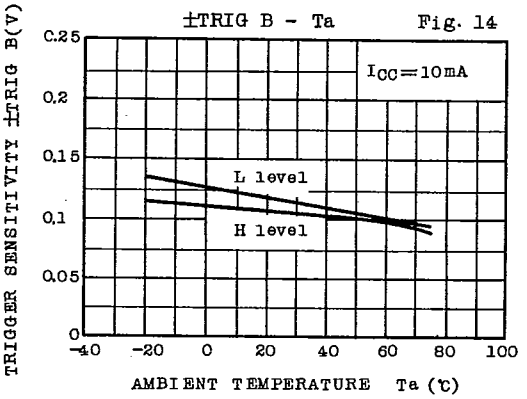
V_2 - Ta Fig. 12



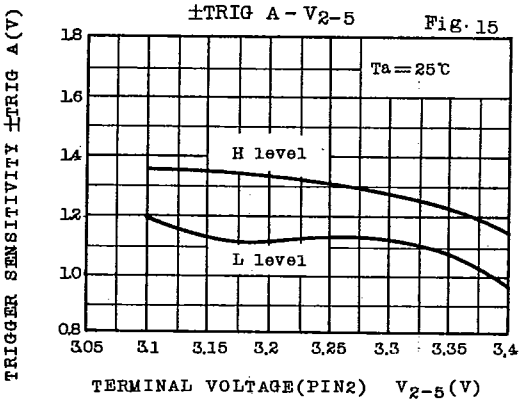
±TRIG A - Ta Fig. 13



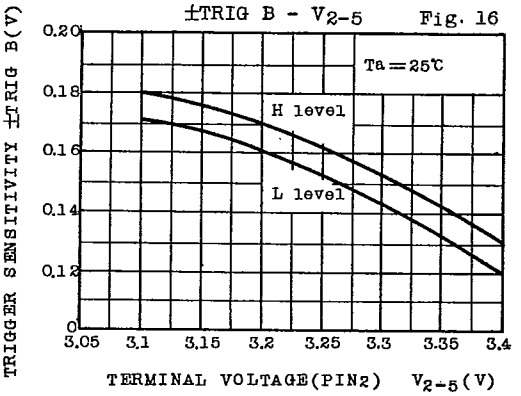
±TRIG B - Ta Fig. 14



±TRIG A - V_{2-5} Fig. 15



±TRIG B - V_{2-5} Fig. 16



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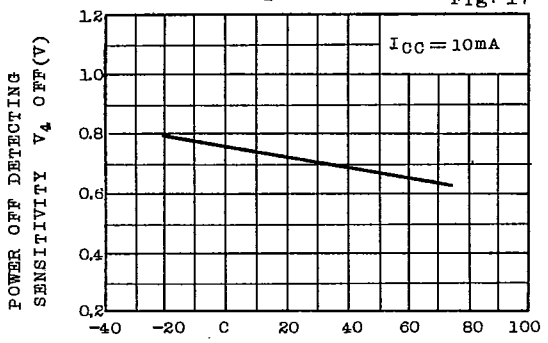
V_4 OFF - Ta Fig. 17



ATT - R_g Fig. 18