FH3308 **VER 2.1**

8 Port 10Mb stackable Hub Controller

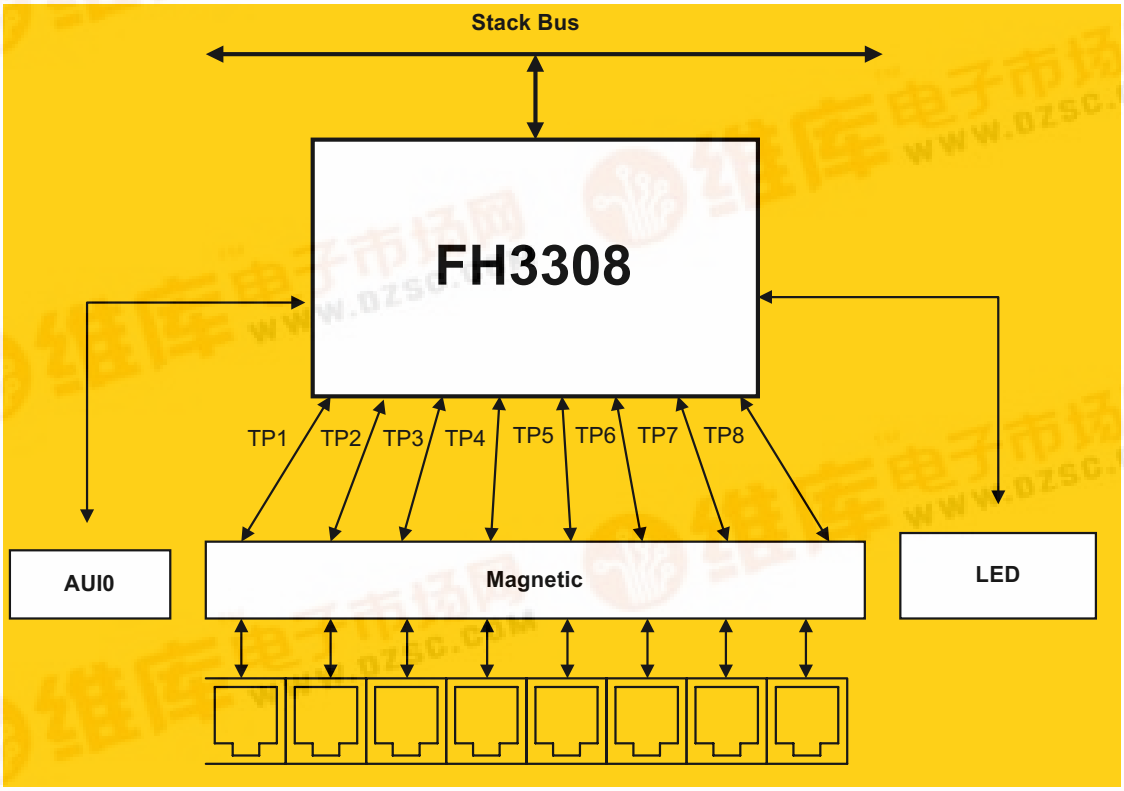
General Description

The FH3308 is a highly integrated Hub Controller designed for mixed-media network. It provided all active circuitry required for the repeater function specified in IEEE 802.3 standard in one single CMOS device. It includes eight 10BASE-T transceivers, one Attachment Unit Interface (AUI) port and one cascade bus. The AUI port allows connection of external transceiver (10BASE2, 10BASE5, 10BASE-T, FOIRL) or a drop cable. The stack Bus allows more FH3308 to be cascaded together to increase the total number of hub ports. FH3308 offers rich-set of LED display outputs. They can provide a friendly interface to recognize the network status.

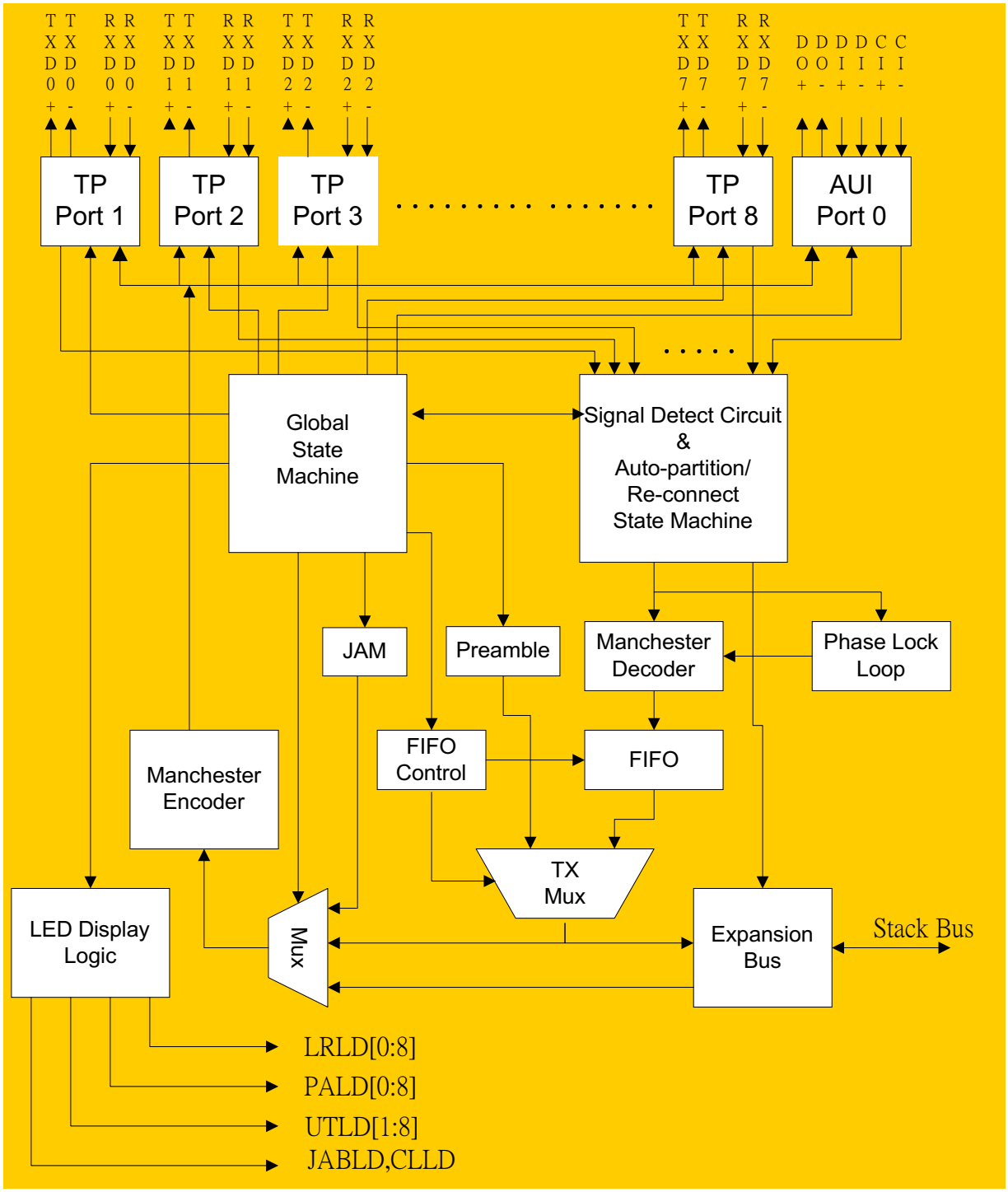
Features

- IEEE802.3 (1998 Edition) compliant
- Eight 10BASE-T transceivers and one AUI port included in one single chip.
- Stack® Bus provides large cascade hub application.
- On-chip FIFO, PLL, Manchester encoder/decoder
- Automatic polarity detection and correction
- Automatic partitioning of faulty ports
- Rich-function LED drivers support for per port Link, Activity, partition, global Jabber, collision status and network utilization.
- Embedded pre-distortion resistor for every TP port
- Low Power CMOS technology with a single +5V supply
- 100-pin QFP

System Diagram



Block Diagram



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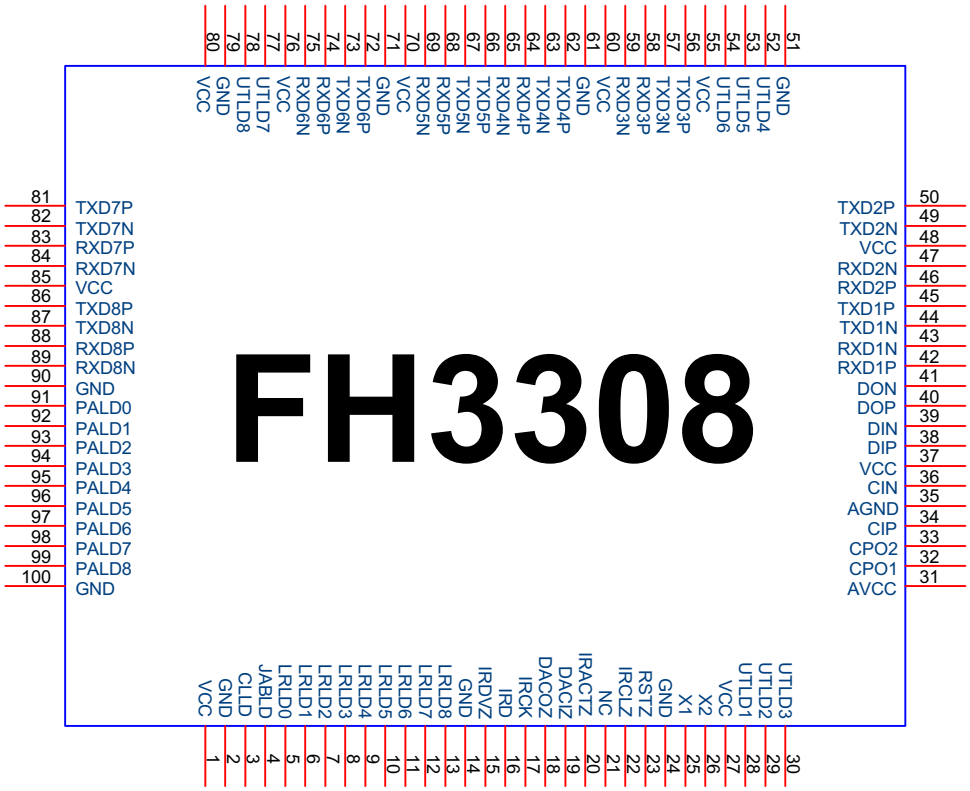
1.0 PIN Assignment



2.0 PIN Description

2.1 Network Interface Pins

Signal Name	Type	Pin No	Description
TXD1P	O	45	**Twisted-Pair Data Outputs (Positive and Negative):**
TXD1N	O	44	These pins are positive (TXD1P-TXD8P) and negative (TXD1N-TXD8N) outputs to the network from the respective twisted-pair ports.
TXD2P	O	50	
TXD2N	O	49	
TXD3P	O	56	
TXD3N	O	57	
TXD4P	O	62	
TXD4N	O	63	
TXD5P	O	66	
TXD5N	O	67	
TXD6P	O	72	
TXD6N	O	73	
TXD7P	O	81	
TXD7N	O	82	
TXD8P	O	86	
TXD8N	O	87	
RXD1P	I	42	**Twisted-Pair Data Inputs (Positive and Negative):**
RXD1N	I	43	These pins are positive (RXD1P-RXD8P) and negative (RXD1N-RXD8N) inputs from the network to the respective twisted-pair ports.
RXD2P	I	46	
RXD2N	I	47	
RXD3P	I	58	
RXD3N	I	59	
RXD4P	I	64	
RXD4N	I	65	
RXD5P	I	68	
RXD5N	I	69	
RXD6P	I	74	
RXD6N	I	75	
RXD7P	I	83	
RXD7N	I	84	
RXD8P	I	88	
RXD8N	I	89	
DOP	O	40	**AUI Data Output (Positive and Negative):**
DON	O	41	These pins are positive and negative data outputs for AUI port.
DIP	I	38	**AUI Data Input (Positive and Negative):**
DIN	I	39	These pins are positive and negative data inputs for AUI port.
CIP	I	34	**AUI Collision Input (Positive and Negative):**
CIN	I	36	These pins are positive and negative collision inputs for AUI port.

2.2 LED Drivers

Signal Name	Type	Pin No	Description
CLLD	O 8mA	3	**Global Collision LED Driver (Active Low):** The output pin is used to indicate the status of collision activity.
JABLD	O 8mA	4	**Jabber LED Driver (Active Low):** LED Mode 0,2 This output pin will go active when any TP port is in partition state or excessive network traffic. It will not drive low if AUI port is in partition state. LED Mode 1 The pin is configured to indicate the status of Jabber.
UTLD1/LED_SEL0/ ACTIVITY UTLD2 UTLD3 UTLD4/LED_SEL1 UTLD5 UTLD6 UTLD7 UTLD8	O 8mA	28 29 30 52 53 54 77 78	**Utilization LED Drives (Active Low):** These pins are used to indicate how much your network is being used. UTLD1 ≦1% UTLD2 2% UTLD3 3% UTLD4 6% UTLD5 12% UTLD6 25% UTLD7 50% UTLD8 80% UTLD1/LED_S and UTLD4/LED_S1 are also used to configure the LED mode during power on reset. These two pins have internal pull high resistor. UTLD4/LED_S1 UTLD1/LED_S0 1 1 Mode 0 1 0 Mode 1 0 1 Mode 2 0 0 Mode 0 On LED mode 2, UTLD1/LED_SEL0/ACTIVITY pin is configured to indicate the status of receives.
LRLD0 LRLD1 LRLD2 LRLD3 LRLD4 LRLD5 LRLD6 LRLD7 LRLD8	O 8mA	5 6 7 8 9 10 11 12 13	**Link_Receive/Link/Receive LED Drivers: (Active Low)** These pins provide 3 different status indications depending on LED mode selection. LED Mode 0: LRLD1-LRLD8 are configured to indicate Link status of ports on mode 0.These pins go active when Link integrity test is pass on TP port. LRLD0 don't carry any status indication on the mode. LED Mode 1: LRLD1-LRLD8 LEDs go active when Link integrity test is pass on TP port and blinking when there are packets come in the port. LRLD0 indicate the status of AUI port receives. LED Mode 2: These pins indicate the status of receives. These LEDs will blink when packet receiving.

PALD0 PALD1 PALD2 PALD3 PALD4 PALD5 PALD6 PALD7 PALD8	O 8mA	91 92 93 94 95 96 97 98 99	**Partition/Link LED Drivers (Active Low):** LED mode 0 and 1 These pins indicate the status of partition. LED mode 2 PALD1-PALD8 go active when the link integrity test passes on the TP port. PALD0 don't indicate any status on the mode.

2.3 Miscellaneous Pins

Signal Name	Type	Pin No	Description
RSTZ	I IPU	23	**RESET (Active-Low):** This chip is reset when this signal is asserted low.
X1	I	25	**System Clock Input:** An external 20MHz clock source is connected to this pin to provide the operating clock. For crystal application, a 20MHz crystal should be connected to pins X1 and X2, and Both X1 and X2 should be tied to ground through a capacitor (10pF-33pF). One feedback resistor (1MΩ) is suggested to connect between X1 and X2.
X2	O	26	**Crystal Clock feedback:** The pin should be connected to crystal. Pin X2 should left floating when external oscillator is connected to X1.
CPO1 CPO2	I I	32 33	**Phase Lock Loop External Filter:** CPO1 should be left float. CPO2 is suggested to connect with a capacitor to AVCC. (Please Reference to application note of FH3308)
NC	O	21	**NC:** Let the pin float

2.4 Stack® Bus

Signal Name	Type	Pin No	Description
IRDVZ	I/O/Z, IPU, 16mA	15	**INTER REPEATER DATA VALID (Active-Low):** This signal carries the inverted RX_DV state across the inter repeater bus. It is used to frame good packets.
IRCK	I/O/Z, IPD, 16mA	17	**INTER REPEATER CLOCK:** All inter repeater signals are synchronized to the rising edge of this clock.
IRD	I/O/Z, IPD, 16mA	16	**INTER REPEATER DATA:** Serial data input/output. Transfers data from the active FH3308 to all other "inactive" FH3308 by Stack® Bus.
IRACTZ	I/O/Z, IPU, 16mA	20	**INTER REPEATER ACTIVITY (Active-Low):** This signal is asserted when the repeater senses network activity. The pin should be pulled high through a 2.4K resistor.
IRCLZ	I/O/Z, IPU, 16mA	22	**INTER REPEATER COLLISION (Active-Low):** Asserted when the FH3308 senses two or more ports are receiving or one or more ports and Stack® Bus is active simultaneously. It also monitors the line to know whether other Stack® Bus has detected a collision. The pin should be pulled high through a 2.4K resistor.
DACOZ	O, 8mA	18	**Daisy Chain ACTIVITY OUT (Active-Low):** Cascade (Daisy chain) activity out. Connect to another FH3308 Stack® Bus's Cascade (Daisy chain) activity in.
DACIZ	I, IPU	19	**Daisy Chain ACTIVITY IN (Active-Low):** Cascade (Daisy chain) activity in. Connect to another FH3308 Stack® Bus's Cascade (Daisy chain) activity out. The pin should be pulled high through a 2.4K resistor.

2.5 Power & Ground Pins

Signal Name	Type	Pin No	Description
VCC	P	1,27,37, 48,55,60, 70,76,80, 85	5V Power pins. + 10%, - 5%
GND	G	2,14,24, 51,61,71, 79,90, 100	GND pins
AVCC	P	31	Analog power pins.
AGND	G	35	Analog ground pins.

2.6 Pin Type Designation

Pin Type	Description
I	Input buffer.
O	Output buffer, driven high or low at all times.
I/O/Z	Bi-directional buffer with high-impedance output.
O/Z	Output buffer with high-impedance capability.
OC	Open collector like signals. These buffers are either low or in a high-impedance state.
8mA	Output medium/low drive : 8 mA.
16mA	Output medium drive : 16 mA.
IPU	Internal 75K Ohm pull-up
IPD	Internal 75K Ohm pull-down
P/G	Power / Ground

3.0 FUNCTIONAL DESCRIPTION

The FH3308 implements the repeater function specified in the IEEE 802.3 standard. It included eight integral 10BASE-T ports plus one AUI port. FH3308 is also expandable; allows the implementation of high port count repeater. The following sections describe the different main functional blocks of FH3308 repeater Controller.

3.1 10BASE-T Ports

Eight 10BASE-T transceivers are completely self-contained. Each individual 10BASE-T transceiver is compliment to IEEE 802.3 10BASE-T standard. Since filtering is performed in the chip, only simple expansive transformer is required to complete the 10BASE-T interface.

3.2 AUI Port

The AUI port is fully compatible with IEEE 802.3, section 7 requirements for an AUI port. The AUI port provides an interface to connect to 10BASE-2, 10BASE-5, FORIL external Medium Attachment Unit. 10BASE-2 or 10BASE-5 Ethernet can easily connect to 10BASE-T network by the interface.

3.3 REPEATER GLOBAL STATE MACHINE

The basic repeater circuitry is shared with all the ports in FH3308. It included repeater global state machine, timer, counter and timing recovery circuit. The timing recovery circuit also includes a FIFO to retiming the data. The Repeater State Machine (RSM) is the main block that governs the overall operation of the repeater. At any time, the RSM is in one of the following four states: Idle, Repeat, Collision, or One Port Left.

3.3.1 Idle State

The RSM enters this state after reset or when there is no activity on the network and carrier sense is not present. The RSM exits this state if the above conditions are no longer true.

3.3.2 Repeat State

This state is entered when there is a reception on only one of the ports, port N. While in this state, the data is transmitted to all the ports but the reception port (port N). The RSM returns to Idle State when the reception ends, or transitions to collision state if there is reception activity on more than one port.

3.3.3 Collision State

When there is receive activity on more than one port of the repeater, the RSM moves to Collision State. In this state, transmit data is replaced by Jam and sent out to all ports including the original port N. There are two ways for the repeater to leave the Collision State. The first is when there is no receive activity on any of the ports. In this case the repeater moves to Idle State. The second is when there is only one port experiencing collision in which case the repeater enters the One Port Left State.

3.3.4 One Port Left State

This state is entered only from the Collision State. While in this state, Jam is sent out to all ports except the port that has the receive activity. If more receive activity occurs on any other port, then the repeater moves to Collision State, otherwise it will transition to Idle State when the receive activity ends.

3.4 Signal Detect Circuit

When any one port has received activity, the RXE (receive enable) is activated. If multiple ports are active, i.e. a collision scenario, then RXE will not be enabled for any one port. The Port Select Logic asserts the open-collector outputs IRCLZ and IRACTZ to indicate to other cascaded FH3308 that there is collision or receive activity present on this FH3308.

3.5 TXE CONTROL

This control logic enables the appropriate port for data transmission according to the four states of the RSM. That is, during Idle State, no ports are enabled; during Repeat State, all ports but port N are enabled; in Collision State, all ports including port N are enabled; during One Port Left State all ports except the port experiencing the collision, will be enabled.

3.6 DATA PATH

After the port selection logic has enabled the active port, receive data, receive clock and receive data valid will flow through the chip from that port out onto all the other ports and the Inter Repeater Bus (Stack® Bus for FH3308 only), if no collisions are present. The signals on the Stack® Bus flow either in to or out of the chip depending upon the Repeater ' s state.

If the FH3308 is currently receiving and no collisions are present, the Stack® Bus signals flow out of the chip. The chip's Arbitration Logic guarantees that only one chip will gain ownership of the Stack® Bus. In all other states, the Stack® Bus signals are inputs.

3.7 JABBER PROTECTION STATE MACHINE

The device will automatically terminate all transmit activity for at least 96 bit times (unjabber time) if any input port is active for more than 65536bT (bit times).

3.8 AUTO-PARTITION STATE MACHINE

In order to protect the network from a port that is experiencing excessive consecutive collisions, each port has its own auto-partition state machine.

A port with excessive consecutive collisions will be partitioned after 32 consecutive collisions occur on that port. Transmitting ports will not be affected.

A partitioned port will be reconnected when a collision-free packet of length 512 bits or more is transmitted or received.

3.7 FH3308 Stack® Bus Interface

The Stack® Bus is used to connect multiple FH3308 together to form a logical repeater unit. The Stack® Bus allows received data packets to be transferred from the receiving cascaded devices to the other Stack® Bus devices in the system. Notification of collisions to other cascaded FH3308 is as important as data transfer across the network. The Stack® Bus has a set of status lines capable of conveying collision information between FH3308 to ensure their main state machines operate in the appropriate manner.

The FH3308 Stack® Bus consists of the following signals:

- Inter Repeater Data**:** This is the transfer data, in serial format, from the active FH3308 to all other cascaded FH3308.
- Inter Repeater Data Valid (IRDVZ)**:** This signal is used to frame good packets.
- Inter Repeater Data Clock (IRCK)**:** All FH3308 Stack® Bus data is synchronized to this clock.
- Inter Repeater Activity (IRACTZ)**:** When there is network activity the FH3308 asserts this signal in output mode. Normally the pin is in input mode
- Inter Repeater Collision (IRCLZ)**:** If there are multiple receptions on ports of a FH3308 or if the device senses concurrent activity on another cascaded device from Cascade Activity In (DACI) it asserts this output. This input indicates that one of the cascaded FH3308 is experiencing a collision.
- Cascade Activity Out. (Daisy Chain out) (DACOZ): Connect to the DACI (Daisy Chain Input) of another Cascaded FH3308.
- Cascade Activity In. (Daisy Chain in). (DACIZ): Connect to DACO of another Cascaded FH3308.

3.9 LED Interface

FH3308 supports rich-function LED driver, each driver can drive LED directly. They include Link, receive activity, partition, utilization and Jabber status indication. These LED function provide a friendly interface for user to recognize the network status easily. Setting of UTLD1/LEDSEL0 and UTLD4/LEDSEL1 can configure these LED drivers to 3 different modes during power on reset. These two pins have internal pull-high resistor, LED Mode 0 will be the default mode if no external pull-low resistors are tied to these pins.

UTLD4/LEDSEL1	UTLD1/LEDSEL0	LED Mode
1	1	0
1	0	1
0	1	2
0	0	0

3.9.1 LED Mode 0

Signal Name	Description	Global/Port LED
LRLD0-LRLD8	Link status indication: LRLD1-LRLD8 will go active when Link test pass on the TP port. LRLD0 didn't carry any indication in the mode.	Port
PALD0-PALD8	Partition status indication: These LED drivers go active when the port enters the partition state.	Port
UTLD1-UTLD8	Network utilization indication: These LED drivers indicate the network traffic status. UTLD1 ≦1% UTLD2 2% UTLD3 3% UTLD4 6% UTLD5 12% UTLD6 25% UTLD7 50% UTLD8 80%	Global
CLLD	Collision indication: The LED goes active when a collision is detected on the network.	Global

3.9.2 LED Mode 1

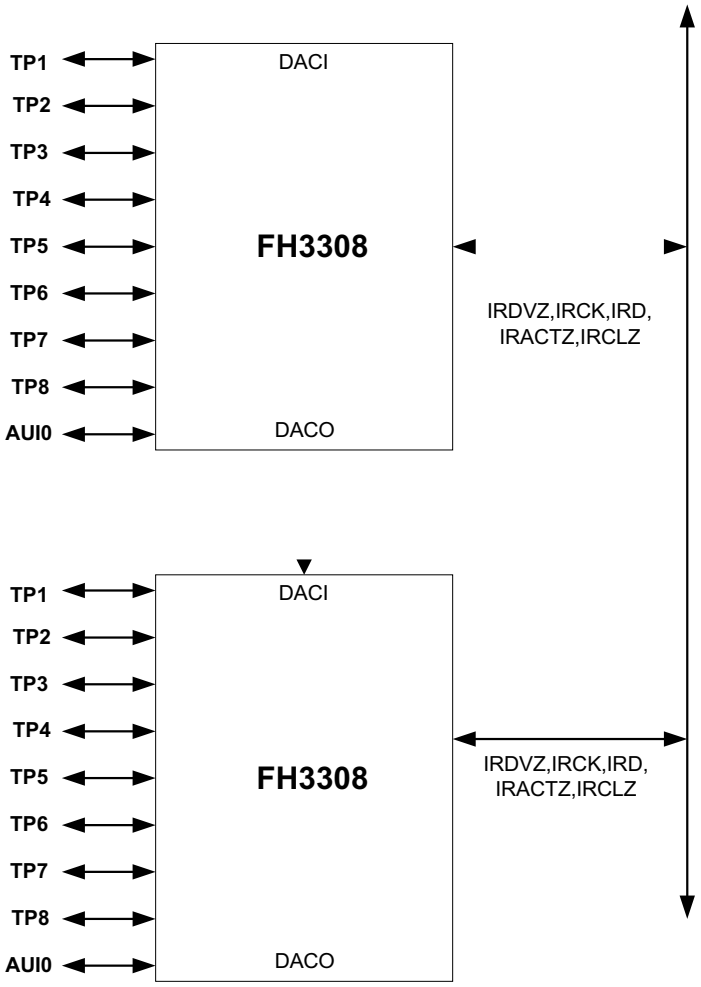
Signal Name	Description	Global/Port LED
LRLD0-LRLD8	Link status and Receive activity indication: These LEDs go active when link test pass on the port and blinking when network activity is detected on the port. LRLD0 indicates the receive activity of the AUI port.	Port
PALD0-PALD8	Partition status indication: These LED drivers go active when the port enters the partition state.	Port
UTLD1-UTLD8	Network utilization indication: These LED drivers indicate the network traffic status. UTLD1 ≦1% UTLD2 2% UTLD3 3% UTLD4 6% UTLD5 12% UTLD6 25% UTLD7 50% UTLD8 80%	Global
JABLD	Jabber LED: The LED indicates the Jabber status.	Global
CLLD	Collision indication: The LED goes active when a collision is detected on the network.	Global

3.9.3 LED Mode 2

Signal Name	Description	Global/Port LED
LRLD0-LRLD8	Receive activity indication: These LED blinking when network activity is detected on the port.	Port
PALD0-PALD8	Link status indication: PALD1-PALD8 will go active when Link test pass on the port. PALD0 didn't carry any indication in the mode.	Port
UTLD1-UTLD8	Network utilization indication: These LED drivers indicate the network traffic status. UTLD1 ≦1% UTLD2 2% UTLD3 3% UTLD4 6% UTLD5 12% UTLD6 25% UTLD7 50% UTLD8 80%	Global
CLLD	Collision indication: The LED goes active when a collision is detected on the network.	Global

4.0 Applications

Stack® Bus Application



5.0 AC AND DC SPECIFICATIONS

5.1 DC SPECIFICATIONS

Symbol	Parameter	Conditions	Min	Max	Units
V_{OH}	Minimum High Level Output Voltage	I_{OH} = -8 to -16 mA	2.4		V
V_{OL}	Minimum Low Level Output Voltage	I_{OL} = 8 to 16 mA		0.4	V
V_{IH}	Minimum High Level Input Voltage	TTL Input	2.0		V
V_{IL}	Maximum Low Level Input Voltage	TTL Input		0.8	V
I_{IN}	Input Current	With Internal Pull-up		±150	µA
		Without Internal Pull-up		±10	
I_{OZ}	TRI-STATE Output Leakage Current	With Internal Pull-up		±150	µA
		Without Internal Pull-up		±10	
I_{CC}	Average Supply Current	Typical V_{CC} = 5V	-	-	mA

5.2 AC Specifications

Note : All AC timings given are based on calculations. They are not the result of device characterization so cannot be guaranteed over temperature or supply voltage variations.

5.2.1 Clock Timing

Parameter	Description	Notes	Min	Typ	Max	units
t_{CK_CYC}	System Clock cycle time			50		ns
t_{CK_DC}	System Clock duty cycle		40		60	%
	System Clock Tolerance				±50	ppm
T_{reset_pd}	Reset Time		10			µs

5.2.2 AUI Electrical Characteristic

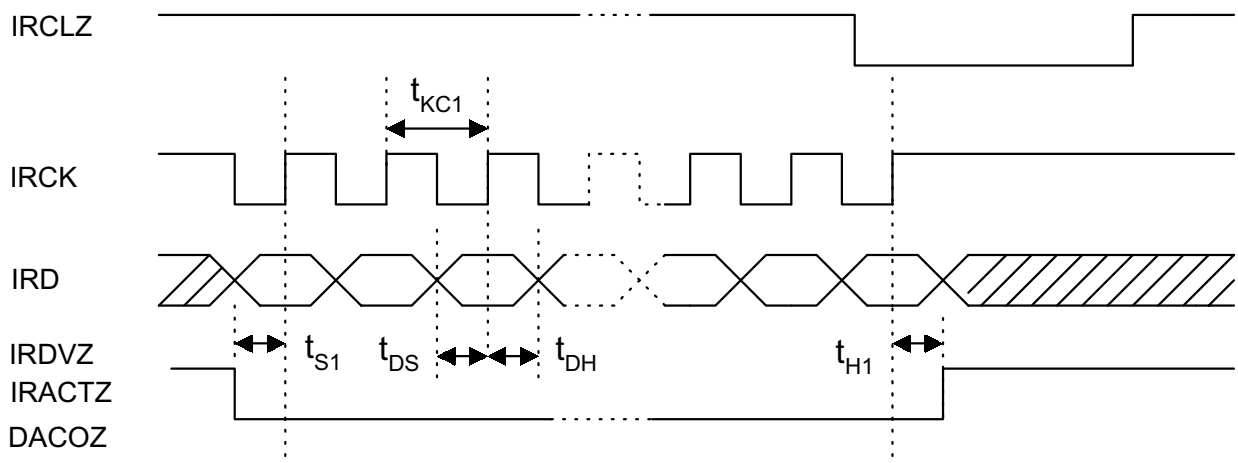
Parameter	Description	Notes	Min	Typ	Max	units
V_{OD}	Differential output voltage		±500	-	±1200	mV
Z_{IN}	Receive input impedance		-	20K	-	Ω
V_{DS}	Differential squelch threshold			220		mV

5.2.3 10BASE-T Electrical Characteristic

Parameter	Description	Notes	Min	Typ	Max	units
V_{OD}	Differential output voltage		2.2	-	2.8	V
Z_{IN}	Receive input impedance		-	20K	-	Ω
V_{DS}	Differential squelch threshold		200			mV
Z_{IN}	Receive input impedance		-	20K	-	Ω
t_{link_pd}	Link transmit period		8		24	ms

5.2.4 Inter Repeater Bus Timing

Parameter	Description	Notes	Min	Typ	Max	units
t_{KC1}	IRCK cycle time			100		ns
t_{KD}	IRCK duty cycle		35		65	%
t_{DS}	IRD output data setup time		TBD			
t_{DH}	IRD] output data hold time		TBD			
t_{S1}	DACOZ, IRACTZ, IRDVZ setup time		TBD			
t_{H1}	DACOZ, IRACTZ, IRDVZ hold time		TBD			



6.0 Physical Dimensions

SYMBOL	Dimension in inch			Dimension in mm		
	MIN	NOM	MAX	MIN	NOM	MAX
A	-	-	0.130	-	-	3.30
A1	0.004	-	-	0.10	-	-
A2	0.107	0.112	0.117	2.73	2.85	2.97
B	0.010	0.012	0.016	0.25	0.30	0.40
C	0.004	0.006	0.010	0.1	0.15	0.25
D	0.964	0.976	0.988	24.49	24.80	25.10
D1	0.782	0.787	0.792	19.87	20.00	20.13
E	0.728	0.740	0.752	18.49	18.80	19.10
E1	0.546	0.551	0.556	13.87	14.00	14.13
e	0.020	0.026	0.032	0.50	0.65	0.80
L	0.039	0.047	0.055	1.00	1.20	1.40
L1	0.087	0.094	0.103	2.21	2.40	2.62
y	-	-	0.004	-	-	0.10
θ	0°	-	12°	0°	-	12°

NOTE :

1. DIMENSIONS D1 AND E1 DO NOT INCLUDE MOLO PROTRUSION. BUT MOLO MISMATCH IS INCLUDED ALLOWABLE PROTRUSION IS .25mm/.010" PER SIDE.
2. DIMENSION B DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION .08mm/.003" TOTAL IN EXECESS OF THE B DIMENSION AT MAXIMUM MATERIAL CONDITION. DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OR THE FOOT.
3. CONTROLLING DIMENSION : MILLIMETER.