M74ALS191P

SYNCHRONOUS PRESETTABLE UP/DOWN 4-BIT BINARY COUNTER WITH MODE CONTROL

T-45-23-09

DESCRIPTION

The M74ALS191P is a semiconductor integrated circuit containing a synchronous 4-bit binary (hexadecimal) counter function with up/down control and load inputs.

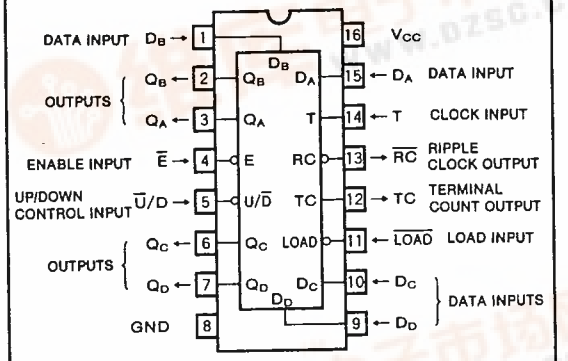
FEATURES

- Up/down switching with up/down control input
- Asynchronous load input provided
- Enable input provided
- Easy cascade connection possible
- Wide operating temperature range (Ta = −20 ~ +75°C)

APPLICATION

General purpose, for use in industrial and consumer equipment.

PIN CONFIGURATION (TOP VIEW)



Outline 16P4

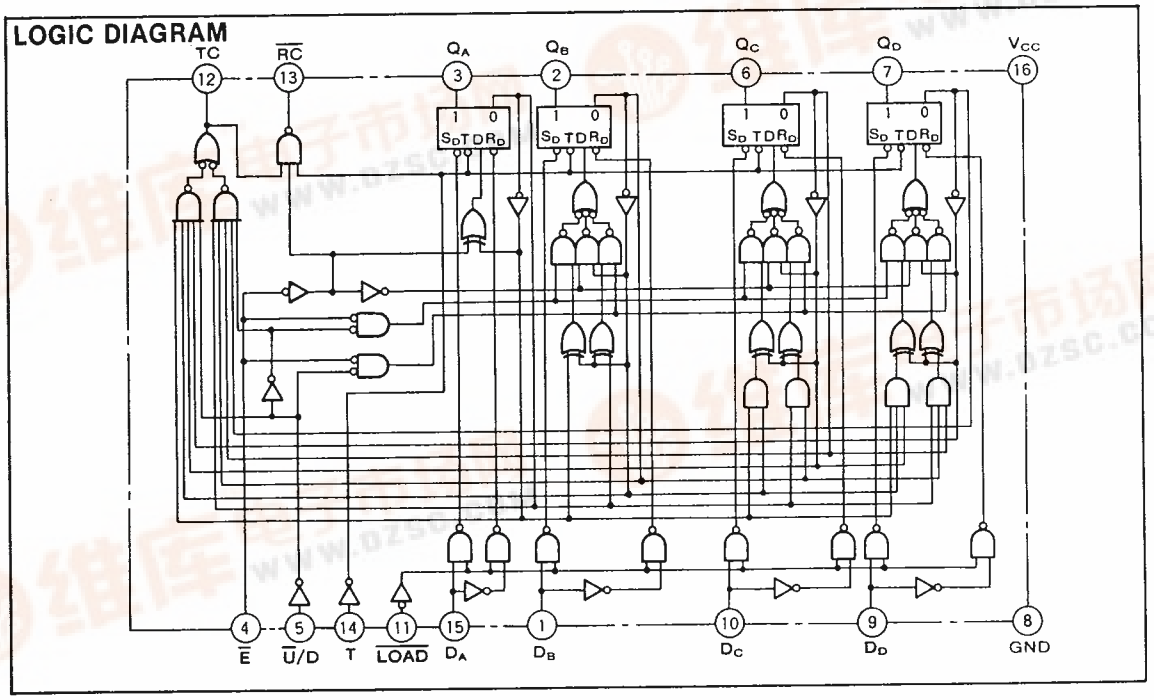
FUNCTIONAL DESCRIPTION

When ednable input $\overline{E}$ is low, load input $\overline{LOAD}$ is high and the count pulses are applied to clock input T, the number of count pulses appears as 4-bit binary code in the outputs , Q_A, Q_B, Q_C and Q_D in synchronization with the count pulses. When the up/down control input $\overline{U}/D$ is made low, count-up begins and when made high, count-down begins. Counting is performed when T changes from low to high.

Presetting is performed regardless of the count pulses and by applying the data to data inputs D_A, D_B, D_C and D_D and by setting $\overline{LOAD}$ low, the D_A, D_B, D_C and D_D signals appear in outputs Q_A, Q_B, Q_C and Q_D irrespective of the status of the other inputs and the count can be preset.

High appears in the terminal count output TC during count-up while 15_2 appears in Q_A, Q_B, Q_C and Q_D and during count-down while 0_2 appears. Low appears in the ripple clock output $\overline{RC}$ only when $\overline{E}$ and T are low and 15_2 appears in outputs Q_A, Q_B, Q_C and Q_D during count-up or 0_2 appears in the outputs during count-down. $\overline{E}$, TC and $\overline{RC}$ are used when cascade-connecting the counter.

LOGIC DIAGRAM



SYNCHRONOUS PRESETTABLE UP/DOWN 4-BIT BINARY COUNTER WITH MODE CONTROL

FUNCTION TABLE (Note 1)

Operation mode	Inputs				Outputs			
	$\overline{LOAD}$	$\overline{E}$	$\overline{U}/D$	T	Q_A	Q_B	Q_C	Q_D
Asynchronous mode	L	X	X	X	D_A	D_B	D_C	D_D
Count-up	H	L	L	↑	Count-up (hexadecinal)			
Count-down	H	L	H	↑	Count-down (hexadecinal)			
Inhibit	H	H	X	X	Count Inhibit			

Note 1. ↑ : Transition from low to high level
X : Irrevant

$\overline{RC}$ FUNCTION TABLE

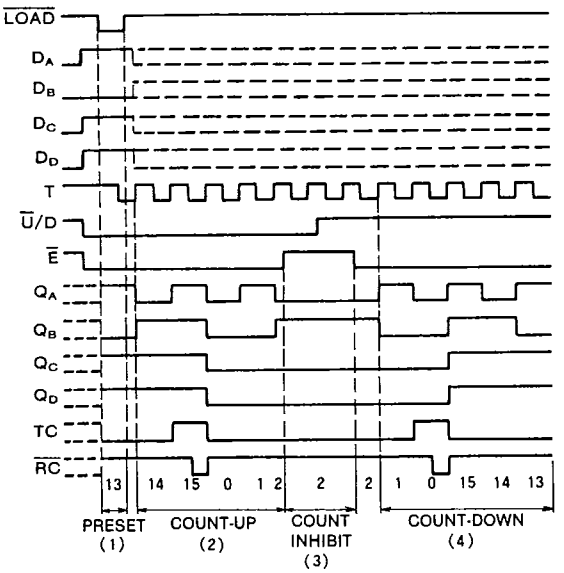
Inputs			Output
$\overline{E}$	TC*	T	$\overline{RC}$
L	H	L	L
L	H	H	H
H	X	X	H
X	L	X	H

* : TC is the output but the signal generated internally by according to the below TC Function table.

TC FUNCTION TABLE

Input	Outputs (Internal Signal)				Output
$\overline{U}/D$	Q_A	Q_B	Q_C	Q_D	TC
L	H	H	H	H	H
L	L	X	X	X	L
L	X	L	X	X	L
L	X	X	L	X	L
L	X	X	X	L	L
H	L	L	L	L	H
H	H	X	X	X	L
H	X	H	X	X	L
H	X	X	H	X	L
H	X	X	X	H	L

OPERATION TIMING DIAGRAM



Details of timing diagram
(1) Preset to 13
(2) Count-up 14, 15. 0, 1, 2
(3) Count Inhibit
(4) Count-down 1, 0, 15, 14, 13

ABSOLUTE MAXIMUM RATINGS (T_a = −20 ~ +75°C, unless otherwise noted)

Symbol	Parameter	Conditions	Ratings	Unit
V_{CC}	Supply voltage		−0.5~+7	V
V_I	Input voltage		−0.5~+7	V
V_O	Output voltage	High-level state	−0.5~V_{CC}	V
T_{opr}	Operating free-air ambient temperature range		−20~+75	℃
T_{stg}	Storage temperature range		−65~+150	℃

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Limits			Unit
		Min	Typ	Max	
V_{CC}	Supply voltage	4.5	5	5.5	V
V_{IH}	High-level input voltage	2			V
V_{IL}	Low-level input voltage			0.8	V
I_{OH}	High-level output current	0		−0.4	mA
I_{OL}	Low-level output current	0		8	mA
T_{opr}	Operating free-air ambient temperature range	−20		+75	℃

SYNCHRONOUS PRESETTABLE UP/DOWN 4-BIT BINARY COUNTER WITH MODE CONTROL

ELECTRICAL CHARACTERISTICS (T_a = −20 ~ +75°C, unless otherwise noted)

Symbol	Parameter		Test conditions		Limits			Unit
					Min	Typ *	Max	
V_{IC}	Input clamp voltage		V_{CC}=4.5V, I_{IC}=−18mA				−1.2	V
V_{OH}	High-level output voltage		V_{CC}=4.5~5.5V, I_{OH}=−0.4mA		V_{CC}−2			V
V_{OL}	Low-level output voltage		V_{CC}=4.5V	I_{OL}=4mA		0.25	0.4	V
				I_{OL}=8mA		0.35	0.5	
I_I	Input current at maximum voltage		V_{CC}=5.5V, V_I=7V				0.1	mA
I_{IH}	High-level input current		V_{CC}=5.5V, V_I=2.7V				20	μA
I_{IL}	Low-level input current	$\overline{E}$, T	V_{CC}=5.5V, V_I=0.4V				−0.2	mA
		Other inputs					−0.1	
I_O	Output current		V_{CC}=5.5V, V_O=2.25V		−30		−112	mA
I_{CC}	Supply current		V_{CC}=5.5V			12	22	mA

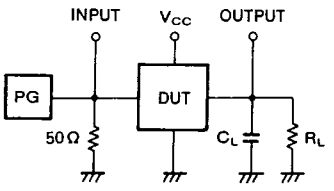
* : All typical values are at V_{CC} = 5V, T_a = 25°C.

SWITCHING CHARACTERISTICS

Symbol	Parameter			Test conditions/Limits (Note 2)							Unit
				V_{CC}=5V, C_L=15pF, R_L=500Ω	V_{CC}=4.5~5.5V, C_L=50pF, R_L=500Ω						
				T_a=25°C	T_a=0~70°C			T_a=−20~+75°C			
		Inputs	Outputs	Typ	Min	Typ *	Max	Min	Typ *	Max	
f_{max}	Maximum clock frequency	T	Q_A~Q_D		30	40		28	40		MHz
t_{PLH}	Propagation time	$\overline{LOAD}$	Q_A~Q_D	14	8	16	30	8	16	31	ns
t_{PHL}				16	8	18	30	8	18	31	
t_{PLH}		D_A~D_D	Q_A~Q_D	7	4	9	21	4	9	22	
t_{PHL}				12	4	14	21	4	14	22	
t_{PLH}	Propagation time	T	$\overline{RC}$	6	5	8	20	5	8	21	ns
t_{PHL}				11	5	13	20	5	13	21	
t_{PLH}		T	Q_A~Q_D	8	3	10	18	3	10	19	
t_{PHL}				8.5	3	10	18	3	10	19	
t_{PLH}		T	TC	13	8	15	31	8	15	32	
t_{PHL}				19	8	22	31	8	22	32	
t_{PLH}	Propagation time	$\overline{U}$/D	$\overline{RC}$	18	15	20	37	15	20	38	ns
t_{PHL}				14	10	16	28	10	16	29	
t_{PLH}		$\overline{U}$/D	TC	11	8	13	25	8	13	26	
t_{PHL}				13	8	15	25	8	15	26	
t_{PLH}		$\overline{E}$	$\overline{RC}$	6	4	8	18	4	8	19	
t_{PHL}				11	4	13	18	4	13	19	

* : All typical values are at V_{CC} = 5V, T_a = 25°C

Note 2. Measurement circuit



(1) The pulse generator (PG) has the following characteristics:

PRR≦1MHz

t_r=2ns、t_f=2ns

V_{IH}=3.5V、V_{IL}=0.3V

duty cycle=50%

Z_O=50Ω

(2) C_L includes probe and jig capacitance.

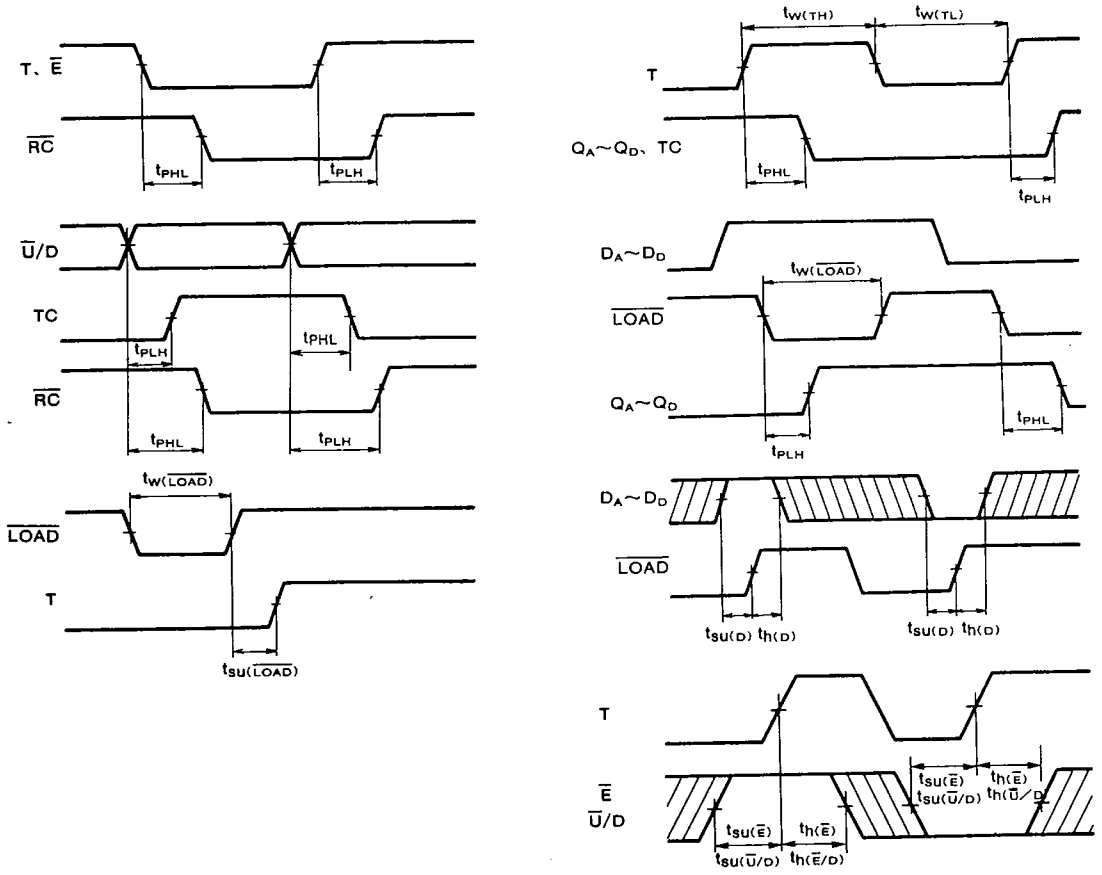
TIMING REQUIREMENTS (V_{CC} = 4.5 ~ 5.5V, C_L = 50pF, R_L = 500Ω)

Symbol	Parameter		Limits						Unit
			T_a=0~70℃			T_a=−20~+75℃			
			Min	Typ *	Max	Min	Typ *	Max	
$t_{w(TH)}$	Pulse width	T "H"	16.5	10		17.5	10		ns
$t_{w(TL)}$		T "L"	16.5	13		17.5	13		
$t_{w(\overline{LOAD})}$		$\overline{LOAD}$ "L"	20	10		21	10		
$t_{su(D)}$	Setup time before $\overline{LOAD}$↑	D_A~D_D	20	6		21	6		ns
$t_{su(\overline{E})}$	Setup time before T↑	$\overline{E}$ "L"	20	12		21	12		ns
$t_{su(\overline{U}/D)}$		$\overline{U}$/D	24	19		25	19		
$t_{su(\overline{LOAD})}$		$\overline{LOAD}$ "H" (inactive)	20	10		21	10		
$t_{h(D)}$	Hold time after $\overline{LOAD}$↑	D_A~D_D	5	0		6	0		ns
$t_{h(\overline{E})}$	Hold time after T↑	$\overline{E}$ "L"	0	−2		1	−2		ns
$t_{h(\overline{U}/D)}$		$\overline{U}$/D	0	−8		1	−8		

* : All typical values are at V_{CC} = 5V, T_a = 25°C.

↑ : Transition from low to high.

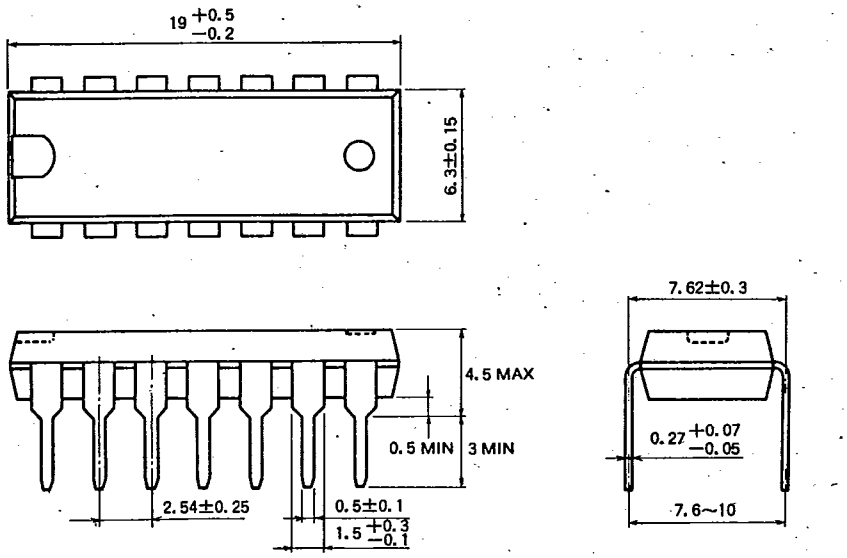
TIMING DIAGRAM (Reference level = 1.3V)



Note 3. The shaded areas indicate when the input is permitted to change for predictagle output performance.

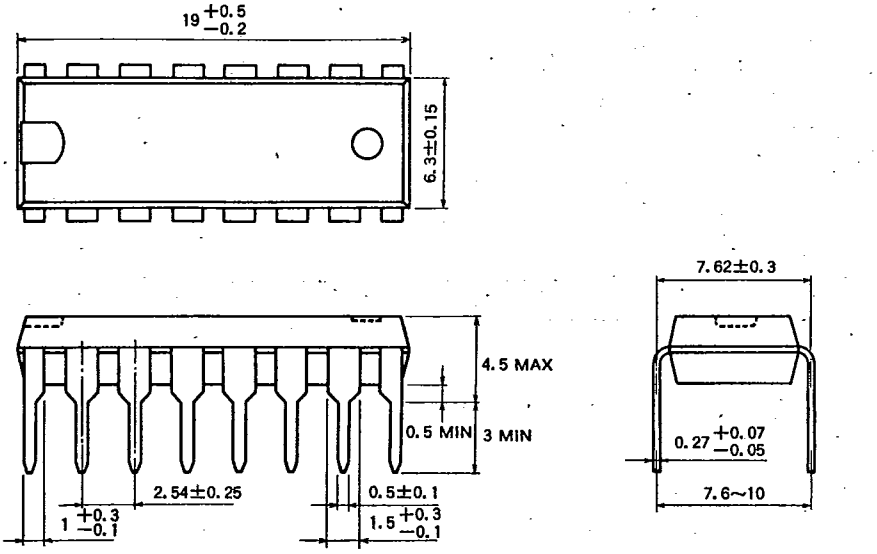
TYPE 14P4 14-PIN MOLDED PLASTIC DIP

Dimension in mm



TYPE 16P4 16-PIN MOLDED PLASTIC DIP

Dimension in mm

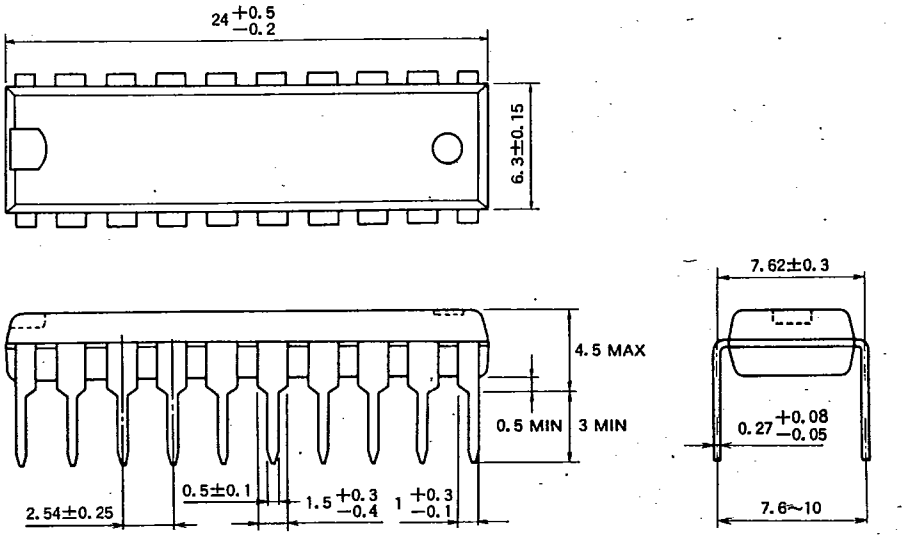


PACKAGE OUTLINES

6249827 MITSUBISHI (DGTL LOGIC)
91D 12324 D T-90-20

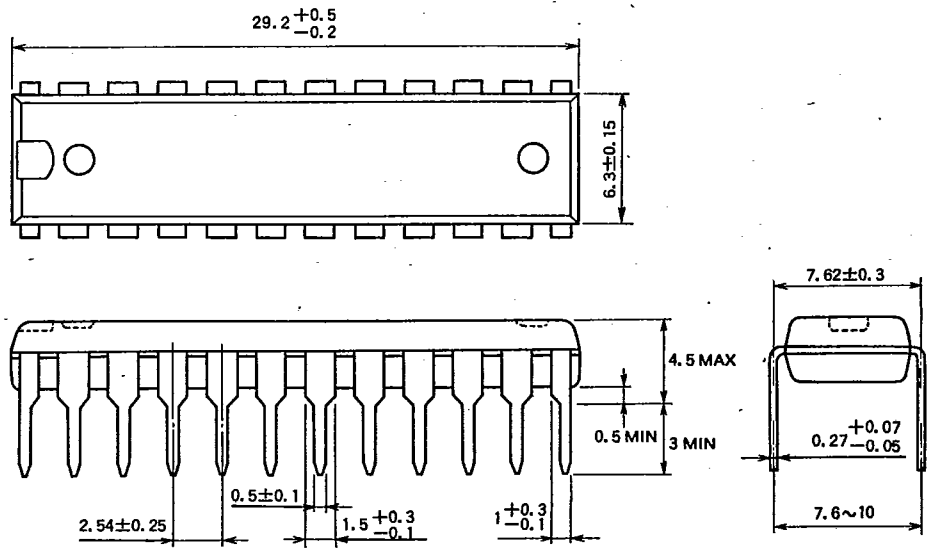
TYPE 20P4 20-PIN MOLDED PLASTIC DIP

Dimension in mm



TYPE 24P4D 24-PIN MOLDED PLASTIC DIP

Dimension in mm



TYPE DESIGNATION TABLE

ALSTTL SERIES SOP TYPE DESIGNATION TABLE

Type		Circuit function	Package Outlines
M74ALS00ADP	★	Quadruple 2-Input Positive NAND Gate	14P2P
M74ALS02DP	★	Quadruple 2-Input Positive NOR Gate	14P2P
M74ALS04ADP	★	Hex Inverter	14P2P
M74ALS05ADP	★★	Hex Inverter with Open Colletor Output	14P2P
M74ALS08DP	★	Quadruple 2-Input Positive AND Gate	14P2P
M74ALS09DP	★★	Quadruple 2-Input Positive AND Gate with Open Collector Output	14P2P
M74ALS10ADP	★	Triple 3-Input Positive NAND Gate	14P2P
M74ALS11ADP	★	Triple 3-Input Positive AND Gate	14P2P
M74ALS20ADP	★★	Dual 4-Input Positive NAND Gate	14P2P
M74ALS27DP	★★	Triple 3-Input Positive NOR Gate	14P2P
M74ALS30ADP	★★	Single 8-Input Positive NAND Gate	14P2P
M74ALS32DP	★	Quadruple 2-Input Positive OR Gate	14P2P
M74ALS37ADP	★★	Quadruple 2-Input Positive NAND Buffer	14P2P
M74ALS38ADP	★★	Quadruple 2-Input Positive NAND Buffer with Open Collector Output	14P2P
M74ALS74ADP	★	Dual D-Type Positive Edge-Triggered Flip-Flop with Set and Reset	14P2P
M74ALS109ADP	★★	Dual J-$\overline{K}$ Positive Edge-Triggered Flip-Flop with Set and Reset	16P2P
M74ALS112ADP	★	Dual J-K Negative Edge-Triggered Flip-Flop with Set and Reset	16P2P
M74ALS131DP	★★	3-Line to 8-Line Decoder/Demultiplexer with Address Register	16P2P
M74ALS138DP	★	3-Line to 8-Line Decoder/Demultiplexer	16P2P
M74ALS153DP	★★	Dual 4-Line to 1-Line Data Selector/Multiplexer with Strobe	16P2P
M74ALS157DP	★	Quadruple 2-Line to 1-Line Data Selector/Multiplexer	16P2P
M74ALS161BDP	★★	Synchronous Presettable 4-Bit Binary Counter with Direct Reset	16P2P
M74ALS163BDP	★★	Fully Synchronous Presettable 4-Bit Binary Counter	16P2P
M74ALS169BDP	★★	Synchronous 4-Bit Binary Counter	16P2P
M74ALS174DP	★	Hex D-Type Positive Edge-Triggered Flip-Flop with Reset	16P2P
M74ALS175DP	★★	Quadruple D-Type Positive Edge-Triggered Flip-Flop with Reset	16P2P
M74ALS193DP	★★	Synchronous Presettable Up/Down 4-Bit Binary Counter	16P2P
M74ALS240ADWP	★	Octal Buffer/Line Driver with 3-State Output (Inverted)	20P2V
M74ALS244ADWP	★	Octal Buffer/Line Driver with 3-State Output (Noninverted)	20P2V
M74ALS245ADWP	★★	Octal Bus Transceiver with 3-State Output (Noninverted)	20P2V
M74ALS245A-1DWP	★★	Octal Bus Transceiver with 3-State Output (Noninverted)	20P2V
M74ALS257DP	★	Quadruple 2-Line to 1-Line Data Selector/Multiplexer with 3-State Output	16P2P
M74ALS273DWP	★★	Octal D-Type Positive Edge-Triggered Flip-Flop with Reset	20P2V
M74ALS299DWP	★★	8-Bit Universal Shift/Storage Register with 3-State Output	20P2V
M74ALS373DWP	★★	Octal D-Type Transparent Latch with 3-State Output	20P2V
M74ALS374DWP	★★	Octal D-Type Positive Edge-Triggered Flip-Flop with 3-State Output	20P2V
M74ALS533DWP	★★	Octal D-Type Transparent Latch with 3-State Output (Inverted)	20P2V
M74ALS534DWP	★★	Octal D-Type Positive Edge-Triggered Flip-Flop with 3-State Output (Inverted)	20P2V
M74ALS561ADWP	★★	Synchronous Presettable 4-Bit Binary Counter with 3-State Output	20P2V
M74ALS569ADWP	★★	Synchronous Up/Down 4-Bit Binary Counter with 3-State Output	20P2V
M74ALS573ADWP	★★	Octal D-Type Transparent Latch with 3-State Output (Noninverted)	20P2V
M74ALS574ADWP	★★	Octal D-Type Positive Edge-Triggered Flip-Flop with 3-State Output (Noninverted)	20P2V
M74ALS640ADWP	★★	Octal Bus Transceiver with 3-State Output (Inverted)	20P2V
M74ALS642ADWP	★★	Octal Bus Transceiver with Open Collector Output (Inverted)	20P2V
M74ALS645ADWP	★★	Octal Bus Transceiver with 3-State Output (Noninverted)	20P2V
M74ALS1034DP	★★	Hex Noninverting Buffer	14P2P

★: New product ★★: Under development

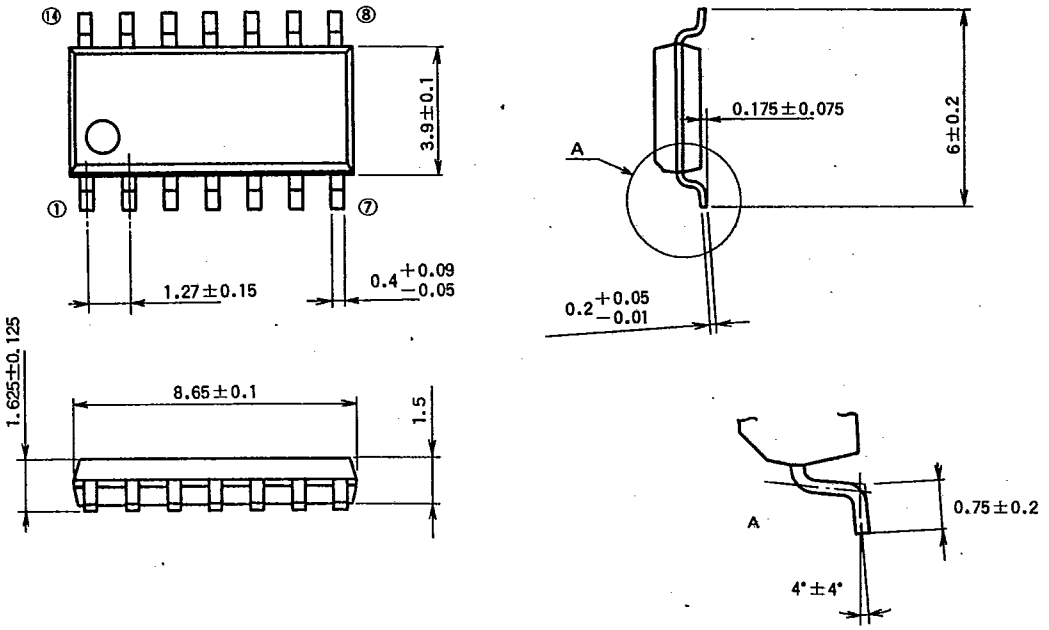
DESCRIPTION

The ALSTTL SOP (Small Outline Package) devices are identical in all respects except for their package outlines to DIP (Dual Inline Package).

MITSUBISHI (DGTL LOGIC) 91D D 6249827 0012786 0 MIT3
T-90-20

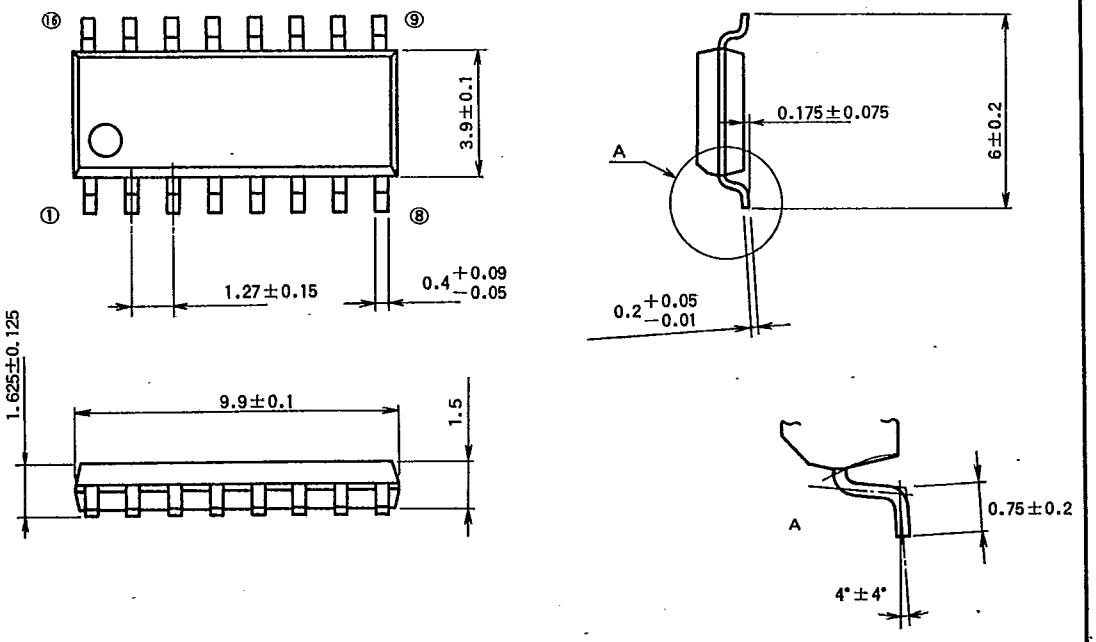
TYPE 14P2P 14-PIN MOLDED PLASTIC SOP (JEDEC 150mil body)

Dimension in mm



TYPE 16P2P 16-PIN MOLDED PLASTIC SOP (JEDEC 150mil body)

Dimension in mm



PACKAGE OUTLINES

TYPE 20P2V 20-PIN MOLDED PLASTIC SOP (JEDEC 300mil body)

Dimension in mm