NEC Electronics Inc.

μPD75008 Family (μPD75004/006/008/P008) 4-Bit General-Purpose Single-Chip Microcontrollers

October 1994

Description

The μPD75008 family of high performance 4-bit single-chip CMOS microcontrollers includes the following devices:

μPD75004 μPD75004(A) μPD75006 μPD75006(A)
μPD75008 μPD75008(A) μPD75P008

These general-purpose microcontrollers have up to 8K bytes of ROM and 512 nibbles of RAM. The instruction set operates on 1, 4, and 8 bits of data.

Timing is generated by two oscillators. The main oscillator drives the CPU and all peripherals. The 32.768-kHz subsystem oscillator provides time keeping when the main oscillator is turned off. Since CMOS power dissipation is proportional to clock rate, the μPD75008 family provides selectable instruction cycle times from 0.95 to 122 μs. The STOP and HALT modes turn off parts of the microcontroller for additional power savings. The data retention mode retains RAM contents down to 2.0 volts.

Features

- 8-bit synchronous serial interface
  - Full-duplex, three-wire mode
  - Half-duplex, two-wire mode
  - NEC serial bus interface (SBI) mode
- Timers: three channels
  - 8-bit interval timer
  - 8-bit timer/event counter
  - Watch (clock) timer:
    0.5 second interrupt requests
- 34 I/O lines
  - Eight input-only lines
  - 18 bidirectional I/O lines of which four can directly drive LEDs
  - Eight 10-V n-channel, open-drain lines that can directly drive LEDs
  - 25 software selectable pullup resistors
  - Eight mask option selectable resistors (mask ROM devices only)
- Bit sequential buffer
  - 16 bits of bit addressable RAM in peripheral address space.
- Standard CPU instruction set
  - 107 instructions
  - Bit manipulation instructions
  - 4-bit arithmetic instructions
  - 4- and 8-bit move instructions
- Minimum instruction execution time
  - 0.95, 1.91, and 15.3 μs using 4.19-MHz main system clock
  - 122 μsec using 32.768-kHz subsystem clock
- Eight 4-bit registers
  - Usable as four 8-bit registers
- Memory-mapped, on-chip peripherals
- Vectored interrupt controller
  - 12 external and 4 internal sources
  - 12 edge detection inputs
  - 5 vectored interrupt addresses
- Power saving and battery backup
  - Variable CPU clock rate; 2.5 mA typical at 5 V and 4.19 MHz
  - HALT mode stops CPU; 0.5 mA typical at 5 V and 4.19 MHz
  - STOP mode stops main clock; 0.5 μA typical at 5 V
  - 2.0 V data retention mode
- Subsystem oscillator allows watch timer to operate in power-down modes.
- CMOS operation
  - ROM devices; V_{DD} = 2.7 to 6.0 V
  - μPD75P008 OTP; 5 V ±10%

Internal High-Capacity ROM and RAM

Memory	μPD75004	μPD75006	μPD75008	μPD75P008
ROM	4K bytes	6K bytes	8K bytes	—
PROM	—	—	—	8K bytes
RAM	512 nibbles	512 nibbles	512 nibbles	512 nibbles

Ordering Information

Part Number	Quality Grade	ROM	Package	Package Drawing
μPD75004CU-xxx	Standard	Mask	42-pin plastic shrink DIP	P42C-70-600A
μPD75004CU(A)-xxx	Special			
μPD75006CU-xxx	Standard			
μPD75006CU(A)-xxx	Special			
μPD75008CU-xxx	Standard			
μPD75008CU(A)-xxx	Special			
μPD75004GB-xxx-3B4	Standard	Mask	44-pin plastic QFP	P44GB-80-3B4-2
μPD75004GB(A)-xxx-3B4	Special			
μPD75006GB-xxx-3B4	Standard			
μPD75006GB(A)-xxx-3B4	Special			
μPD75008GB-xxx-3B4	Standard			
μPD75008GB(A)-xxx-3B4	Special			
μPD75P008CU	Standard	OTP	42-pin plastic shrink DIP	P42C-70-600A
μPD75P008GB-3B4	Standard	OTP	44-pin plastic QFP	44GB-80-3B4-2

Notes:

(1) Engineering samples are available in a 42-pin shrink DIP or 44-pin ceramic QFP

(2) xxx indicates ROM code number

Device Quality Grades

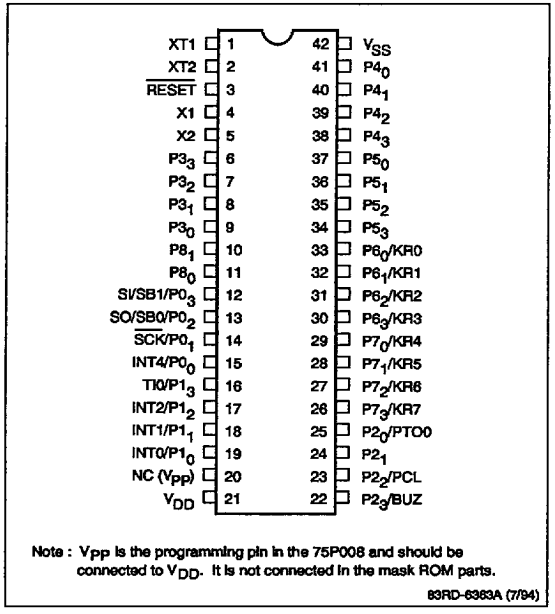
The devices in the μPD75008 family are available in standard or special quality grades devices. Special grade devices have the symbol (A) embedded in the part number. A μPD75008CU is a standard grade and a μPD75008CU(A) is a special grade device. The selection of the correct grade depends upon the application.

Differences Between Special and Standard Quality Grades

Item	Special	Standard
Applications	Automotive and transportation equipment, traffic control systems, anti-disaster systems, anti-crime systems	Computers, office equipment, communications, test and measurement, machine tools, industrial robots, audio and visual equipment, other consumer products.
LED direct drive	No	Yes
Absolute maximum ratings	Differences in low and high output current	
DC characteristics	Differences in low-voltage outputs	

Pin Configurations

42-Pin Plastic SDIP

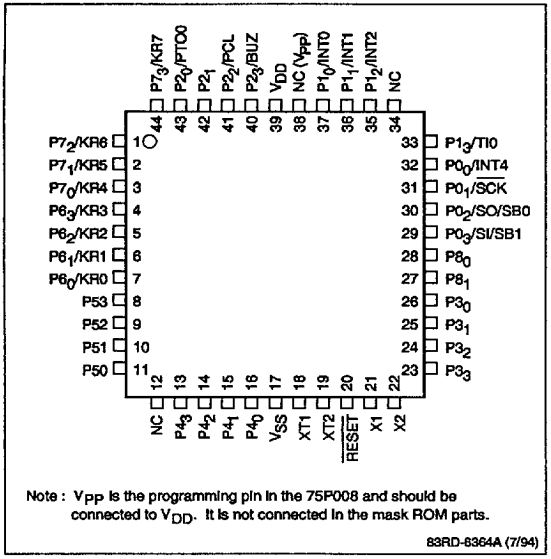


Note : V_{PP} is the programming pin in the 75P008 and should be connected to V_{DD}. It is not connected in the mask ROM parts.

83RD-6363A (7/94)

Pin Configurations

44-Pin Plastic QFP



Note : V_{PP} is the programming pin in the 75P008 and should be connected to V_{DD}. It is not connected in the mask ROM parts.

83RD-8364A (7/94)

Pin Identification

Symbol	Function
NC (V_{PP})	No connection (programming voltage for μPD75P008
$P0_0$/INT4	Port 0 input; interrupt 4
$P0_1$/$\overline{SCK}$	Port 0 input; serial clock
$P0_2$/SO/SB0	Port 0 input; serial out; serial interface
$P0_3$/SI/SB1	Port 0 input; serial in; serial interface
$P1_0$/INT0	Port 1 input; interrupt 0
$P1_1$/INT1	Port 1 input; interrupt 1
$P1_2$/INT2	Port 1 input; interrupt 2
$P1_3$/TI0	Port 1 input; timer 0 input
$P2_0$/PTO0	Port 2 I/O; timer/event counter output
$P2_1$	Port 2 I/O
$P2_2$/PCL	Port 2 I/O; clock output
$P2_3$/BUZ	Port 2 I/O; buzzer output
$P3_0$-$P3_3$	Port 3 I/O
$P4_0$-$P4_3$	Port 4 I/O
$P5_0$-$P5_3$	Port 5 I/O
$P6_0$/KR0	Port 6 I/O; key scan input 0
$P6_1$/KR1	Port 6 I/O; key scan input 1
$P6_2$/KR2	Port 6 I/O; key scan input 2
$P6_3$/KR3	Port 6 I/O; key scan input 3
$P7_0$/KR4	Port 7 I/O; key scan input 4
$P7_1$/KR5	Port 7 I/O; key scan input 5
$P7_2$/KR6	Port 7 I/O; key scan input 6
$P7_3$/KR7	Port 7 I/O; key scan input 7
$P8_0$-$P8_1$	Port 8 I/O
$\overline{RESET}$	Reset input
V_{DD}	Positive power supply
V_{SS}	Ground
X1, X2	Main clock inputs
XT1, XT2	Subsystem clock inputs

PIN FUNCTIONS

$P0_0$-$P0_3$, INT4, $\overline{SCK}$, SO/SB0, SI/SB1 (Port 0, Interrupt 4, Serial Interface). These pins can be used as 4-bit input port 0. $P0_0$ can also be used for vectored interrupt 4, which interrupts on either the leading edge or the trailing edge of the signal. $P0_1$-$P0_3$ may also be used for the serial interface in the SBI, 2-wire or 3-wire mode. SI is the serial input, SO is the serial output, and $\overline{SCK}$ is the serial clock. Reset causes these pins to default to the port 0 input mode.

$P1_0$-$P1_3$, INT0-INT2, TI0 (Port 1, Edge-Triggered Interrupts, Timer Input). These pins can be used as 4-bit input port 1. $P1_0$ and $P1_1$ can also be used for edge-triggered interrupts INT0 and INT1. $P1_2$ can be used for INT2, which is also an edge-triggered input, but one that generates an interrupt request and does not cause an interrupt. $P1_3$ can be used as an input clock to the timer/event counter to count external events. Reset causes these pins to default to the port 1 input mode.

$P2_0$-$P2_3$, PTO_0, PCL, BUZ (Port 2, Timer/Event Counter, Clock, or Buzzer Output). These pins can be used as 4-bit I/O port 2. When used as an output the data is latched. When used as an input port the port outputs are three-state. $P2_0$ can also be used as the output of the timer/event counter flip flop (TOUT); $P2_2$ can be used as the output for the clock generator (PCL); and $P2_3$ can be used to output square waves for a buzzer. Reset causes these pins to default to the port 2 input mode.

$P3_0$-$P3_3$ (Port 3). These pins are used for I/O port 3. Each bit in this port can be independently programmed to be either an input or an output. This port has latched outputs, and can directly drive LEDs. A reset signal causes this port to default to the input mode.

$P4_0$-$P4_3$, $P5_0$-$P5_3$ (Ports 4 and 5). Ports 4 and 5 are 4-bit I/O ports that can be combined together to function as a single 8-bit port. They have latched outputs. Ports 4 and 5 will directly drive LEDs. Outputs are n-channel open drain, and can withstand up to 10 volts; pullup resistor mask options are available for these ports. A reset signal causes these ports to default to the input mode.

$P6_0$-$P6_3$, $P7_0$-$P7_3$, KR0-KR7 (Ports 6, 7, and Edge Detection). Ports 6 and 7 are 4-bit I/O ports with latched outputs. Each pin of port 6 can be independently programmed to be either an input or an output, while port 7 can be programmed to be either all inputs or all outputs. Ports 6 and 7 can be paired together to function as one 8-bit port. Alternately, these pins may be used to detect the falling edge of inputs KR0-KR3 (port 6) and KR4-KR7 (port 7). A reset signal causes these ports to default to the input mode.

$P8_0$-$P8_1$ (Port 8). Port 8 is a 2-bit I/O port. Outputs are latched. A reset signal causes this port to default to the input mode.

NC/V_{PP} (No Connection/Programming Pin). When using the programmable devices, this pin is used to input the programming voltage during the EPROM/OTP write/verify cycles. During normal operation of the programmable device, this pin should be tied to V_{DD}. This pin may be left unconnected when using the mask ROM device, μPD7500x; however, to maintain socket compatibility with the EPROM/OTP devices, it is recommended that this pin be tied to V_{DD}.

X1, X2 (Main System Clock Inputs). These pins are the main system clock inputs. The clock can be either a ceramic resonator or a crystal; an external logic signal may also be used.

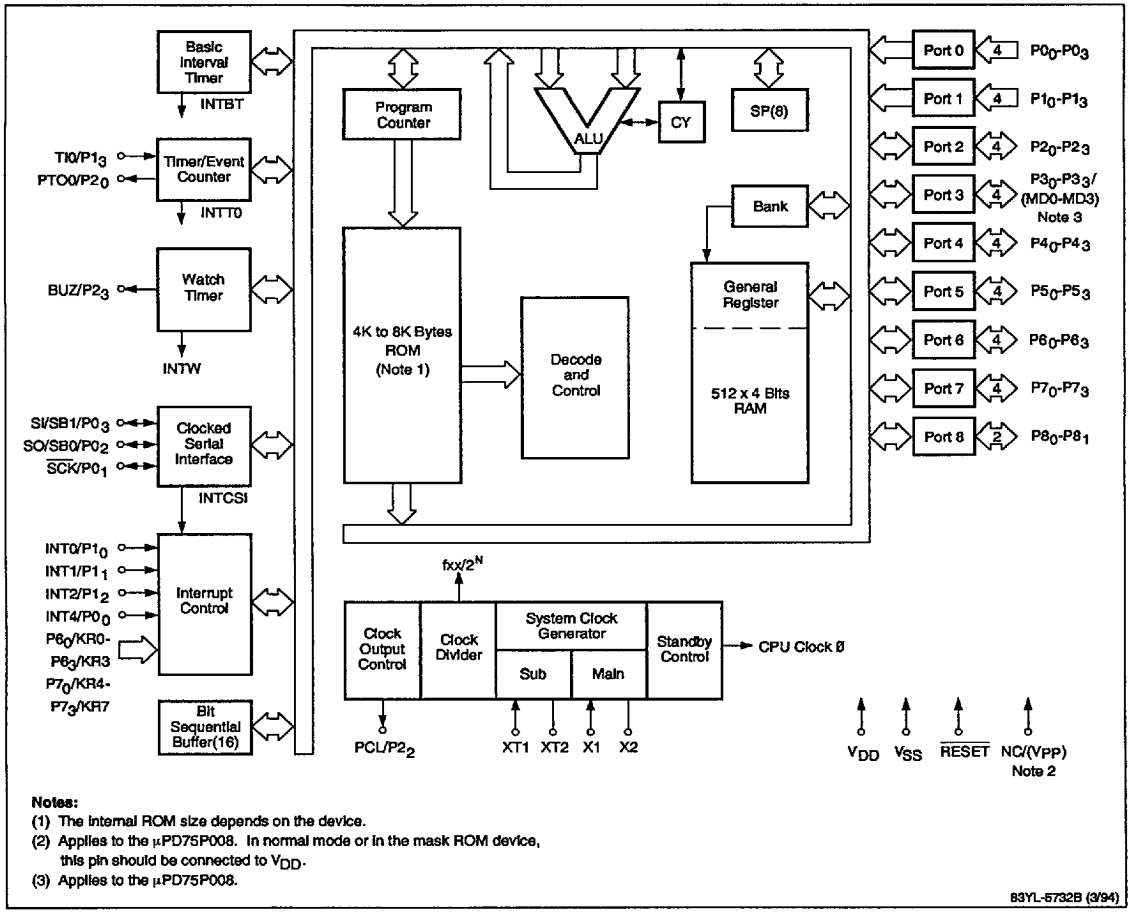
XT1, XT2 (Subsystem Clock Inputs). These pins are the subsystem clock inputs. The clock can be either a ceramic resonator or a crystal; an external logic signal may also be used.

$\overline{RESET}$ (Reset). This is the reset input and it is active low.

V_{DD} (Power Supply). The system positive power supply pin.

V_{SS} (Ground). System ground.

Block Diagram



Notes:

(1) The internal ROM size depends on the device.

(2) Applies to the μPD75P008. In normal mode or in the mask ROM device, this pin should be connected to V_{DD}.

(3) Applies to the μPD75P008.

83YL-5732B (3/94)

Product Comparison

Item	75004	75006	75008	75P008
Program Memory	Mask ROM 00H–FFH 4096 x 8 bits	Mask ROM 0000H–177FH 6016 x 8 bits	Mask ROM 0000H–1F7FH 8064 x 8 bits	PROM 0000H–1F7FH 8064 x 8 bits
Data memory	512 x 4 bits			
3-byte branch instructions	No	Yes	Yes	Yes
Other instruction set	Common to the products			
Program counter	12-bit	13-bit	13-bit	13-bit
Ports 0-3, ports 6-8 pullup resistor	Software selectable			
Ports 4 and 5 pullup resistor	Mask option	Mask option	Mask option	No
V_{PP}, PROM programming pins	No	No	No	Yes
Operating voltage range	2.7 to 6.0 V	2.7 to 6.0 V	2.7 to 6.0 V	5 V ± 5%
Package	42-pin plastic shrink DIP (600 mil) 44-pin plastic QFP (10 x 10 mm)			

CPU AND MEMORY ARCHITECTURE

The 75X architecture has two separate address spaces, one for program memory (ROM) and another for data memory (RAM).

Program Memory (ROM)

The ROM is addressed by the 12- or 13-bit program counter. The size of the program counter and the amount of ROM present depend on which part is being used. The ROM contains program object code, an interrupt vector table, a GETI instruction reference table, and table data. Table data can be obtained using table reference instruction MOVT.

Figure 1 shows the addressing range which can be made using a branch instruction or subroutine call instruction. In addition, the BR PCDE and BR PCXA instructions can be used for a branch where only the low 8 bits of the PC are changed. The program memory addresses are:

75004: 000H to FFFH
75006: 0000H to 177FH
75008: 0000H to 1F7FH
75P008: 0000H to 1F7FH

All locations in ROM except 0000H and 0001H can be used as program memory. However, if interrupts or GETI instructions are used, the locations corresponding to those functions cannot be used. Addresses are normally reserved as follows:

0000H to 0001H	This address area is used as the vector address for $\overline{\text{RESET}}$, and also contains the MBE bit.
0002H to 000BH	This area is used for interrupt vector addresses. Each vector address contains an MBE bit value and the interrupt can start from any location except where noted above.
0020H to 007FH	This is the table area for GETI instructions. The GETI instruction is used to access one 2-byte or two 1-byte instructions using one byte of program memory. This is useful in compacting code.

Program Counter (PC)

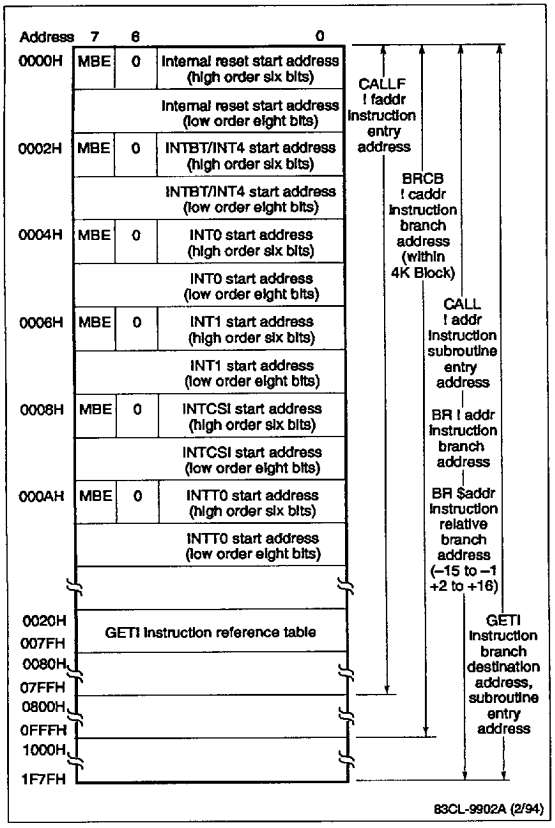
This is a 12/13-bit binary counter that contains the address of the current program memory location. The μPD75004 contains a 12-bit PC and the 75006/008/P008 have a 13-bit PC.

When an instruction is executed, the PC is automatically incremented by the number of bytes of the current instruction. When a branch instruction (BR, BRCB) is executed, the contents of the immediate data or register pair indicating the new address are loaded into some or all bits of the PC.

When a subroutine call instruction (CALL, CALLF) is executed or an interrupt is generated, the PC is incremented to point to the next instruction, and this information is saved on the stack. During an interrupt, the program status word (PSW) is also automatically saved on the stack. The address to be jumped to by the CALL or interrupt is then loaded into the PC.

When a return instruction (RET,RETS, or RETI) is executed, the contents of the stack are restored to the PC.

Figure 1. Program Memory Map



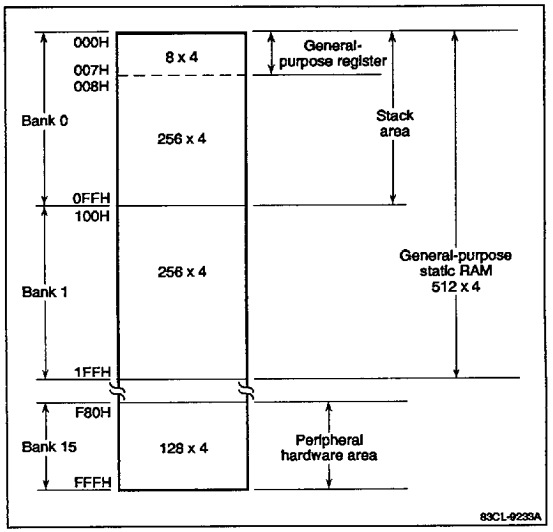
Data Memory (RAM)

The data memory contains three memory banks: 0, 1, and 15. The RAM memory map is shown in figure 2. The memory consists of general-purpose static RAM and peripheral control registers.

The memory banks are accessed by using MBE (memory bank enable) and by programming the BS (bank select register). If MBE = 0, the lower 128 nibbles of memory bank 0 and the upper 128 nibbles of memory bank 15 are accessed. If MBE = 1, the upper four bits in the BS register will specify the memory bank. The values are 0H for memory bank 0, 1H for memory bank 1, and 0FH for memory bank 15.

Memory banks 0 and 1 each contain 256 nibbles. Although the memory is organized in nibbles, the 75X architecture allows the data to be manipulated in bytes, nibbles, and individual bits.

Figure 2. μPD75008 Family Data Memory Map



The data memory is used for storing processed data, general-purpose registers, and as a stack for subroutine or interrupt service. Because of its static nature, the RAM will retain its data when CPU operation is stopped and the chip is in the standby mode, provided V_{DD} is at least 2 volts.

There are eight 4-bit general-purpose registers (figure 3) in bank 0 starting at location 00H. These registers may also be used as four 8-bit registers. The on-chip peripheral control registers and ports reside in the upper 128 nibbles of bank 15. Bank 15 addresses that are not assigned to a register are not available as random memory except for the 16-bit sequential buffer. Also, the lower 128 nibbles of bank 15 do not contain RAM.

Addressing Modes. The μPD75008 family can address data memory and ports as individual bits, nibbles, or bytes. These addressing modes are as follows:

1-bit direct data memory
4-bit immediate
4-bit register indirect (@rpa)
4-bit direct data memory
8-bit immediate
8-bit register indirect (@HL)
8-bit direct data memory

Tables 1 and 2 and figure 4 show the data memory addressing modes for the μPD75008 family.

Figure 3. General-Purpose Register Configurations

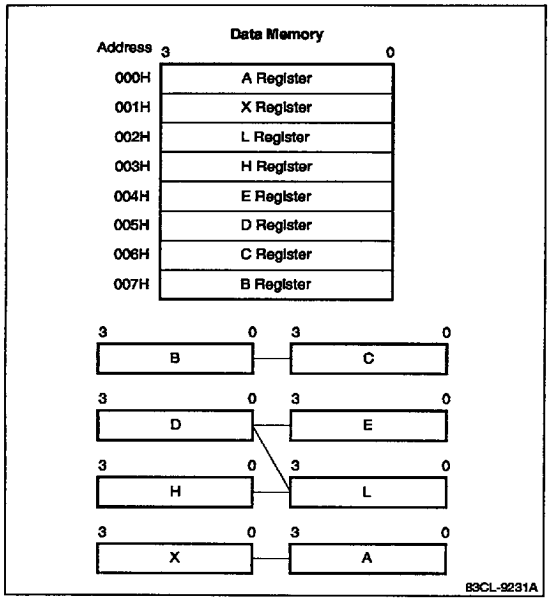


Table 1. Data Memory Addressing Modes (Note 1)

Addressing Mode	Format	Address

1-bit direct addressing	mem. bit	The memory bank is:
		if MBE = 0:
		MB = 0 for addr 00H-7FH
		MB = 15 for addr 80H-FFH
		if MBE = 1:
		MB = (MBE)•(MBS Reg)
		The memory location and bit within the memory bank is: mem.bit

4-bit direct addressing	mem	The memory bank is:
		if MBE = 0:
		MB = 0 for addr 00H-7FH
		MB = 15 for addr 80H-FFH
		if MBE = 1:
		MB = (MBE)•(MBS Reg)
		The memory location within the memory bank is: mem

Table 1. Data Memory Addressing Modes (Note 1) (cont)

Addressing Mode	Format	Address

8-bit direct addressing	mem	The memory bank is
		if MBE = 0:
		MB = 0 for addr 00H-7FH
		MB = 15 for addr 80H-FFH
		if MBE = 1:
		MB = (MBE)•(MBS Reg)
		The memory location within the memory bank is: mem
		mem must be an even address

4-bit register indirect addressing	@ HL	The memory bank is: MB = (MBE)•(MBS Reg) The memory location within the memory bank is: contained in register HL
	@ DE	The memory bank is always bank 0. The memory location within the memory bank is: contained in register DE
	@ DL	The memory bank is always bank 0. The memory location within the memory bank is: contained in register DL
8-bit register indirect addressing	@ HL	The memory bank is: MB = (MBE)•(MBS Reg) The memory location within the memory bank is: contained in register HL HL must contain an even address
Bit manipulation addressing	fmem. bit	The memory bank is bank 15. The memory location in bank 15 is fmem where: fmem = B0H-BFH for interrupts fmem = F0H-FFH for I/O ports The bit is specified in: fmem.bit
	pmem.@L	The memory location is independent of MBE and MBS. The upper 10 bits of the location are in the high order 10-bits of pmem and the 2 lower address bits are in the upper 2-bits of register L. The bit to be manipulated is specified by the 2 LSBs of register L.

Table 1. Data Memory Addressing Modes (Note 1)

Addressing Mode	Format	Address
Bit manipulation addressing (cont)	@ H + mem. bit	The memory bank is: MB = (MBE)•(MBS Reg) The memory location within the memory bank is: 4 upper bits are in register H 4 lower bits are mem The bit is specified in: mem.bit
Stack addressing		The stack is always in bank 0 and the address is indicated by stack pointer SP

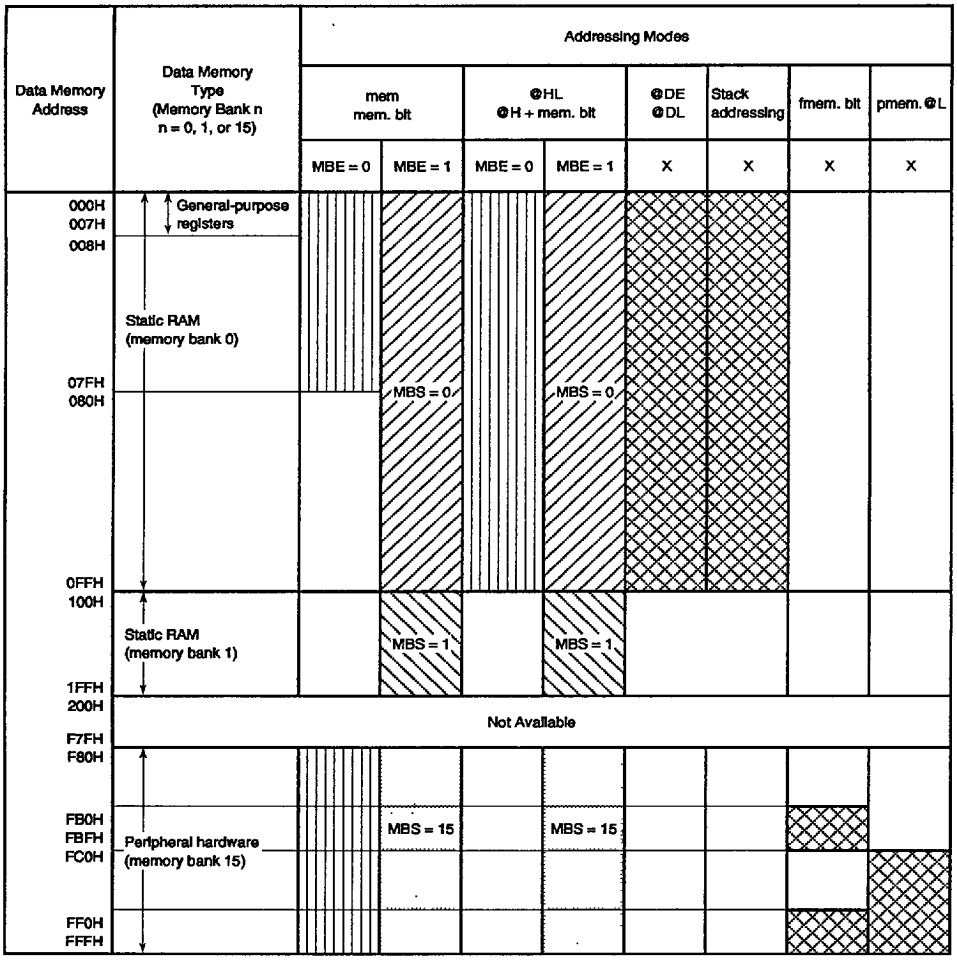
Note:

(1) MBE: Memory bank enable bit
MB: Memory bank
MBS: Memory bank select register
mem: A memory location within a memory bank
mem.bit: A memory location and a bit at that location

Table 2. On-Chip Peripherals Addressing Modes

Type of Manipulation	Addressing Mode	Hardware
Bit	MBE = 0 or MBE = 1 and MBS = 15; direct addressing with bank address specified in mem.bit.	All hardware where bit manipulation can be performed
	Direct addressing regardless of the setting of MBE and MBS. Bank address specified in fmem. bit.	ISTO, MBE; IExxx, IRQxxx, PORTn.x
	Indirect addressing regardless of the setting of MBE and MBS. Bank address specified in pmem. @L.	BSBn.x; PORTn.x
4-bit	MBE = 0 or MBE = 1 and MBS = 15; direct addressing with bank address specified in mem.	All hardware where 4-bit manipulation can be performed
	MBE = 1 and MBS = 15; register indirect addressing with bank address specified in HL.	
8-bit	MBE = 0 (or MBE = 1 and MBS = 15); direct addressing with bank address specified in mem; mem must be an even address.	All hardware where 8-bit manipulation can be performed
	MBE = 1 and MBS = 15; register indirect addressing with bank address specified in HL; L register must contain an even number.	

Figure 4. Data Memory Organization and Addressing Modes



X MBE has no effect
MBE Memory bank enable bit
MBS Memory bank select register

83CL-9236B (7/94)

FUNCTIONAL DESCRIPTION

Input/Output Ports

The μPD7500x provides eight 4-bit ports and one 2-bit port. Seven are input/output and two are input only. Table 3 lists the function and operation of the I/O ports. Figure 5 shows the internal circuits of the ports, which are classified as types A through Z.

Software selectable internal pullup resistors are available on ports 0, 1, 2, 3, 6, 7, and 8. They are selectable in 4-bit units except port 8, which is in 2-bit units. Port 0, bit 0 does not have a pullup resistor. Mask option, bit selectable internal pullup resistors are available for ports 4 and 5 on all mask ROM parts.

Table 3. Types and Features of Digital Ports

Port	Function	Operation and Features	Remarks
P0, P1	4-bit input	Can be read or tested regardless of the operation mode of the following pins: SO/SB0, SI/SB1, $\overline{SCK}$, INT0, INT1, INT2, INT4, or TI0.	Pins are also used for SO/SB0, SI/SB1, $\overline{SCK}$, INT0, INT1, INT2, INT4, and TI0
P3	4-bit input/output	Can be set-up in input or output mode in 1-bit units.	
P6			Pins are also used for KR0-KR3
P2	4-bit input/output	Can be set-up in input or output mode in 4-bit units. Ports 6 and 7 can be paired for data input/output in 8-bit units.	Pins are also used for PTO0, PCL and BUZ
P7			Pins are also used for KR4-KR7
P8	2-bit input/output	Can be set-up as either all inputs or all outputs.	
P4, P5	4-bit input/output (N-channel open drain, 10 volts)	Can be set-up in input or output mode in 4-bit units. Ports 4 and 5 can be paired for data input/output in 8-bit units. An LED can be driven directly.	Internal pullup resistor can be specified in 1-bit units by using mask option.

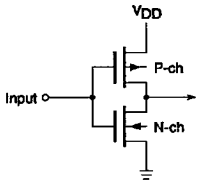
Notes:

(1) These ports directly drive LEDs.

(2) Port 3 lines are also used for MD0-MD3 in only.

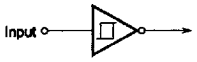
Figure 5. Input/Output Circuits

Type A. Part of type E-B



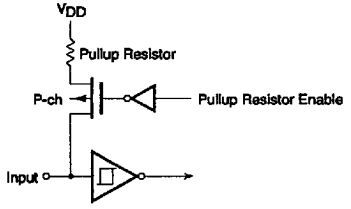
CMOS standard input buffer

Type B. $P0_0$, $\overline{RESET}$

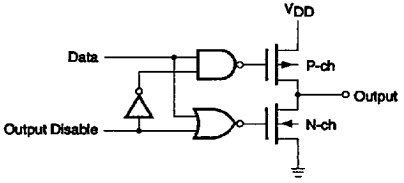


Schmitt trigger input with hysteresis characteristic.

Type B-C. $P1_0$-$P1_3$

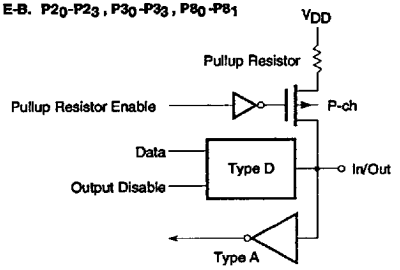


Type D. Part of type E-B, F-A

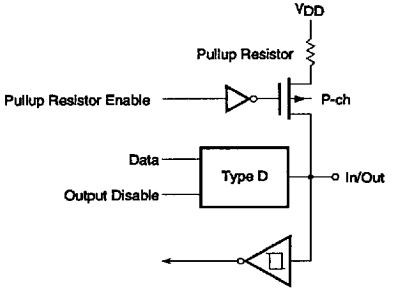


Push-pull output where output can be placed in high impedance. P and N channels are turned off.

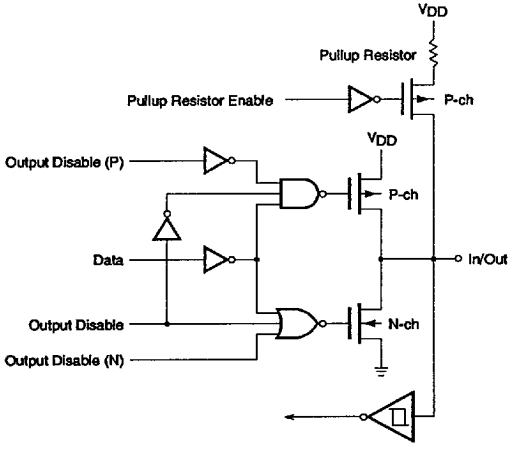
Type E-B. $P2_0$-$P2_3$, $P3_0$-$P3_3$, $P8_0$-$P8_1$



Type F-A. $P0_1$, $P8_0$-$P8_3$, $P7_0$-$P7_3$

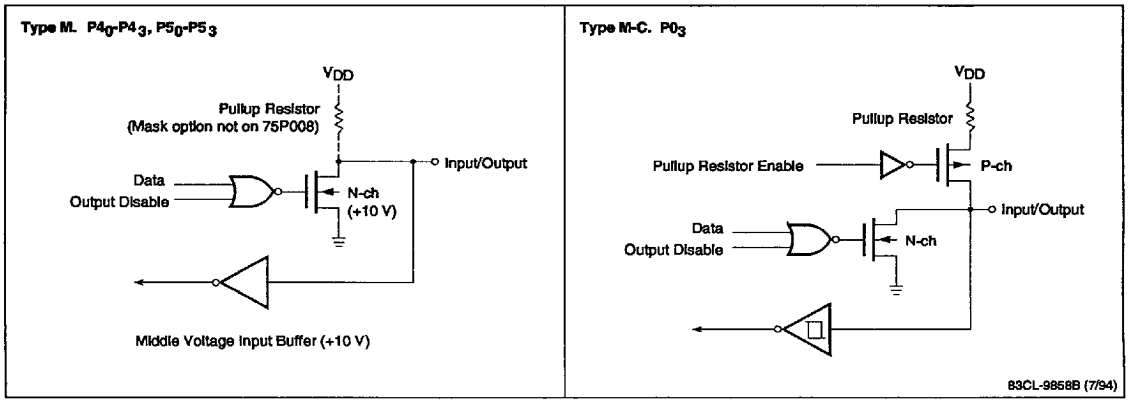


Type F-B. $P0_2$



83CL-9857B (1/94)

Figure 5. Input/Output Circuits (cont)



Clock Generator

The clock generator uses a crystal as a time base to generate its clocks. Figure 6 shows the generator, which consists of main and subsystem oscillators, frequency dividers, multiplexers, and three control registers (PCC, SCC, and CLOM). Registers PCC and SCC are programmed to supply frequencies derived from the crystal to the CPU at one of four speeds. Register CLOM controls the clock output to the output pin PCL. Registers PCC and SCC control the HALT and STOP logic.

The μPD75008 family contains a subsystem clock with an oscillator driven by an external crystal. The clock operates from 32 to 35 kHz. It can be used as a clock source for the watch timer and the CPU.

Basic Interval Timer

The basic interval timer provides continuous real time interrupts. The timer consists of a multiplexer, 8-bit free running counter, and the 4-bit BTM control register. See figure 7. Every time the counter increments to FFH, it generates an interrupt, overflows to 00H, and continues to count. In addition to clearing the counter and its interrupt request, the BTM register is used to select one of four clock inputs. The counter can generate 250 ms interrupts with a 4.19-MHz crystal. It also provides the oscillator stabilization time when the chip leaves the STOP mode.

Timer/Event Counter

The timer/event counter consists of a binary 8-bit up-counter, an 8-bit modulo register, an 8-bit comparator, a clock multiplexer, mode control register (TM0), and a TOUT flip-flop. See figure 8. Control logic allows the TOUT flip-flop signal to be output to port 2, bit 0.

The counter operates when an 8-bit value is loaded into the modulo register. A count register clock is selected in the clock multiplexer by control register TM0. The 8-bit up-counter is incremented every time it receives a counter pulse (CP). When the count value equals the modulo register count, the 8-bit comparator outputs a signal.This toggles the TOUT flip-flop and resets the count register to 00H. The count register continues to count up unless it is stopped. Every time the comparator has a match, the TOUT flip-flop changes state and generates interrupt IRQT0. Signal TOUT can also be used as a clock for the serial interface.

Watch Timer

The watch timer (figure 9) is normally used as a time source for keeping track of the time of day. With a 4.19-MHz crystal, it will generate interrupt requests (not interrupts) at 0.5 second or 3.9 msec intervals. The timer consists of an input clock multiplexer, a frequency divider, an output multiplexer, control logic, and control register WM. When a subsystem clock is present, the timer can operate when the chip is in the STOP mode. Also, the watch timer can output a 2-kHz buzzer signal.

Figure 6. Clock Generator

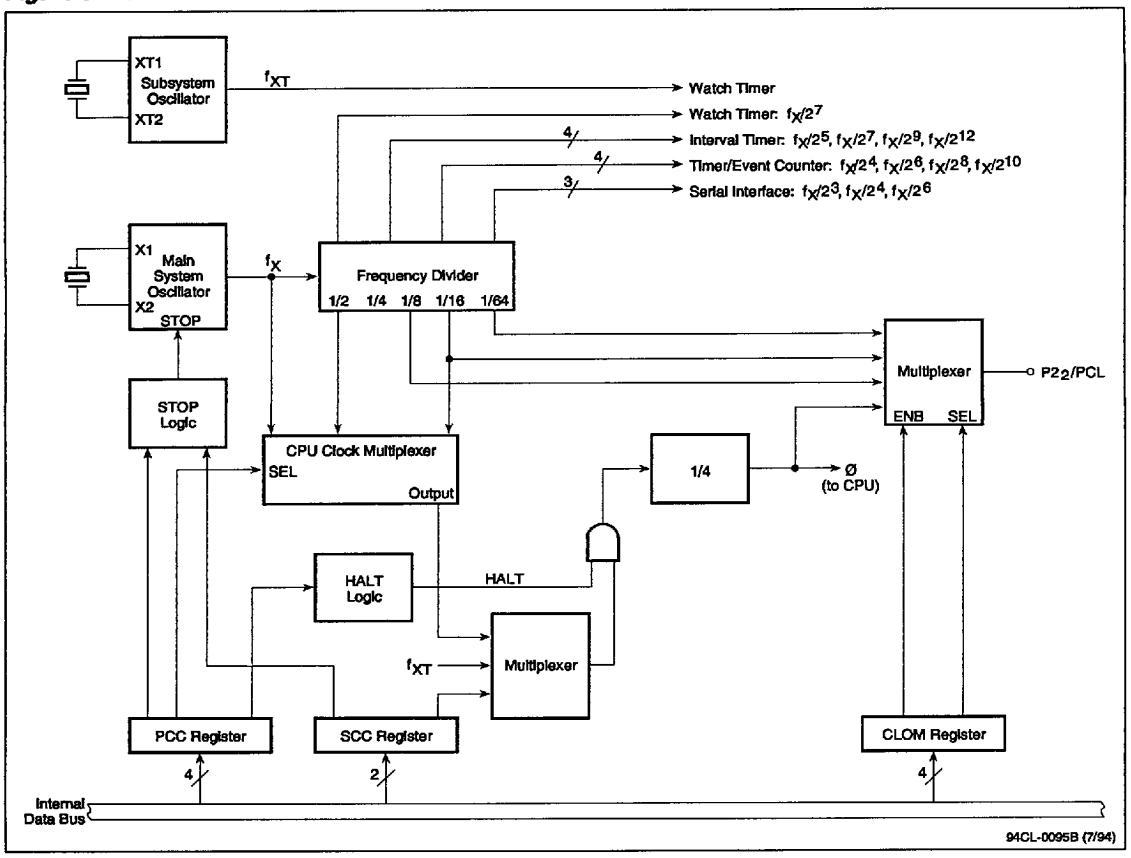


Figure 7. Basic Interval Timer

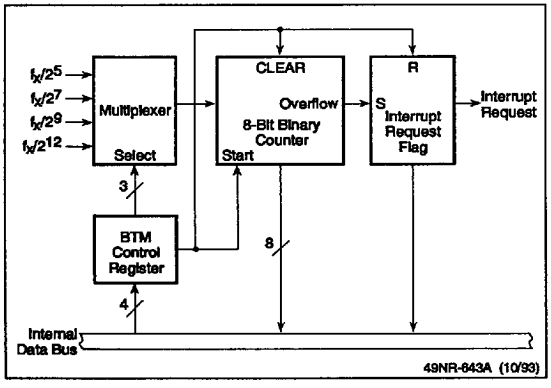


Figure 8. Timer/Event Counter

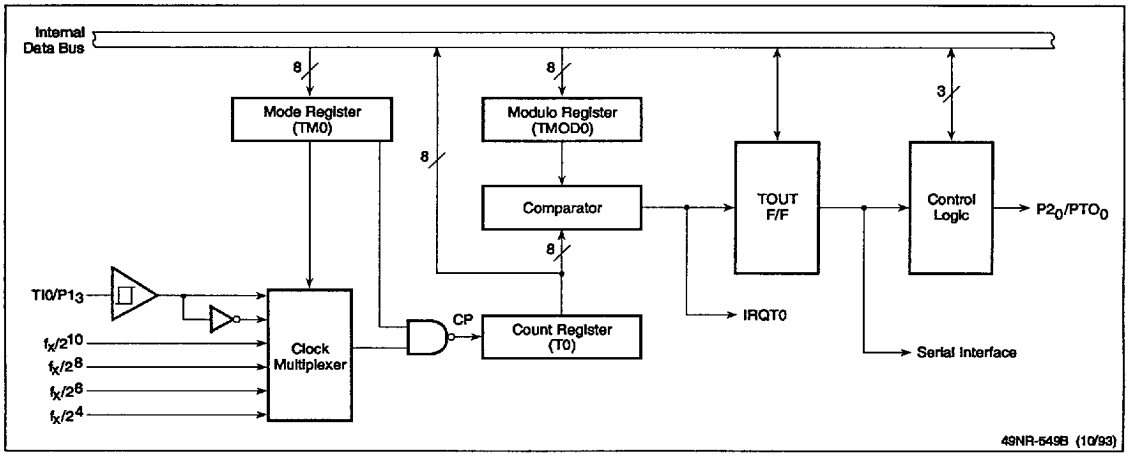
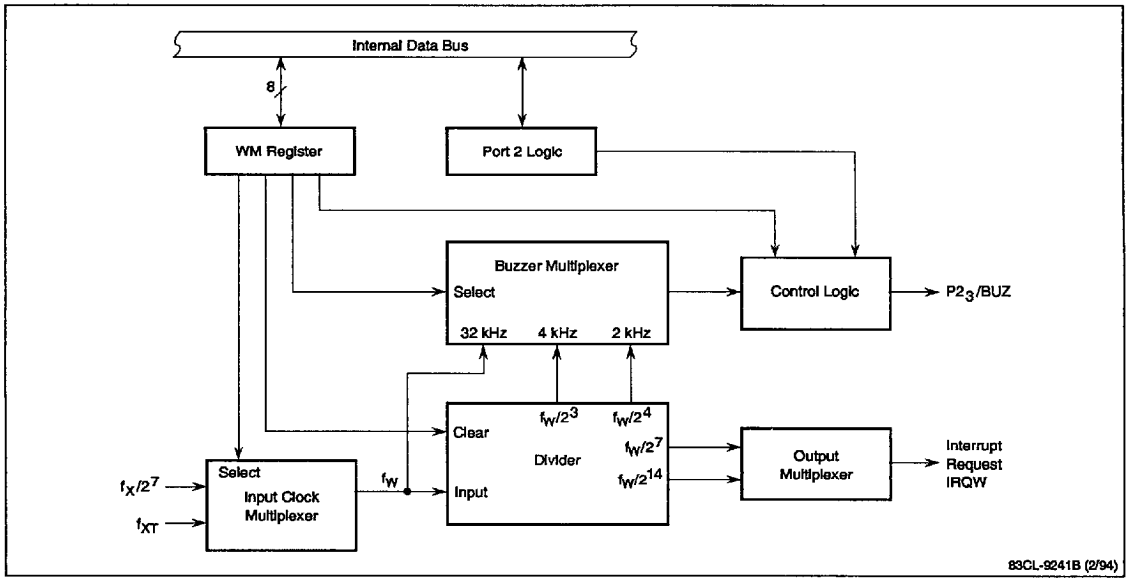


Figure 9. Watch/Timer

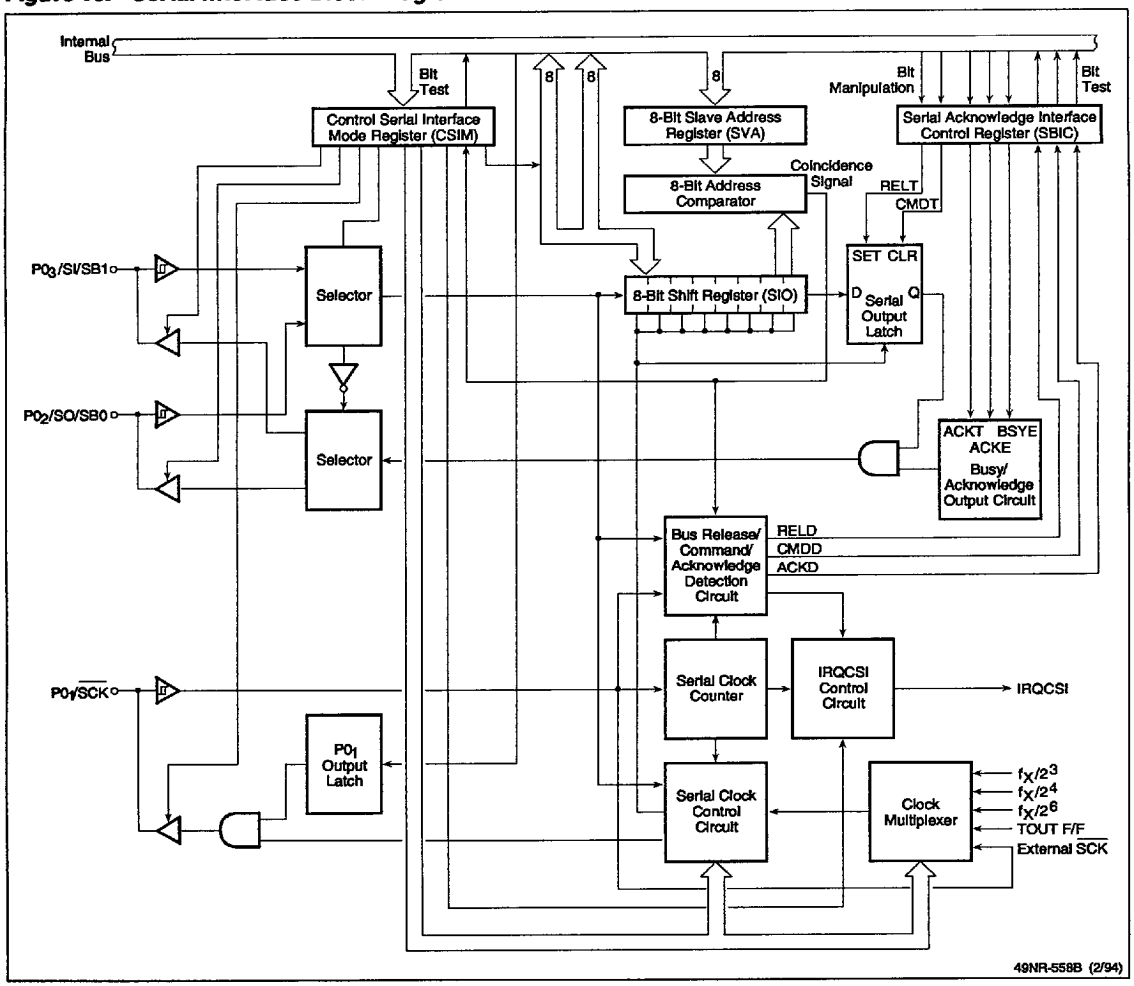


Serial Interface

The 8-bit serial interface allows the μPD75008 family devices to communicate with other NEC or NEC-like serial interfaces. The serial interface consists of an 8-bit shift register (SIO), serial output latch (SO), 8-bit address comparator, slave address register (SVA), control registers (CSIM and SBIC), busy/acknowledge circuitry, and bus release/detect circuitry. See figure 10. The interface also contains a serial clock counter, clock multiplexer, and serial clock control logic. The serial interface contains a three-wire interface, which consists of the following:

- Serial Data In (SI/SB1)
- Serial Data Out (SO/SB0)
- Serial Shift Clock ($\overline{SCK}$)

Figure 10. Serial Interface Block Diagram



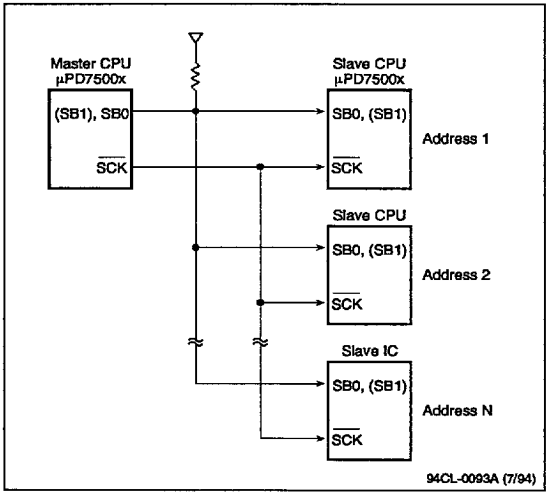
The three serial interface operation modes are:

- Two-wire serial mode
- Three-wire serial mode
- Two-wire SBI mode

The two or three-wire serial modes are the simplest modes; the 8-bit shift register is loaded with a byte of data and eight clock pulses are generated. The pulses shift data out the SO line and in from the SI line, thereby communicating in full duplex. When a byte of data is sent, a burst of eight clock pulses is generated and 8 bits of data are sent. The data may be sent with the LSB or MSB first. The interface can also be set to receive data only, consequently SO will be in the high impedance state. One of four internal clocks or an external clock clocks the data.

The SBI mode uses a two-wire interface with devices in a master/slave configuration. See figure 11. There is only one master device at a time; all others are slaves. The master sends addresses, commands, and data over the bus. The slaves are able to detect in hardware if their addresses were sent, a command was sent, or a portion of data was sent. There can be up to 256 slave addresses, 256 commands, and 256 data types. All commands are user definable. Commands can be sent to change slaves into masters; previous masters become slaves. Firmware performs this type of operation and thus the user decides whether the bus is simple or complex.

Figure 11. SBI Mode Master/Slave Configuration



Bit Sequential Buffer

The 16-bit sequential buffer is the only general-purpose RAM in the upper half of data memory bank 15. All the other locations in this bank contain either on-chip peripheral control registers or unused addresses. Its bits are addressed by register L. The buffer can be sequentially scanned by incrementing or decrementing register L. A typical application for this buffer is data storage for the next serial output or input. Another application is as a port output data storage area. The bit sequential buffer can be bit, nibble, or byte manipulated.

Interrupts

The three external and three internal interrupts are all vectored interrupts and are shown in figure 12. Table 4 lists a summary of the interrupts. Input INT2 detects rising edge inputs and generates an interrupt request flag, which is testable. Inputs KR0 through KR7 detect a falling edge and generate the same interrupt request flag as INT2. INT2 and KR0 through KR7 do not cause an interrupt, but can be used to release the standby mode. Interrupt requests and all interrupts except INT0 release the standby mode.

Figure 12. Interrupt Controller Block Diagram

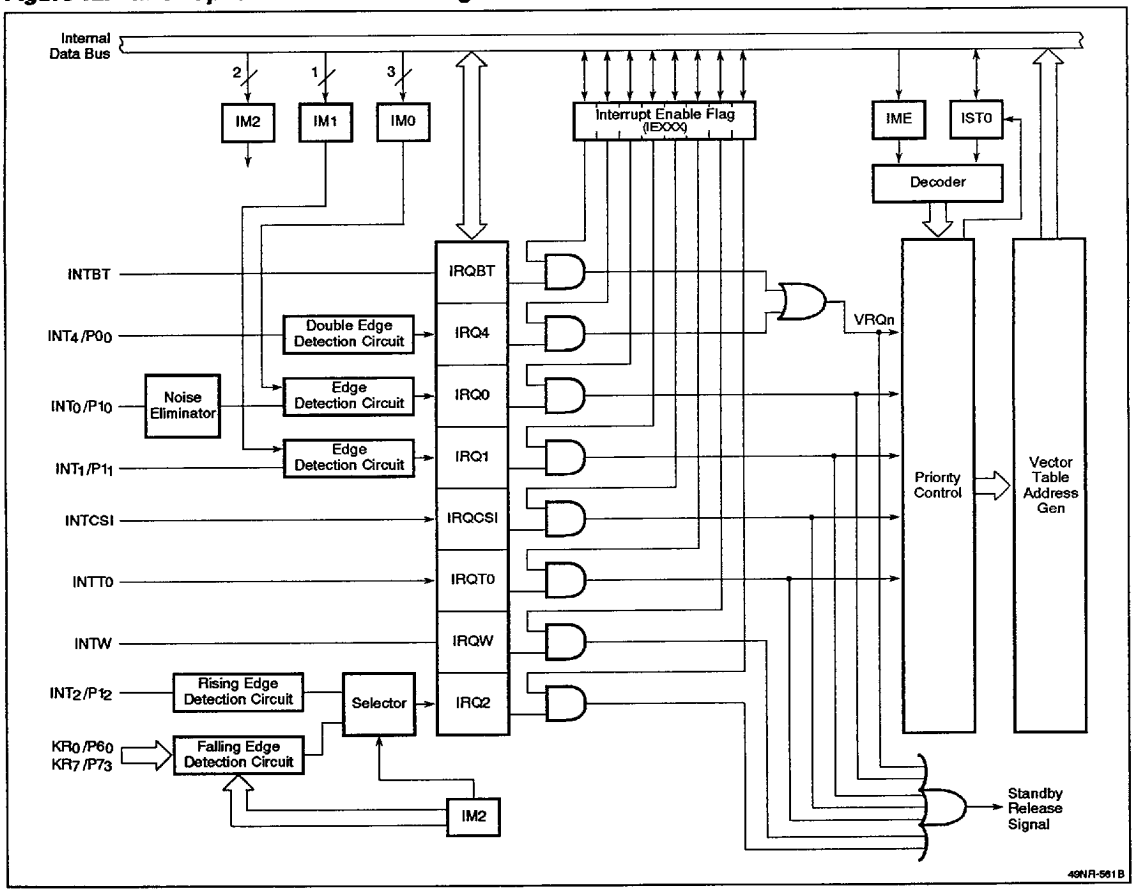


Table 4. Interrupt Sources

Interrupt Source	Internal/External	Interrupt Priority (see note)	Vectored Interrupt Request/ Table Address
INTBT (Time reference interval signal from the basic interval timer)	Internal	1	VRQ1/0002H
INT4 (Rising and falling edge detection)	External		
INT0 (Rising/falling edge detection)	External	2	VRQ2/0004H
INT1 (Rising/falling edge detection)	External	3	VRQ3/0006H
INTCSI (Serial data transfer end signal)	Internal	4	VRQ4/0008H
INTT0 (Signal generated when programmable timer/ counter count register and modulo register coincide)	Internal	5	VRQ5/000AH
INT2 (Rising edge input detection to INT2 pin or falling edge input detection to KR_0-KR_7)	External	Testable input signals (Test if IRQ2 and IRQW are set)	
INTW (Watch timer signal)	Internal		

Note: The interrupt priority determines the order when two or more simultaneous interrupts occur.

Standby Modes

The three standby modes are described below and in table 5.

HALT Mode. The HALT mode is entered by executing the HALT instruction. In this mode, the clock to the CPU is shut off (thus stopping the CPU), while all other partsof the chip, with the exception of INT0, remain fully functional.

STOP Mode. The STOP mode is entered by executing the STOP instruction. In this mode, the chip's main system oscillator is shut off, thereby stopping all portions of the chip except those which function off the subsystem clock or interrupt requests. If the subsystem clock is used, it always remains on.

The HALT and STOP modes are released by a $\overline{\text{RESET}}$ or by any interrupt request except INT0.

Data Retention Mode. This mode may be entered after entering the STOP mode. Here, supply voltage V_{DD} may be lowered to 2 volts to further reduce power consumption. The contents of the RAM and registers are retained. This mode is released by first raising V_{DD} to the proper operating voltage range and then releasing the STOP mode.

Reset

See table 6 for the state of the chip after a $\overline{\text{RESET}}$ is applied.

Table 5. Operation of the Standby Modes

Item	STOP Mode (Note 1)	HALT Mode (Note 2)
Clock oscillator	Only the main system clock oscillator is stopped. If a subsystem clock is present, it continues to oscillate.	Only CPU clock ϕ is stopped. Main and subsystem oscillators continue to operate.
Basic interval timer	Operation stops	Operation continues (IRQBT is set at reference time intervals).
Serial interface	Operates only when external $\overline{SCK}$ input is selected for serial clock.	Operational
Timer/event counter	Operates only when TIO pin input is selected for clock count.	Operational
Watch timer	Operates when f_{XT} is selected for the clock count.	Operational
External interrupts	INT1, INT2, and INT4 are allowed to operate. Only INT0 cannot operate.	All operational except INT0
CPU	Operational only from subsystem clock	Operation stops
Release signal	Enabled interrupt request signal (except INT0) or $\overline{RESET}$ input.	Enabled interrupt request signal (except INT0) or $\overline{RESET}$ input.

Notes:

(1) Use STOP instruction with main clock or SCC register with subsystem clock.

(2) Use HALT instruction for main or subsystem clock.

Table 6. State of the Device After Reset

Hardware		$\overline{RESET}$ Input During Standby Mode	$\overline{RESET}$ Input During Normal Operation
Program counter (PC)	μPD75004	The low-order 4 bits of program memory address 0000H are loaded into PC11 - PC8. The contents of address 0001H are loaded into PC7 - PC0.	
	μPD75006 μPD75008 μPD75P008	The low-order 5 bits of program memory address 0000H are loaded into PC12 - PC8. The contents of address 0001H are loaded into PC7 - PC0.	
PSW	Carry flag (CY)	Held	Undefined
	Skip flags (SK0 - SK2)	0	0
	Interrupt status flag (IST0)	0	0
	Memory bank enable flag (MBE)	Bit 7 of program memory address 0000H is loaded into MBE	
Stack pointer (SP)		Undefined	Undefined
Data memory (RAM)		Held (Note 1)	Undefined
General-purpose registers (X, A, H, L, D, E, B, C)		Held	Undefined
Memory bank selection register (MBS)		0	0
Basic interval timer	Counter (BT)	Undefined	Undefined
	Mode register (BTM)	0	0
Timer/event counter	Counter (T0)	0	0
	Modulo register (TMOD0)	FFH	FFH
	Mode register (TM0)	0	0
	TOE0, TOUT F/F	0, 0	0, 0
Watch timer	Mode register (WM)	0	0

Table 6. State of the Device After Reset (cont)

Hardware		RESET Input During Standby Mode	RESET Input During Normal Operation
Serial interface	Shift register (SIO)	Held	Undefined
	Operation mode register (CSIM)	0	0
	SBI control register (SBIC)	0	0
	Slave address register (SVA)	Held	Undefined
Clock generator and clock output circuit	Processor clock control register (PCC)	0	0
	System clock control register (SCC)	0	0
	Clock output mode register (CLOM)	0	0
Interrupt function	Interrupt request flags (IRQxxx)	Reset to 0	Reset to 0
	Interrupt enable flags (IExxx)	0	0
	Interrupt master enable flag (IME)	0	0
	INT0, INT1, and INT2 and mode registers (IM0, IM1, and IM2)	0, 0, 0	0, 0, 0
Digital ports	Output buffers	Off	Off
	Output latches	Cleared to 0	Cleared to 0
	Input/output mode registers (PMGA, B, C)	0	0
	Pullup resistor specification register (POGA, POGB)	0	0
Bit sequential buffer		Held	Undefined
Pin conditions	$P0_0$–$P0_3$, $P1_0$–$P1_3$, $P2_0$–$P2_3$, $P3_0$–$P3_3$, $P6_0$–$P6_3$, $P7_0$–$P7_3$, $P8_0$-$P8_1$	Input	Input
	$P4_0$–$P4_3$, $P5_0$–$P5_3$,	With incorporated pullup resistor, high level; with open drain, high impedance	

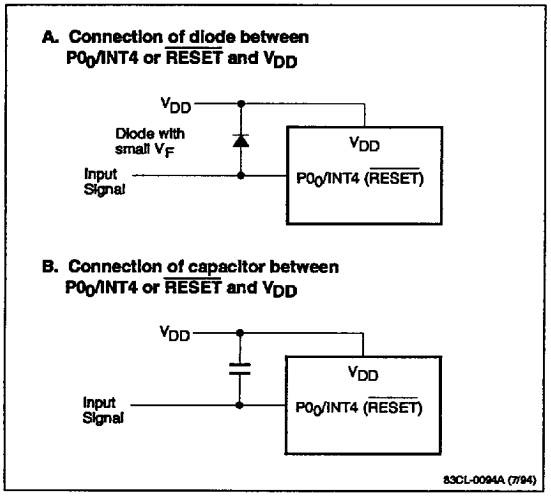
Note: (1) The data of data memory address 0F8H-0FDH is undefined by RESET.

Caution

Apart from their normal functions, The $P0_0$/INT4 and $\overline{RESET}$ pins are used to test the internal operation of the programmable devices. The test mode is entered by applying a voltage greater than V_{DD} to either of these pins.

For this reason, care must be taken to limit the voltage applied to these two pins. For example, it is conceivable that even during normal operation enough spurious noise may be present to set the chip into the test mode. If this happens, further normal operation is impossible. Consequently, it is important that interwiring noise be suppressed as much as possible. If this is inconvenient, anti-noise measures, like those shown in figure 13, should be implemented.

Figure 13. Noise Reduction Techniques



ELECTRICAL SPECIFICATIONS

Absolute Maximum Ratings

T_A = 25°C

Supply voltage, V_{DD}	−0.3 to +7.0 V
Programming voltage, V_{PP} (μPD75P008 only)	-0.3 to +13.5 V
Input voltage, V_{I1} (Note 1)	−0.3 to V_{DD} + 0.3 V
Input voltage, V_{I2} (Ports 4 and 5 with open drain)	−0.3 to 11 V
Output voltage, V_O	−0.3 to V_{DD} + 0.3 V
High-level output current, I_{OH} (Single pin; standard grade)	−10 mA
High-level output current, I_{OH} (Single pin; special grade)	−10 mA peak −5 mA rms (Note 2)
High-level output current, I_{OH} (Total of all pins; standard grade)	−30 mA
High-level output current, I_{OH} (Total of all pins; special grade)	−30 mA peak −15 mA rms (Note 2)
Low-level output current, I_{OL} (Single pin; ports 0, 3-5; standard grade)	30 mA peak, 15 mA rms (Notes 2, 3)
Low-level output current, I_{OL} (Single pin; ports 3-5; special grade)	20 mA peak, 10 mA rms (Note 2)
Low-level output current, I_{OL} (Single pin; all ports except 0, 3-5; standard grade)	20 mA peak, 10 mA rms (Notes 2, 3)
Low-level output current, I_{OL} (Single pin; all ports except 3-5; special grade)	10 mA peak, 5 mA rms (Note 2)
Low-level output current, I_{OL} (Total of ports 0, 3-5, 8; standard grade)	160 mA peak, 120 mA rms (Notes 2, 3)
Low-level output current, I_{OL} (Total of ports 0, 3, 8; special grade)	80 mA peak, 40 mA rms (Notes 2, 3)
Low-level output current, I_{OL} (Total of ports 2, 6-7; standard grade)	66 mA peak, 33 mA rms (Note 2)
Low-level output current, I_{OL} (Total of ports 2, 6-7; special grade)	40 mA peak, 20 mA rms (Note 2)
Low-level output current, I_{OL} (Total of ports 4-5; special grade)	100 mA peak, 60 mA rms (Note 2)
Storage temperature, T_{STG}	−65 to +150°C
Operating temperature, T_{OPT} (μPD7500x and μPD7500x(A))	−40 to +85°C
Operating temperature, T_{OPT} (μPD75P008 only)	−10 to +70°C

Exposure to Absolute Maximum Ratings for extended periods may affect device reliability; exceeding the ratings could cause permanent damage. The device should be operated within the limits specified under DC and AC characteristics.

Notes:

(1) All ports: ports 4 and 5 have pullup resistors. Does not apply to μPD75P008.

(2) Effective value = Peak value x $(\text{Duty})^{1/2}$

(3) Does not include port 0, bit 0.

Capacitance

T_A = 25°C; V_{DD} = 0 V

Parameter	Symbol	Min	Max	Unit	Conditions
Input capacitance	C_{IN}		15	pF	f = 1 MHz; all unmeasured pins returned to ground
Output capacitance	C_{OUT}		15	pF	
I/O capacitance	C_{IO}		15	pF	

Main System Clock Oscillator

Refer to figures 14 and 16.
μPD7500x/00x(A): T_A = −40 to +85°C, V_{DD} = 2.7 to 6.0 V
μPD75P008: T_A = −10 to +70°C, V_{DD} = 4.5 to 5.5 V

Oscillator	Parameter	Symbol	Min	Typ	Max	Unit	Conditions
Ceramic resonator (Figure 14 A)	Oscillation frequency (Note 1)	f_X	1.0		5.0	MHz	V_{DD} is in the oscillator voltage range.
	Oscillation stabilization time (Note 2)				4 (Note 3)	ms	After V_{DD} reaches the minimum oscillator operating voltage range.
Crystal resonator (Figure 14 A)	Oscillation frequency (Note 1)	f_X	1.0	4.19	5.0 (Note 4)	MHz	
	Oscillation stabilization time (Note 2)				10 (Notes 3)	ms	V_{DD} = 4.5 to 6.0 V for 7500x and 7500x(A) or 4.5 to 5.5 V for μPD75P008.
					30 (Notes 3)	ms	For μPD7500x and 7500x(A) only at V_{DD} = 2.7 – 6.0 V.
External clock (Figure 14 B)	X1 input frequency (Note 1)	f_X	1.0		5.0 (Note 4)	MHz	
	X1 input low- and high-level width	t_{XH}, t_{XL}	100		500	ns	

Notes:

(1) The oscillation frequency and X1 input frequency are included only to show the characteristics of the oscillators. Refer to the AC Characteristics table for actual instruction execution times.

(2) The oscillation stabilization time is the time required for the oscillator to stabilize after voltage is applied or the STOP mode is released.

(3) Values shown are for the recommended resonators. Values for resonators not shown in this data sheet should be obtained from the manufacturer's specification sheets.

(4) When the oscillation frequency is f_x = 4.19 to 5.0 MHz, do not select PCC = 0011 as the instruction execution time; otherwise, one machine cycle is set to less than 0.95 μs, falling short of the rated minimum value of 0.95 μs.

Subsystem Clock Oscillator

Refer to figures 15 and 16.
μPD7500x and 7500x(A): T_A = −40 to +85°C; V_{DD} = 2.7 to 6.0 V
μPD75P008: T_A = −10 to +70°C; V_{DD} = 4.5 to 5.5 V

Oscillator	Parameter	Symbol	Min	Typ	Max	Unit	Conditions
Crystal resonator (figure 15 A)	Oscillation frequency	f_{XT}	32	32.768	35	kHz	
	Oscillation stabilization time			1.0	2	s	V_{DD} = 4.5 to 6.0 V for 7500x and 7500x(A) or 4.5 to 5.5 V for μPD75P008.
					10	s	For μPD7500x and 7500x(A) only at V_{DD} = 2.7 – 6.0 V.
External clock (figure 15 B)	XT1 input frequency	f_{XT}	32		100	kHz	
	XT1 input low- and high-level width	t_{XTH}, t_{XTL}	5		15	μs	

Recommended Oscillator Circuit Constants (For 7500x only)

Main system clock = Ceramic; T_A = −40 to +85°C

Manufacturer	Part Number (Note 1)	Frequency (MHz)	C1 (pF)	C2 (pF)	Oscillation Voltage Min (V)	Oscillation Voltage Max (V)
Murata	CSA x.xxMK	1.0–1.99	30	30	2.7	6.0
	CSA x.xxMG093	2.0–2.44	30	30	2.7	6.0
	CST x.xxMG093	2.0–2.44	(Note 2)	(Note 2)	2.7	6.0
	CSA x.xxMGU	2.45–5.0	30	30	2.7	6.0
	CST x.xxMGU	2.45–5.0	(Note 2)	(Note 2)	2.7	6.0
	CSA x.xxMG	2.0–5.0	30	30	3.0	6.0
	CST x.xxMG	2.0–5.0	(Note 2)	(Note 2)	3.0	6.0
Kyocera	KBR-1000H	1.0	100	100	2.7	6.0
	KBR-2.0MS	2.0	47	47	2.7	6.0
	KBR-4.0MS	4.0	33	33	2.7	6.0
	KBR-5.0M	5.0	33	33	3.0	6.0
Toko	CRHB4.00M	4.0	27	27	3.0	6.0

Notes:

(1) x.xx indicates frequency.

(2) C1 and C2 not required; they are in the oscillator.

Figure 14. Main System Clock Configurations

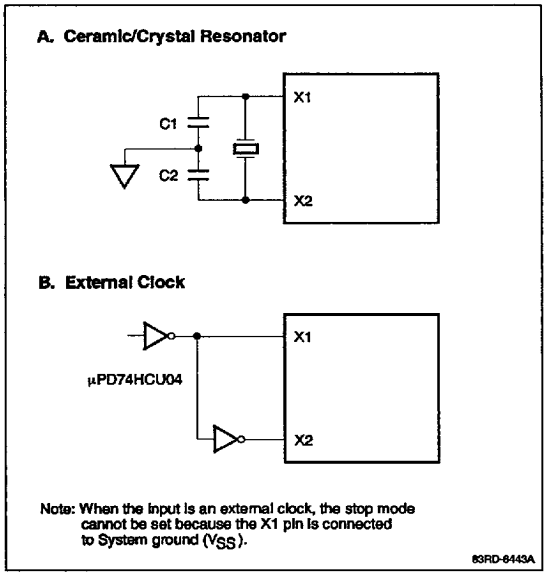


Figure 15. Subsystem Clock Configurations

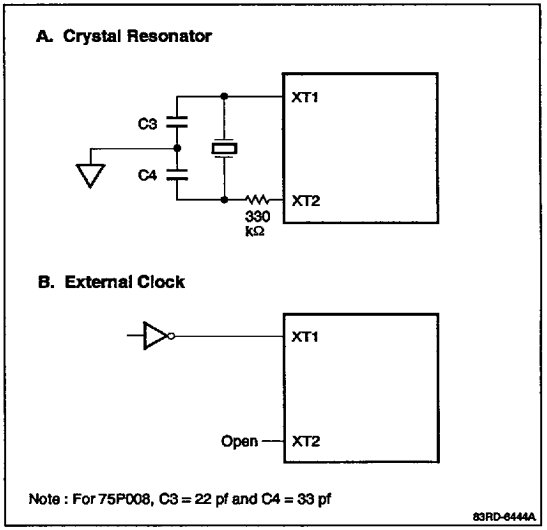
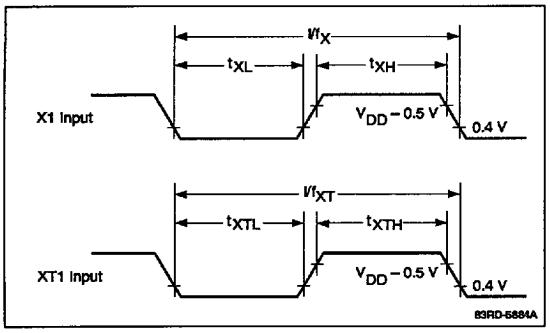


Figure 16. Clock Timing



Recommended Oscillator Circuit Constants (For 7500x only)

Main system clock = Crystal; T_A = –20 to +70°C

Manufacturer	Part Number	Frequency (MHz)	C1 (See note) (pF)	C2 (pF)	Oscillation Voltage Min (V)	Oscillation Voltage Max (V)
Kinseki	HC-6U	1.0–2.0	20	22	2.7	6.0
	HC-18U, HC-43/U, HC-49/U	2.0–5.0	20	22	2.7	6.0

Note: Keep C1 between 15 and 33 pF when adjusting the oscillation frequency.

Recommended Oscillator Circuit Constants (For 7500x only)

Subsystem clock = Crystal; T_A = –10 to +60°C

Manufacturer	Part Number	Frequency (MHz)	C3 (See note) (pF)	C4 (pF)	R (kΩ)	Oscillation Voltage Min (V)	Oscillation Voltage Max (V)
Kinseki	P-3	32.768	18	18	330	2.7	6.0

Note: Keep C3 between 10 and 33 pF when adjusting the oscillation frequency.

DC Characteristics

Refer to figure 17 for μPD7500x only
μPD7500x and 7500x(A): T_A = −40 to +85°C, V_{DD} = 2.7 to 6.0 V
μPD75P008: T_A = −10 to +70°C, V_{DD} = 4.5 to 5.5 V

Parameter	Symbol	Min	Typ	Max	Unit	Conditions
High-level input voltage	V_{IH1}	0.7 V_{DD}		V_{DD}	V	Ports 2, 3, 8
	V_{IH2}	0.8 V_{DD}		V_{DD}	V	Ports 0, 1, 6, 7, and $\overline{RESET}$
	V_{IH3}	0.7 V_{DD}		V_{DD}	V	Ports 4 and 5; built-in pullup resistor except PD75P008
		0.7 V_{DD}		10	V	Ports 4 and 5 with open drain
	V_{IH4}	V_{DD} − 0.5		V_{DD}	V	X1, X2, XT1
Low-level input voltage	V_{IL1}	0		0.3 V_{DD}	V	Ports 2, 3, 4, 5, 8
	V_{IL2}	0		0.2 V_{DD}	V	Ports 0, 1, 6, 7; $\overline{RESET}$
	V_{IL3}	0		0.4	V	X1, X2, XT1
High-level output voltage	V_{OH1} (Note 1)	V_{DD} − 1.0			V	Ports 0, 2, 3, 6, 7, 8; I_{OH} = −1 mA
	V_{OH2} (Note 2)	V_{DD} − 0.5			V	Ports 0, 2, 3, 6, 7, 8; V_{DD} = 2.7 to 6.0 V; I_{OH} = −100 μA
Low-level output voltage	V_{OL1}		0.4	2.0	V	Ports 4 and 5; (Note 3); I_{OL} = 15 mA
			0.15	1.0	V	Ports 4 and 5; (Note 4); I_{OL} = 5 mA
			0.6	2.0	V	Port 3; (Note 3); I_{OL} = 15 mA
			0.20	1.0	V	Port 3; (Note 4); I_{OL} = 5 mA
				0.4	V	Ports 0, 2-8; (Note 1); I_{OL} = 1.6 mA
				0.5 (Note 2)	V	Ports 0, 2-8; I_{OL} = 400 μA, V_{DD} = 2.7 to 6.0 V
	V_{OL2}			0.2 V_{DD} (Note 1)	V	SB0, SB1 open drain; pullup resistance ≥ 1kΩ
				0.2 V_{DD} (Note 2)	V	SB0, SB1 open drain pullup resistance ≥ 5kΩ, V_{DD} = 2.7 to 6.0 V
High-level input leakage current	I_{LIH1}			3	μA	All except X1, X2, and XT1; V_{IN} = V_{DD}
	I_{LIH2}			20	μA	X1, X2, and XT1; V_{IN} = V_{DD}
	I_{LIH3}			20	μA	Ports 4, 5 with open drain; V_{IN} = 10 V
Low-level input leakage current	I_{LIL1}			−3	μA	All except X1, X2, and XT1; V_{IN} = 0 V
	I_{LIL2}			−20	μA	X1, X2, and XT1; V_{IN} = 0 V
High-level output leakage current	I_{LOH1}			3	μA	All except ports 4 and 5 with open drain; V_{OUT} = V_{DD}
	I_{LOH2}			20	μA	Ports 4 and 5 with open drain; V_{OUT} = 10 V
Low-level output leakage current	I_{LOL}			−3	μA	V_{OUT} = 0 V
Built-in pullup resistor	R_{L1}	15	40	80	kΩ	Ports 0-3, 6-8 (except $P0_0$); V_{IN} = 0 V; V_{DD} = 5.0 V ± 10%
		30 (Note 2)		300 (Note 2)	kΩ	Ports 0-3, 6-8 (except $P0_0$); V_{IN} = 0 V; V_{DD} = 3.0 V ± 10%
	R_{L2} (Note 2)	15	40	70	kΩ	Ports 4, 5; V_{OUT} = V_{DD} − 2.0 V; V_{DD} = 5.0 V ± 10%
		10		60	kΩ	Ports 4, 5; V_{OUT} = V_{DD} − 2.0 V; V_{DD} = 3.0 V ± 10%

DC Characteristics (cont)

Parameter	Symbol	Min	Typ	Max	Unit	Conditions
Supply current (Note 5)	I_{DD1}	(Note 2)	2.5	8.0	mA	V_{DD} = 5.0 V ± 10% (Notes 6, 7, 8)
		(Note 2)	0.35	1.2	mA	V_{DD} = 3.0 V ± 10% (Notes 6, 7, 9)
		(Note 10)	5	15	mA	V_{DD} = 5 V ±10%; (Notes 6, 7, 8)
	I_{DD2}		500	1500	μA	HALT mode; V_{DD} = 5 V ± 10% (Notes 6, 7)
		(Note 2)	150	450	μA	HALT mode; V_{DD} = 3 V ± 10% (Notes 6, 7)
	I_{DD3}	(Notes 2, 7, 11)	30	90	μA	V_{DD} = 3 V ± 10%
		(Notes 7, 10, 11)	350	1000	μA	V_{DD} = 5 V ±10%
	I_{DD4}	(Notes 2, 7, 11)	5	15	μA	HALT mode; V_{DD} = 3 V ± 10%
		(Notes 7, 10, 11)	35	100	μA	HALT mode V_{DD} = 5 V ±10%
	I_{DD5}		0.5	20	μA	STOP mode; XT1 = 0 V; V_{DD} = 5.0 V ± 10%
		(Note 2)	0.1	10	μA	STOP mode; XT1 = 0 V; V_{DD} = 3.0 V ± 10%
		(Note 2)	0.1	5	μA	STOP mode; XT1 = 0 V; V_{DD} = 3.0 V ± 10%; T_A = 25°C

Notes:

(1) V_{DD} = 4.5 to 6.0 V for 7500x and 7500x(A) and V_{DD} = 4.5 to 5.5 V for 75P008.

(2) For 7500x and 7500x(A) only.

(3) For 7500x with V_{DD} = 4.5 to 6.0 V and 75P008 with V_{DD} = 4.5 to 5.5 V.

(4) For 7500x(A) only and V_{DD} = 4.5 to 6.0 V.

(5) Does not include pullup resistor current.

(6) 4.19-MHz crystal oscillator; C1 = C2 = 22 pF.

(7) 32.768-kHz subsystem crystal oscillator is operating.

(8) When operated in the high-speed mode with the processor clock control register (PCC) set to 0011.

(9) When operated in the low-speed mode with the PCC set to 0000.

(10) For 75P008 only.

(11) The system clock control register (SCC) is set to 1001 and the main system oscillator is stopped.

Figure 17. DC Characteristics

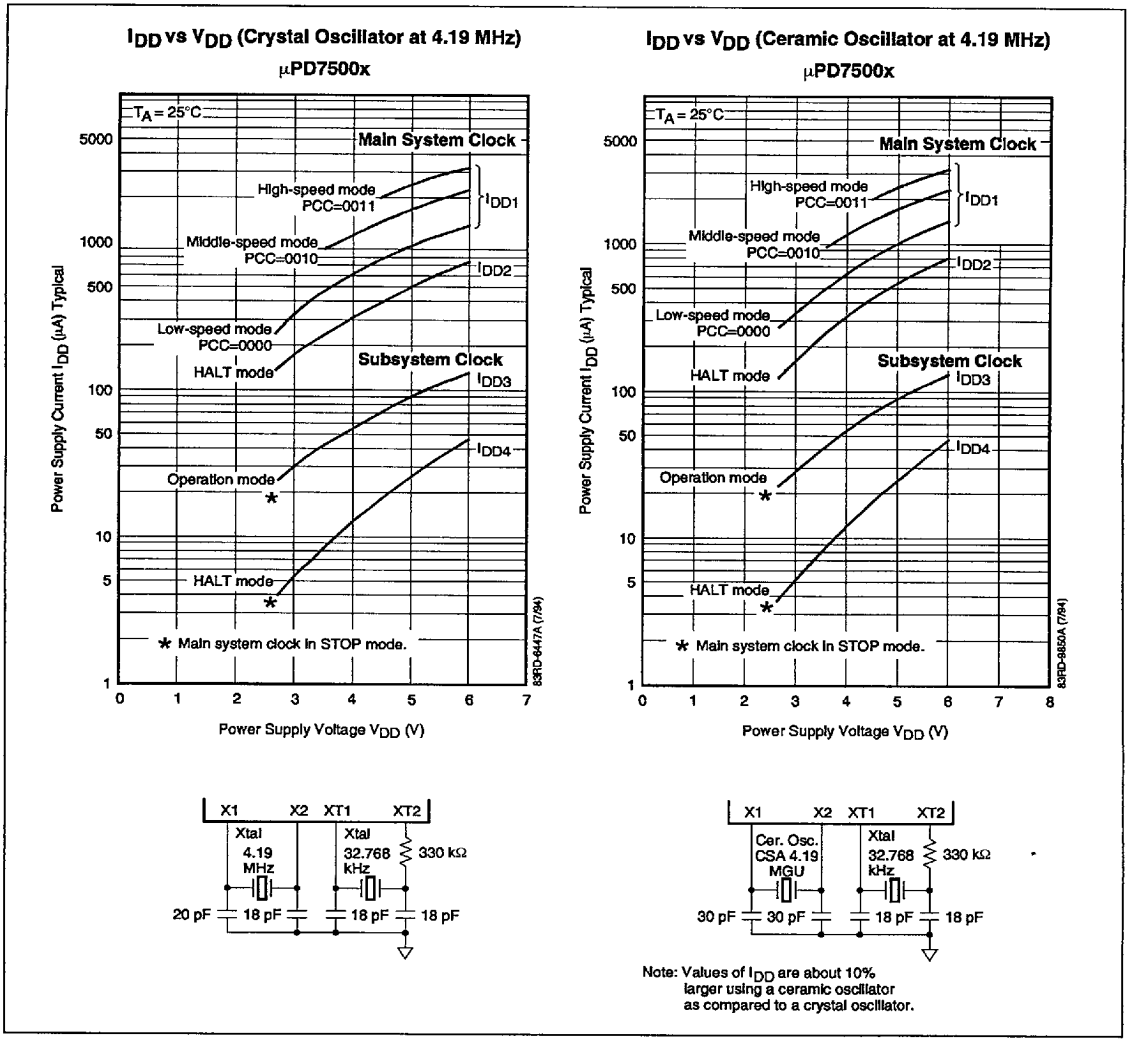
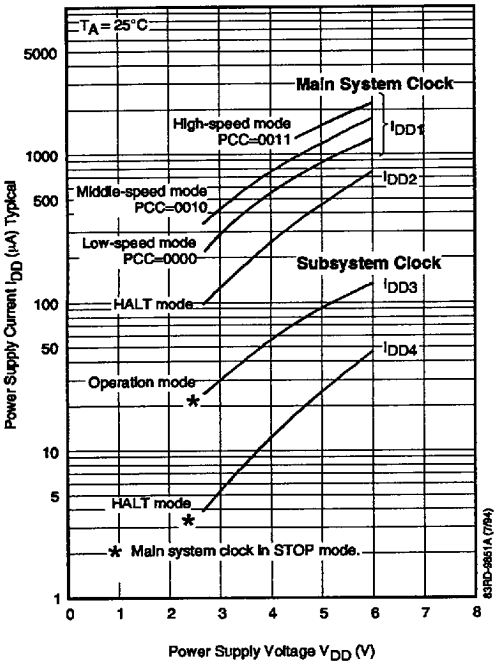
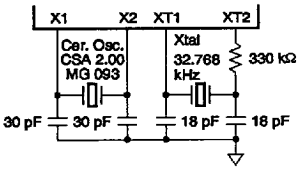


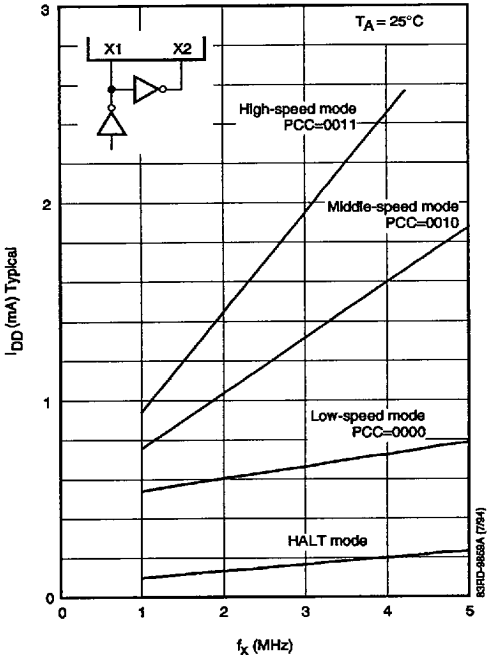
Figure 17. DC Characteristics (cont)

I_{DD} vs V_{DD} (Ceramic Oscillator at 2.00 MHz)
μPD7500x





I_{DD} vs f_X (V_{DD} = 5 V)
μPD7500x



I_{DD} vs f_X (V_{DD} = 3 V)
μPD7500x

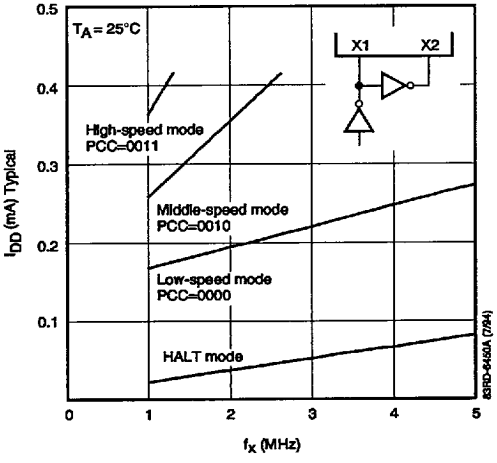


Figure 17. DC Characteristics (cont)

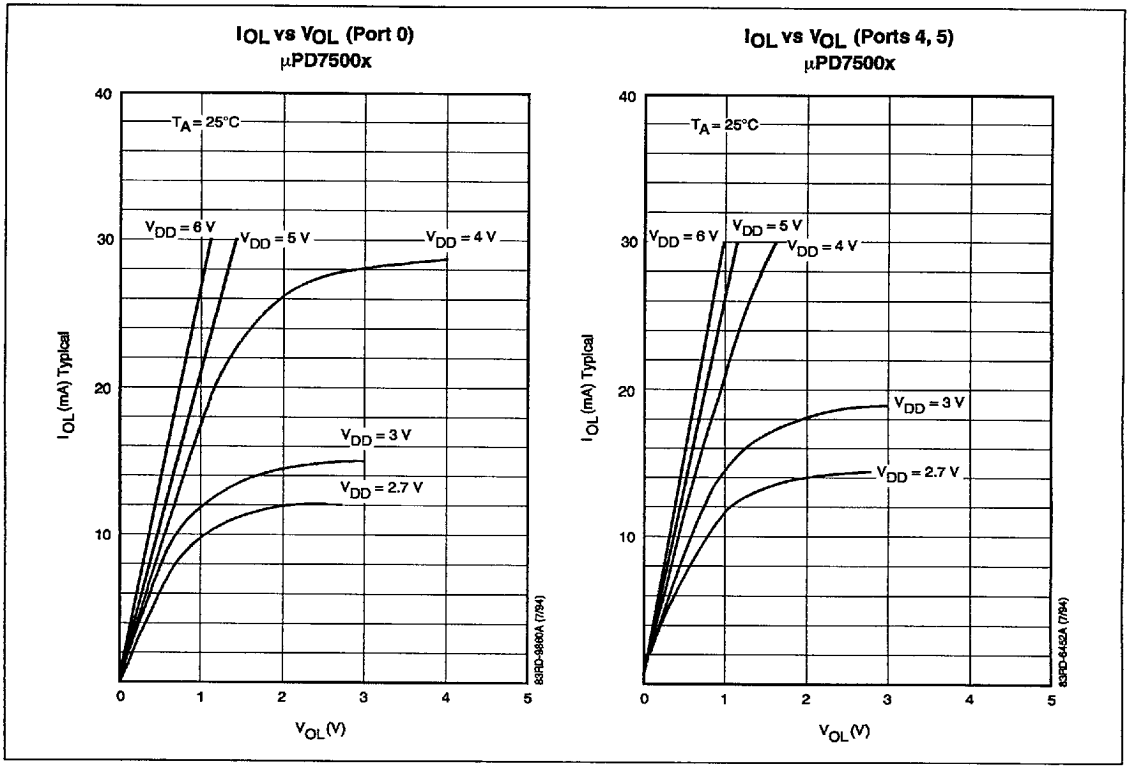


Figure 17. DC Characteristics (cont)

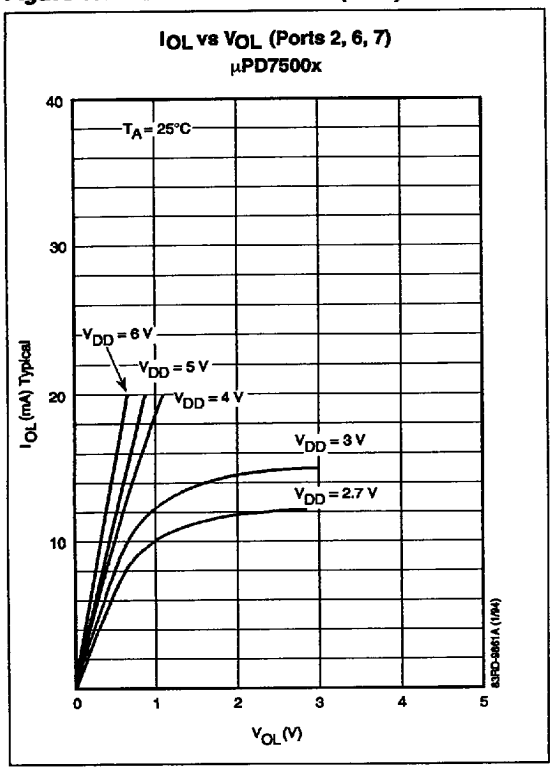
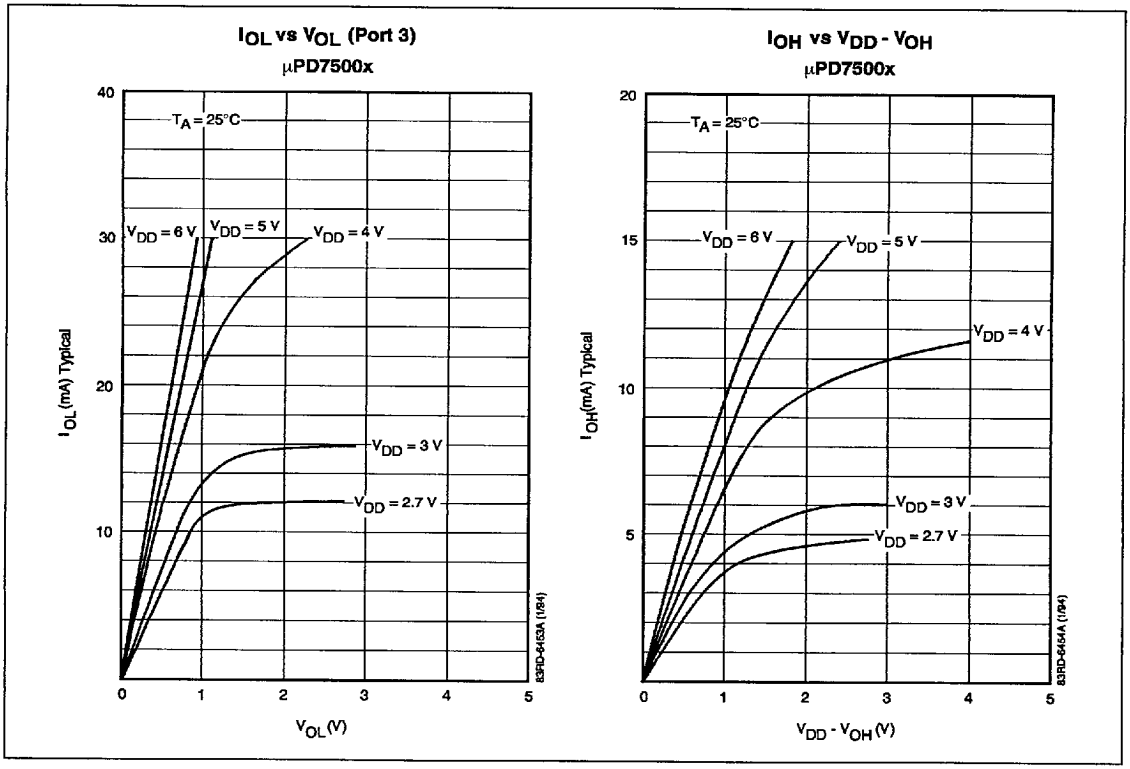


Figure 17. DC Characteristics (cont)



AC Characteristics

Refer to figures 18 through 22
μPD7500x and μPD7500x(A): T_A = −40 to +85°C, V_{DD} = 2.7 to 6.0 V
μPD75P008: T_A = −10 to +70°C, V_{DD} = 4.5 to 5.5 V.

Parameter	Symbol	Min	Typ	Max	Unit	Conditions
Cycle time (Note 1)	t_{CY} (figure 18)	0.95		64	μs	Main system clock (Note 2)
		3.8	(Note 3)	64	μs	Main system clock; V_{DD} = 2.7 to 6.0 V
		114	122	125	μs	Subsystem clock
TI0 input frequency	f_{TI} (figure 20)	0		1	MHz	(Note 2)
		0	(Note 3)	275	kHz	V_{DD} = 2.7 to 6.0 V
TI0 input low- and high-level width	t_{TIH}, t_{TIL} (figure 20)	0.48			μs	(Note 2)
		1.8	(Note 3)		μs	V_{DD} = 2.7 to 6.0 V
Interrupt inputs low- and high-level width	t_{INTH}, t_{INTL} (figure 21)	(Note 4)			μs	INT0
		10			μs	INT1, INT2, INT4
		10			μs	KR0-KR7
$\overline{\text{RESET}}$ low-level width	t_{RSL} (figure 22)	10			μs	

Notes:

(1) Cycle time (minimum instruction execution time) is determined by the frequency of the oscillator connected to the microcontroller, system clock control register (SCC), and the processor clock control (PCC).

(2) V_{DD} = 4.5 to 6.0 V for 7500x and 7500x(A) and V_{DD} = 4.5 to 5.5 V for 75P008.

(3) For 7500x and 7500x(A) only.

(4) $2t_{CY}$ or 128/fx, depending on the setting of the interrupt mode register (IM0).

Figure 18. Main System Clock Operation, t_{CY} vs V_{DD}

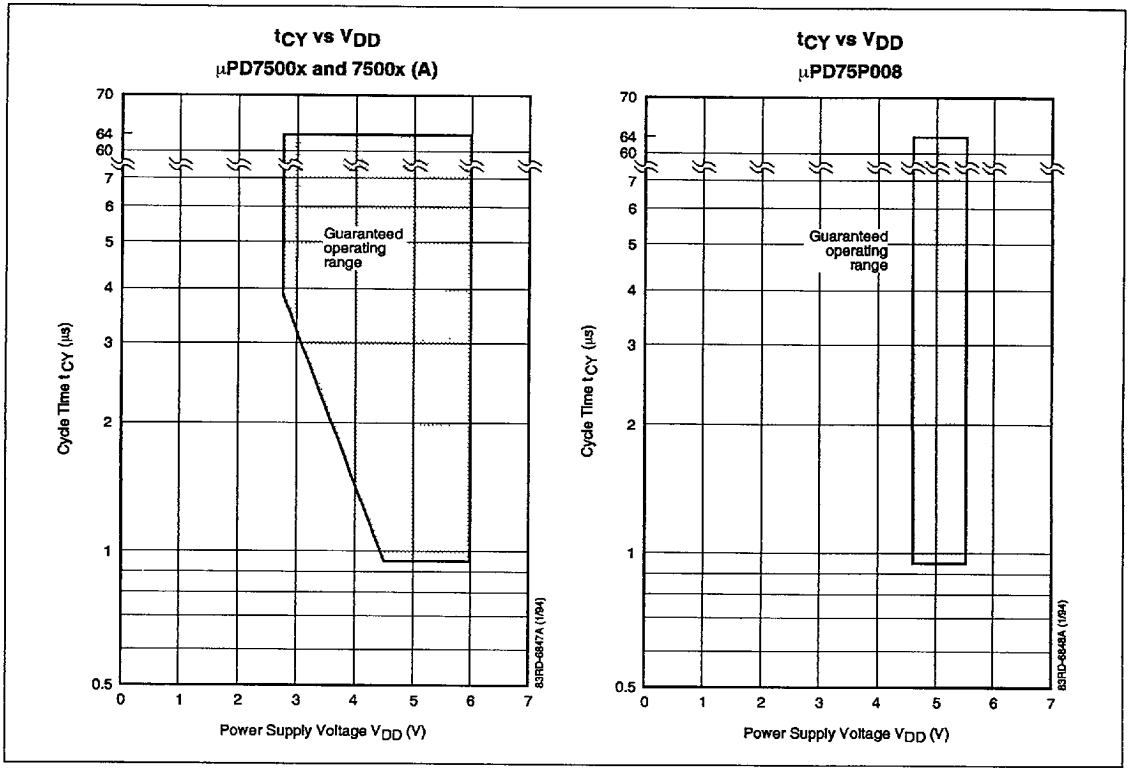


Figure 19. AC Timing Measurement Point

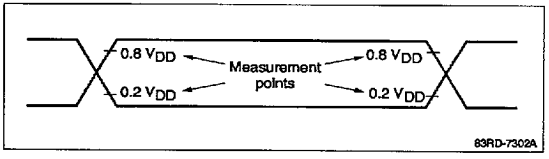


Figure 20. TIO Timing

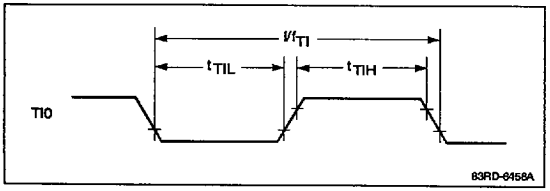


Figure 21. Interrupt Input Timing

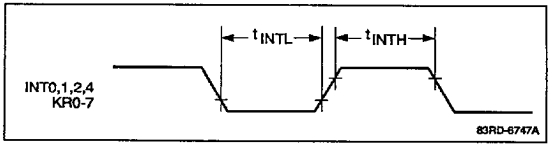
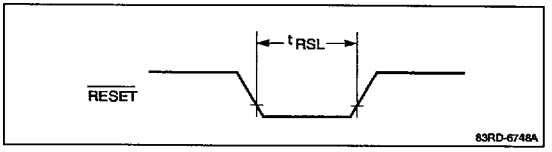


Figure 22. $\overline{\text{RESET}}$ Input Timing



Serial Interface, 2/3-Wire, I/O Mode; Internal $\overline{SCK}$ Output

Refer to figure 23

μPD7500x and 7500x(A): T_A = −40 to +85°C, V_{DD} = 2.7 to 6.0 V

μPD75P008: T_A = −10 to +70°C, V_{DD} = 4.5 to 5.5 V

Parameter	Symbol	Min	Typ	Max	Unit	Conditions
$\overline{SCK}$ cycle time	t_{KCY1}	1600			ns	(Note 1)
		3800			ns	V_{DD} = 2.7 to 6.0 V (Note 2)
$\overline{SCK}$ low- and high-level width	t_{KL1}, t_{KH1}	$0.5t_{KCY}$ − 50			ns	(Note 1)
		$0.5t_{KCY}$ − 150			ns	V_{DD} = 2.7 to 6.0 V (Note 2)
SI setup time to $\overline{SCK}$ ↑	t_{SIK1}	150			ns	(Note 3)
SI hold time to $\overline{SCK}$ ↑	t_{KSI1}	400			ns	(Note 3)
$\overline{SCK}$ ↓ to SO output delay time (Note 4)	t_{KSO1}	0		250	ns	(Note 1)
		0		1000	ns	V_{DD} = 2.7 to 6.0 V (Note 2)

Serial Interface, 2/3-Wire, I/O Mode; External $\overline{SCK}$ Input

Refer to figure 23

μPD7500x and 7500x(A): T_A = −40 to +85°C, V_{DD} = 2.7 to 6.0 V

μPD75P008: T_A = −10 to +70°C, V_{DD} = 4.5 to 5.5 V

Parameter	Symbol	Min	Typ	Max	Unit	Conditions
$\overline{SCK}$ cycle time	t_{KCY2}	800			ns	(Note 1)
		3200			ns	V_{DD} = 2.7 to 6.0 V (Note 2)
$\overline{SCK}$ low- and high-level width	t_{KL2}, t_{KH2}	400			ns	(Note 1)
		1600			ns	V_{DD} = 2.7 to 6.0 V (Note 2)
SI setup time to $\overline{SCK}$ ↑	t_{SIK2}	100			ns	(Note 3)
SI hold time to $\overline{SCK}$ ↑	t_{KSI2}	400			ns	(Note 3)
$\overline{SCK}$ ↓ to SO output delay time (Note 4)	t_{KSO2}	0		300	ns	(Note 1)
		0		1000	ns	V_{DD} = 2.7 to 6.0 V (Note 2)

Notes:

(1) V_{DD} = 4.5 to 6.0 V for 7500x and 7500x(A) and V_{DD} = 4.5 to 5.5 V for 75P008.

(2) For 7500x and 7500x(A) only.

(3) V_{DD} = 2.7 to 6.0 V for 7500x and 7500x(A); V_{DD} = 4.5 to 5.5 V for 75P008.

(4) R_L = 1 kΩ and C_L = 100 pF are load resistance and load capacitance for the SO line.

Serial Interface, SBI Mode; Internal $\overline{SCK}$ Output (Master)

Refer to figure 23

μPD7500x: T_A = −40 to +85°C, V_{DD} = 2.7 to 6.0 V

μPD75P008: T_A = −10 to +70°C, V_{DD} = 4.5 to 5.5 V

Parameter	Symbol	Min	Typ	Max	Unit	Conditions
$\overline{SCK}$ cycle time	t_{KCY3}	1600			ns	(Note 1)
		3800			ns	V_{DD} = 2.7 to 6.0 V (Note 2)
$\overline{SCK}$ low- and high-level width	t_{KL3}, t_{KH3}	$0.5t_{KCY3}$ − 50			ns	(Note 1)
		$0.5t_{KCY3}$ − 150			ns	V_{DD} = 2.7 to 6.0 V (Note 2)
SB0, SB1 setup time to $\overline{SCK}$ ↑	t_{SIK3}	150			ns	(Note 3)
SB0, SB1 hold time to $\overline{SCK}$ ↑	t_{KSI3}	$0.5t_{KCY3}$			ns	(Note 3)
$\overline{SCK}$ ↓ to SB0, SB1 output delay time (Note 4)	t_{KSO3}	0		250	ns	(Note 1)
		0		1000	ns	V_{DD} = 2.7 to 6.0 V (Note 2)
$\overline{SCK}$ ↑ to SB0, SB1 ↓	t_{KSB}	t_{KCY3}			ns	(Note 3)
SB0, SB1 ↓ to $\overline{SCK}$ ↓	t_{SBK}	t_{KCY3}			ns	(Note 3)
SB0, SB1 low-level width	t_{SBL}	t_{KCY3}			ns	(Note 3)
SB0, SB1 high-level width	t_{SBH}	t_{KCY3}			ns	(Note 3)

Serial Interface, SBI Mode; External $\overline{SCK}$ Input (Slave)

Refer to figure 23

μPD7500x and 7500x(A): T_A = −40 to +85°C, V_{DD} = 2.7 to 6.0 V

μPD75P008: T_A = −10 to +70°C, V_{DD} = 4.5 to 5.5 V

Parameter	Symbol	Min	Typ	Max	Unit	Conditions
$\overline{SCK}$ cycle time	t_{KCY4}	800			ns	(Note 1)
		3200			ns	V_{DD} = 2.7 to 6.0 V (Note 2)
$\overline{SCK}$ low- and high-level width	t_{KL4}, t_{KH4}	400			ns	(Note 1)
		1600			ns	V_{DD} = 2.7 to 6.0 V (Note 2)
SB0, SB1 setup time to $\overline{SCK}$ ↑	t_{SIK4}	100			ns	(Note 3)
SB0, SB1 hold time to $\overline{SCK}$ ↑	t_{KSI4}	$0.5t_{KCY4}$			ns	(Note 3)
$\overline{SCK}$ ↓ to SB0, SB1 output delay time (Note 4)	t_{KSO4}	0		300	ns	(Note 1)
		0		1000	ns	V_{DD} = 2.7 to 6.0 V (Note 2)
$\overline{SCK}$ ↑ to SB0, SB1 ↓	t_{KSB}	t_{KCY4}			ns	(Note 3)
SB0, SB1 ↓ to $\overline{SCK}$ ↓	t_{SBK}	t_{KCY4}			ns	(Note 3)
SB0, SB1 low-level width	t_{SBL}	t_{KCY4}			ns	(Note 3)
SB0, SB1 high-level width	t_{SBH}	t_{KCY4}			ns	(Note 3)

Notes:

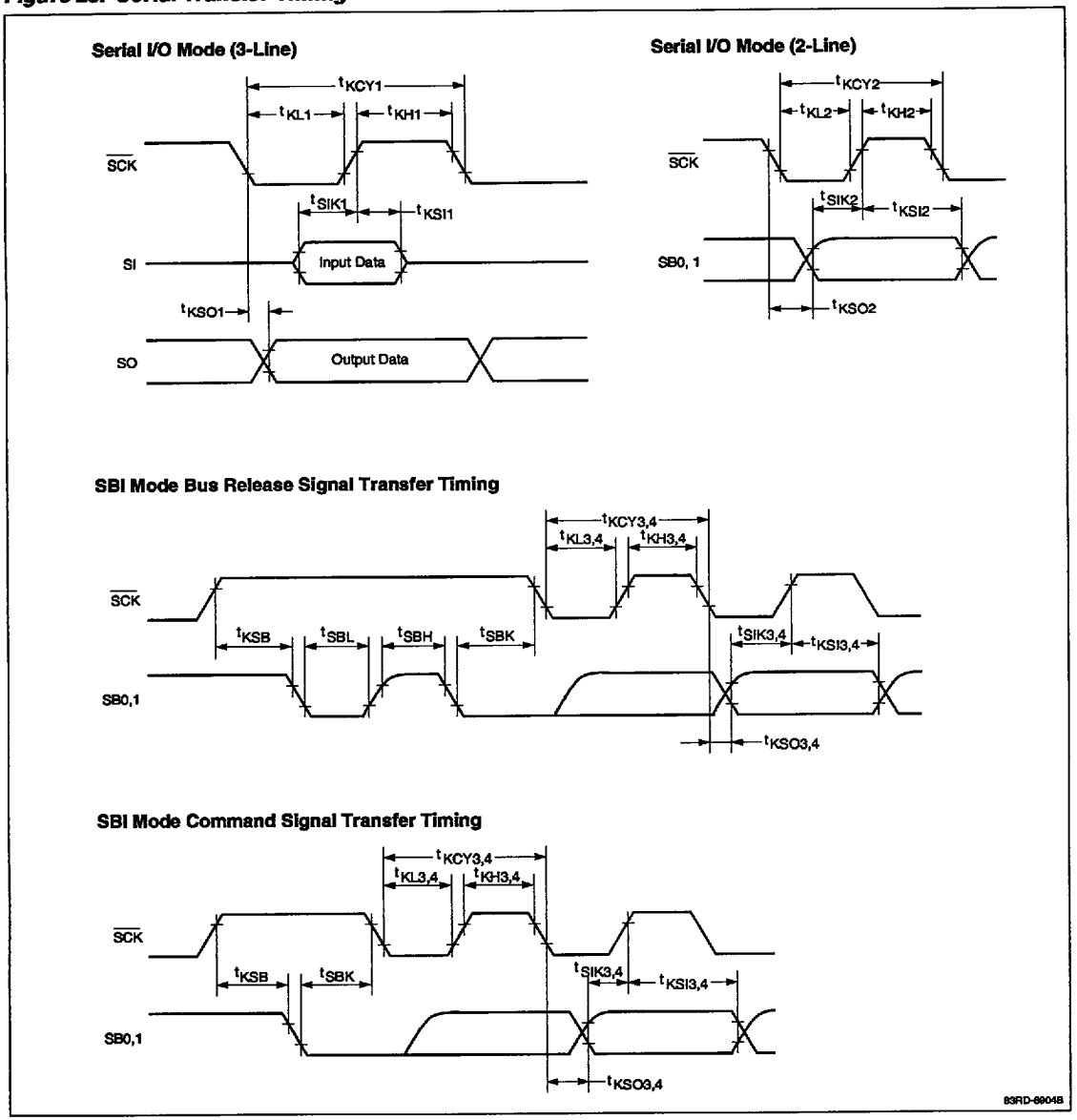
(1) V_{DD} = 4.5 to 6.0 V for 7500x and 7500x(A) and V_{DD} = 4.5 to 5.5 V for 75P008.

(2) For 7500x and 7500x(A) only.

(3) V_{DD} = 2.7 to 6.0 V for 7500x and 7500x(A); V_{DD} = 4.5 to 5.5 V for 75P008.

(4) R_L = 1 kΩ, C_L = 100 pF, R_L is the resistance of the SB0 or SB1 output line load. C_L is the capacitance of the SB0 or SB1 output load line.

Figure 23. Serial Transfer Timing



Data Memory STOP Mode Low Voltage Data Retention Characteristics

Refer to figure 24

μPD7500x and 7500x(A): T_A = −40 to +85°C

μPD75P008: T_A = −10 to +70°C

Parameter	Symbol	Min	Typ	Max	Unit	Conditions
Data retention voltage	V_{DDDR}	2.0			V	(Note 1)
Data retention current (Note 2)	I_{DDDR}		0.1	10	μA	V_{DDDR} = 2.0 V
Release signal set time	t_{SREL}	0			μs	
Oscillation stabilization time (Note 3)	t_{WAIT}		(Notes 4, 5)		s	Release by $\overline{\text{RESET}}$ input
			(Note 4)		ms	Release by interrupt request

Notes:

(1) Max = 6.0 V for 7500x and 7500x(A) and 5.5 V for 75P008.

(2) Pullup resistor current is not included in this table.

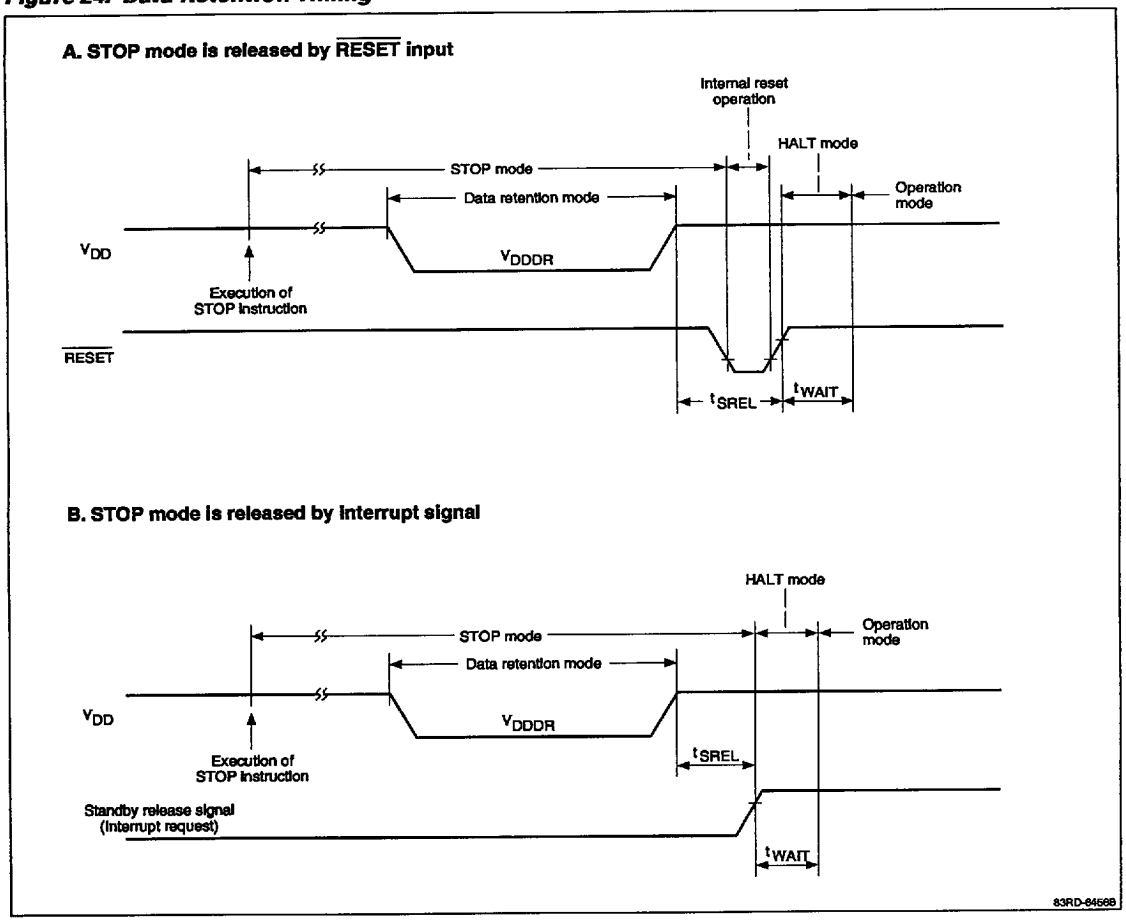
(3) Oscillation stabilization WAIT time is the time during which the CPU is stopped and the crystal is stabilizing. The time is required to prevent unstable operation while the oscillator is started. The interval timer can be used to delay the CPU from executing instructions by using the basic interval timer mode register (BTM) according to the following table:

BTM3	BTM2	BTM1	BTM0	WAIT time (f_x = 4.19 MHz)
—	0	0	0	$2^{20}/f_x$ (approx 250 ms)
—	0	1	1	$2^{17}/f_x$ (approx 31.3 ms)
—	1	0	1	$2^{15}/f_x$ (approx 7.82 ms)
—	1	1	1	$2^{13}/f_x$ (approx 1.95 ms)

(4) Consult the manufacturer's resonator or crystal specifications for this value.

(5) The interval timer will cause a delay of $2^{17}/f_x$ after a reset.

Figure 24. Data Retention Timing



PROM PROGRAMMING

The PROM in the μPD75008 family is one-time programmable (OTP). In the μPD part numbers below, CU and GB denote the package type. Please refer to the Packaging and Soldering Information table and the package drawings for specifics on the packages since there are variations among the types.

μPD	PROM	Bytes	Package
75P008CU	OTP	8064	SDIP
75P008GB-3B4	OTP	8064	QFP

The PROM is programmed using the pins listed in table 7. Note that it is not necessary to enter an address, since the address is updated by pulsing the clock pins. During programming, addresses are incremented by applying clock pulses to the X1 and X2 input pins. When +6 V is applied to V_{DD} and +12.5 V to V_{PP}, the PROM is placed in the write/verify mode. Pins MD0-MD3 select the applicable operation as shown in table 8.

Table 7. PROM Write/Verify Pin Functions

Pin Name	Function
X1, X2	Pulsed to increment address during PROM write/verify operation. The inverse of X1 is applied to X2. Note that these pins are also pulsed during a read.
MD0-MD3	Operation mode selection pins.
$P4_0$-$P4_3$ (four low-order bits) $P5_0$-$P5_3$ (four high-order bits)	8-bit data input/output pins for write/verify
V_{DD}	Supply voltage. Normally 5 volts; 6 volts applied during write/verify
V_{PP}	Normally 5 volts; +12.5 volts is applied during write/verify

PROM Write/Verify Procedure

PROMs can be written at high speed using the following procedure. See figure 25 for the timing.

(1) Connect unused pins to V_{SS} through resistors. Set the X1 pin low.

(2) Supply 5 volts to the V_{DD} and V_{PP} pins.

(3) Wait 10 μs.

(4) Select program memory address clear mode.

(5) Supply 6 volts to V_{DD} and 12.5 volts to V_{PP}.

(6) Select program inhibit mode.

(7) Write data in the 1 ms write mode.

(8) Select the program inhibit mode.

(9) Select the verify mode. If the data is correct, proceed to step 10. If not, repeat steps 7, 8, and 9 up to a maximum of 20 times. If data is still incorrect, terminate programming and declare the device defective.

(10) Perform one additional write with an MD0 pulse width (in ms) equal to the number of writes performed in step 7. For example, MD0 = 10 ms if the location was written to 10 times in step 7.

(11) Select the *program inhibit* mode.

(12) Apply four pulses to the X1 pin to increment the program memory address by one.

(13) Repeat steps 7-12 until the end address is reached.

(14) Select program memory address clear mode.

(15) Return the V_{DD} and V_{PP} pins back to +5 volts.

(16) Turn off the power.

Table 8. Mode Selection

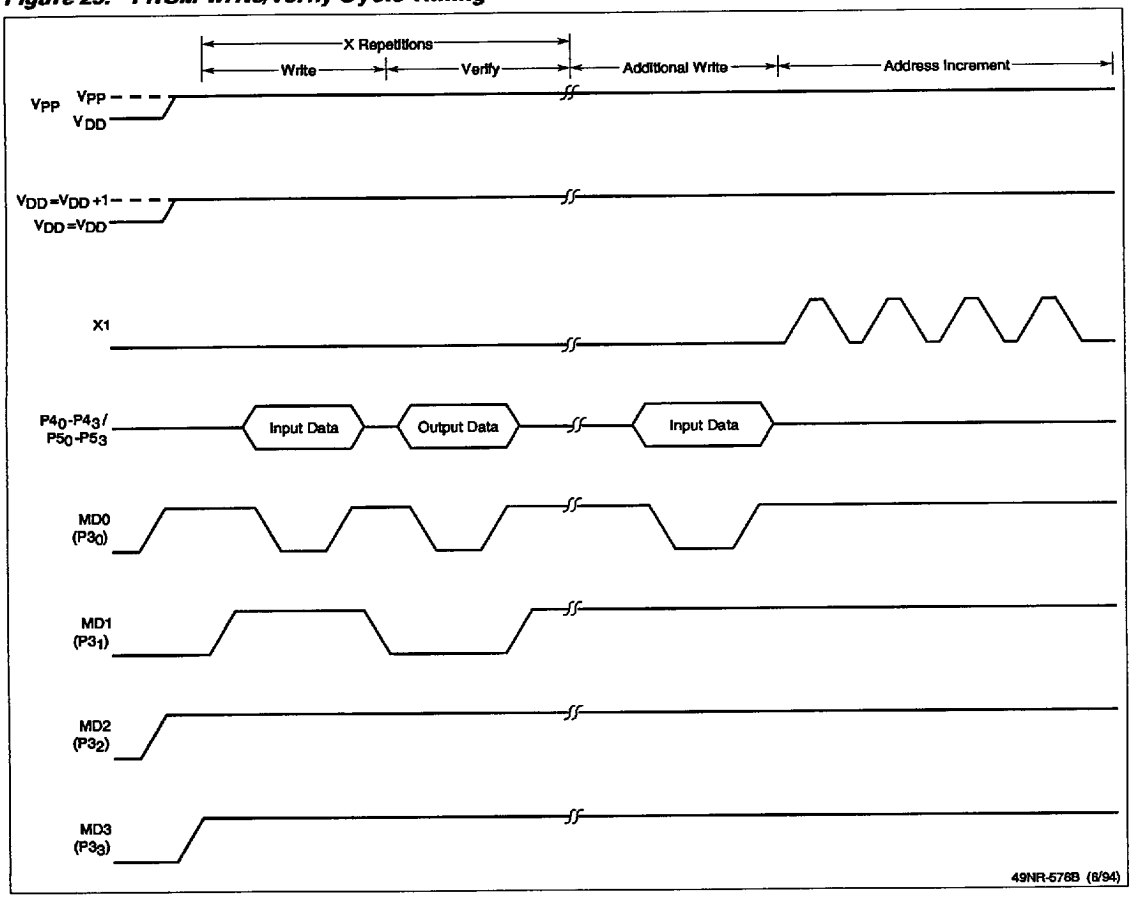
V_{PP} 12.5 V V_{DD} = +6.0 V

Operation Mode Specification				
MD0	MD1	MD2	MD3	Operation Mode
1	0	1	0	Program memory address clear
0	1	1	1	Write mode
0	0	1	1	Verify mode
1	X	1	1	Program inhibit

Note:

(1) X = Don't care.

Figure 25. PROM Write/Verify Cycle Timing



PROM Read Procedure

The PROM contents can be read by using the following procedure. Figure 26 is the timing diagram for steps 2-9.

(1) Connect unused pins to V_{SS} through resistors. Set the X1 pin low.

(2) Supply +5 volts to V_{DD} and V_{PP} pins.

(3) Wait 10 μs.

(4) Select program memory address clear mode.

(5) Supply +6 volts to V_{DD} pin and +12.5 volts to V_{PP} pin.

(6) Select program inhibit mode.

(7) Select verify mode. Apply four pulses to the X1 pin. The data in address 0 will be output. Every additional four clock pulses will output the data stored in the next address.

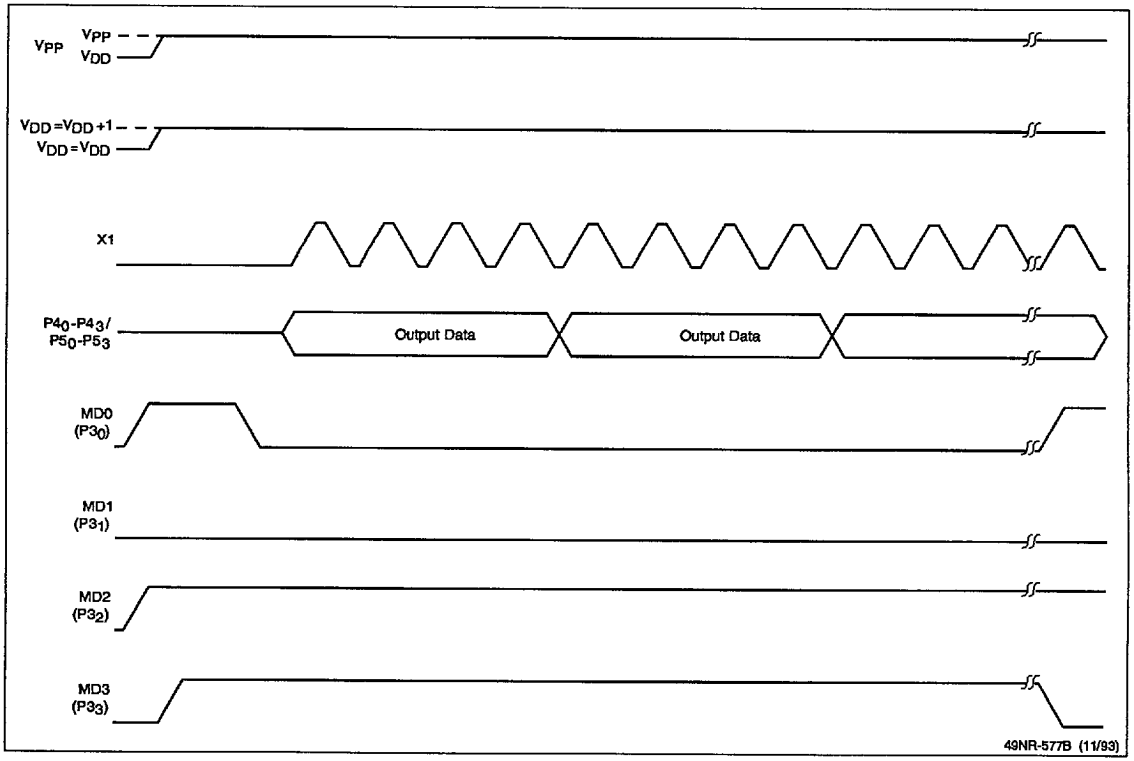
(8) Select program inhibit mode.

(9) Select program memory address clear mode.

(10) Return V_{DD} and V_{PP} pins to +5 volts.

(11) Turn off power.

Figure 26. PROM Read Cycle Timing



DC Programming Characteristics (75P008 only)

T_A = 25 ±5°C; V_{DD} = 6.0 ±0.25 V; V_{PP} = 12.5 ±0.3 V; V_{SS} = 0 V (Notes 1, 2)

Parameter	Symbol	Min	Typ	Max	Unit	Conditions
High-level input voltage	V_{IH1}	0.7 V_{DD}		V_{DD}	V	All except X1, X2
	V_{IH2}	V_{DD} – 0.5		V_{DD}	V	X1, X2
Low-level input voltage	V_{IL1}	0		0.3 V_{DD}	V	All except X1, X2
	V_{IL2}	0		0.4	V	X1, X2
Input leakage current	I_{LI}			10	μA	V_{IN} = V_{IL} or V_{IH}
High-level output voltage	V_{OH}	V_{DD} – 1.0			V	I_{OH} = –1 mA
Low-level output voltage	V_{OL}			0.4	V	I_{OL} = 1.6 mA
V_{DD} supply current	I_{DD}			30	mA	
V_{PP} supply current	I_{PP}			30	mA	MD0 = V_{IL}; MD1 = V_{IH}

Notes:

(1) V_{PP} must not exceed +13.5 V, including overshoot.

(2) V_{DD} must be applied before V_{PP} and is turned off after V_{PP} is removed.

AC Programming Characteristics (75P008 only)

Refer to figures 27 and 28

T_A = 25 ± 5°C; V_{DD} = 6.0 ± 0.25 V; V_{PP} = 12.5 ± 0.3 V; V_{SS} = 0 V

Parameter	Symbol	(Note 1)	Min	Typ	Max	Unit	Conditions
Address setup time to MD0 ↓ (Note 2)	t_{AS}	t_{AS}	2			μs	
MD1 setup time to MD0 ↓	t_{M1S}	t_{OES}	2			μs	
Data setup time to MD0 ↓	t_{DS}	t_{DS}	2			μs	
Address hold time from MD0 ↑ (Note 2)	t_{AH}	t_{AH}	2			μs	
Data hold time from MD0 ↑	t_{DH}	t_{DH}	2			μs	
Data output float delay time from MD0 ↑	t_{DF}	t_{DF}	0		130	ns	
V_{PP} setup time to MD3 ↑	t_{VPS}	t_{VPS}	2			μs	
V_{DD} setup time to MD3 ↑	t_{VDS}	t_{VCS}	2			μs	
Initialized program pulse width	t_{PW}	t_{PW}	0.95	1.0	1.05	ms	
Additional program pulse width	t_{OPW}	t_{OPW}	0.95		21	ms	
MD0 setup time to MD1 ↑	t_{M0S}	t_{CES}	2			μs	
Data output delay time from MD0 ↓	t_{DV}	t_{DV}			1	μs	MD0 = MD1 = V_{IL}
MD1 hold time to MD0 ↑	t_{M1H}	t_{OEH}	2			μs	t_{M1H} + t_{M1R} ≥ 50 μs
MD1 recovery time from MD0 ↓	t_{M1R}	t_{OR}	2			μs	t_{M1H} + t_{M1R} ≥ 50 μs
Program counter reset	t_{PCR}		10			μs	
X1 input low- and high-level width	t_{XH}, t_{XL}		0.125			μs	
X1 input frequency	f_X				4.19	MHz	
Initial mode set time	t_I		2			μs	
MD3 setup time to MD1 ↑	t_{M3S}		2			μs	
MD3 hold time from MD1 ↓	t_{M3H}		2			μs	

AC Programming Characteristics (75P008 only) (cont)

Parameter	Symbol	(Note 1)	Min	Typ	Max	Unit	Conditions
MD3 setup time to MD0 ↓	t_{M3SR}		2			μs	During program read cycle
Data delay time from address (Note 2)	t_{DAD}	t_{ACC}			2	μs	
Data output hold time from address (Note 2)	t_{HAD}	t_{OH}	0		130	ns	
MD3 output hold time from MD0 ↑	t_{M3HR}		2			μs	
Data output float delay time from MD3 ↓	t_{DFR}				2	μs	

Notes:

(1) These symbols correspond to those of the μPD27C256 EPROM.

(2) The internal address signal is incremented by the rising edge of the fourth X1 pulse; it is not connected to an external pin.

Figure 27. Program Memory Write/Verify Timing (μPD75P008)

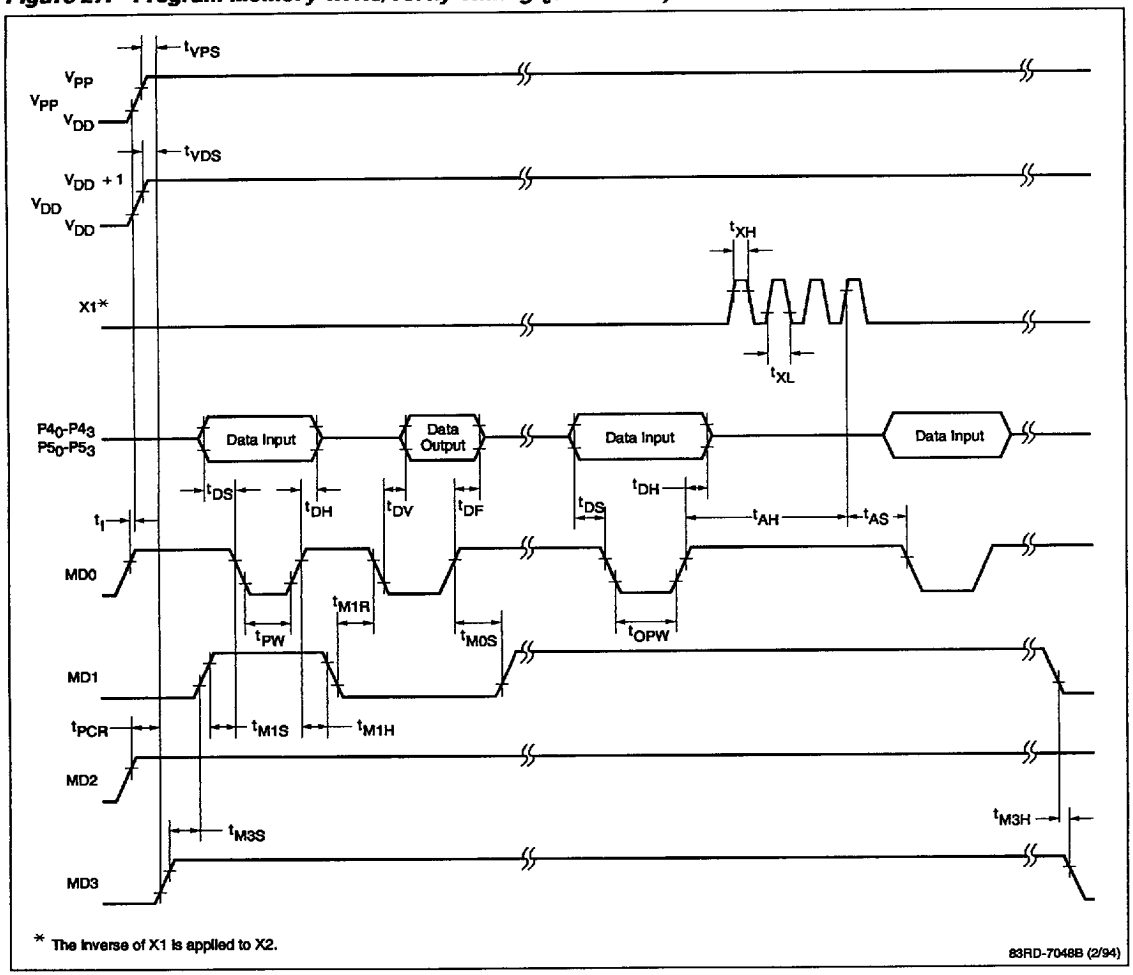
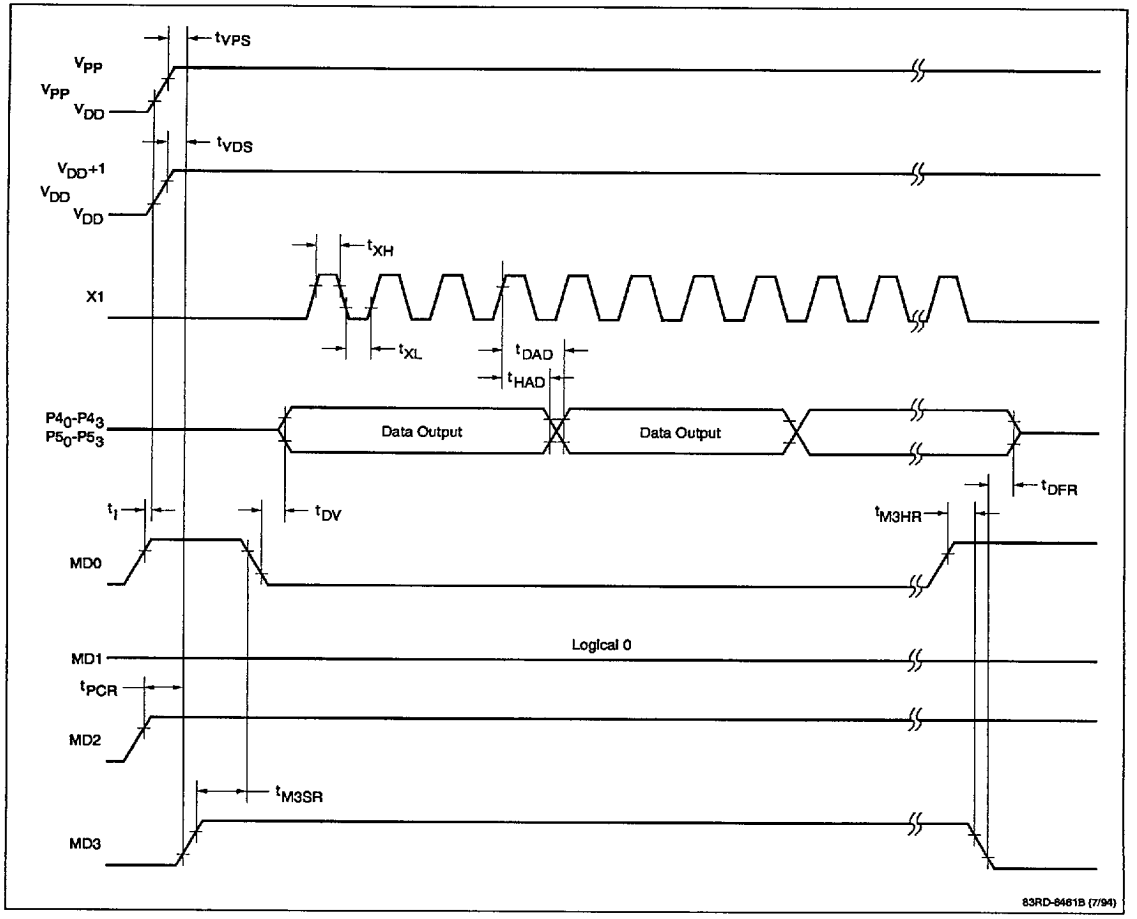


Figure 28. Program Memory Read Timing (μPD75P008)



SOLDERING

Packaging and Soldering Information

Part Number	Package	Package Drawing	Recommended Soldering Code
μPD75004CU-xxx μPD75004CU(A)-xxx μPD75006CU-xxx μPD75006CU(A)-xxx μPD75008CU-xxx μPD75008CU(A)-xxx	42-pin plastic shrink DIP	P42C-70-600A	WS60-00-1
μPD75004GB-xxx-3B4 μPD75004GB(A)-xxx-3B4 μPD75006GB-xxx-3B4 μPD75006GB(A)-xxx-3B4 μPD75008GB-xxx-3B4 μPD75008GB(A)-xxx-3B4	44-pin plastic QFP	P44GB-80-3B4-2	IR30-107-1, VP15-107-1, WS60-00-1
μPD75P008CU	42-pin plastic shrink DIP	P42C-70-600A	WS60-00-1
μPD75P008GB-3B4	44-pin plastic QFP	P44GB-80-3B4-2	IR30-162-1, VP15-162-1, WS60-162-1

Soldering Conditions

Method (Note 1)	Code (Note 2)	Soldering Conditions	Exposure Limit (Note 3)
Infrared reflow	IR30-107-1	Package peak temp: 230°C Time: 30 sec max (210°C min)	Max no. of days: 7 (thereafter, 10 hours baking at 125°C is required)
	IR30-162-1		Max no. of days: 2 (thereafter, 16 hours baking at 125°C is required)
Vapor phase	VP15-107-1	Package peak temp: 215°C Time: 40 sec max (200°C min)	Max no. of days: 7 (thereafter, 10 hours baking at 125°C is required)
	VP15-162-1		Max no. of days: 2 (thereafter, 16 hours baking at 125°C is required)
Wave soldering (Note 4)	WS60-00-1	Solder bath temp: 260°C max Time: 10 sec max Preheating temp: 120°C max (package surface temp)	No limit
	WS60-162-1		Max no. of days: 2 (thereafter, 16 hours baking at 125°C is required)
Pin partial heating		Pin partial temp: 260°C max Time: 10 sec max (per device side)	For SDIP package only
Pin partial heating		Pin partial temp: 300°C max Time: 3 sec max (per device side)	For QFP package only

Notes:

(1) Do not use different soldering methods together. However, on all devices the pin partial heating soldering method can be used alone or in combination with other soldering methods.

(2) The maximum number of soldering operations is one or two as indicated by the last digit of the soldering code: -1 or -2.

(3) Maximum no. of days refers to the number of days after unpacking the dry pack. Storage conditions are 25°C and 65% RH max.

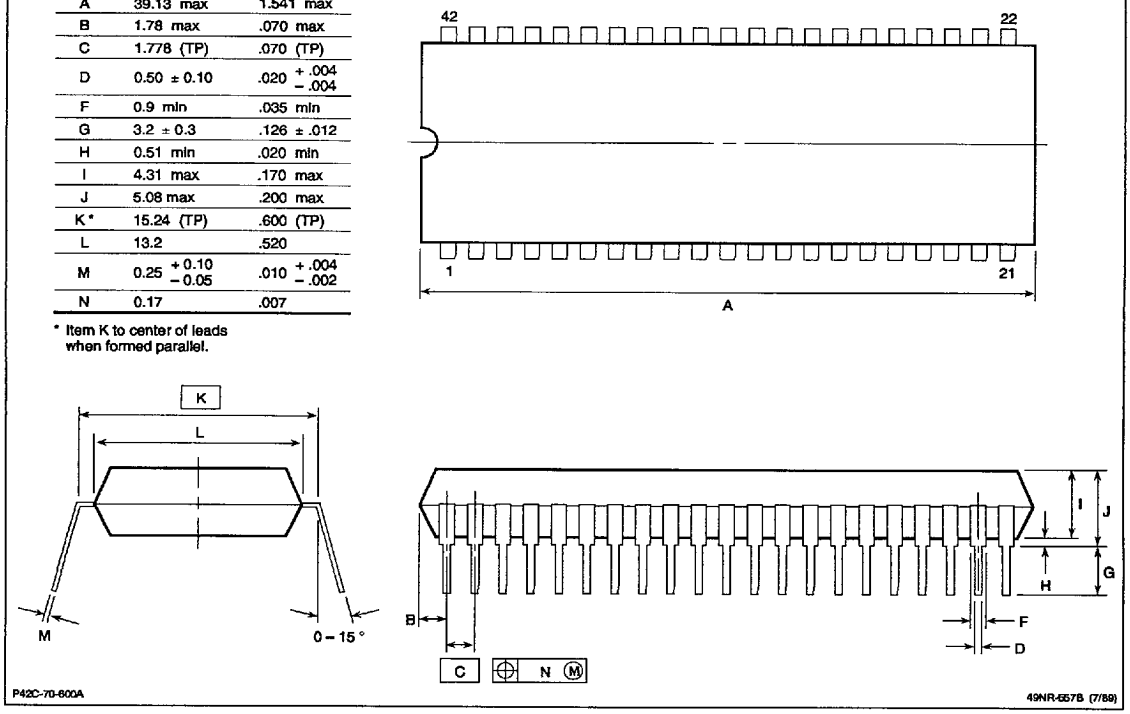
(4) For through hole devices, subject only the leads to the solder bath. The package body should not be immersed into the solder bath.

PACKAGE DRAWINGS

42-Pin Plastic Shrink DIP (P42C-70-600A)

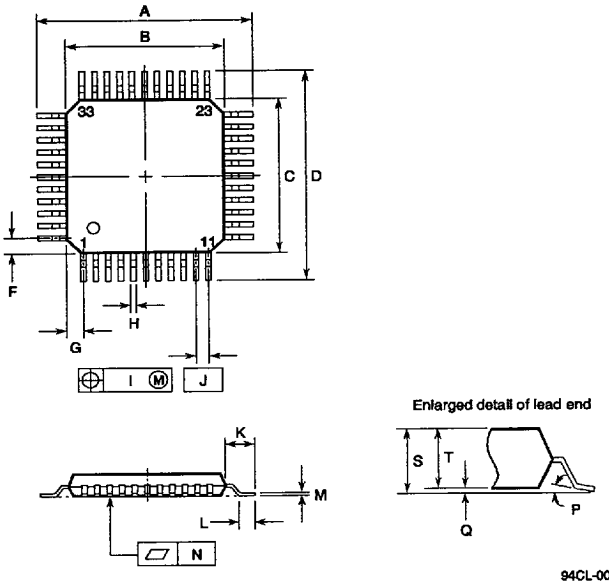
Item	Millimeters	Inches
A	39.13 max	1.541 max
B	1.78 max	.070 max
C	1.778 (TP)	.070 (TP)
D	0.50 ± 0.10	.020 $^{+.004}_{-.004}$
F	0.9 min	.035 min
G	3.2 ± 0.3	.126 ± .012
H	0.51 min	.020 min
I	4.31 max	.170 max
J	5.08 max	.200 max
K*	15.24 (TP)	.600 (TP)
L	13.2	.520
M	0.25 $^{+0.10}_{-0.05}$	.010 $^{+.004}_{-.002}$
N	0.17	.007

* Item K to center of leads when formed parallel.



44-Pin Plastic QFP (P44GB-80-3B4-2)

Item	Millimeters	Inches
A	13.6 ± 0.4	.535 $^{+.017}_{-.016}$
B	10.0 ± 0.2	.394 $^{+.008}_{-.009}$
C	10.0 ± 0.2	.394 $^{+.008}_{-.009}$
D	13.6 ± 0.4	.535 $^{+.017}_{-.016}$
F	1.0	.039
G	1.0	.039
H	0.35 $^{+0.10}_{-0.10}$	.014 $^{+.008}_{-.005}$
I	0.15	.006
J	0.8 (TP)	.031 (TP)
K	1.8 ± 0.2	.071 $^{+.008}_{-.009}$
L	0.8 ± 0.2	.031 $^{+.008}_{-.008}$
M	0.15 $^{+0.10}_{-0.05}$	.006 $^{+.004}_{-.003}$
N	0.12	.005
P	5° ± 5°	.000 $^{+5°}_{-5°}$
Q	0.1 ± 0.1	.004 ± .004
S	3.0 max	.118 max
T	2.7	.106



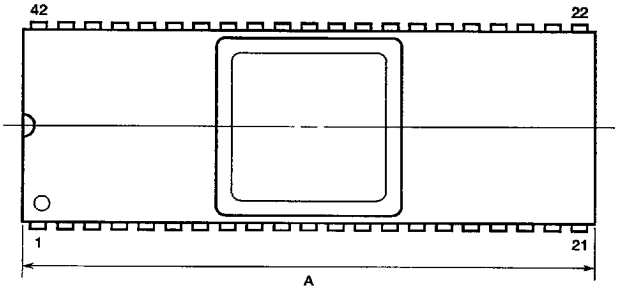
P44-GB-80-3B4-2

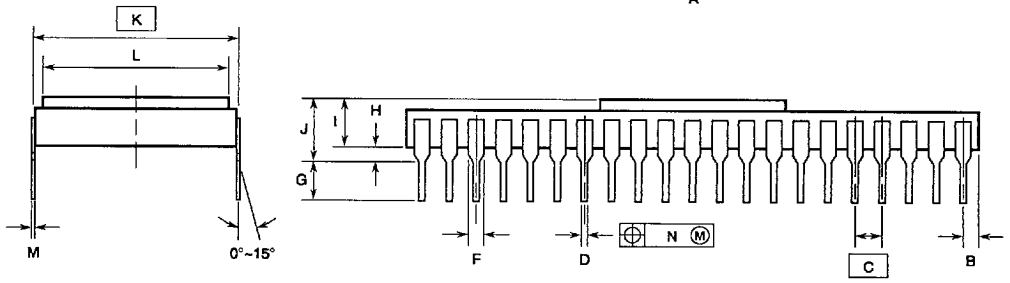
94CL-0097B (8/94)

42-Pin Ceramic Shrink DIP for Engineering Samples

Item	Millimeters	Inches
A	39.12 max	1.540 max
B	1.78 max	.070 max
C	1.778	.070
D	0.46 ± 0.05	.018 ± .002
F	0.8 min	.031 min
G	3.5 ± 0.3	.138 ± .012
H	0.91 min	.036 min
I	3.2	.126
J	5.08 max	.200 max
K*	15.24 (TP)	.600 (TP)
L	14.93	.588
M	0.25 ± 0.05	.010 $^{+.002}_{-.003}$
N	0.18	.007

* Item K to center of leads when formed parallel.





P42D-70-600B

94CL-0096B (7/94)

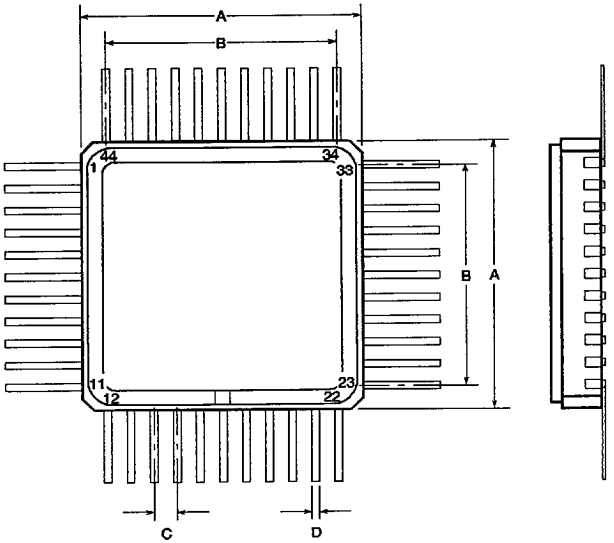
44-Pin Ceramic QFP for Engineering Samples

Item	Millimeters	Inches
A	11.43	0.45
B	8.0	.315
C	0.8	.031
D	0.32	.012
E	0.15	.006
F	2.25	.089

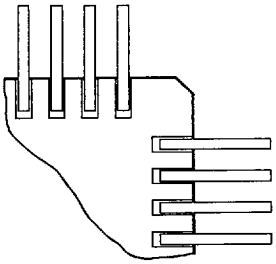
Notes:

(1) Note that the metal cover is connected to pin 17 (V_{SS}).

(2) The length of the leads is not specified since the cutting of the lead tips is not controlled during the manufacturing process.



Enlarged detail of bottom



83RC-9903B (9/94)