GEC PLESSEY
SEMICONDUCTORS

PRELIMINARY INFORMATION

DS4468-2.1

P2800

2K x 64BIT MULTI-PORT CONTENT ADDRESSABLE MEMORY

The P2800 2K x 64bit Multi-port Content Addressable Memory (CAM) is designed for address filtering, routing and translation applications in Ethernet, Token Ring, SMDS and ATM systems where high speed operation is necessary. The P2800 will operate up to and beyond the OC-12 data rate of 622MBits s^{-1}. The architecture of the P2800 makes high-speed operation possible through pipelining and interleaving.

FEATURES

- 2K x 64bit Content Addressable Memory
- 50ns Compare cycle time
- 20ns Register Read/Write cycle time
- Configurable into areas of CAM and RAM on 16-bit boundaries
- One Parallel Port with full 64bit-wide I/O interface configurable for 16-, 32- or 64-bit operation
- Two Serial Ports configurable for 1-, 4- or 8-bit operation
- Synchronization between Parallel and Serial Ports
- Direct hardware control through Control Bus
- Two 64-bit Comparand Registers
- Four 64-bit Mask Registers
- Two 32-bit Match Address Registers
- Two 64-bit Match Data Registers
- One 48-bit Configuration Register
- One Next Free Address Register
- Priority Encoder to resolve multiple matches
- Data validity control per location
- Support for list entry aging
- Simple Vertical cascading using daisy chain scheme
- Support for 802.3 to/from 802.5 mapping on all ports
- High-speed pipelined and interleaved operation
- 5 Volt I/O operation
- CMOS Technology
- Packaged in a 208-pin flatpack

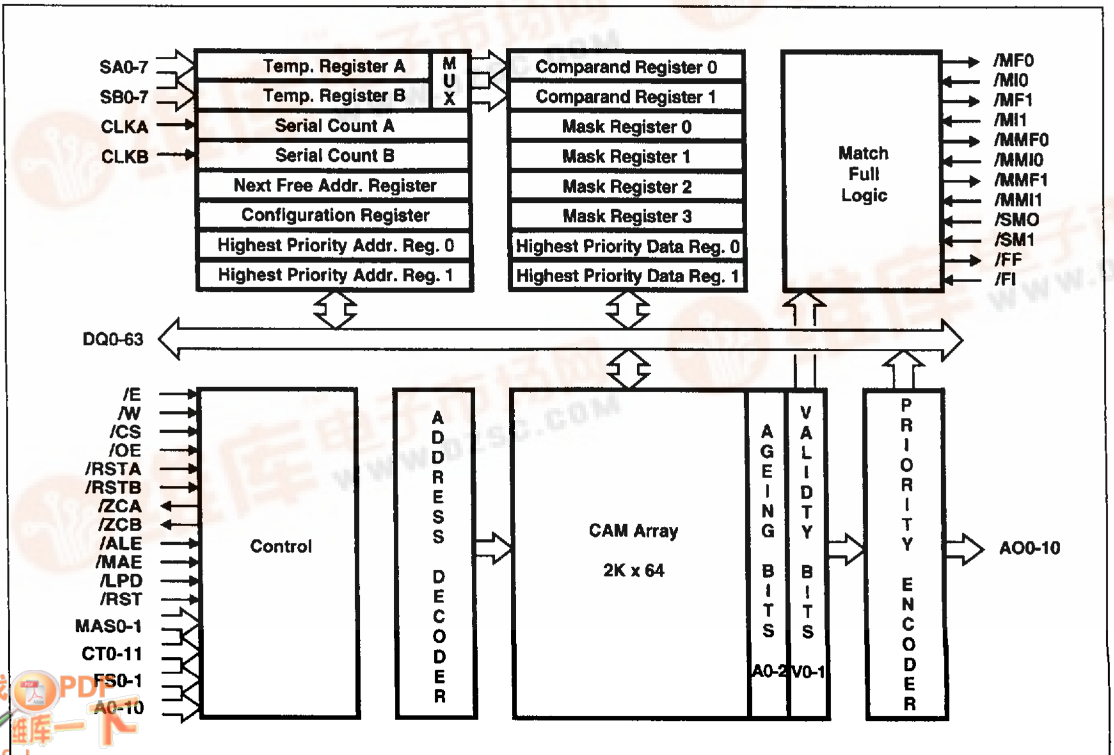


Fig.1 System block diagram

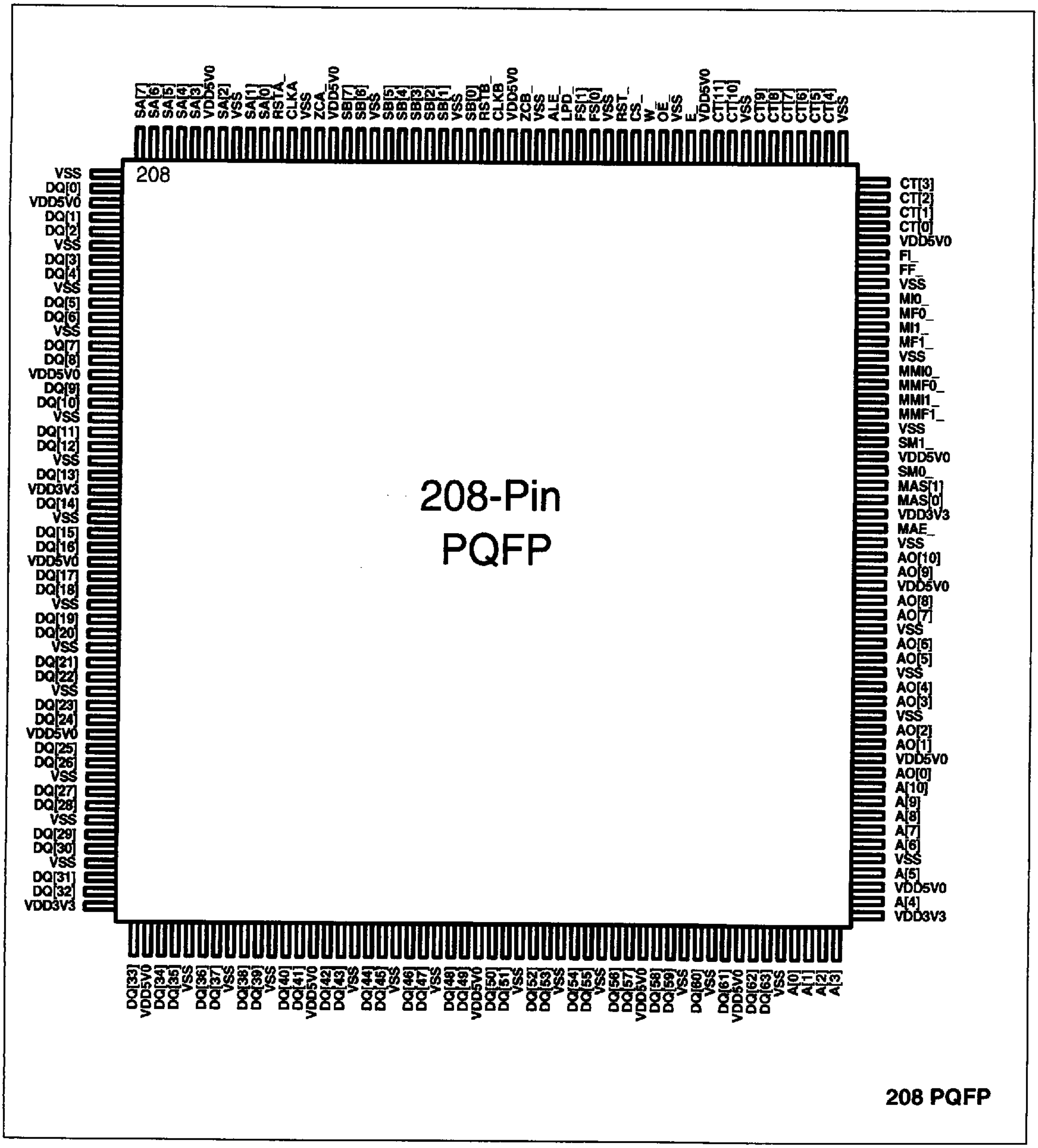


Fig.2 Pin connections - top view

ELECTRICAL CHARACTERISTICS

ABSOLUTE MAXIMUM RATINGS

Supply voltage V_{CC}	–0.5 to 7.0 volts
Supply voltage V_{dd}	–0.5 to 4.6 volts
DC input voltage	–0.5 to V_{CC} +0.5volts
DC output voltage	–0.5 to V_{CC} +0.5volts
DC input current	+/–20mA
DC output current	+/–20mA
Temperature under bias	-40°C to +85°C
Storage temperature	-55°C to +125°C

OPERATING CONDITIONS

Symbol	Characteristic	Value		Units	Conditions
		Min.	Max.		
V_{CC}	Operating voltage (periphery)	4.50	5.50	volts	
V_{dd}	Operating voltage (core)	3.00	3.60	volts	
VIH	Input voltage logic "1"	2.0	VCC+0.5	volts	
VIL	Input voltage logic "0"	–0.50	0.8	volts	
TA	Ambient operating temperature	0	70	°C	still air

ELECTRICAL CHARACTERISTICS

Symbol	Characteristic	Value		Units	Conditions
		Min.	Max.		
I_{CC}	Operating supply current periphery	-	170	mA	tCC1=tCC1(min) assume $^1/_2$ DQ pins toggle
I_{CC}(SB)	Stand-by supply current (periphery)	-	30	mA	/E = HIGH
I_{dd}	Operating supply current core	-	200	mA	tCC1=tCC1(min)
I_{dd}(SB)	Stand-by supply current (core)	-	30	mA	/E = HIGH
VOH	Output voltage logic "1"	2.4	-	volts	IOH = 8mA, V_{CC}=V_{CC}(min)
VOL	Output voltage logic "0"	-	0.4	volts	IOL = 8mA, V_{CC}=V_{CC}(max)
IIZ	Input leakage current	0	±1	µA	V_{in}<=V_{CC} or V_{SS}
IOZ	Output leakage current	0	±1	µA	V_{SS}<= V_{in}<=V_{CC}

CAPACITANCE

Symbol	Characteristic	Value		Units	Conditions
		Min.	Max.		
C_{in}	Input capacitance	-	6.00	pF	f=1MHz, V_{in}=0V
C_{out}	Output capacitance	-	7.00	pF	f=1MHz, V_{in}=0V

AC TEST CONDITIONS

Input signal transactions	0.0 to 3.0 volts
Input signal rise times	<3ns
Input signal fall times	<3ns
Input timing reference	1.5 volts
	0.8 to 2.4 volts

FUNCTIONAL DESCRIPTION

CAM Array

The CAM Array contains 2K locations that are 64 bits wide. Each location also has two validity bits to indicate Empty, Valid, Temporarily Invalid and Random Access. Three further bits are included to hold age information for the contents of a location.

The CAM Array can be configured into an area of CAM and an area of RAM across the width of the array on 16-bit boundaries. The CAM section holds associative data while the RAM section holds associated data. Associated data can be accessed as a function of a match in the associated data.

Parallel Port

The Parallel Port is 64 bits wide and provides full bandwidth access into the CAM Array. For architectures that use microprocessors or state machines with narrower data buses, the Parallel Port can be alternatively configured as 16 bits or 32 bits wide; under these circumstances, data is multiplexed on the lower-order bits of the parallel port.

Data is read from and written to the CAM Array and the Register Set via the Parallel Port.

Serial Ports

The Serial Ports operate independently, and can be configured to receive data 1 bit, 4 bits or 8 bits per clock cycle. Data from each Serial Port is assembled in a temporary register ready for transfer into either of the two Comparand Registers.

The amount of data to be assembled from each Serial Port is loaded into a Serial Port Counter which sets a flag when the preset number clock cycles have been received.

Port Synchronization

The Parallel and Serial Ports are synchronized through a handshaking scheme. When the preset count value has been reached by one of the Serial Ports, the flag is set which indicates to the local processor that a value has been assembled and is ready for use. The local processor now transfers that data to one of the Comparand Registers ready for comparison.

While the Serial Port flag remains set, that Serial Port cannot clock in more data. When the local processor has dealt with the data, it resets the flag and the Serial Port can resume clocking. Therefore, the local processor arbitrates between the asynchronous operation of the Parallel and Serial Ports.

Register Set

The Register Set comprises two Comparand Registers, four Mask Registers, two Match Address Registers, two Match Data Registers, a Configuration Register, and a Next Free Address Register. The Comparand Registers hold the values for comparison. The comparison is masked by a selected Mask Register. Only bits in the Comparand Register that correspond with bits set LOW in the selected Mask Register are compared, other bits are ignored.

Results of comparison are read from the corresponding Match Address Register or Match Data Register. The Match Data Registers provide access to the associated data of the highest-priority matching location. The Next Free Address Register holds the address of the next free location in the device. This information is used for 'associative' write cycles to the next free location. The Full Flag daisy chain ensures that write at next free address cycles work globally. The Configuration Register sets up persistent operating conditions within the device, and is defined as follows:

The configuration register is a 48 bit register

Config. 2:0 - CAM/RAM Division
000 - 64 bits CAM 0 bits RAM
001 - 48 bits CAM 16 bits RAM
010 - 32 bits CAM 32 bits RAM
011 - 16 bits CAM 48 bits RAM
100 - 0 bits CAM 64 bits RAM
101 - Reserved
11X - Reserved

Config. 4:3 - Data Bus Width
00 - 64 bits
01 - 32 bits
10 - 16 bits
11 - Reserved

Config. 8 - Address Latch Enable
0 - Disable address latch
1 - Enable address latch

Config. 7:6 - Port A Serial Bus Width
00 - SA 1 bit wide
01 - SA 4 bits wide
10 - SA 8 bits wide
11 - Reserved
Set to 1 bit wide on reset.

Config. 9:8 - Port B Serial Bus Width
00 - SB 1 bit wide
01 - SB 4 bits wide
10 - SB 8 bits wide
11 - Reserved
Set to 1 bit wide on reset.

Config. 15:10 - SA Count
e.g. Config. 15:10 = 000101 will mean serial port A is clocked 5 times before zero count flag is activated.
Set to 000000 on reset (count 64).

Config. 21:16 - SB Count

Config. 31:22 - Reserved
(set to zero)

Config. 47:32 - Address Tag
These 16 bits are used to indicate a device address in a multi-LANCAM system. Up to 64K devices can be implemented in any system.

Control States

Unlike earlier instruction-driven CAM devices, the P2800 is controlled through the hardware Control Bus, leading to single-cycle operation. This approach provides a substantial increase in operating speed.

Control states are input to the P2800 on the Control Bus. These control states divide into four classifications: Read/Write Register, Read/Write Memory, Conditional Write and Compare. The control states give powerful and flexible control over the device.

Match Logic

Results of comparison are indicated through the Match Flag. There is one Match Flag per Comparand Register. In a vertically cascaded system, each Match Flag is fed from one device into Match Input of the next lower-priority device. This connection forms a match daisy chain, allowing match results to be established on a global basis.

Pipelining and Interleaving

The combination of Comparand Register, Match Address Register, Match Data Register and Match Flag Input and Output forms a comparison channel. There are two such channels in the P2800. The data is loaded into the Comparand Register associated with one comparison channel, and comparison is initiated; while the comparison is taking place, results from an earlier comparison in the other comparison channel can be read from the Match Address or Data Register associated with that channel. Therefore, a constant stream of data and results can flow through the device, to provide uninterrupted high-speed operation.

Vertical Cascading

As well as the Match Flag daisy chain, there are daisy chains for both channels of Multiple Match Flags, and a Full Flag daisy chain. All daisy chains operate independently.

Aging

List entry aging is supported through three extra bits per location. A location can be set to age or not, as data is written to the memory. A fully associative aging algorithm is implemented through the control states.

MEMORY MAPPING

P2800P2800The P2800 can be controlled either from a microprocessor or a state machine. In the case of the microprocessor, the wide Control Bus can be driven by using memory mapping. Twelve bits are needed to implement the control states summarised above. Therefore, an address space of 4K locations must be reserved for controlling the P2800. Read or Write cycles to those locations initiate the control state, with data transactions occurring on the DQ0-63 bus. Included in the control states are mask selection, aging control and validity bit control. Note that Read cycles to the Next Free Address output the address on the DQ bus, and can be read by the processor.

VERTICAL CASCADING

Fig.3 shows a vertically cascaded system of P2800s. Both comparison channels have their own Match Flag and Multiple Match Flag daisy chain. The Match daisy chain prioritizes the individual devices.

Global Match, Multiple Match and Full Flags appear from the lowest priority device in the daisy chain. System Match information is fed back up the daisy chain per channel on the /SM0 and /SM1 lines.

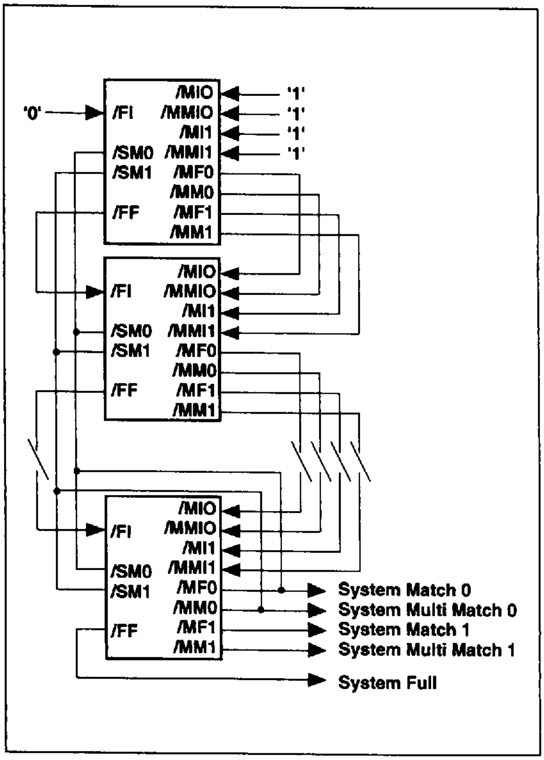


Fig.3 Vertically cascaded P2800 system

PIN DESCRIPTIONS

DQ0-DQ63 (Data Bus, Tri-state, Input/Output, TTL)

The DQ0-DQ63 lines convey data to and from the P2800. When the /E line is HIGH the DQ0-DQ63 lines are held at high impedance. The state of the /W line determines whether the data flow is into or out of the device. The falling edge of /E at the beginning of an Read Cycle causes the data on the DQ0-DQ63 lines to be registered. The source or destination of data on the DQ0-DQ63 lines is determined by the states of the CT0-CT11 lines. The width of the input/output transactions on the DQ0-DQ63 lines is configurable as 16 bits, 32 bits or 64 bits, and is controlled through the Configuration Register. When operating with a bus width of less than 64 bits, the lowest-order bit of a 16- or 32-bit data field is always transmitted via DQ0. The FS0-1 lines determine which field of the internal 64-bit data is accessed by a Read or Write Cycle.

FS0-FS1 (Field Select, Input, TTL)

The FS lines select which field is accessed within the internal 64 data bits during an I/O transaction. The falling edge of /E at the beginning of an Input/Output cycle causes the data on the FS0-FS1 lines to be registered. The mapping from DQ lines to internal data lines is dependent on the configuration of both the Parallel Port and the selected Memory Array organization.

/CS (Chip Select, Input, TTL)

The /CS input is used to select or deselect a particular device within a vertically cascaded system. When the /CS input is LOW, the P2800 is selected and will be active during the cycle; when the /CS line is HIGH, the P2800 will be deselected and will not be active during the cycle. The Match Flag daisy chain is unaffected by the state of the /CS line: when a device is deselected during a Compare Cycle, the Match Daisy chain passes through that device without being conditioned by it. After the Compare Cycle, the deselected device will behave as if it had a mismatch during the Compare Cycle so that old comparison results it may have contained will not upset new comparison results. The state of the /CS line is registered on the falling edge of /E.

/OE (Output Enable, Input, TTL)

The /OE input determines whether the DQ0-DQ63 lines are active during a Read or Write@NFA cycle. When /OE is HIGH, the DQ0-DQ63 lines remain in their high-impedance state. When /OE is LOW, the DQ0-DQ63 lines are active during a Read or Write@NFA cycle. The state of the /OE line is registered on the falling edge of /E.

/W (Write Enable, Input, TTL)

The /W input selects the direction of data transfer on the DQ0-DQ63 lines during a cycle. It is used in conjunction with the CT0-CT11 lines to define the operation performed by the P2800 during a cycle. The falling edge of /E at the beginning of an input cycle causes the /W line to be registered.

AO0-AO10 (Address Output Bus, Tri-state, Output, TTL)

The AO0-AO10 lines carry address information from four sources: Comparison Channel 0 Match Address, Comparison Channel 1 Match Address, Address inputs A0-A10, and the Next Free Address Register. The address source is selected with the MAS0-1 lines, and the bus is enabled by the Address enable line, /MAE. In a vertically cascaded system, only the AO0-AO10 bus of the highest-priority responding device will be active, all other devices will have their AO0-AO10 lines in the high impedance state regardless of the condition of the /MAE input.

MAS0-1 (Address Select, Input, TTL)

The MAS0-1 inputs select the source of the address output on the AO0-AO10 bus. The possible sources of address are Comparison Channel 0 Match Address, Comparison Channel 1 Match Address, Address inputs A0-A11, and the Next Free Address Register. The address source is selected as follows:

MA1/0	Address Source
0 0	Comparison Channel 0 Match Address
0 1	Comparison Channel 1 Match Address
1 0	Address Inputs A0-A11
1 1	Next Free Address Register

/MAE (Match Address Enable, Input, TTL)

The /MAE input controls the impedance of the AO0-AO10 bus. When /MAE is LOW the AO0-AO10 lines are active; when /MAE is HIGH the AO0-AO10 lines are in their high-impedance state. In a vertically cascaded system, only the AO0-AO10 bus of the highest-priority responding device will be active, all other devices will have their AO0-AO10 lines in high impedance regardless of the condition of the /MAE input.

SA0-SA7, SB0-SB7 (Serial Bus A, B, Input, TTL)

The SA0-SA7 lines convey the serial data to Serial Port SA of the P2800. The data is clocked into Temporary Register TEMPA on the rising edge of the CLKA clock. Data is transferred from TEMPA to either Comparand Register under control of the CT0-CT11 lines. The width of the SA bus is set in the Configuration Register to be 1, 4 or 8 bits. The lowest order bit is always conveyed on the SA0 line. The SB bus is identical to the SA bus with respect to TEMPB and CLKB.

CLKA, CLKB (Serial Clock A, B, Input, TTL)

The CLKA input conveys the clock for Serial Port SA0-SA7. Data on SA0-SA7 is clocked in on the rising edge of CLKA, and the Serial Bit Counter A is also incremented on the rising edge. The serial data is shifted into Temporary Register TEMPA. The number of bits, nibbles or bytes to be clocked in is held in the Configuration Register. After the specified number of bits, nibbles or bytes have been received on Serial Port A, the /ZCA output goes LOW. The rising edge of CLKA is used to synchronize the setting and resetting of /ZCA and the resetting of the Serial Bit Counter for Serial Port SA. Similarly, CLKB clocks the SB bus.

/RSTA, /RSTB (Reset Serial Input A/B, Input TTL)

The /RSTA bit resets the Serial Bit Counter A to zero when LOW on the rising edge of CLKA. When Serial Bit Counter A is set to zero, /ZCA goes HIGH. /RSTB resets Serial Bit Counter A to zero.

/ZCA, /ZCB (Zero Count A/B, Output TTL)

/ZCA goes HIGH when Serial Bit Counter A is set to zero. /ZCA goes LOW when the Serial bit count is equal to the count value held in the Configuration Register for Serial Port A; it can also be forced HIGH or LOW by a control state on the CT0-CT11 inputs synchronized by the rising edge of CLKA. Serial Bit Counter A is reset to zero by a LOW condition on the /RSTA input at the time of the rising edge of CLKA. /ZCB indicates zero count on Serial Bit Counter B.

CT0-CT11 (Control Bus, Inputs TTL)

CT0-CT11 are the main control inputs of the P2800. They operate in conjunction with the /W input to determine the state of the DQ bus during an active cycle and the operation performed during that cycle. The CT0-CT11 lines are registered by the falling edge of /E.

/MF0, MF1 (Match Flag 0/1, Output, TTL)

The /MF0 output is the Match Flag for Comparison Channel 0 and indicates whether a valid match has occurred during a Compare Cycle. If there are one or more valid matches in a device, then the /MF0 goes LOW. If the /MI0 line is LOW, then the /MF0 output will go LOW regardless of the match condition in the device. For all other cases the /MF0 output is HIGH. /MF1 is the Match Flag for Comparison Channel 1.

/MI0, /MI1 (Match Input 0, 1, Input, TTL)

The /MI0 input is used in vertically-cascaded systems to prioritize devices for Compare Cycles in Comparison Channel 0. If the /MI0 input is HIGH there is no higher-priority device with a valid match in Comparison Channel 0; the device can then respond to match in its own Memory Array. If the /MI0 input is LOW, then there is a higher-priority device with a valid match in Comparison Channel 0; the device will then not respond to a match in its own Memory Array, although its /MF0 flag will be set LOW indicating a match in Comparison Channel 0 within the CAM system. Similarly, /MI1 prioritizes devices for Comparison Channel 1.

/MMF0, /MMF1 (Multiple-match 0, 1, Output, TTL)

The /MMF0 output is the multiple-match flag for Comparison Channel 0 and indicates whether a multiple match has occurred during a Compare Cycle. If there is more than one valid match within a device, the /MMF0 output goes LOW. The /MMF0 output also goes LOW when there is a single match within the device AND the /MI0 input is LOW. The /MMF0 output is forced LOW if the /MMI0 input is LOW, regardless of the match condition in Comparison Channel 0 within the device. Under all other conditions the /MMF0 output is HIGH. Similarly, /MMF1 is the multiple-match flag for Comparison Channel 1.

/MMI0, /MMI1 (Multiple-match Input 0, 1, Input, TTL)

The /MMI0 input is used in vertically cascaded systems to provide multiple-match information for Comparison Channel 0 throughout the system. If the /MMI0 line is HIGH, there are no multiple matches amongst higher priority devices. If the /MMI0 line is LOW, there are multiple matches amongst higher-priority devices, so the /MMF0 output is forced LOW indicating a multiple match within the CAM system. Similarly, /MMI1 provides the multiple-match information for Comparison Channel 1.

/SM0, /SM1 (System Match 0, 1, Input, TTL)

The /SM0 input is used in a vertically cascaded system to convey the presence or absence of a match in a lower-priority device to higher-priority devices within the system for Comparison Channel 0. The P2800 uses this information for conditional Write Cycles. The signal is fed from the /MF0 output of the lowest-priority device in the system. /SM1 conveys the presence or absence of a match in a lower-priority device for Comparison Channel 1.

/LPD (Lowest Priority Device, Input, TTL)

The /LPD input is used to indicate the lowest priority device in a vertically cascaded system. The /LPD input of the lowest priority device is connected to Ground, the /LPD inputs of all other devices in the system are connected to Vdd. In a single-chip system, the /LPD line must be connected to Ground.

/FF (Full Flag, Output, TTL)

The /FF output is the Full Flag that indicates whether the device is full. If there are one or more empty locations, the /FF output is HIGH; if all locations are full, and the /FI input is LOW, then the /FF goes LOW. In a vertically-cascaded system, the /FF output of a higher-priority device is connected to the /FI input of the next-lower-priority device. If the /FI input is HIGH, the /FF flag will go HIGH regardless of the full condition within the device. The /FF output of the lowest-priority device in a vertically cascaded system represents

/FI (Full Input, Input, TTL)

The /FI input is used in vertically-cascaded systems to establish the Full condition within the CAM system. If the /FI input is HIGH for a particular device, there is at least one empty location in a higher-priority device in the system. If the /FI input is LOW for a particular device, then there is no empty location in the higher-priority devices; the device will then condition its own /FF line HIGH if it has any empty locations, or LOW if it does not. The /FI input and /FF output indicate to an individual device within a vertically cascaded system how to respond to a Write-at-next-free-address Cycle when the empty locations are distributed non-contiguously throughout the system.

/RST (Reset, Input, TTL)

This pin provides a hardware reset of the P2800. At power-up this pin must be pulled LOW for the device to initialize. After the /RST line returns HIGH the device will be in the reset condition. Pulling the /RST LOW has the same result as the control code CT11-CT0 = 200H of 201H.

V_{CC} (Positive Power Supply +5V)

These pins are the main power supply connections to the P2800. Vcc must be held at +5V $\pm$10% relative to the GND pin for correct operation of the device.

V_{dd} (Positive Power Supply +3.3V)

These pins are the auxiliary power supply connections to the P2800. Vdd must be held at +3.3V $\pm$10% relative to the GND pin for correct operation of the device.

GND (Ground)

The common GND pins, which must be held at 0V, system reference potential, for correct operation of the device.

CONTROL STATE SUMMARY

Register Write Cycles

- DQ0-63 to Comparand Register 0,1
- DQ0-63 to Configuration Register
- DQ0-63 to Mask Register 0,1,2,3
- Reset CAM
- Reset Serial Port A,B
- Match Address to Match Data Register 0,1
- Temporary Register to Comparand Register A,B
- Set Aging Counter

Memory Write Cycles

- Comparand Register 0,1 to Address
- Configuration Register to Address
- DQ0-63 to Address
- DQ0-63 to Next Free Address
- Set Validity/Aging at Address
- Mask Register 0,1,2,3 to Address

Conditional Write Cycles

- If Match 0,1 then Comparand 0,1 to Address
- If No Match 0,1 then Comparand 0,1 to Address
- If Match 0,1 then Set Validity at Address
- If Match 0,1 then Set Validity at All Matching Locs
- If Match 0,1 then Set Age at Highest Prio Match
  else Comparand Register 0,1 to Addr
- If Match 0,1 then Set Age at All Matching Locations
  else Comparand Register 0,1 to Addr

Compare Cycles

- Compare Comparand Register 0,1 with CAM Array
- Compare DQ0-63 with CAM Array

Register Read Cycles

- Comparand Register 0,1 to DQ0-63
- Configuration Register to DQ0-63
- Address Latch to DQ63-0
- Mask Register 0,1,2,3 to DQ0-63
- Match Address Register 0,1 to DQ0-63
- Match Data Register 0,1 to DQ0-63
- Next Free Address Register to DQ0-63
- Read Aging Counter

Memory Read Cycles

- Address to Comparand Register 0,1
- Comparand Register 0,1 to Next Free Address
- Address to Configuration Register
- Configuration Register to Next Free Address
- Address to DQ0-63
- Read Validity/Aging at Address
- Address to Mask Register 0,1,2,3
- Mask Register 0,1,2,3 to Next Free Address

Conditional Write Cycles

- If Match 0,1 then Comparand 0,1 to Next Free Addr
- If No Match 0,1 then Cmprnd 0,1 to Next Free Addr
- If Match 0,1 then Comparand 0,1 to Highest Match
- If Match 0,1 then Set Validity at Highest Match
- If Match 0,1 then Set Age at Highest Prio Match
  else Comparand Register 0,1 to Next Free Addr
- If Match 0,1 then Set Age at All Matching Locations
  else Comparand Register 0,1 to Next Free Addr

Compare Cycles

- Compare Aging Bits with CAM Array
- Compare Validity with CAM Array

CONTROL INTERFACE

The control interface of the P2800 comprises the /E Strobe line, the /W Write Enable line, the /CS Chip Select line and CT0-CT11 Control inputs. The functions selected by the CT0-CT11 lines divide into the following categories: Read/Write Register, Read/Write Memory, Conditional Write, and Compare. The Write and Compare operations can be masked by any one of the four Mask registers.

The CT0-CT11 inputs are grouped according to the following scheme:

FUNCTION						QUALIFYING BITS					
CT11	CT10	CT9	CT8	CT7	CT6	CT5	CT4	CT3	CT2	CT1	CT0

CT11 - CT6 Define the function to be executed by the control state.

CT5 - CT0 Provide qualification to the function and control the following aspects of the control state:

- Enable/disable/select Masking
- Set Validity of a location
- Enable/Disable aging in a location
- Enable/disable IEEE802.3/5 mapping
- Select Serial Port data source
- Suppress conditional writes
- Control Reset functions

A full description of the instructions defined by CT11-CT6 and the CT5-CT0 control pins for each instruction is available in Application Note AN4728 - The Control States of the P2800.

In the following description of the control states, when a data move to the next free address is executed, the entire contents of the Next Free Address Register are output on DQ0-DQ31, and include the Full Flag on DQ31. Similarly, when a Highest Priority Match Address Register is read, on DQ0-DQ31 it includes the System Match flag for the comparison channel on DQ31.

CONTROL STATES

READ/WRITE REGISTER

CT11 - CT6	/W = LOW	/W = HIGH
000 000	DQ>C0	C0>DQ
000 001	DQ>C1	C1>DQ
000 010	DQ>CF	CF>DQ
000 011	RESERVED	AL>DQ
000 100	DQ>M0	M0>DQ
000 101	DQ>M1	M1>DQ
000 110	DQ>M2	M2>DQ
000 111	DQ>M3	M3>DQ
001 000	RST CAM	HA0>DQ
001 001	RST SA/B	HA1>DQ
001 010	AD>HD0	HD0>DQ
001 011	AD>HD1	HD1>DQ
001 100	TMP>C0/1	NF>DQ
001 101	SAC	RAC
001 110	RESERVED	RESERVED
001 111	NOP	NOP

READ/WRITE MEMORY

CT11 - CT6	/W = LOW	/W = HIGH
010 000	C0>[ADDR]	[ADDR]>C0
010 001	RESERVED	C0>[NFA] ADDR>DQ
010 010	C1>[ADDR]	[ADDR]>C1
010 011	RESERVED	C1>[NFA] ADDR>DQ
010 100	CF>[ADDR]	[ADDR]>CF
010 101	DQ>[NFA]	CF>[NFA] ADDR>DQ
010 110	DQ>[ADDR]	[ADDR]>DQ
010 111	SVA[ADDR]	RVA[ADDR]
011 000	M0>[ADDR]	[ADDR]>M0
011 001	RESERVED	M0>[NFA] ADDR>DQ
011 010	M1>[ADDR]	[ADDR]>M1
011 011	RESERVED	M1>[NFA] ADDR>DQ
011 100	M2>[ADDR]	[ADDR]>M2
011 101	RESERVED	M2>[NFA] ADDR>DQ
011 110	M3>[ADDR]	[ADDR]>M3
011 111	RESERVED	M3>[NFA] ADDR>DQ

CONDITIONAL WRITE

CT11 - CT6	/W = LOW	/W = HIGH
100 000	If /SM0=LOW C0>[ADDR]	If /SM0=LOW C0>[NFA] ADDR>DQ
100 001	If /SM1=LOW C1>[ADDR]	If /SM1=LOW C1>[NFA] ADDR>DQ
100 010	If /SM0=HIGH C0>[ADDR]	If /SM0=HIGH C0>[NFA] ADDR>DQ
100 011	If /SM1=HIGH C1>[ADDR]	If /SM1=HIGH C1>[NFA] ADDR>DQ
100 100	If /SM0=LOW SV[ADDR]	If /SM0=LOW C0>[HPM] ADDR>DQ
100 101	If /SM1=LOW SV[ADDR]	If /SM1=LOW C1>[HPM] ADDR>DQ
100 110	If /SM0=LOW SV[AML]	If /SM0=LOW SV[HPM] ADDR>DQ
100 111	If /SM1=LOW SV[AML]	If /SM1=LOW SV[HPM] ADDR>DQ
101 000	If /SM0=LOW SET AG[HPM] Else C0>[ADDR]	If /SM0=LOW SET AG[HPM] Else C0>[NFA] ADDR>DQ
101 001	If /SM1=LOW SET AG[HPM] Else C1>[ADDR]	If /SM1=LOW SET AG[HPM] Else C1>[NFA] ADDR>DQ
101 010	If /SM0=LOW SET AG[AML] Else C0>[ADDR]	If /SM0=LOW SET AG[AML] Else C0>[NFA] ADDR>DQ
101 011	If /SM1=LOW SET AG[AML] Else C1>[ADDR]	If /SM1=LOW SET AG[AML] Else C1>[NFA] ADDR>DQ

COMPARE

CT11 - CT6	/W = LOW	/W = HIGH
101 100	C0//CAM	AG(0)//CAM
101 101	C1//CAM	AG(1)//CAM
101 110	C0//CAM AD>HD0	V(0)//CAM
101 111	C1//CAM AD>HD1	V(1)//CAM
110 000	DQ>C1 C0//CAM	RESERVED
110 001	DQ>C0 C1//CAM	RESERVED
110 010	DQ>C1 C0//CAM;AD>HD0	RESERVED
110 011	DQ>C0 C1//CAM;AD>HD1	RESERVED
110 1XX	RESERVED	RESERVED
111 000	Factory Diagnostics	Factory Diagnostics
111 001	Factory Diagnostics	Factory Diagnostics
111 01X	RESERVED	RESERVED
111 1XX	RESERVED	RESERVED

CONTROL STATE ABBREVIATIONS

ADDR	Address Value
AD	Associated Data
AG	Aging Counter Value
AML	All Matching Locations
C0, C1	Comparand Register 0, 1
CAM	Associative Section of the Memory Array
CF	Configuration Register
DQ	Data Bus
HA0, HA1	Highest-priority-match Address Register 0, 1
HD0, HD1	Highest-priority-match Data Register 0, 1
HPM	Highest-priority Matching
INC	Increment
M0, M1, M2, M3	Mask Register 0, 1, 2, 3
NFA	Next Free Address
RST	Reset
RAC	Read Aging Counter
RVA	Read Validity/Aging
SAC	Set Aging Counter
SVA	Set Validity/Aging
[ ]	Contents of Location(s)
>	Move to
//	Compare

EXAMPLE CONTROL STATE DETAILS

Write Cycle: Data Bus to Comparand Register 0
Read Cycle: Comparand Register 0 to Data Bus

CT11 - CT0		/W = LOW	/W = HIGH
000 000 mmm avv		DQ>C0	C0>DQ
mmm	0XX	No Mask	Don't Care
	100	Mask with M0	Don't Care
	101	Mask with M1	Don't Care
	110	Mask with M2	Don't Care
	111	Mask with M3	Don't Care
a	0	No Data Map	No Data Map
	1	802.3/5 Map	802.3 /5 Map
vv	XX	Don't Care	Don't Care

Cycle Type: Write Cycle: Register Cycle
Read Cycle: Register Cycle

Description: Move data between Comparand Register 0 and DQ Bus. Direction of transfer determined by /W. IEEE 802.3 to/from IEEE 802.5 data mapping is selected with a. Data written into Comparand Register 0 can be masked by the Mask Register selected by mmm.

SWITCHING CHARACTERISTICS

No.	Symbol	Parameter	Min	Max	Units	Notes
1	tELEL1	Register Read/Write Cycle Time	20	-	ns	
2	tELEH1	Strobe LOW Pulse Width (Register)	10	-	ns	
3	tEHEL	Strobe HIGH Pulse Width	6	-	ns	
4	tWVEL	Write Setup to Strobe LOW	5	-	ns	
5	tELWX	Write Hold from Strobe LOW	0	-	ns	
6	tCTVEL	Control Setup to Strobe LOW	14	-	ns	
7	tELCTX	Control Hold from Strobe LOW	0	-	ns	
8	tFSVEL	Field Select Setup to Strobe LOW	8	-	ns	
9	tELFSX	Field Select Hold from Strobe LOW	0	-	ns	
10	tAQVEL	Address Setup to Strobe LOW	5	-	ns	
11	tELAQX	Address Hold from Strobe LOW	0	-	ns	
12	tELQX	Strobe LOW to Outputs Active	1	-	ns	
13	tELQV	Strobe LOW to Read Data Valid	-	10	ns	
14	tEHQZ	Strobe HIGH to Outputs Hi-Z	-	6	ns	
15	tDVEH1	Write Data Setup to Strobe HIGH (Register)	8	-	ns	
16	tEHDX1	Write Data Hold from Strobe HIGH (Register)	0	-	ns	
17	tELFFV	Strobe LOW to Full Flag Valid	-	35	ns	
18	tFIVFFV	Full Input to Full Flag Valid	-	5	ns	
19	tCKHCKH	Serial Port Clock Cycle Time	12.5	-	ns	
20	tCKHCKL	Serial Port Clock LOW Pulse Width	4	-	ns	
21	tCKLCKH	Serial Port Clock HIGH Pulse Width	4	-	ns	
22	tSVCKH	Serial Data Setup to Clock HIGH	3	-	ns	
23	tCKHSX	Serial Data Hold from Clock HIGH	2	-	ns	
24	tCKHZCV	Serial Clock HIGH to Zero Count Valid	-	8	ns	
25	tRSTLRSTH	Device Reset LOW Pulse Width	32	-	ns	
26	tRSTLCKH	Serial Port Reset LOW Setup to Clock	2	-	ns	
27	tELEL2	Memory Read/Write Cycle Time	45	-	ns	
28	tELEH2	Strobe LOW Pulse Width (Memory)	32	-	ns	
29	tELQV2	Strobe LOW to Read Data Valid (Memory)	-	30	ns	
30	tMIVMFV	Match Input Valid to Match Flag Valid	-	3	ns	
31	tMIXMFX	Match Input Invalid to Match Flag Invalid	2	-	ns	
32	tELMFV	Match Flag Valid from Compare Cycle	-	50	ns	/M10,1=HIGH
33	tEHQX	Strobe HIGH to Outputs Invalid	1	-	ns	
34	tCKHRSTH	Serial Clock HIGH to Reset Hold	2	-	ns	
35	tDVEH1	Write Data Setup to Strobe HIGH (Memory)	15	-	ns	
36	tEHDX1	Write Data Hold from Strobe HIGH (Memory)	0	-	ns	
37	tCC1	Comparison Cycle Time	50	-	ns	
38	tCC2	Comparison Cycle Time, Composite	70	-	ns	
39	tMASAOV	Select Input to Address Out Valid	-	5	ns	
40	tMAELAOX	Address Enable LOW to Address Out Active	1	5	ns	
41	tMAELAOV	Address Enable LOW to Address Out Valid	-	8	ns	
42	tMAEHAOZ	Address Enable HIGH to Address Out Hi-Z	-	6	ns	
43	tELAOV	Strobe LOW to Address Out Valid	5	50	ns	

TIMING DIAGRAMS

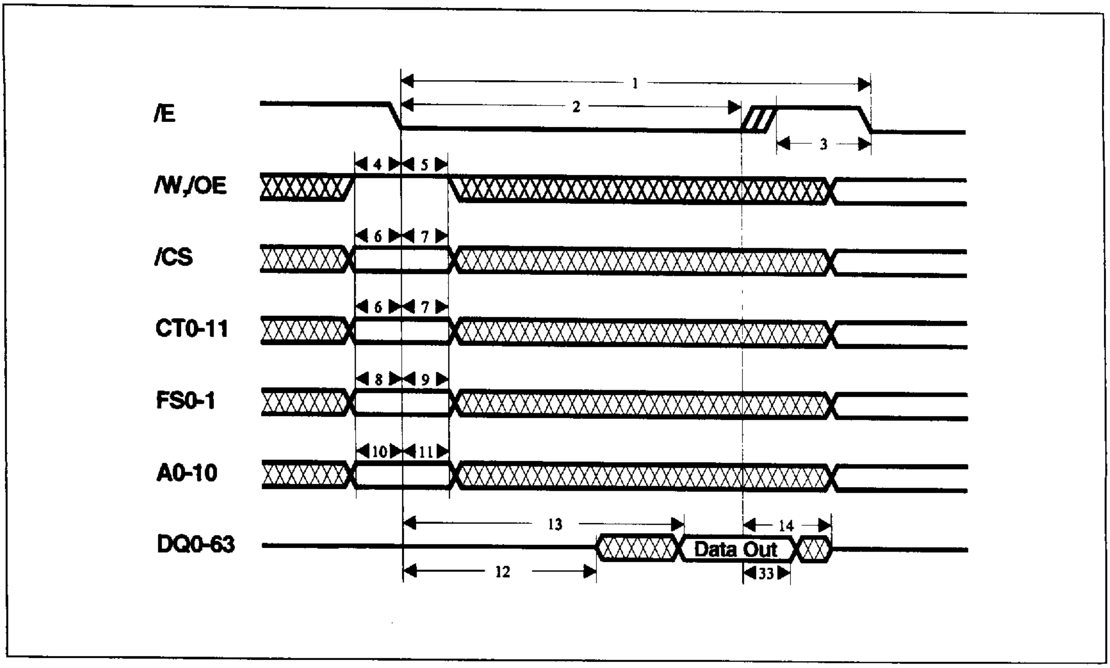


Fig. 4 Register read cycle, pipelined read cycle

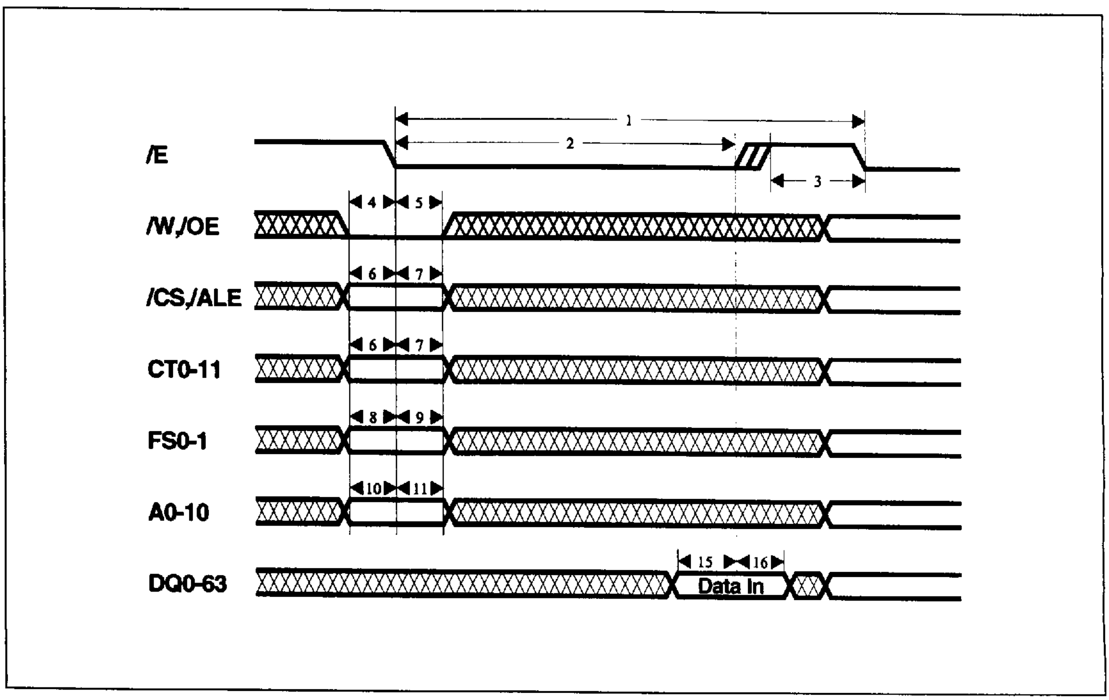


Fig. 5 Register write cycle, pipelined write cycle

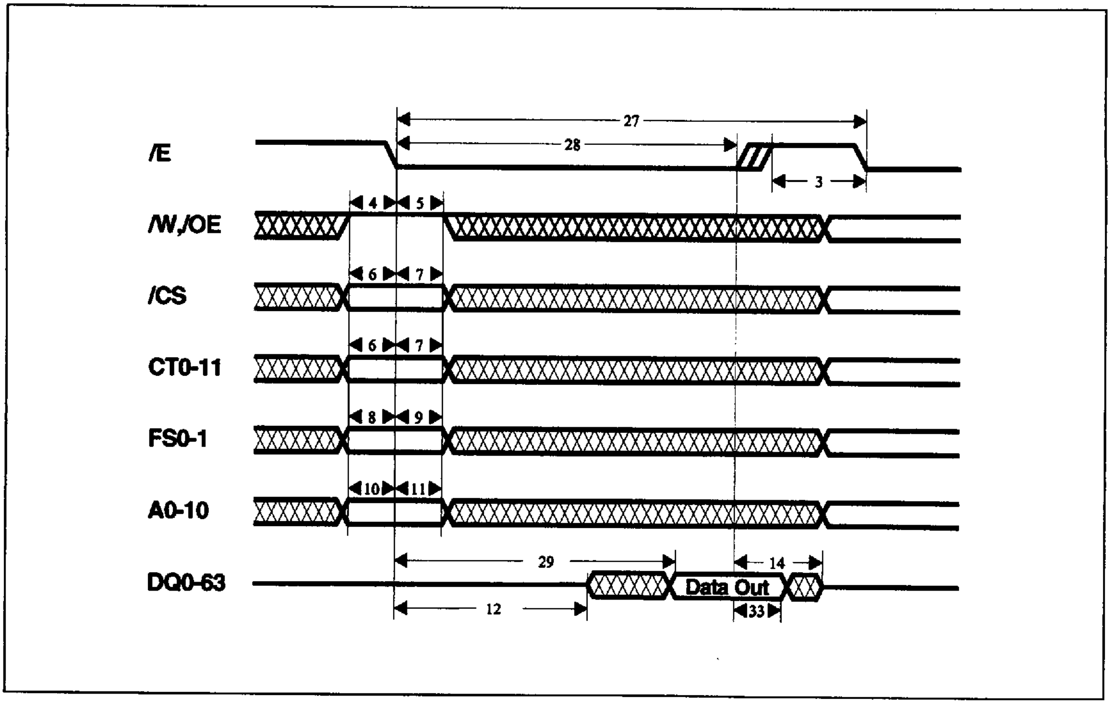


Fig. 6 Memory read cycle

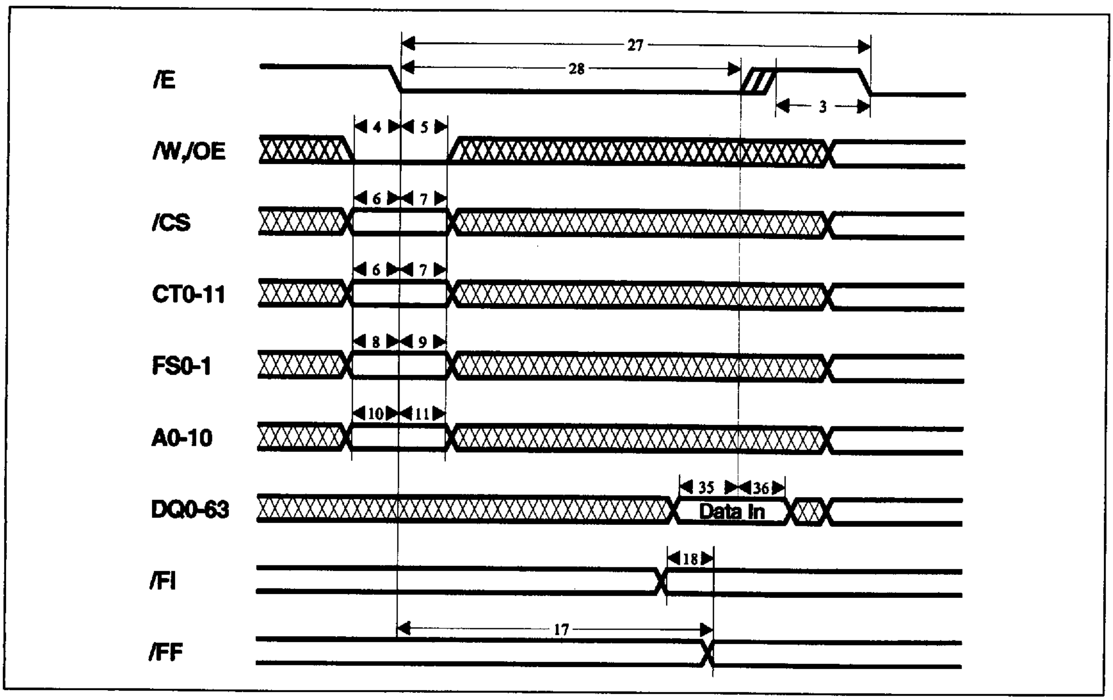


Fig. 7 Memory write cycle

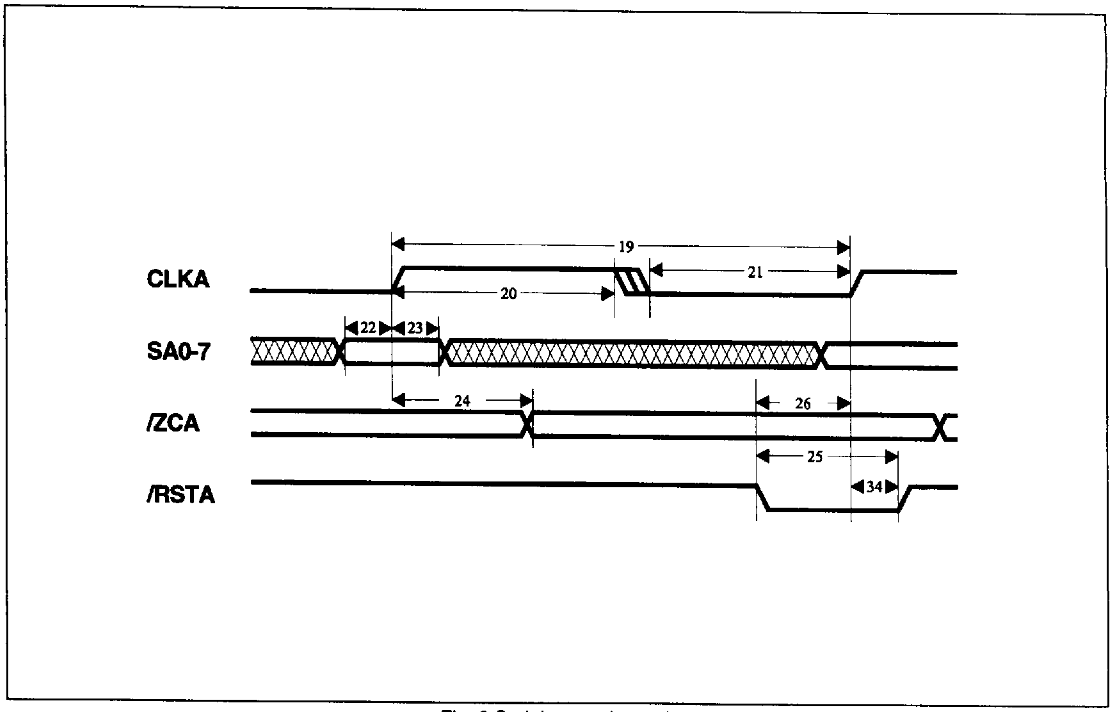


Fig. 8 Serial port write cycle

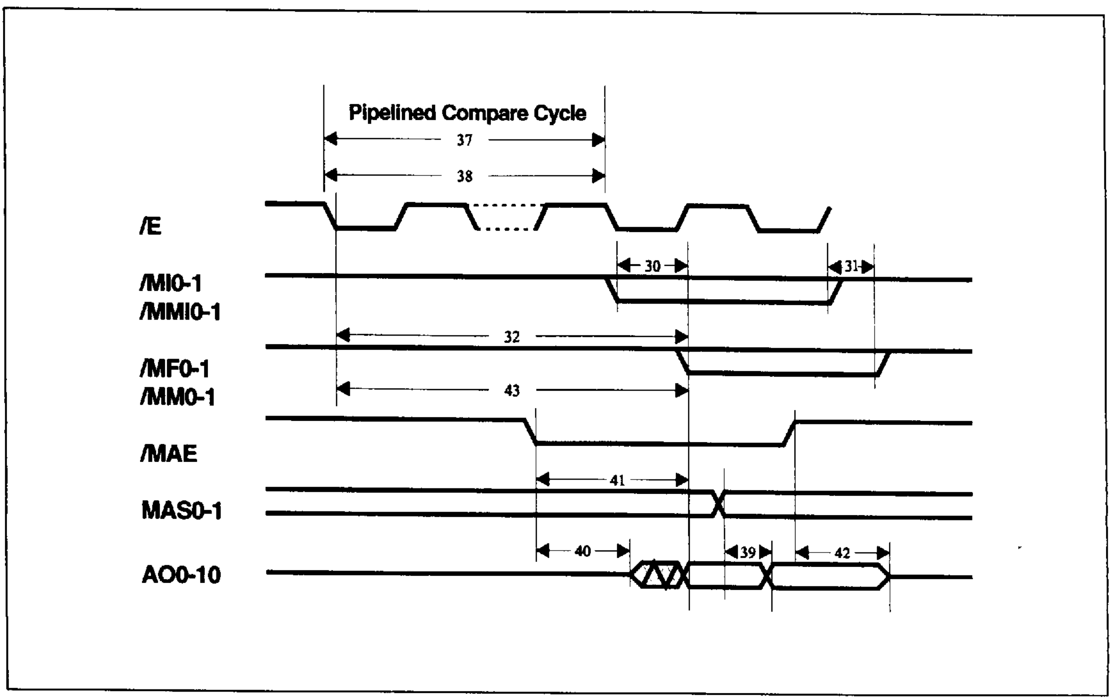


Fig. 9 Compare cycle

TYPICAL APPLICATION

Fig.10 shows the P2800 in a typical memory-mapped architecture, controlled from a local microprocessor. The Address Decoder maps the control structure of the P2800 into a 4K block of address space. The control states are then fed from the processor Address Bus into the Control Bus CT0-11 inputs. The remaining address space can be used for RAM, ROM and other memory mapping areas.

The P2800 does not need direct addressing because it can be written associatively, at the next free address. Under these circumstances, the address bus is only used to convey control states to the device, although it does support direct addressing for random access cycles if required.

The comparison channels are selected through the control states, and the results of a comparison cycle remain until a subsequent comparison is executed within that channel.

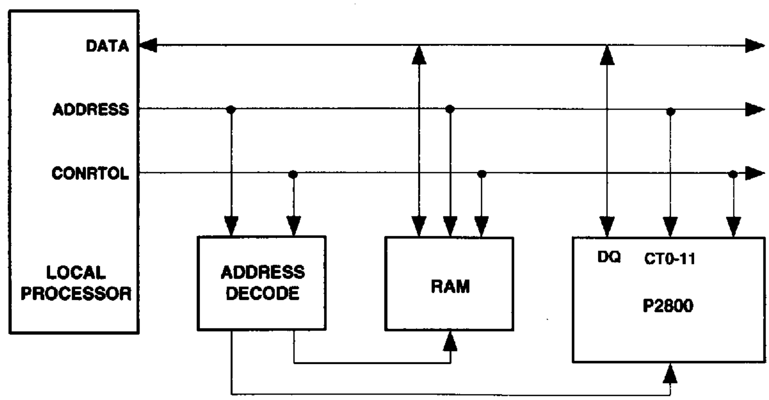
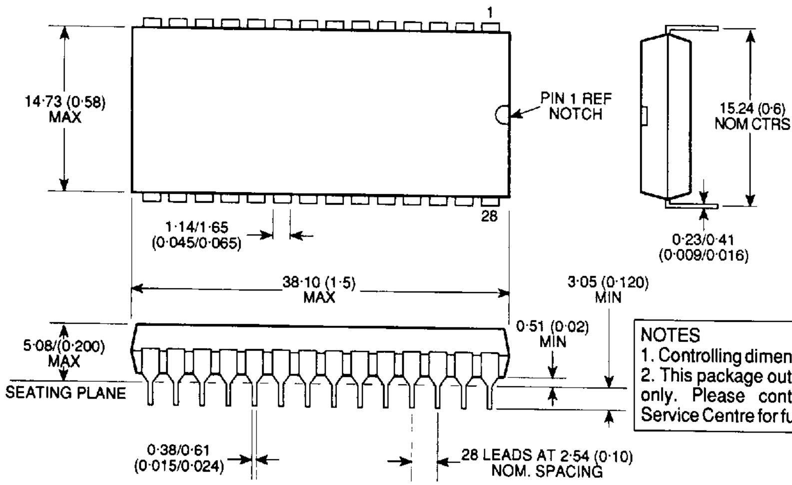
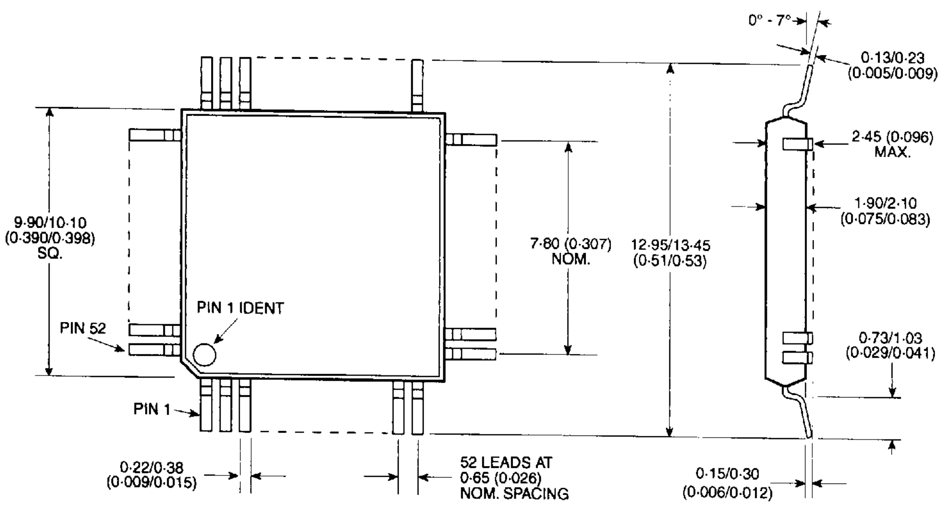


Fig. 10 Memory mapped P2800 system



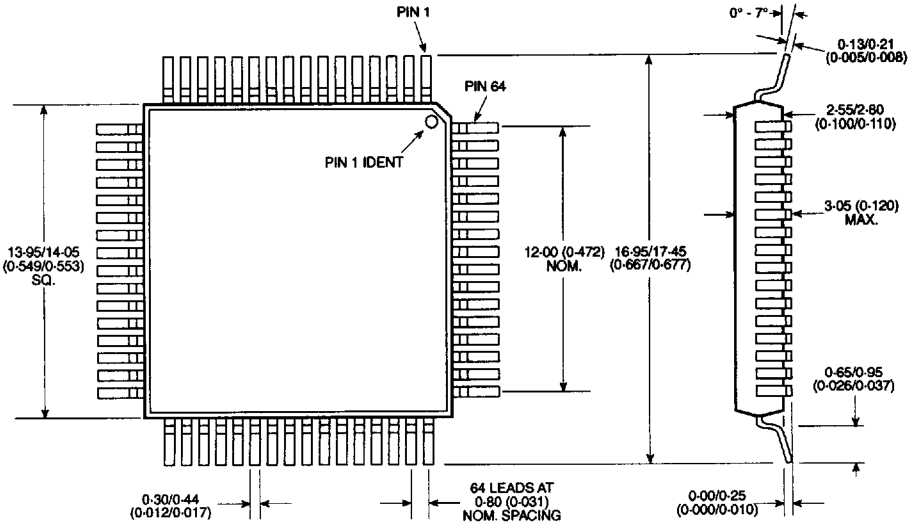
NOTES
1. Controlling dimensions are inches.
2. This package outline diagram is for guidance only. Please contact your GPS Customer Service Centre for further information.

28-LEAD PLASTIC DIL – DP28



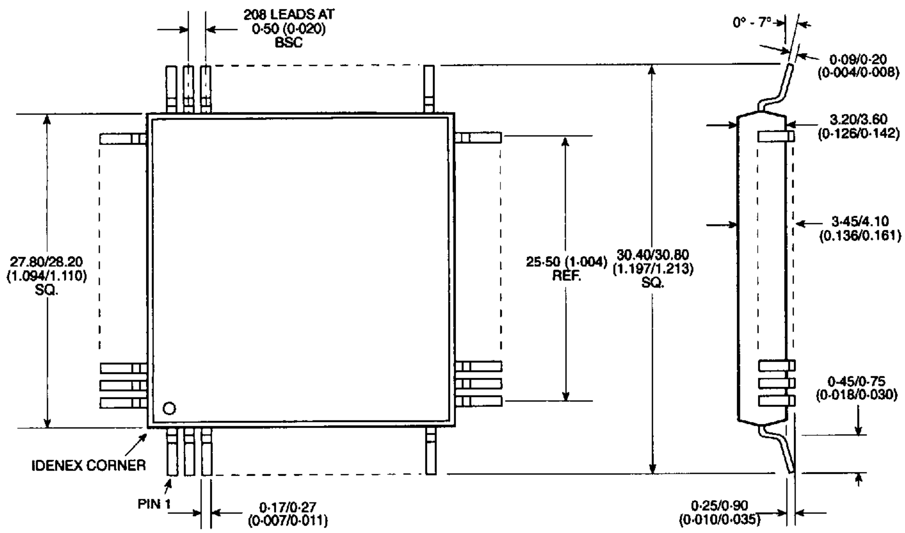
NOTES
1. Controlling dimensions are millimetres.
2. This package outline diagram is for guidance only. Please contact your GPS Customer Service Centre for further information.

52-LEAD QUAD FLATPACK – GP52



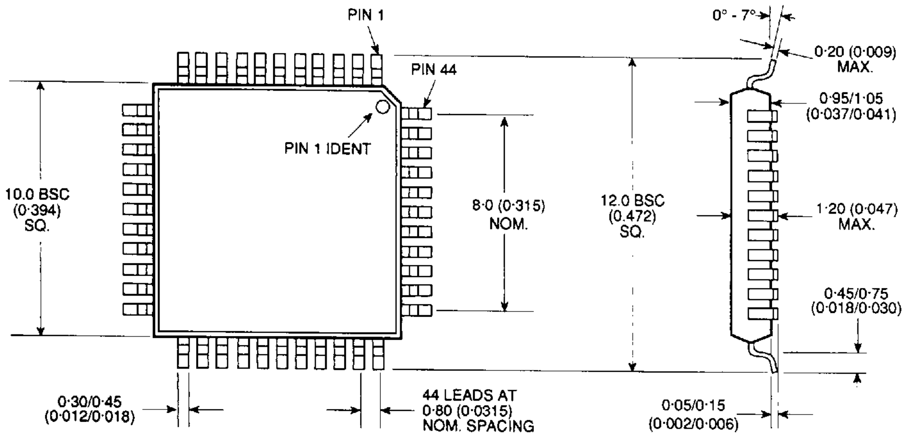
NOTES
1. Controlling dimensions are inches.
2. This package outline diagram is for guidance only. Please contact your GPS Customer Service Centre for further information.

64-LEAD PLASTIC QUAD FLATPACK – GP64



NOTES
1. Controlling dimensions are inches.
2. This package outline diagram is for guidance only. Please contact your GPS Customer Service Centre for further information.

208-LEAD PLASTIC QUAD FLATPACK – GP208



NOTES
1. Controlling dimensions are millimetres.
2. This package outline diagram is for guidance only. Please contact your GPS Customer Service Centre for further information.

44-LEAD THIN PLASTIC QUAD FLATPACK – TP44