

YAMAHA LSI

V6366 (PCDC)

■ OUTLINE

The PCDC (Panel Display & CRT Display Controller) is a display controller that has the two functions: (1) the display control of a high-capacity flat-panel display (hereafter referred to as a "Panel") and (2) the display control of a raster-scan type CRT. By merely performing initialization, however, even the Panel can be used without changing the software for conventional CRTs, enabling the simple system configuration of a handheld or portable computer which uses the Panel. (If so required, the PCDC can also be used to switch the display monitor between a CRT and a Panel.)

The PCDC is compatible with the CGA (Color Graphics Adapter), MDA (Monochrome Display Adapter), and HGC (Hercules Graphics Card), all for IBM PC application. In case the software and hardware for connecting a regular monitor come as a pair, the PCDC offers compatibility without requiring software changes (initialization is also unnecessary). Even in case of connecting different monitors, initialization will only be performed once at Power Start-Up, then compatibility will be available without requiring any software changes. It is thus possible, for example, to run CGA software using an IBM monochrome monitor and the Panel. (A gray scaling/hatching display can be used with a monochrome monitor.)

Because the PCDC has the display capacity of the IBM PC as well as numerous other expansion functions, including Kanji display, Color Palette, and the capability to simultaneously display up to 256 colors, a high-performance display system can be easily configured.

YAMAHA CORPORATION

V6366 CATALOG

CATALOG No.:LSI-2163662

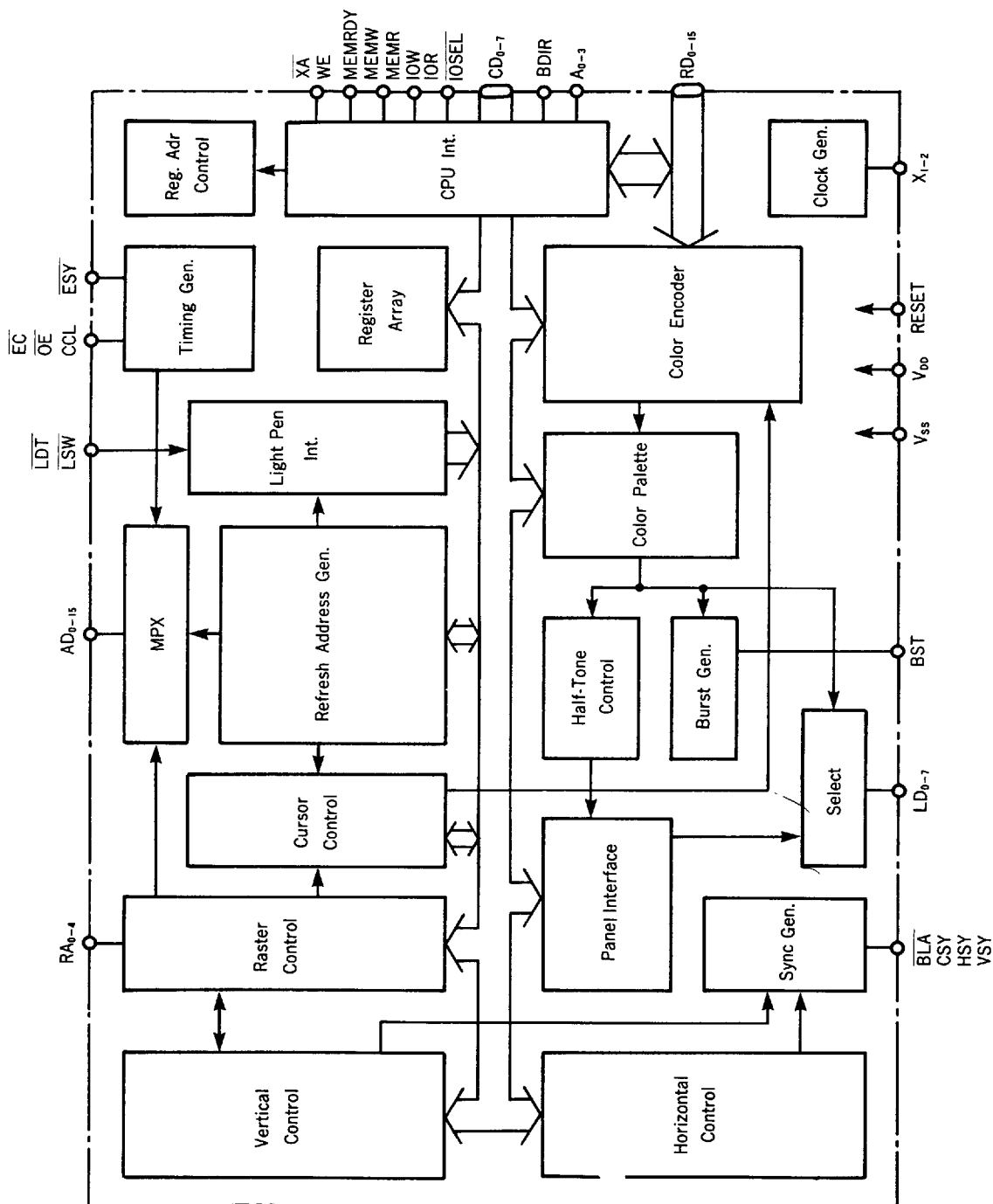
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■ FEATURES

- All functions of MC6845 are built in (excluding the Interlacing & Video Mode and the Skew function).
- In addition to a CRT or LCD, a EL and Plasma Display can also be connected.
- A 640 by 400 PEL Panel can be driven (a 720 by 350 PEL Panel can also be driven).
- A one-screen Panel or two-screen Panel (split into top and bottom halves) can be used.
- A two-screen panel allows, at a maximum duty, display of up to 512 lines (1/256).
- Selection of 1-, 2-, 4- or 8-bit parallel transmission of data to the Panel.
- A gray scaling/hatching display can be used with the Panel or a monochrome monitor.
- IBM PC software for 640 by 200 PELs can be directly displayed on a 640 by 400 PEL screen. (An 8 by 16 character font can be used, and can be displayed even in Double Scan Mode.)
- In addition to the standard IBM PC Graphics Modes, a variety of other Graphics Modes are provided: 320 by 200 PELs x 16 or 256 colors, 320 by 400 PELs x 4 or 16 colors, 640 by 200 PELs x 4 or 16 colors, 640 by 400 PELS x 4 colors, 640 by 350 PELs x 16 colors, and so on.
- A Protect Bit is provided for software protection.
- An SRAM or DRAM can be used as the VRAM. (Because the timing for display and the CPU are separate, the CPU can access VRAM at any time (without awaiting the retrace-timing.))
- Built-in interface for the Light Pen
- With a linear RGB monitor, 16 out of 512 colors can be simultaneously displayed.
- With an EGA monitor, 16 out of 64 colors can be simultaneously displayed.
- A Color Lookup Table can even be used with an IBM color monitor.
- A Standby function is provided to conserve power dissipation.
- Kanji display capacity of 16 by 16, 24 by 24 or 32 by 32 "PELs" (picture elements or pixels). (Attributes can also be used).
- The font configuration can be selected. Horizontal: 6, 7, 8, 9, 10, or [8 x integer] PELs (capable of a mixed display of half-width and full-width text); Vertical: 1 to 32 PELs.
- Capable of smooth scrolling and (in Interlace Mode only) external synchronization
- Simultaneous display capability with an IBM color monitor and a one-screen LCD of 640 x 200.
- CMOS, 5V power supply, 100-pin QFP or 84-pin PLCC

■ BLOCK DIAGRAM



■ DESCRIPTION OF TERMINAL FUNCTIONS

Signal Name	I/O	Terminal Functions
A ₀ { A ₃	I	Address for I/O register selection. A ₀ is also used for selecting the high or low byte.
CD ₀ { CD ₇	I/O	Data Bus for the CPU
MEMRDY MEMW MEMR IOW IOR IOSEL	O I I I I I	Read/Write Ready signal for the Memory ('0': Wait) Controls writing to Memory Controls reading from Memory Controls writing to the I/O registers Controls reading from the I/O registers Enable signal to the I/O Register D and E ('0': Enable)
RESET LSW LDT X ₁ X ₂ BDIR	I I I I I/O O	Reset signal Light Pen Switch signal (At RESET, specifies an 8- or 16-bit Data Bus for VRAM) Light Pen Detection signal (At RESET, specifies VRAM from SRAM or DRAM)) For X'tal oscillation or external clock input Direction control of the bi-direction buffer for the CPU Data Bus
RA ₀ { RA ₃ RA ₄	O O I/O	Raster Address Raster Address or AC Conversion signal (At RESET, specifies the Hercules or CGA Mode)
RD ₀ { RD ₇ RD ₈ { RD ₁₅	I/O I/O I/O I/O	Data bus for VRAM (Low side) Data bus for VRAM (High side)
\overline{EC} \overline{OE} CCL \overline{WE} XA	O O O O O	Transmission control for the RD Bus of Character Font Data Output control (for SRAM) Latch clock for character codes Controls writing of VRAM CPU-related timing for VRAM
V _{SS} V _{SS} V _{DD} V _{DD}	I I I I) 0V) +5V

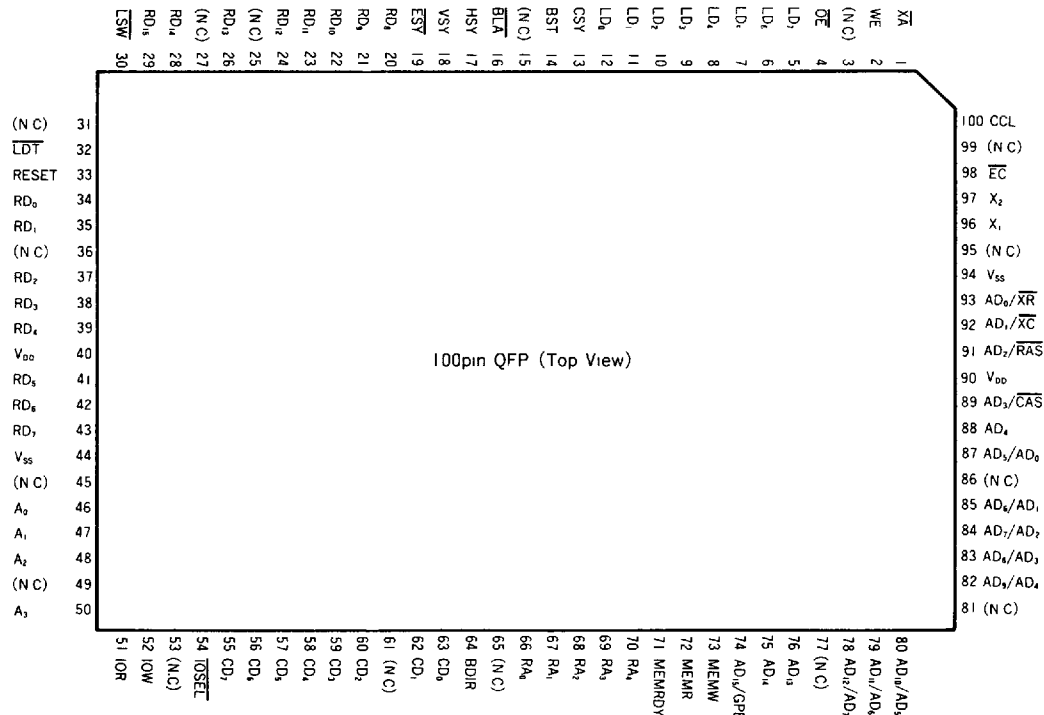


Signal Name	I/O	Terminal Functions				
AD ₀ / <u>XR</u>	O	<div><div>Addresses of SRAM</div><div>Addresses of DRAM</div></div>	CPU RAS Address timing for DRAM			
AD ₁ / <u>XC</u>	O		CPU CAS Address timing for DRAM			
AD ₂ / <u>RAS</u>	O		<u>RAS</u> for DRAM			
AD ₃ / <u>CAS</u>	O		<u>CAS</u> for DRAM			
AD ₄	O					
AD ₅ /AD ₀	O					
AD ₆ /AD ₁	O					
AD ₇ /AD ₂	O					
AD ₈ /AD ₃	O					
AD ₉ /AD ₄	O					
AD ₁₀ /AD ₅	O					
AD ₁₁ /AD ₆	O					
AD ₁₂ /AD ₇	O					
AD ₁₃	O					
AD ₁₄	O					
AD ₁₅ /GPE	O	Also, OR output of Bits 0 and 1 of the Control Register in Hercules Mode				
LD ₄	O	DB	Primary B	B ₀	LD ₄	<div><div>for linear RGB monitor</div><div>for Panel</div></div>
LD ₅	O	DG	Primary G	B ₁	LD ₅	
LD ₆	O	DR	Primary R	B ₂	LD ₆	
LD ₇	O	DI	Secondary G	G ₀	LD ₇	
LD ₀	O	BFP	←	←	LD ₀	
LD ₁	O			G ₁	LD ₁	
LD ₂	O		Secondary R	G ₂	LD ₂	
LD ₃	O	<u>Video</u>	Secondary B	R ₀	<u>LD₃</u>	
<u>BLA</u>	O	<u>BLANK</u>	←	R ₁	<u>HSY</u>	
BST	O	Color Burst	←	R ₂	<u>SCK</u>	
CSY	O	Composite Sync	←	←	<u>VSY</u>	
HSY	O	Horizontal synchronization	←	←	(ECK)	
VSY	O	Vertical synchronization	←	←		
<u>ESY</u>	I/O	for external synchronization				

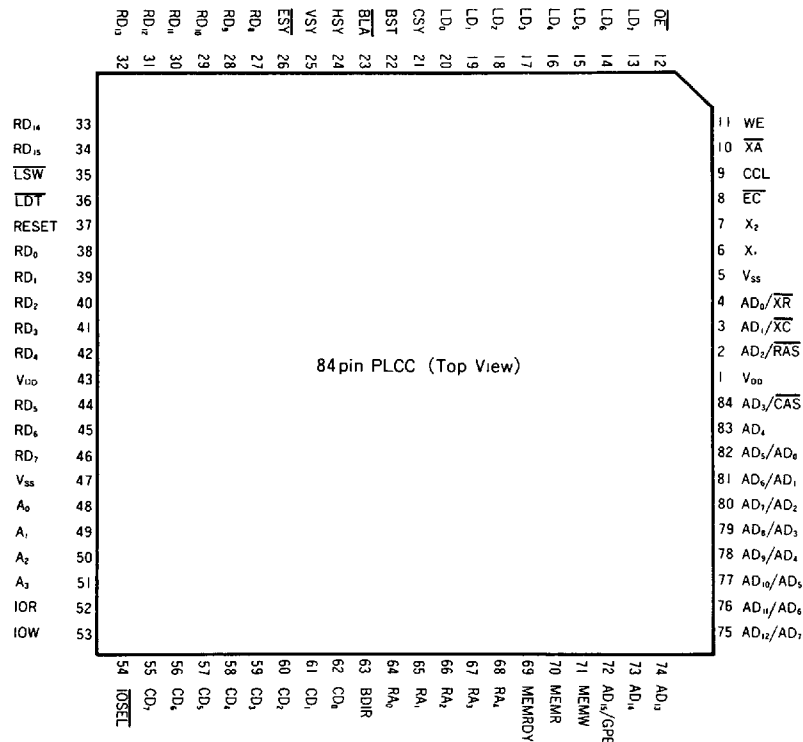


■ PIN ASSIGNMENT

(1) 100pin QFP



(2) 84pin PLCC



■ ELECTRICAL CHARACTERISTICS

Absolute Maximum Ratings

Item	Symbol	Min.	Max.	Unit
Supply voltage	V _{DD}	-0.3	+7.0	V
Input voltage	V _I	-0.3	V _{DD} + 0.3	V
Output voltage	V _O	-0.3	V _{DD} + 0.3	V
Operating temperature	T _{OP}	0	+70	°C
Storage temperature	T _{STG}	-50	+125	°C

(Based on the reference voltage of V_{SS} = 0.0V)

Recommended Condition for Use

Supply voltage: +5V ± 5% (based on V_{SS} = 0.0V)
 Operating temperature: 0 ~ 70°C

DC Characteristics (V_{DD} = 5V ± 5%, T_{OP} = 0 ~ 70°C)

Item	Symbol	Condition	Min.	Max.	Unit
High-level output voltage (for TTL driving)	V _{OH}	I _{OH} = -0.4mA	2.7		V
Low-level output voltage (for TTL driving)	V _{OL}	I _{OL} = 0.8mA		0.4	V
High-level output voltage (for CMOS driving)	V _{OH}	I _{OH} < 10μA	V _{DD} - 0.4		V
Low-level output voltage (for CMOS driving)	V _{OL}	I _{OL} < 10μA		0.4	V
High-level input voltage	V _{IH}		2.2		V
Low-level input voltage	V _{IL}			0.8	V
Input leak current	I _L		-10	10	μA
OFF status leak current	I _{LZ}		-10	10	μA
Power current (during normal operation)	I _{DD}			70	mA
Power current (during Standby)	I _{DD}			10	mA

NOTE: I_{LZ} applies while the CD0-CD7, RD0-RD15, X2, RA4, or $\overline{\text{ESY}}$ pins are in input status or while the AD0/XR ~ AD15/GPE or MEMRDY pins are in high-impedance status.

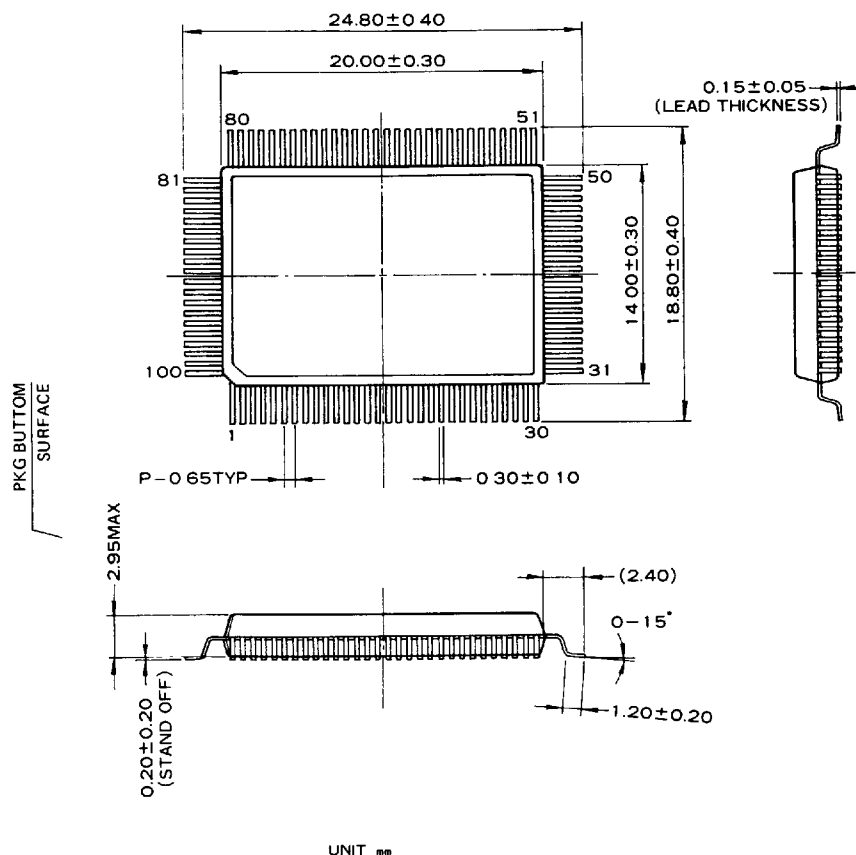


(1) Use of SRAM (For 16-Bit Bus, CGA)

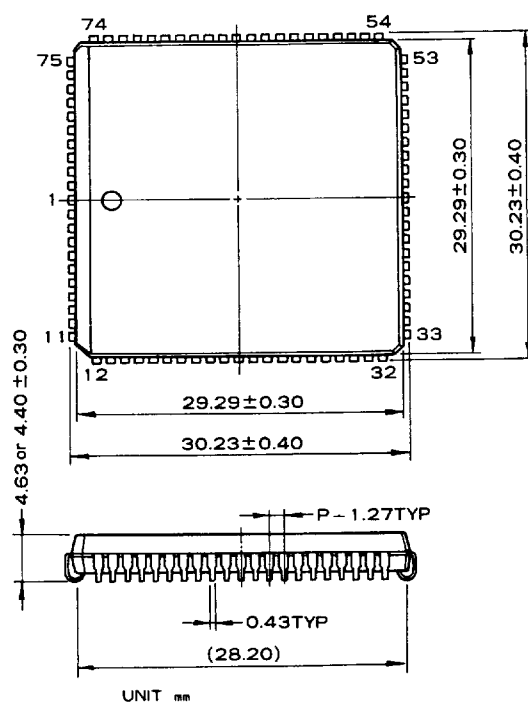


■ PACKAGE OUTLINES

(1) 100pin QFP



(2) 84pin PLCC



The specifications of this product are subject to improvement changes without prior notice.

AGENCY

—YAMAHA CORPORATION—

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