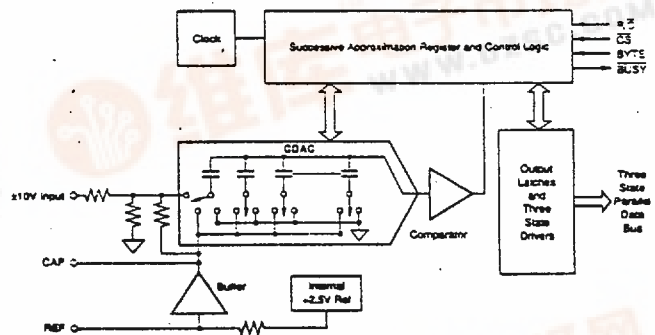


16 Bit A/D Converter - Radiation Hardened 7805LPRP

CMOS High Speed
Analog to Digital Converter

*For Space
Applications*

SEI's 7805LPRP (RP for RAD-PAK®) high speed 8 analog to digital converter features a minimum of 100 kilorad (Si) total dose tolerance. Using SEI's radiation hardened RAD-PAK® packaging technology, the 7805LPRP is fully equivalent to the commercial ADS7805 from Burr-Brown. This device is latchup protected by Space Electronics LPT™ technology. It is a 28 pin, 16 bit sampling A/D using state-of-the-art CMOS structures. It contains a complete 16-bit capacitor-based SAR A/D with S/H, reference, clock, interface for microprocessor use, and three-state output drivers. The 7805LPRP is specified at a 100 kHz sampling rate, and guaranteed over the full temperature range. Laser trimmed scaling resistors provide an industry standard $\pm 10V$ input range, while the innovative design allows operation from a single +5V supply, with power dissipation of under 100mW. The patented radiation hardened RAD-PAK® technology incorporates radiation shielding in the microcircuit package. Capable of surviving in space environments, the 7805LPRP is ideal for satellite, spacecraft, and space probe missions. This product is available in Class S packaging and screening.



SEI 7805LPRP RADHARD 16bit AtoD CONVERTER

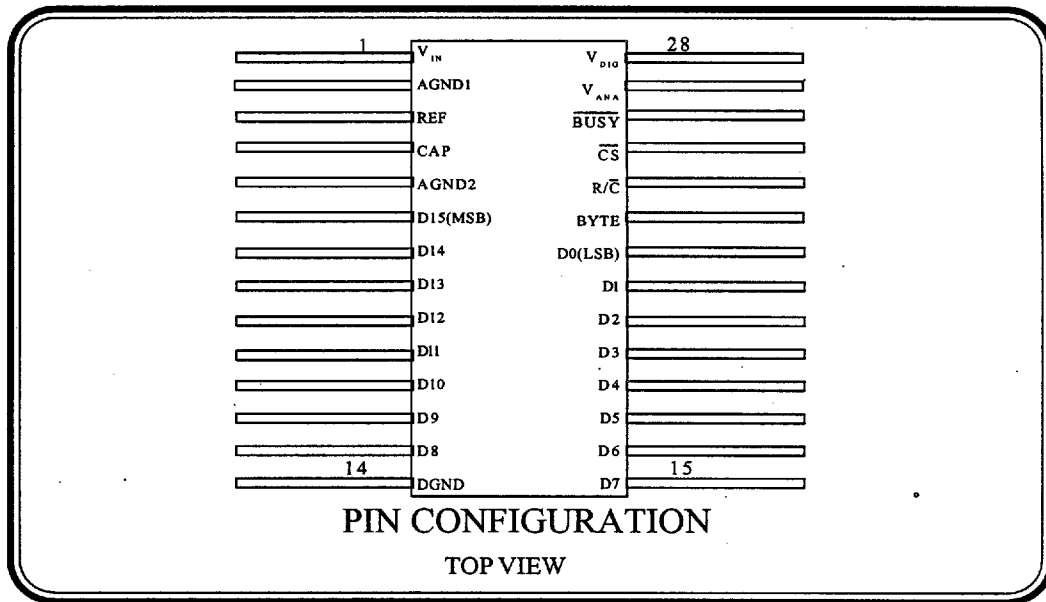


SPACE
ELECTRONICS
INCORPORATED

Tel: (619) 452-4167 Fax: (619) 452-5499

Radiation Hardened 7805LPRP

CMOS 16 Bit High Speed
Analog to Digital Converter



Features:

- 16 Bit Organization
- Pin Compatible with Burr-Brown ADS7805
- Latchup Protected by SEI LPT™ Technology
- RAD-PAK® Radiation Hardened Against Natural Space Radiation
- Total Dose Hardness > 100 krad (Si)
- Package:
 - 28 Pin RAD-PAK® DIP (0.550 inches x 1.500 inches)
 - Weight - 5.2 grams
- 100kHz min Sampling Rate
- Standard +10V Input Range
- Advance CMOS Technology
 - 86dB min SINAD with 45kHz Input
 - Single +5V Supply Operation
 - Utilizes Internal or External Reference
 - Full Parallel Data Output
 - Power Dissipation: 100mW Max
- Screening per TM5004
- QCI per TM5005

Specifications and design are subject to change without notice.



June, 1996

For Further Information Contact:

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7805LPRP ABSOLUTE MAXIMUM RATINGS

PARAMETER	MIN	TYP	MAX	UNIT
Specified Performance V_{CC} I_{CC}	4.75	5 19.1	5.2	V mA
Power Dissipation			115	mW
Specified Performance Temperature	-40		+85	°C
Derated Performance Temperature	-55		+125	°C
Storage Temperature	-65		+150	°C
Thermal Resistance		75		°C/W

7805LPRP DC ACCURACY SPECIFICATIONS

PARAMETER	MIN	TYP	MAX	UNIT
Integral Linearity Error			+3	LSB ¹
Differential Linearity Error			+3, -2	LSB
No Missing Codes	15			Bits
Transition Noise ²		1.3		LSB
Full Scale Error ^{3,4}			+0.5	%
Full Scale Error Drift		+7		ppm/°C
Full Scale Error ^{3,4}			+0.5	%
Full Scale Error Drift		+2		ppm/°C
Bipolar Zero Error ³			+10	mV
Bipolar Zero Error Drift		+2		ppm/°C
Power Supply Sensitivity 4.75V < V_{IN} < 5.2V			±8	LSB

- Notes:
1. LSB stands for Least Significant Bit. One LSB is equal to 305µV.
 2. Typical rms noise at worst case transitions and temperatures.
 3. Measured with various fixed resistors.
 4. Full scale error is the worst case of -Full Scale or +Full Scale untrimmed deviation from ideal first and last code transitions, divided by the transition voltage (not divided by the full-scale range) and includes the effect of offset error.



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7805LPRP AC ACCURACY SPECIFICATIONS

PARAMETER	MIN	TYP	MAX	UNIT
Spurious-Free Dynamic Range, $f_{in}=45\text{kHz}$	90			dB ⁵
Total Harmonic Distortion, $f_{in}=45\text{kHz}$			-90	dB
Signal-to-(Noise+Distortion), $f_{in}=45\text{kHz}$, -60dB Input	83	30		dB
Signal-to-Noise, $f_{in}=45\text{kHz}$	83			dB
Full-Power Bandwidth ⁶		250		kHz

- Notes: - 5. All specifications in dB are referred to a full-scale +10V input.
 6. Full-Power Bandwidth defined as Full-Scale input frequency at which Signal-to-(Noise+Distortion) degrades to 60dB, or 10 bits accuracy.

7805LPRP SAMPLING DYNAMICS

PARAMETER	MIN	TYP	MAX	UNIT
Aperture Delay		40		ns
Aperture Jitter ⁷				
Transient Response FS Step			2	us
Overvoltage Recovery ⁸		150		ns

- Notes: 7. Sufficient to meet 7805LPRP AC specs.
 8. Recovers to specified performance after 2 x FS input overvoltage.

7805LPRP REFERENCE

PARAMETER	MIN	TYP	MAX	UNIT
Internal Reference Voltage	2.48	2.5	2.52	V
Internal Reference Source Current (Must use ext. buffer)		1		uA
External Reference Voltage Range for Specified Linearity	2.3	2.5	2.7	V
External Reference Current Drain			100	uA

7805LPRP DIGITAL INPUTS

PARAMETER	SYMBOL	MIN	MAX	UNIT
Logic Levels				
V_{IL}	-0.3		+0.8	V
V_{IH}	+2.0		$V_D+0.3V$	V
I_{IL}			± 10	uA
I_{IH}			+10	uA



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7805LPRP DIGITAL OUTPUTS

PARAMETER	MIN	TYP	MAX	UNIT
Data Coding V_{OL} ($I_{SNK}=1.6mA$) V_{OH} ($I_{SOURCE}=500\mu A$)	+4		+0.4	V V
Leakage Current High-Z State, $V_{OUT}=0V$ to V_{DIG}			± 5	μA
Output Capacitance High-Z State			15	pF

7805LPRP DIGITAL TIMING

PARAMETER	MIN	TYP	MAX	UNIT
Bus Access Time			96	ns
Bus Relinquish Time			92	ns

7805LPRP CONVERSION TIMING

SYMBOL	DESCRIPTION	MIN	TYP	MAX	UNITS
t1	Convert Pulse Width	40			ns
t2	Data Valid Delay after R/\bar{C} Low			8	μs
t3	\overline{BUSY} Delay from R/\bar{C} LOW			65	ns
t4	\overline{BUSY} LOW			8	μs
t5	\overline{BUSY} Delay after End of Conversion		220		ns
t6	Aperture Delay		40		ns
t7	Conversion Time		5.7	8	μs
t8	Acquisition Time			2	μs
t9	Bus Relinquish Time	10	35	83	ns
t10	\overline{BUSY} Delay after Data Valid	50	200		ns
t11	Previous Data Valid Delay after R/\bar{C} Low		5.5		μs
t7 + t8	Throughput Time		7.5	10	μs
t12	R/\bar{C} to \overline{CS} Setup Time	10			ns
t13	Time Between Conversions	10			μs
t14	Bus Access Time and BYTE Delay	10		83	ns

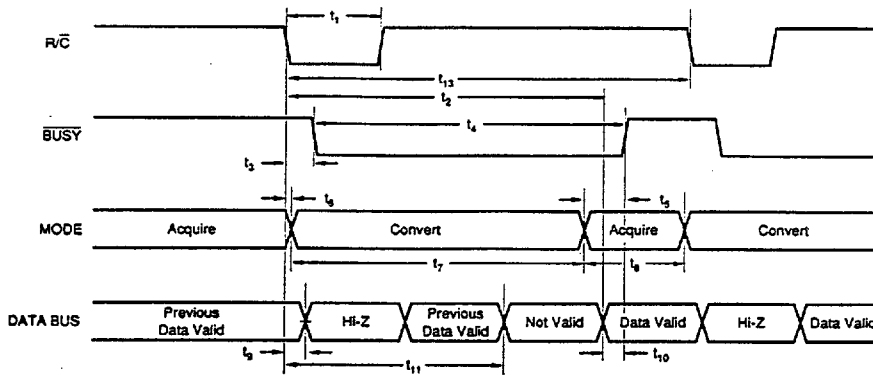


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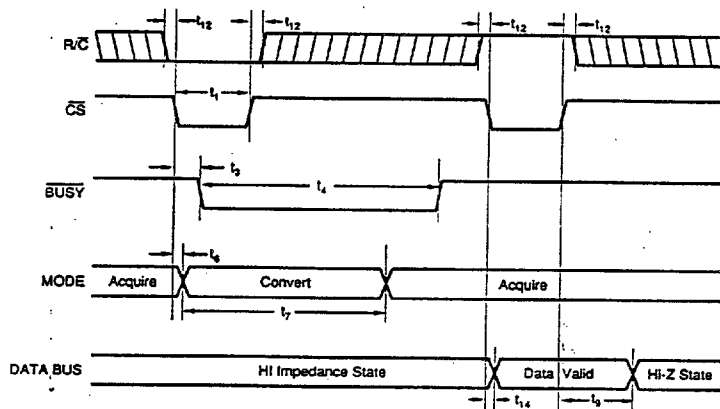
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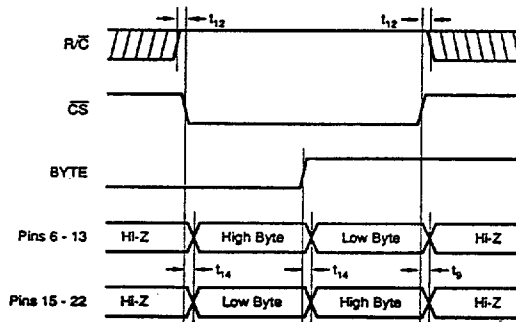
Conversion Timing with Outputs Enabled after Conversion (\overline{CS} Tied LOW.)



Using \overline{CS} to Control Conversion and Read Timing.



Using \overline{CS} and BYTE to Control Data Bus.



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7805LPRP PINOUT

PIN	DESCRIPTION
1	Vin
2	AGND1
3	REF
4	CAP
5	AGND2
6	D15
7	D14
8	D13
9	D12
10	D11
11	D10
12	D9
13	D8
14	DGND
15	D7
16	D6
17	D5
18	D4
19	D3
20	D2
21	D1
22	D0
23	BYTE
24	R/C\
25	CS\
26	BUSY\
27	Vdcoup
28	Vdig

7805LPRP Package Ordering Guide

Package Style	Case Outline	1/	Description
D	D-28		28 Pin Dual In Line Package

Note:

1/ For outline information, see Appendix A (Package Information - Outline Dimension)



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