HEWLETT PACKARD

Gigabit Rate Transmit Receive Chip Set

Technical Data

HDMP-1000 Tx/Rx Pair
HDMP-1002 Transmitter
HDMP-1004 Receiver

Features

- **Transparent, Extended Ribbon Cable Replacement**
- **High-Speed Serial Rate** 110-1400 MBaud
- **Standard 100K ECL Interface** 16, 17, 20, or 21 Bits Wide
- **Reliable Monolithic Silicon Bipolar Implementation**
- **On-chip Phase-Locked Loops**
  - Transmit Clock Generation
  - Receive Clock Extraction

Applications

- **Point to Point Data Links**
- **Implement SCI-FI Standard**
- **Implement Serial HIPPI Specification**
- **Backplane Extender**

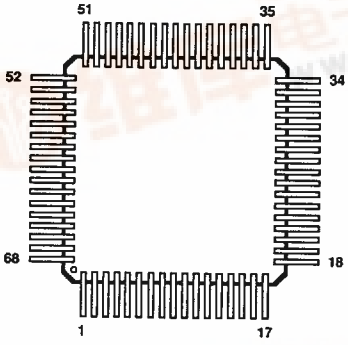
Description

The HDMP-1002 transmitter and the HDMP-1004 receiver are used to build a high speed data link for point to point communication. The HDMP-1000 consists of one HDMP-1002 and one HDMP-1004. The monolithic silicon bipolar transmitter chip and receiver chip are each provided in a standard, 68 pin, ceramic quad flat pack (CQFP).

From the user's viewpoint, these products can be thought of as providing a "virtual ribbon cable" interface for the transmission of data. Parallel data loaded into the Tx (transmitter) chip is delivered to the Rx (receiver) chip over a serial channel, which can be either a coaxial copper cable or optical link.

The chip set hides from the user all the complexity of encoding, multiplexing, clock extraction, demultiplexing and decoding. Unlike other links, the phase-locked-loop clock extraction circuit also transparently provides for frame synchronization - the user is not troubled with the periodic insertion of frame synchronization words. In addition, the dc balance of the line code is automatically maintained by the chip set. Thus, the user can transmit arbitrary data without restriction. The Rx chip also includes a state-machine controller (SMC) that provides a startup handshake protocol for the duplex link configuration.

Package Outline



PIN VIEW

The serial data rate of the T/R link is selectable in four ranges (see tables on page 3), and extends from 110Mbits/s up to 1.4Gbits/s. The parallel data interface is 16 or 20 bit single-ended ECL, pin selectable. A flag bit is available and can be used as an extra 17th or 21st bit under the user's control. The flag bit can also be used as an even or odd frame indicator for dual-frame transmission. If not used, the link performs expanded error detection. The serial link is synchronous, and both frame synchronization and bit synchronization are maintained. When data is not available to send, the link

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maintains synchronization by transmitting fill frames. Two (training) fill frames are reserved for handshaking during link startup.

User control words are supported. If CAV* is asserted at the Tx chip, the least significant 14 or 18 bits of the data are sent and the Rx CAV* line will indicate the data as a control word.

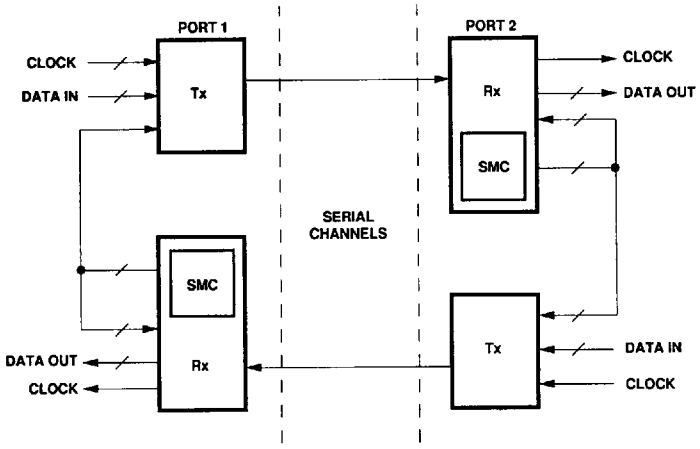


Figure 1. Point-to-Point Gigabit Data Link.

HDMP-1002 (Tx), HDMP-1004 (Rx)
Absolute Maximum Ratings

T_c = 25°C, except as specified. Operation in excess of any one of these conditions may result in permanent damage to this device.

Symbol	Parameter	Units	Minimum	Maximum
V_{EE}	Supply Voltage	V	-7	+0.5
$V_{IN,ECL}$	ECL Input Voltage	V	-3	+0.5
$V_{IN,BBL}$	H50 Input Voltage	V	-2	+1
$I_{O,ECL}$	ECL Output Source Current	mA		+50
T_{stg}	Storage Temperature	°C	-40	+130
T_J	Junction Temperature	°C	-40	+130
T_{max}	Maximum Assembly Temperature (for 10 seconds maximum)	°C		+260

HDMP-1002 (Tx), HDMP-1004 (Rx) Guaranteed Operating Rates For 16 Bit Mode[1]

T_c = 0°C to +85°C, V_{EE} = -4.5 V to -5.5 V

DIV1	DIV0	Parallel Word Rate (Mbit/sec)		Serial Data Rate (Mbit/sec)		Serial Baud Rate (MBaud)	
		Min.	Max.	Min.	Max.	Min.	Max.
0	0	42.5	65	680	1040	850	1300
0	1	21.3	41	340	656	425	820
1	0	10.6	20.7	169.6	332	212	415
1	1	5.5	10.2	88	164	110	205

Note:
1. Extended operating rates to 1520 MBaud/sec (typ) are possible for T_c = 0°C to +55°C.

HDMP-1002 (Tx), HDMP-1004 (Rx) Guaranteed Operating Rates For 20 Bit Mode[1]

T_c = 0°C to +85°C, V_{EE} = -4.5 V to -5.5 V

DIV1	DIV0	Parallel Word Rate (Mbit/sec)		Serial Data Rate (Mbit/sec)		Serial Baud Rate (MBaud)	
		Min.	Max.	Min.	Max.	Min.	Max.
0	0	35.4	58.3	708.3	1166.7	850	1400
0	1	17.7	34.2	354.2	683.3	425	820
1	0	8.8	17.3	176.6	345.8	212	415
1	1	4.6	8.5	91.7	170.8	110	205

Note:
1. Extended operating rates to 1640 MBaud/sec (typ) are possible for T_c = 0°C to +55°C.

HDMP-1002 (Tx), HDMP-1004 (Rx)
DC Electrical Specifications

T_c = 0°C to +85°C, V_{GND} = Ground, V_{EE} = -4.5 V to -5.5 V

Symbol	Parameter	Unit	Minimum	Typical	Maximum
$V_{IH,ECL}$	ECL Input High Voltage Level, Guaranteed high signal for all inputs	mV	-1150		
$V_{IL,ECL}$	ECL Input Low Voltage Level, Guaranteed low signal for all inputs	mV			-1600
$V_{OH,ECL}$	ECL Output High Voltage Level, Terminated with 300 Ω to -2.0 V	mV	-1050		
$V_{OL,ECL}$	ECL Output Low Voltage Level, Terminated with 300 Ω to -2.0 V	mV			-1500
$V_{IP,H50}$	H50 Input Peak-to-Peak Voltage	mV	200		
$V_{OH,BLL}$	BLL Output High Voltage Level, Terminated with 50 Ω to -1.3 V	V		-0.9	
$V_{OL,BLL}$	BLL Output Low Voltage Level, Terminated with 50 Ω to -1.3 V	V		-1.70	
$V_{OP,BLL}$	BLL Output Peak-to-Peak Voltage, Terminated with 50 Ω, ac coupled	V		+0.8	
$I_{EE,Tx}$	Transmitter V_{EE} Supply Current, with HCLKSEL off, V_{EE} = -5.0 V, T_c = 25°C	mA		+340	
$I_{EE,Rx}$	Receiver V_{EE} Supply Current, V_{EE} = -5.0 V, T_c = 25°C	mA		+427	

HDMP-1002 (Tx), HDMP-1004 (Rx)
AC Electrical Specifications, T_c = 25°C

Symbol	Parameter	Unit	Min.	Typ.	Max.
$t_{r,ECL}$	ECL Rise Time, (20-80%), Terminated with 300 Ω to -2.0 V	nsec		1	
$t_{f,ECL}$	ECL Fall Time, (80-20%), Terminated with 300 Ω to -2.0 V	nsec		2	
$t_{r,BLL}$	BLL Rise Time, (20-80%), Terminated with 50 Ω, ac coupled	psec		170	
$t_{f,BLL}$	BLL Fall Time, (80-20%), Terminated with 50 Ω, ac coupled	psec		200	
$VSWR_{i,H50}$	H50 Input VSWR			2:1	
$VSWR_{o,BLL}$	BLL Output VSWR			2:1	

HDMP-1002 (Tx)
Timing Characteristics

T_c = 0°C to +85°C, V_{EE} = -4.5 V to -5.5 V

Symbol	Parameter	Unit	Min.	Typ.	Max.
t_s	Setup Time, for Rising Edge of STRBIN Relative to D_0-D_{19}, ED, FF, DAV*, CAV*, and FLAG	nsec		2.0	
t_h	Hold Time, for Rising Edge of STRBIN Relative to D_0-D_{19}, ED, FF, DAV*, CAV*, and FLAG	nsec		2.0	
t_d	Delay Time, from Rising Edge of STRBIN to First Data Bit Out (D_0)	nsec		1.0	
ΔT_{strb}	STRBOUT - STRBIN Delay	nsec	1	3	5

HDMP-1004 (Rx)
Timing Characteristics

T_c = 0°C to +85°C

Symbol	Parameter	Unit	Min.	Typ.	Max.
t_{d1}	Synchronous Output Delay	nsec		2.0	
t_{d2}	State Machine Output Delay	nsec		4.0	

HDMP-1002 (Tx), HDMP-1004 (Rx)
Typical Lock-Up Time, T_c = 25°C

DIV1	DIV0	HDMP-1002, msec	HDMP-1004, msec	LINK[1], msec
0	0	2.0	2.2	2.5
0	1	3.0	3.2	3.5
1	0	4.5	4.7	5.0
1	1	8.0	11.0	12.0

Note:
1. Measured in Local Loop-Back mode with the state machine engaged and 0 cable length.

HDMP-1002 (Tx)
Thermal Characteristics, T_A = 25°C

Symbol	Parameter	Units	Typical
θ_{jc}	Thermal Resistance Die to Case	°C/Watt	12
P_D	Power Dissipation, V_{EE} = -5 V	Watt	1.75

HDMP-1004 (Rx)
Thermal Characteristics, T_A = 25°C

Symbol	Parameter	Units	Typical
θ_{jc}	Thermal Resistance Die to Case	°C/Watt	12
P_D	Power Dissipation, V_{EE} = -5 V	Watt	2.25

I/O Type Definitions

I/O Type	Definition
I-ECL	Input ECL. Similar to 100K ECL, but with pull-down. Thus, if the input is left unconnected, the buffer generates a default value of "0". The input can also be directly connected to ground to generate a "1".
O-ECL	Output ECL. Similar to 100K ECL but should be terminated with RTT ≥300 Ω, and do not exceed 10 cm connection distance.
IT-ECL	Input Test ECL. Can be turned off when not used.
OT-ECL	Output Test ECL. Can be turned off when not used.
O-BLL	50 Ω buffer line logic output driver. Will put out ECL levels if terminated with 50 Ω to -1.3 V, otherwise can be AC coupled to drive any 50 Ω loads. It can also drive the I-H50 inputs through differential direct coupling. Note: all unused outputs should be terminated with 50 Ω to ground.
I-H50	Input with internal 50 Ω terminations. Input is diode level shifted so that it can swing around ground. Can be driven with single-end configuration. Commonly used with input single-end AC coupling from an O-BLL driver or another 50 Ω source, or differential direct coupling from an O-BLL driver.
C	Filter capacitor node.
S	Power supply or ground.

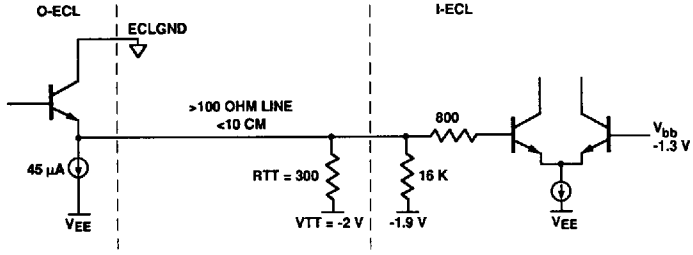
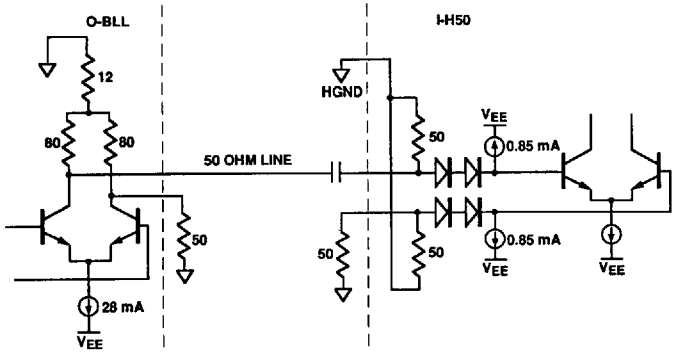


Figure 2. O-ECL and I-ECL Simplified Circuit Schematic.



plified Circuit Schematic.

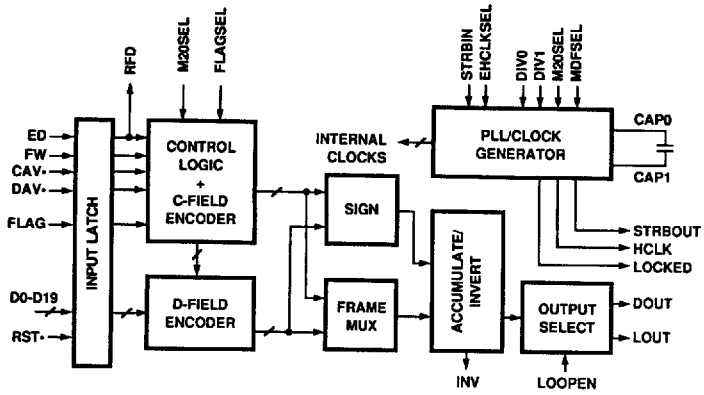


Figure 4. HDMP-1002 (Transmitter) Block Diagram.

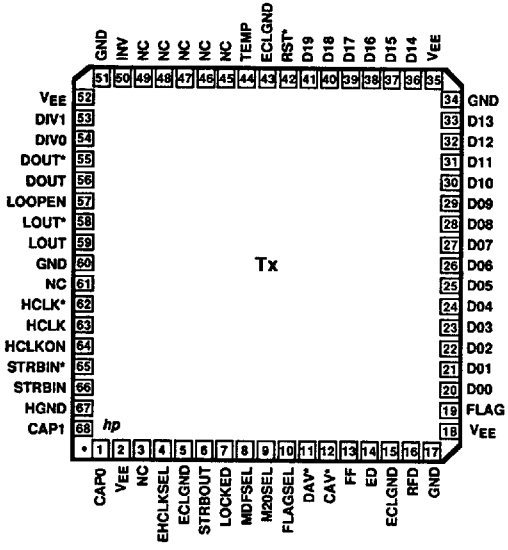


Figure 5. HDMP-1002 Package Layout, Pin View.

Tx I/O Definition

Name	Pin	Type	Signal
D00 D01 D02 D03 D04 D05 D06 D07 D08 D09 D10 D11 D12 D13 D14 D15 D16 D17 D18 D19	20 21 22 23 24 25 26 27 28 29 30 31 32 33 36 37 38 39 40 41	I-ECL	**Data Inputs:** 20 Bit data is encoded and transmitted when M20SEL is active; otherwise the 16 least significant bits are encoded and transmitted. The encoded bits are transmitted LSB first, e.g.: D0 is sent first, through to either D15 or D19, followed by the 4 coding bits C0-C3.
FLAG	19	I-ECL	**Extra Flag Bit:** When FLAGSEL is active, this input is sent as an extra data bit in addition to the normal Data inputs. When FLAGSEL is not Asserted, this input is ignored and the transmitted Flag bit is internally alternated to allow the Rx chip to perform enhanced frame error detection.
DAV*	11	I-ECL	**Data Available Input:** This active-low input tells the chip that the user has valid data to be transmitted. This pin should be asserted only after the user has determined that the RFD line is active for a given frame cycle. When this pin is asserted, the information on the Data and Flag inputs is encoded and sent as a Data frame.
CAV*	12	I-ECL	**Control Word Available Input:** This active-low input tells the chip that the user is requesting a control word be transmitted. This pin should only be asserted after the user has determined the RFD line is active for a given frame cycle. When this pin is asserted, the information on the Data inputs is sent as a control frame. If CAV and DAV are asserted simultaneously, CAV takes precedence.
RFD	16	O-ECL	**Ready for Data:** Output to tell the user the Link is ready to transmit data. This pin is a retimed version of the ED input, which is driven by the Rx chip state machine controller.
STRBIN STRBIN*	66 65	I-H50	**Data Clock Input:** When EHCLKSEL is low, this input is phase locked and multiplied to generate the high speed serial clock. The chip expects a clock frequency which is equal to the input frame rate if MDFSEL (double frame mode) is low, and 1/2 the frame rate if MDFSEL is high. When EHCLKSEL is high, the PLL is bypassed, and STRBIN directly becomes the high speed serial clock. In all cases, STRBOUT is derived from the high speed serial clock, and the input data is latched in on the rising edge of STRBOUT.

Tx I/O Definition (cont'd.)

Name	Pin	Type	Signal
STRBOUT	6	O-ECL	**Frame-rate Data Clock Output:** This output is always a frame rate clock derived from STRBIN. Input data is latched on the rising edge of STRBOUT. With a buffer or pulled down with a 1 K resistor to V_{EE} and ac-coupled, this output is ideal for triggering an oscilloscope for examining the serial output eye pattern DOUT or LOUT.
DOUT DOUT*	56 55	O-BLL	**Normal Serial Data Output:** Output used when LOOPEN is not active. This output is a special *buffer line logic* driver which is a 50 Ω back-terminated ECL compatible output.
LOUT LOUT*	59 58	O-BLL	**Loop Back Serial Data Output:** Output used when LOOPEN is active. Typically, this output will be used to drive the LIN, LIN* inputs of the Rx chip.
LOOPEN	57	I-ECL	**Loop Back Control:** Input which controls whether the DOUT, DOUT* or the LOUT, LOUT* outputs are currently enabled. If active, LOUT, LOUT* are enabled. The unused output is powered down to reduce dissipation.
FLAGSEL	10	I-ECL	**Flat Bit Mode Select:** When this input is high, the extra FLAG bit input is sent as an extra transparent data bit. Otherwise, the FLAG input is ignored and the transmitted flag bit is internally alternated by the transmitter. The Rx chip can provide enhanced frame error detection by checking for strict alternation of the flag bit during data frames. The FLAGSEL input on the Rx chip should be set to the same value as the Tx FLAGSEL input.
M20SEL	9	I-ECL	**16 or 20 Bit Word Select:** When this signal is high, the link operates in 20 Bit data transmission mode. Otherwise, the link operates in 16 Bit mode.
MDFSEL	8	I-ECL	**Select Double Frame Mode:** When this signal is high, the PLL expects a 1/2 speed parallel clock at STRBIN. The chip then internally multiplies this clock and produces a full-rate parallel clock at STRBOUT. This feature is provided so that either a 40 bit or 32 bit word can be easily transmitted as two 20, or two 16 bit words. When MDFSEL is low, the PLL expects a full-rate parallel clock at STRBIN, and returns a locked replica of STRBIN on the STRBOUT pin. In both modes Data is latched on the rising edge of STRBOUT.
DIV0 DIV1	54 53	ECL	**VCO Divider Select:** These two pins program the VCO divider chain to operate at full speed, half speed, quarter speed, or one-eighth speed.
RST*	42	I-ECL	**Chip Reset:** This active-low pin initializes the internal chip registers. It should be asserted during power up for a minimum of 5 parallel-rate clock cycles to ensure a complete reset.
ED	14	I-ECL	**Enable Data:** This signal comes from the Rx chip state machine and is used to control the RFD output of the Tx chip. The state machine only allows data to be enabled when both sides of the link have established stable lock.

Tx I/O Definition (cont'd.)

Name	Pin	Type	Signal
FF	13	I-ECL	**Fill Frame Select:** When neither CAV or DAV is asserted, or when ED is false, fill frames are automatically transmitted to allow the Rx chip to maintain lock. The type of fill frame sent is determined by the state of this pin. FF0s are sent if low, and either FF1a or FF1b is sent if FF is high. The choice of FF1a or FF1b is determined by the state of the cumulative line DC balance.
LOCKED	7	O-ECL	**Loop In-lock Indication:** This signal indicates the lock status of the Tx PLL. A high value indicates lock. This signal is normally connected to the SMTRST1 reset input of the Rx state machine to force the link into the start-up state until the Tx PLL has locked. This signal may give multiple false-lock indications during the acquisition process, so should be debounced if it is used for any other purpose than to drive the Rx chip.
CAP0D CAP0S CAP1D CAP1S	1 1 68 68	C	**Loop Filter Capacitor:** A loop filter capacitor may be connected across the CAP0 and CAP1 inputs to increase the loop time constant. The packaged part contains a nominal capacitance internally so that under normal conditions no external capacitor is required.
INV	50	O-ECL	**Invert Signal:** A high value of INV implies that the current frame is being sent inverted to maintain long-term DC balance. With a buffer, or pulled down with a 1K resistor to V_{EE} and ac coupled, this signal is useful as an aid to analyzing the serial output stream with an oscilloscope.
TEMP	44	T	**Temperature Sense Diode:** Used during wafer and package test only. It should be left open otherwise.
HCLKON	64	I-ECL	**HCLK Power-down Control:** When this pin is de-asserted, the HCLK, HCLK* outputs are powered down to reduce power dissipation.
HCLK HCLK*	63 62	O-BLL	**High Speed Clock Monitor:** Used to monitor actual clock signal used to transmit the serial data. This signal will either be the divided VCO output, or the divided external clock input, depending on the value of the EHCLKSEL input.
EHCLKSEL	4	I-ECL	**EHCLK Enable:** When active, this input causes the STRBIN inputs to be used for the transmit serial clock, rather than the internal VCO clock. This is useful for generating extremely low jitter test signals, or for operating the link at speeds that are not within the VCO range. When the EHCLKSEL is active, it is necessary for the data source to take its clock from the link rather than the usual operation where the Link phase-locks onto the data source clock.
GND	60 51 34 17	S	**Ground:** Normally 0 volts. This ground is used for everything other than the noisy ECL outputs

Tx I/O Definition (cont'd.)

Name	Pin	Type	Signal
HGND	67	S	**High Speed Ground:** Normally 0 volts. This ground is used to provide a clean reference for STRBIN and STRBIN* inputs. For optimum impedance matching, it is suggested that the physical distance between this pin and the ground plane be minimized.
ECLGND	43 15 5	S	**ECL Ground:** Normally 0 volts. This ground is used for the ECL pad drivers. For best performance it is suggested that coupling of the noisy ECLGND to the clean GND and HGND grounds be minimized.
V_{EE}	52 35 18 2	S	**Power:** Normally -5 V ± 10%.

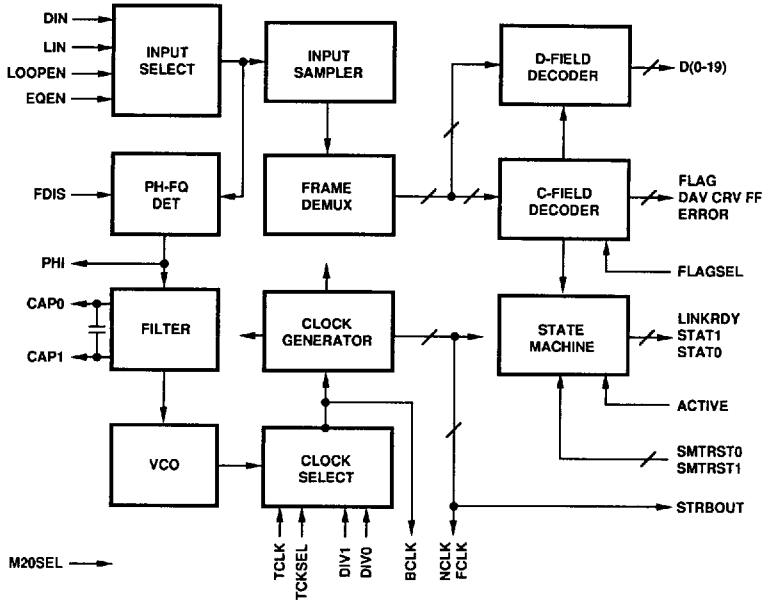


Figure 6. HDMP-1004 (Receiver) Block Diagram.

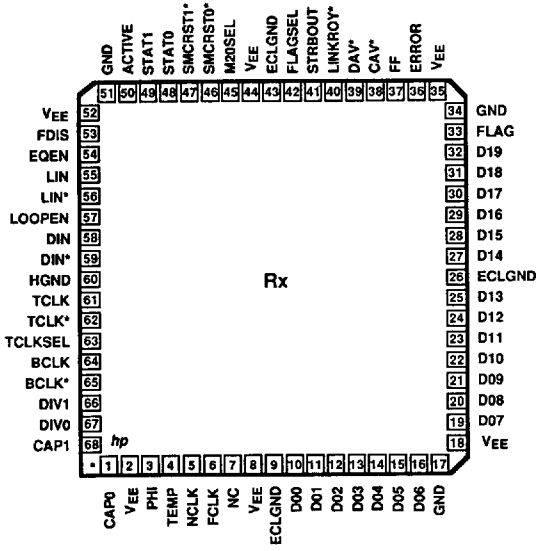


Figure 7. HDMP-1004 (Rx) Package Layout, Pin View.

Rx I/O Definition

Name	Pin	Type	Signal
DIN DIN*	58 59	I-H50	**Normal Serial Data Input:** This is the input used when LOOPEN is not active. When LOOPEN is high, the loop back data inputs LIN, LIN* are used instead. An optional cable equalizer may be enabled for the DIN, DIN* inputs by asserting EQEN.
LIN LIN*	55 56	I-H50	**Loop Back Serial Data Input:** Use this input when LOOPEN is active. Unlike the DIN, DIN* inputs, this input does not have a cable equalizer. In normal usage, this input will be connected to the Tx chip LOUT, LOUT* outputs. This allows the user to check the near-end functionality of the Tx and Rx pair independent of the transmission medium.
LOOPEN	57	I-ECL	**Loop Back Control:** When asserted, this signal causes the loop back inputs LIN, LIN* to be used instead of the normal data inputs DIN, DIN*.
EQEN	54	I-ECL	**Enable Input for Cable Equalization:** When asserted, this signal activates the cable equalization amplifier on the DIN, DIN* serial data inputs.

Rx I/O Definition (cont'd.)

Name	Pin	Type	Signal
D00 D01 D02 D03 D04 D05 D06 D07 D08 D09 D10 D11 D12 D13 D14 D15 D16 D17 D18 D19	10 11 12 13 14 15 16 19 20 21 22 23 24 25 27 28 29 30 31 32	O-ECL	**Data Outputs:** 20 Bit data is received and decoded when M20SEL is active; otherwise 16 bit data is decoded and the D16-D19 bits are undefined.
FLAG	33	O-ECL	**Flag Bit:** If both Tx and Rx have FLAGSEL asserted, this output indicates the value of the transmitted flag bit, then this received bit can be treated just like an extra data bit. If both Tx and Rx have FLAGSEL set to low, FLAG is used to differentiate the even frame from the odd frame in the line code.
LINKRDY*	40	O-ECL	**Link Ready Indicator:** This active-low output is a retimed version of the ACTIVE input. ACTIVE is normally driven by the Rx state machine output. LINKRDY then indicates that the startup sequence is complete and that the data and control indications are valid.
DAV*	39	O-ECL	**Data Available Output:** This active-low output indicates that the Rx chip data outputs are received Data frames. Data should be latched on the rising edge of STRBOUT. Note that during link startup, false data indications may be given. If the user is concerned about this possibility, then the DAV indication should be combined with the LINKRDY output before being used.
CAV*	38	O-ECL	**Control Frame Available Output:** This active-low output indicates that the Rx chip data outputs are receiving Control Frames. False CAV indications may be generated during link startup.
FF	37	O-ECL	**Fill Frame Status:** During a given STRBOUT clock cycle, if neither DAV, CAV, or ERROR are active, then the currently received frame is a Fill frame. The type of Fill frame received is indicated by the FF pin. If FF is low, then FF0 has been received. If FF is high, then either FF1a or FF1b has been received.
ERROR	36	O-ECL	**Received Data Error:** Asserted when a frame is received that does not correspond to either a *valid* Data, Control, or Fill frame encoding.When FLAGSEL is not active, the Rx chip also tests for strict alternation of flag bits during data frames. A flag bit alternation error will also cause an ERROR indication.

Rx I/O Definition (cont'd.)

Name	Pin	Type	Signal
STRBOUT	41	O-ECL	**Recovered Frame-rate Data Clock Output:** This output is the PLL recovered frame rate clock. D0-D19, FLAG, DAV CAV, FF, LINKRDY, and ERROR should all be latched on the rising edge of STRBOUT.
FLAGSEL	42	I-ECL	**Flag Bit Mode Select:** When this input is high, the extra FLAG bit output is effectively an extra transparent data bit. Otherwise, the FLAG bit is checked for alternation during data frames. Any break in strict alternation results in an ERROR indication to the user.
M20SEL	45	I-ECL	**16 or 20 Bit Word Select:** When this signal is high, the link operates in 20 Bit data reception mode. Otherwise, the link operates in 16 Bit mode and data outputs D16-D19 are undefined.
DIV0 DIV1	67 66	I-ECL	**VCO Divider Select:** These two pins program the VCO divider chain to operate at full speed, half speed, quarter speed or one-eighth speed.
FDIS	53	I-ECL	**Frequency Detector Disable Input:** When active, this input disables the Rx PLL Frequency detector and enables a phase detector. The Frequency detector is used during the start-up sequence to acquire wide-band lock on Fill Frames, but must be disabled prior to sending data patterns. This input is normally controlled by the Rx state machine.
ACTIVE	50	I-ECL	**Chip Enable:** This input is normally driven by the Rx state machine output. The ACTIVE signal is internally retimed by STRBOUT and presented to the user as the LINKRKDY signal. This is how the Rx state machine signals the user that the start-up sequence is complete.
SMCRST0* SMCRST1*	46 47	I-ECL	**State Machine Reset Inputs:** Each of these active-low input pins reset the Rx state machine to the initial start-up state. This initiates a complete PLL restart and handshake at both ends of the duplex link. Normally, SMCRST0* is connected to a power-up reset circuit or a host system reset signal. The SMCRST1* input is normally connected to the Tx LOCKED output. The LOCKED signal holds the state-machine in the start-up state until the Tx PLL is locked.
STAT0 STAT1	48 49	O-ECL	**State Machine Status Outputs:** These outputs indicate the current state-machine state. They are used to directly control the Tx ED, Tx FF, Rx FDIS, and Rx ACTIVE lines.
CAP0D CAP0S CAP1D CAP1S	1 1 68 68	C	**Loop Filter Capacitor:** A loop filter capacitor may be connected across the CAP0 and CAP1 inputs to increase the loop time constant. The packaged part contains a nominal capacitance internally so that under normal conditions no external capacitor is required. Each package pin is split into two die pads: suffixed "D" for drive and "S" for sense. This enables a four-point probe arrangement to be used to reduce noise in the loop.

Rx I/O Definition (cont'd.)

Name	Pin	Type	Signal
PHI	3	O-ECL	**Phase Detector Test Output:** The output from the phase/ frequency detector in the Rx PLL. When PHI is high, the VCO should increase frequency. If low, the VCO should decrease frequency.
NCLK	5	O-ECL	**Nibble Clock Monitor:** Leave unterminated in normal use.
FCLK	6	O-ECL	**Frame Clock Monitor:** Leave unterminated in normal use.
TEMP	4	T	**Temperature Sense Diode:** Used during wafer and package test only. It should be left open otherwise.
BCLK BCLK*	64 65	O-BLL	**VCO Monitor Output:** These pins provide access to the internal VCO clock.
TCLKSEL	63	I-ECL	**Enable Test Clock Input:** When this input is active, the TCLK, TCLK* inputs are used in place of the normal VCO signal. This feature is useful both for synchronous systems and for chip testing.
TCLK TCLK*	61 62	I-H50	**External VCO Replacement Test Clock:** When TCLKSEL is enabled, this input is used in place of the normal VCO signal, effectively disabling the PLL and allowing the user to provide an external retiming clock for testing.
GND	17 34 51	S	**Ground:** Normally 0 volts. This ground is used for all the core logic other than the output drivers.
HGND	60	S	**High Speed Ground:** Normally 0 volts. This ground is used to provide clean references for the high speed DIN, DIN*, LIN, LIN*, TCLK, TCLK* inputs.
ECLGND	9 26 43	S	**ECL Ground:** Normally 0 volts. This ground is used for the ECL pad drivers. For best performance it is suggested that coupling of the noisy ECLGND to the clean GND and HGND grounds be minimized.
V_{EE}	2 8 18 35 44 52	S	**Power:** Normally -5 V ± 10%
NC	5 6 7	B	**Pins Not Connected:** Pins that are not used, or are reserved for future use. No connection should be made to any of these signals to ensure compatibility with future releases.

HDMP-1002 (Tx) Timing

Figure 8 shows the Tx timing diagram. Under normal operation, the Tx PLL locks to the STRBIN input with an internal frame clock. This frame clock is buffered to form STRBOUT with a delay of ΔT_{strb}. For the case when MDFSEL is low, INFRMCLK is a phase locked version of STRBIN. If MDFSEL is high, it is assumed that STRBIN is a one half frame rate clock and INFRMCLK is twice the frequency of STRBIN. If EHCLKSEL is high, the Tx uses the external high-speed clock from STRBIN instead of its internal VCO, and generates the appropriate INFRMCLK from the STRBIN inputs. When M20SEL is high, INFRMCLK is 1/24th the frequency of HCLK. When M20SEL is low, INFRMCLK is 1/20th the frequency of HCLK.

The input signals, D0-D19, ED, FF, CAV*, DAV*, and FLAG are latched on the rising edge of INFRMCLK. These inputs must be valid for the set-up time (t_s) before the rising edge and for the hold time (t_h) after the rising edge of INFRMCLK.

The start of a frame in the high speed serial output occurs after a delay of (t_d) after the rising edge of INFRMCLK.

The LOCKED output will stay low for at least 2 frame rate clock cycles when lock is lost.

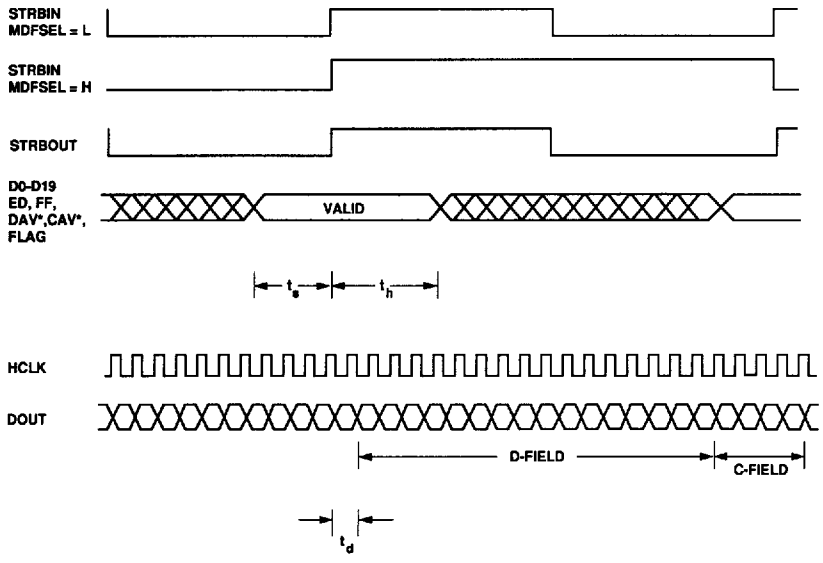


Figure 8. HDMP-1002 (Tx) Timing Diagram.

HDMP-1004 (Rx) Timing

Figure 9 is the Rx timing diagram when the internal phase-locked loop is in synchronization with the incoming serial data. When the PLL is locked, the BCLK's frequency is the same as the input data rate. The nibble clock, NCLK, is derived from the BCLK and a divide-by-4 divider. The size of the input data frame can be either 24 bits (6 nibbles) or 20 bits (5 nibbles), depending on the setting of M20SEL. Whatever the frame size, the FCLK rising edge is located at the frame's boundary, while the falling edge is at the frame's center. STRBOUT is an inverted version of FCLK.

In Figure 9, the Synchronous Outputs are the Rx's output signals clocked by STRBOUT. They are LINKRDY*, FLAG, DAV, CAV, FF, ERROR, and D00-D19. The Synchronous Outputs are updated for every data frame, and changed at the falling edge of STRBOUT. There is a delay of two frames between the serial input and the Synchronous Outputs. As for the state machine status outputs, STATI and STATO, they are also changed upon the STRBOUT's falling edge, but are only updated once in 128 frames.

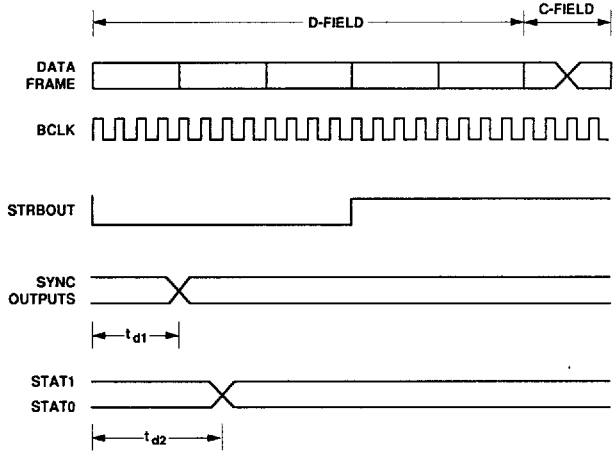


Figure 9. HDMP-1004 (Rx) Timing Diagram.

Line Code Description

The HDMP-1000 line code, Conditional Invert Master Transition (CIMT), is illustrated in Figure 10. The CIMT line code uses three types of frames; Data frames, Control frames, and Fill frames. Fill frames are internally generated by the Tx chip for use during link start up and when there is no input from the user. Each frame consists of a Data Field (D-Field) followed by a Coding Field (C-Field). The D-Field can be either 16 bit or 20-bits wide, depending on link configuration. The C-Field has a master transition which serves as a fixed timing reference for the receivers clock recovery circuit. Users can send arbitrary data carried by Data or Control Frames. The dc balance of the line code is automatically enforced by the Tx. Fill frames have a single rising edge at the master transition which is used for clock recovery and frame synchronization at the receiver.

Detailed coding schemes are described in the following subsections. All the tables given in this section show data bits in the same configuration as a scope display. In other words, the leftmost bit in each table is the first bit to be transmitted in time, while the rightmost bit is the last bit to be transmitted.

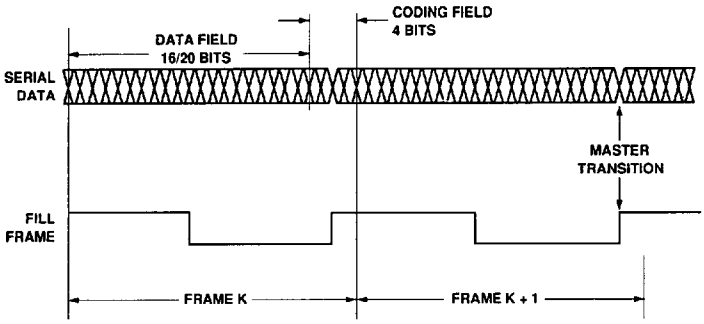


Figure 10. HDMP-1000 (Tx/Rx Pair) Line Code.

Data Frame Codes

When not in FLAGSEL mode, the FLAG bit is not user controllable and is alternately sent as 0 and 1 by the Tx chip during data frames to provide enhanced error detection. Control and Fill frames do not cause toggling between even and odd frames to occur (The FLAG bit is not available during control frames). The receiver performs a differential detection to make sure that every data frame received is the opposite pattern from the previous frame. If a break in the strict alternation is observed, a frame error is flagged by asserting the Rx ERROR output. This pattern detection makes it impossible for a static input data pattern to generate an undetectable false lock point in the transmitted data stream. The detection also reduces the probability that the loop could lock onto random data at a point away from the true master transition for any significant time before it would be detected as a false lock. This mode can detect all single-bit errors in the C-field (non-data bit fields) of the frame.

When the chip is in FLAGSEL mode, the extra FLAG bit is freely user definable as an extra data bit. This provides a 17th bit in 16 bit mode, and a 21st bit in 20 bit mode. The probability of undetected false lock is higher, but the users (e.g., SCI-FI) that need the extra bit can detect false lock at a higher level of the network protocol with CRCs, etc. If the higher level protocols consistently receive wrong data, they can initiate a link restart by resetting the Rx state machine.

HDMP-1002 (Tx), HDMP-1004 (Rx)

Operating Modes

M20SEL	FLAGSEL	Description
0	0	16 bit data plus EO checking
0	1	16 bit data plus $\overline{\text{FLAG}}$
1	0	20 bit data plus EO checking
1	1	20 bit data plus $\overline{\text{FLAG}}$

HDMP-1002 (Tx), HDMP-1004 (Rx)

Data Frame Structure
M20SEL Not Asserted (16 bit data mode)

Data Status	Flag Bit	D-Field	C-Field
True	0	$D_0 - D_{15}$	1101
Inverted	0	$\overline{D_0 - D_{15}}$	0010
True	1	$D_0 - D_{15}$	1011
Inverted	1	$\overline{D_0 - D_{15}}$	0100

HDMP-1002 (Tx), HDMP-1004 (Rx)

Data Frame Structure
M20SEL Asserted (20 bit data mode)

Data Status	Flag Bit	D-Field	C-Field
True	0	$D_0 - D_{19}$	1101
Inverted	0	$\overline{D_0 - D_{19}}$	0010
True	1	$D_0 - D_{19}$	1011
Inverted	1	$\overline{D_0 - D_{19}}$	0100

Control Frame Codes

There are 2^{18} control words provided in 20 bit mode. If the user desires to send a control word, his lower 9 bits $(D_0\text{-}D_8)$ are sent as bits D0-D8 of the D-Field. The user's next 9 bits $(D_9\text{-}D_{17})$ are sent as bits D11-D19 of the D-Field. The control frame is either inverted or not inverted as needed to maintain balance, with the coding bits 0011 used to indicate true control, and the bits 1100 used to indicate complement control. The bits D9 and D10 are always forced to 0 1 for true control frames and 1 0 for complement control frames. These middle bits are used to distinguish true control frames from fill frames, which always have the middle bits set to either 00, 11, or 10. Similarly, there are 2^{14} control words provided in 16 bit mode.

HDMP-1002 (Tx), HDMP-1004 (Rx)

Control Frame Structure
M20SEL Not Asserted (16 bit mode)

D-Field				C-Field			
D0 - D6	D7	D8	D9 - D15	C0	C1	C2	C3
$D_0 - D_6$	0	1	$D_7 - D_{13}$	0	0	1	1
$\overline{D_0 - D_6}$	1	0	$\overline{D_7 - D_{13}}$	1	1	0	0

HDMP-1002 (Tx), HDMP-1004 (Rx)

Control Frame Structure
M20SEL Asserted (20 bit mode)

D-Field				C-Field			
D0 - D8	D9	D10	D11 - D19	C0	C1	C2	C3
$D_0 - D_8$	0	1	$D_9 - D_{17}$	0	0	1	1
$\overline{D_0 - D_8}$	1	0	$\overline{D_9 - D_{17}}$	1	1	0	0

Fill Frame Codes

Two logical fill frames are provided: FF0 and FF1. FF0 is physically a 50% duty cycle wave form with its sole rising edge occurring between C1 and C2. Logical FF1 toggles between two different physical codes, the first of which advances the falling edge of FF0 by one bit, the second of which retards the falling edge of FF0 by one bit. Two logical fill frame types are required for link start up in duplex mode.

HDMP-1002 (Tx), HDMP-1004 (Rx)

Fill Frame Structure
M20SEL Not Asserted (16 bit mode)

Fill Frame	D-Field			C-Field
0	1111111	10	0000000	0011
1a	1111111	11	0000000	0011
1b	1111111	00	0000000	0011

HDMP-1002 (Tx), HDMP-1004 (Rx)

Fill Frame Structure
M20SEL Asserted (20 bit mode)

Fill Frame	D-Field			C-Field
0	111111111	10	000000000	0011
1a	111111111	11	000000000	0011
1b	111111111	00	000000000	0011

HDMP-1004 (Rx)

Detectable Error States
M20SEL Not Asserted (16 bit mode)

D-Field			C-Field
xxxxxxx	xx	xxxxxxx	x00x
xxxxxxx	xx	xxxxxxx	x11x
xxxxxxx	0x	xxxxxxx	1100
xxxxxxx	11	xxxxxxx	1100
xxxxxxx	xx	xxxxxxx	1010
xxxxxxx	xx	xxxxxxx	0101

HDMP-1004 (Rx)

Detectable Error States
M20SEL Asserted (20 bit mode)

D-Field			C-Field
xxxxxxxxx	xx	xxxxxxxxx	x00x
xxxxxxxxx	xx	xxxxxxxxx	x11x
xxxxxxxxx	0x	xxxxxxxxx	1100
xxxxxxxxx	11	xxxxxxxxx	1100
xxxxxxxxx	xx	xxxxxxxxx	1010
		xxxxxxxxx	0101

Tx Operation Principles

The HDMP-1002 (Tx) is implemented in a high performance silicon bipolar process. The Tx performs the following functions for link operation:

- Phase lock to frame rate clock
- Clock multiplication
- Frame Encoding
- Multiplexing

In normal operation, the Tx phase locks to a user supplied frame rate clock and multiplies the frequency to produce the high speed serial clock. When locked, the Tx indicates that it is locked by asserting the LOCKED output. When the ED input is asserted, the Tx asserts the RFD signal indicating that it is now ready to transmit data or control frames.

The Tx can accept either 16 or 17 bit data and produce a 20 bit frame. It also can accept 20 or 21 bit data and produce a 24 bit frame. Similarly, either 14 bit or 18 bit control words can be transmitted in a 20 bit or 24 bit frame respectively.

Tx Encoding

A simplified block diagram of the transmitter is shown in Figure 4. The PLL/Clock Generator Block locks onto the incoming frame rate (or one-half frame rate) clock and multiplies it up to the serial clock rate. It also generates all the internal clock signals required on the Tx chip.

The data inputs, D0-D19, as well as the control signals; ED, FF, DAV*, CAV*, and FLAG are latched in on the rising edge of the frame rate clock. The data field is then encoded depending on the state of the control signals. At the same time, the coding field is generated. At this point, the entire frame has been constructed in parallel form and its sign is determined. This frame sign is compared with the accumulated sign of previously transmitted bits to decide whether to invert the frame. If the sign of the current frame is the same as the sign of the previously transmitted bits, then the frame is inverted. If the signs are opposite, the frame is not inverted. No inversion is performed if the frame is a fill frame.

The Output Select block allows the user to select between two sets of differential high speed serial outputs. This is useful for loop back testing. If LOOPEN is high, LOUT is enabled and DOUT is disabled. If LOOPEN is low, DOUT is enabled and LOUT is disabled.

The active-low RST* input resets the internal registers to a balanced state. This pin should be held low for at least five frame rate clock cycles to ensure a complete reset.

The Data Field and Control Field are encoded depending on ED, FF, DAV*, CAV*, FLAG, FLAGSEL, M20SEL as well as two internally generated signals, O/E and ACCMSB.

When FLAGSEL is high, O/E is equivalent to FLAG. This is equivalent to adding an additional bit to the data field. When FLAGSEL is low, O/E alternates between high and low for data frames. This allows the link to perform more extensive error detection when the extra bit is unused.

ACCMSB is the sign of the previously transmitted data. This is used to determine which type of FF1 should be sent. When ACCMSB is low, FF1a is sent and when ACCMSB is high, FF1b is sent. This effectively drives the accumulated offset of transmitted bits back toward the balanced state.

Tx Phase-Locked Loop

The block diagram of the transmitter phase-locked loop is shown in Figure 11. It consists of a sequential frequency detector, loop filter, VCO, clock generation circuitry and a lock indicator. The outputs of the frequency detector pass through a charge pump filter that controls the center frequency of the VCO. These outputs also go to the VCO directly to effectively add a zero in the loop response. An external high-speed clock can be used instead of the VCO clock. This is accomplished by applying a high signal to EHCLKSEL and a differential clock to STRBIN.

One of four frequency bands may be selected by applying appropriate inputs to DIV0 and DIV1. The VCO or STRBIN frequency is divided by N, where N is 1, 2, 4 or 8 corresponding to the binary number represented by DIV1, DIV0. This divided version of the VCO clock or STRBIN is used as the serial rate clock and is available as a differential signal at the HCLK output.

A clock generator block creates all the clock signals required for the chip. Depending on M20SEL, STRBOUT is either HCLK/20 or HCLK/24. If MDFSEL is low, then

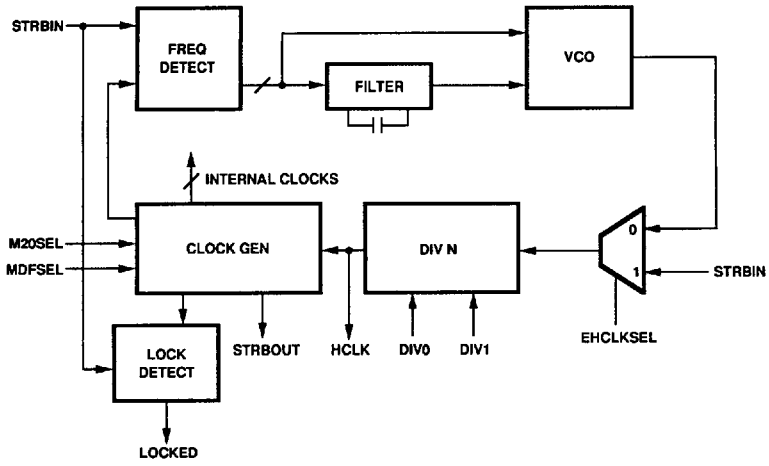


Figure 11. HDMP-1002 (Tx) Phase-Locked Loop.

STRBOUT is a phase-locked version of STRBIN. If MDFSEL is high, STRBOUT is twice the frequency of STRBIN.

The lock detect circuit samples STRBIN with phase shifted versions of STRBOUT. If the samples are not the proper values, the LOCKED signal goes low and stays low for at least two frames.

Rx Operation Principles

The HDMP-1004 (Rx) is monolithically implemented in a high performance 25 GHz f_t bipolar process. When properly configured, the Rx can accept 20B/24B CIMT line code frames, and then output parallel 16B/17B/20B/21B Data Words or 14B/18B Control Words. The Rx provides the following functions for link operation:

- Clock recovery
- Frame synchronization
- Data recovery
- Demultiplexing
- Frame decoding
- Frame error detection
- Link state control

Rx Encoding

Figure 6 shows a simplified block diagram of the receiver. The data path consists of an Input Select, an Input Sampler, a Frame Demultiplexer, a Coding Field (C-Field) Decoder, and a Data Field (D-Field) Decoder. An on-chip phase-locked loop (PLL) is used to extract timing reference from the serial input (DIN or LIN). The PLL includes a Phase-Frequency Detector, a Loop Filter, and a variable-frequency oscillator (VCO). All the Rx internal clock signals are generated from a Clock Generator. The Clock Generator can be driven either by the internal VCO or an external signal, TCLK, depending on the Clock Select configuration.

Integrated on the chip is a Link-Control State Machine for link status monitoring and link startup. Figure 12 shows the details of the Input Selector. The Input Selector chooses either the nominal serial data (DIN) or the loop back (LIN) signal for the Input Sampler's input. If loop back enable (LOOPEN) is asserted, the LIN input is selected. Included in the Input Selector is cable equalization circuitry. When coaxial cable is used as the transmission media, by setting EQEN=1 (enable equalization), the equalization circuitry is in the DIN signal path and provides fixed compensation for high-frequency cable loss.

The Data Field of the CIMT line code can be either 16-bits or 20-bits wide. The width selection for the Rx is made by setting the input pin M20SEL (Figure 6). If M20SEL = 1, then the Rx is configured to accept serial input with 20-bit data field (24 bits per frame). When M20SEL = 0, 16-bit data field is selected.

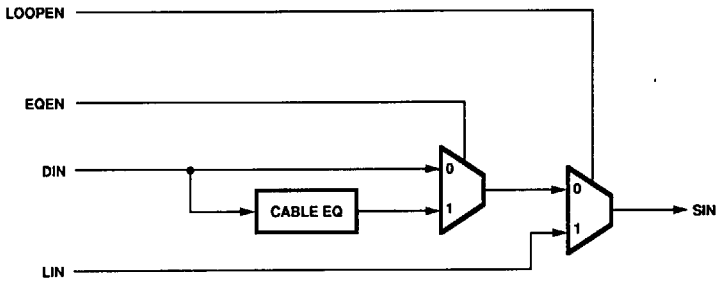


Figure 12. HDMP-1004 (Rx) Input Selector.

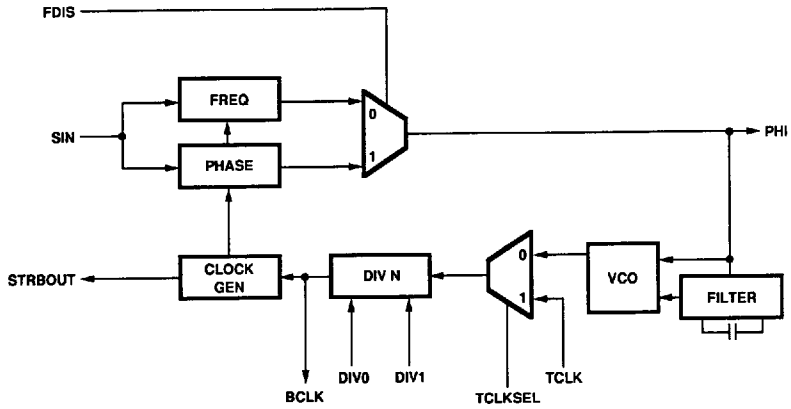
HDMP-1004 (Rx) Phase-Locked Loop

A more detailed block diagram for the Rx phase-locked loop (PLL) is shown in Figure 13. In the PLL, the phase of the serial input, SIN, is compared with synchronizing signals from the internal clock generator, using either a phase detector or a frequency detector. The frequency detector disable signal, FDIS, selects which detector to use. If synchronization in a link has yet to be established, the HDMP-1002 (Tx) should send out Fill Frame 0 (FF0) or Fill Frame 1 (FF1) to the remote Rx. By setting FDIS=0, the Rx uses the frequency detector to align its internal clock with the rising edge of FF0/FF1. Once this is accomplished, FDIS can be set to 1, then the PLL uses only the phase detector for synchronization adjustment and the Rx is ready to accept data. Due to the narrow frequency acquisition range of the phase detector, the frequency detector is used for internal frequency acquisition. The frequency detector, however, can only work with FF0 and FF1 and it then is necessary for the PLL to select the phase detector (by setting FDIS=1) before receiving any random data.

The output of the phase-frequency detector is externally available through pin PHI. An external clock source can also be used (through pin TCLK) by setting TCLKSEL=1. To broaden the usable frequency range of the chip, there is a programmable divider before the clock generator. The VCO or TCLK frequency can be divided by 1, 2, 4, 8 by setting DIV1, DIV0 = 00, 01, 10, 11 (see Operating Rate Tables).

HDMP-1004 (Rx) Decoding

In Figure 6, the frame demultiplexer de-serializes the recovered serial data from the Input Sampler, and outputs the resulting parallel data one frame at a time. Every frame is composed of a 16-bit or 20-bit



e-Locked Loop.

Data Field (D-Field) and a 4-bit Coding Field (C-Field). The C-Field, C0-C3, together with the two center bits of the D-Field (D9 and D10 for 20 bit mode, D7 and D8 for 16 bit mode) are then decoded by the C-Field decoder to determine the content of the frame. The D-Field decoder is controlled by the outputs of the C-Field decoder. If an inverted Data Frame or Control Frame is detected, the D-Field decoder will automatically invert the D-Field data. If a Control Frame is detected, the D-Field decoder will shift the bottom half of the D-Field so that the outputs are at pin D_0 - D_{17} (if M20SEL = 1) or at pin D_0 - D_{13} (if M20SEL = 0). A data Frame is detected by the receiver when DAV = 1. A control Frame is detected by the receiver if CAV = 1. A Fill Frame is detected by the receiver if DAV = 0 and CAV = 0.

The C-Field decoder will set iERR = 1 when it detects an error. The internal error bit (iERR) is combined with the internal flag bit (iFLAG) and the flag-bit mode-select signal (FLAGSEL) to produce the externally available error (ERROR) and flag (FLAG) bits. If FLAGSEL = 1, the FLAG bit can be used as an extra data bit.

- ERROR=iERR.
- FLAG=iFLAG.
- If a Fill Frame is detected, then FLAG=0.
- If a Control Frame is detected, FLAG should be ignored.

If FLAGSEL = 0, the serial input is assumed to consist of alternating even frames (iFLAG = 0) and odd frames (iFLAG = 1).

- If iERR=1, then ERROR=1.
- If a Fill Frame is detected, then FLAG=0.
- If a Data Frame is detected, then FLAG=iFLAG, and iFLAG should alternate between 0 and 1, starting with 0 and ending with 1; otherwise, ERROR=1.
- If a Control Frame is detected, then FLAG automatically alternates between 0 and 1, starting with 0.

The even or odd feature allows a 32/40-bit wide data word to be transmitted through the link. A 2:1 multiplexer and a 1:2 demultiplexer are required. FLAG is used to synchronize the even and odd frames. Note, both Data and Control Frames can be transmitted as even/odd pairs, but only Data Frames can be detected for out of order errors.

HDMP-1004 (Rx) Link-Control State Machine Operation Principle

The link-control state machine (SMC) on the Rx chip provides a link handshake protocol enabling the duplex link to transition from frequency acquisition and training mode into data mode.

The HDMP-1000 Tx/Rx link uses an explicit frequency acquisition mode at startup that operates on a square-wave training sequence. This makes it possible to use a VCO with a very wide tuning range yet avoid the harmonic false lock problems associated with other circuits of this type.

Using the SMC, a full duplex data channel can be implemented without additional controller or hardware.

The State Machine Handshake Protocol

Figure 1 shows a simplified block diagram of the HDMP-1000 data channel configured for full duplex operation. Two HDMP-1000 chipsets are required to perform the handshake in parallel. There are three states that the link must go through to complete the link startup process:

State 0: Frequency Acquisition

State 1: Waiting for Peer

State 2: Sending Data

Each side of the link decides which of the three states that it should be in. The decision is based on its own memory and the type of frame that it is currently receiving from the other side of the link.

Considering only the local port of the link, we have a transmitter (Tx), a receiver (Rx), and a state machine controller (SMC). In practice, the SMC entity, although logically distinct, is implemented on the same die as the Rx chip. The SMC monitors the data frame status indicators (ERROR, DAV, CAV, FF) from the Rx, and is able to force (or

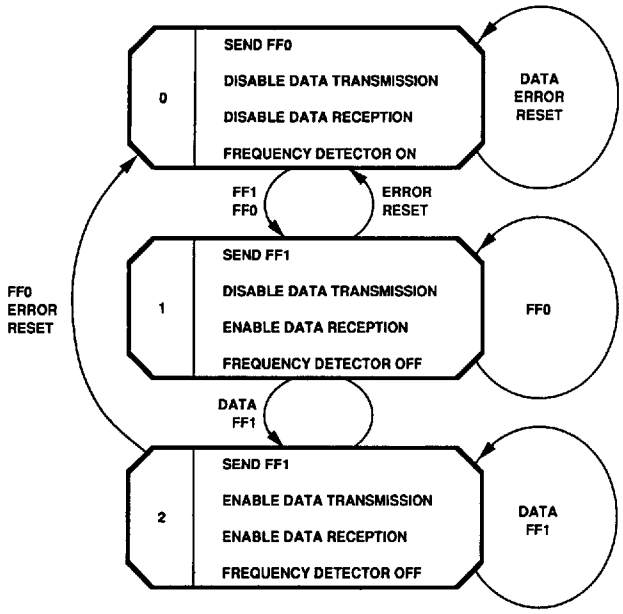


Figure 14. HDMP-1004 (Rx) State Machine State Diagram.

control) various characteristics of the Tx and the Rx chips. The Tx chip has the following controllable features:

- It can be forced to send a Fill Frame using the ED input.
- The type of Fill Frame sent can be controlled using the FF input.

The Rx Chip has the following controllable features:

- It can be in Frequency acquisition or Phase-lock/Data reception mode depending on the state of the FDIS input.
- It can be enabled for data reception or set in a mode in which data frames are ignored depending on the ACTIVE input.

The Rx chip can distinguish frames. It can communicate the frame type to the SMC. The various frame types are:

- Fill Frame 0, (FF0)
- Fill Frame 1 a/b, (FF1)
- Data/Control frames (Data)
- Error frames (ERROR)

The SMC can be reset by either the SMCRST0* or SMCRST1* inputs. Usually one of these inputs is used for power-on reset, and the other is connected to the Tx LOCKED output.

This holds the SMC in state 0 until the transmitter PLL has locked.

Figure 14 shows the state diagram of the SMC. The SMC is debounced by allowing state transitions to be made only after at least 2 consecutive frames give the same indication. This prevents single bit errors from causing false state transitions. In addition to this debouncing mechanism, when two consecutive ERROR or Resets occur, a timer is enabled forcing the SMC into state zero for 128 frames. Any transition out of this initial state can only occur after the link has been error-free for 128 frames. This prevents false transitions from being made during the bit-slipping that occurs in the initial frequency acquisition of both the Tx and Rx PLLs.

When the local port is in State 0, it is in the reset state. Both local Tx and Rx parallel interfaces are disabled. The local Tx transmits FF0 continuously, and the Rx PLL is in the frequency detection mode. When the local Rx is phase-locked to the remote Tx it transitions to State 1. The local Tx transmits FF1 to acknowledge the phase-locked condition (its parallel input is still disabled). The local Rx PLL is in the phase detection mode and its parallel output is enabled. When in State 2, the two-way synchronization between the local port and the remote port is established. Both the local Tx and Rx parallel interfaces are enabled, and the local Rx PLL is in the phase detection mode. Parallel data can be sent by the local Tx, and at the same time, received by the local Rx.

The Rx chip has the state machine logic built in. The SMC has two status outputs, STAT0 and STAT1, that control the various features of the two chips depending on the current state.

SMC Output (STAT0 and STAT1) at Current Link State

State	STAT0	STAT1
0	0	0
1	0	1
2	1	1

The Tx inputs that need to be controlled are FF and ED. The Rx inputs that need to be controlled are FDIS and ACTIVE. To control the chips as shown in the state diagram of Figure 14, these inputs need to be driven as follows:

State	Tx FF	Tx ED	Rx FDIS	Rx ACTIVE
0	0	0	0	0
1	1	0	1	1
2	1	1	1	1

To control the link as shown above the following interchip connections must be made (Figure 15):

- Tx FF is driven by STAT1
- Tx ED is driven by STAT0
- Rx FDIS is driven by STAT1
- Rx ACTIVE is driven by STAT1
- Tx RST and Rx SMCRST0 are driven by a power-on, or user, reset circuit.

Link Configuration Examples

This section shows some application examples using the HDMP-1000 chipset. Refer to Section 2 (I/O Definition) for detailed circuit-level interconnection. For example, the chipset's ECL output drivers have weak driving power; hence, external buffers are required for large loading.

Figure 15 is the schematic for a full-duplex port. The network start-up protocol is provided by the Rx internal state-machine controller, and is transparent to the host. The handshaking between the host and the chipset is provided by the RFD and LINKRDY* signals. The host interface registers are clocked by the falling edges of the STRBOUT from the Tx and the Rx. The user has to make sure that M20SEL, FLAGSEL, DIV0, and DIV1 have the same setting on both the Tx and Rx. The word width of the parallel data from the host can be either 16 bits if M20SEL = 0, or 20 bits if M20SEL=1. Also, the FLAG bit can be used as an additional bit by setting FLAGSEL = 1. In the last case, the parallel data word width is either 17 bits or 21 bits. The local loopback test can be enabled by setting LOOPEN high.

Figure 16 shows how to use the FLAG bit and MDFSEL to transfer parallel data with 36-bit or 40-bit word width. Each data word is multiplexed and carried by two consecutive CIMT frames called even and odd frames. The FLAGSEL is set to high, and the FLAG bit is used to designate the even/odd frame. For the Tx, the MDFSEL is set to high so that the frequency of STRBOUT is twice that of STRBIN. The flag signal to the Tx is generated from STRBIN and STRBOUT. The Tx interface registers are clocked by the Tx FLAG signal. On the Rx side, the FLAG output is retimed by STRBOUT to generate RCLK, which is used to demultiplex the data output. Note that the Rx interface registers for LINKRDY*, ERROR, DAV*, CAV*, and FF are clocked by STRBOUT instead of RCLK; this is due to the fact that the FLAG is reset to "0" when receiving FF0.

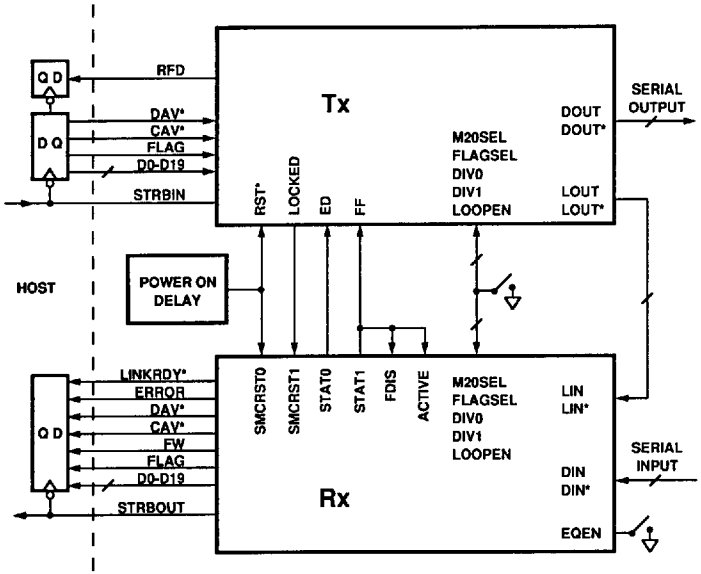
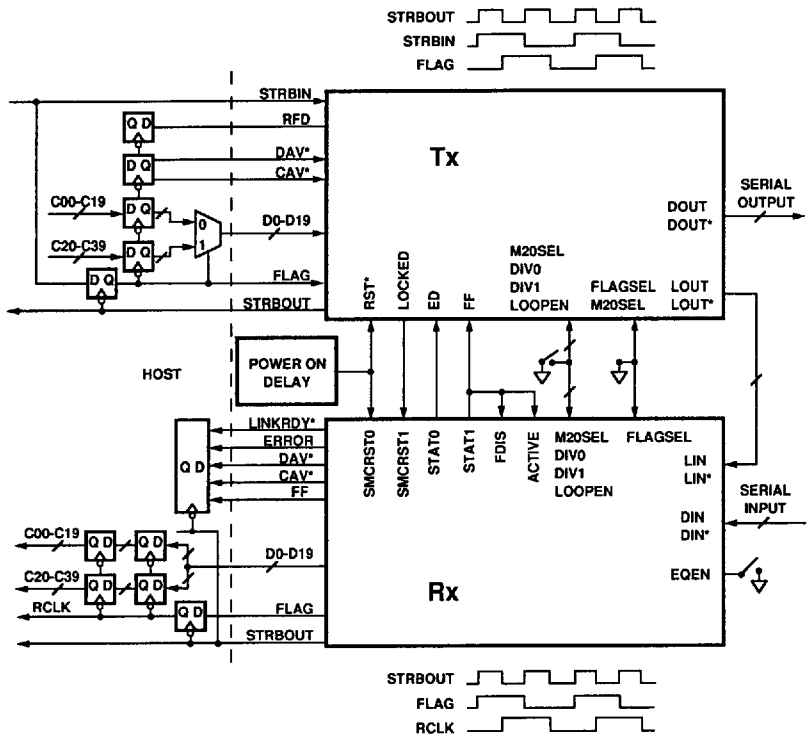


Figure 15. A Full-Duplex Port.



Frame Port.

Although the HDMP-1000 chipset is designed for full-duplex applications, it is possible to configure the chipset for simplex applications as shown in Figure 17. Although the Tx has no knowledge of the status of the remote Rx, the Tx host can periodically allocate a time slot to transmit FF1. This is shown as a negative pulse to the Tx ED input in Figure 17. If the remote Rx is unlocked, it can wait for the next sequence of FF1 to regain synchronization. The length of each FF1 sequence must be longer than the Rx frequency acquisition time (approximately 2 msec). Note that the Rx internal state-machine controller can also be used in this simplex application; no additional controller is necessary.

Surface Mount Assembly Recommendations

The package is designed to be surface mounted with the lid facing the board (lid acts as bottom of the package or pin view facing the board). It is recommended that the leads be formed into a "Gull-Wing" configuration prior to surface mounting. The recommended package stand-off (distance between "bottom" of package to the board surface) is 30 mils. It is also recommended that the leads be solder (Sn/Pb) coated prior to surface mounting. The lead material is Alloy 42. Note: Packages are shipped with unformed leads in carriers.

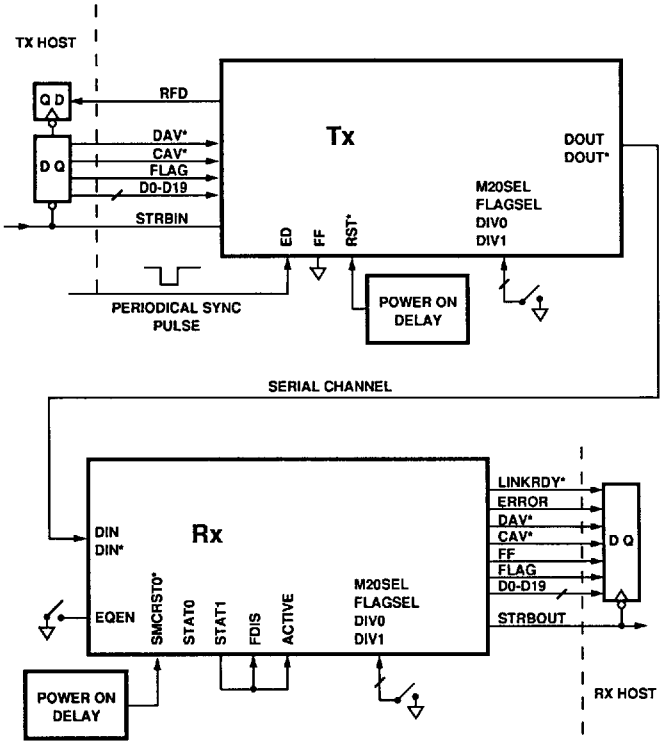
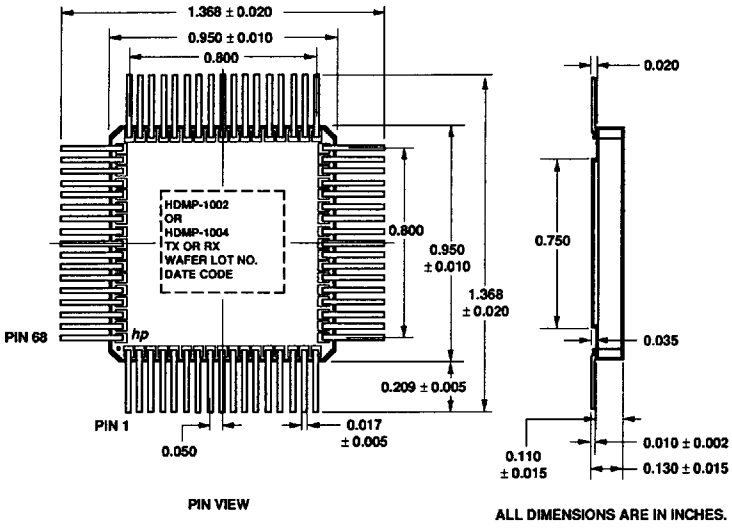


Figure 17. Simplex Configuration.

Outline

68 Lead Ceramic Quad Flatpack



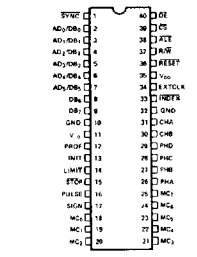
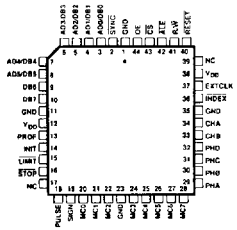
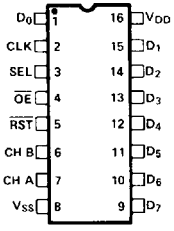
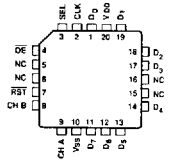
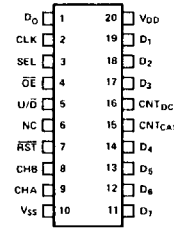
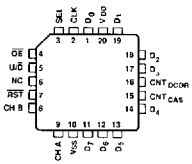
Evaluation Board Ordering Information

A Gigabit Rate Transmit Receive Chipset Evaluation Board may be ordered through your local HP Components Representative or authorized HP Components distributor.

Designer Kit

Part Number	Kit Description
HDMP-100K	Evaluation board for the Gigabit Rate Transmit Receive Chipset, and literature

Motion Control ICS – HCTL-XXXX Series

Package Outline Drawing	Part No.	Package	Description	Page No.
	HCTL-1100	PDIP	CMOS General Purpose Motion Control IC	1-104
	HCTL-1100 OPT PLC	PLCC	CMOS General Purpose Motion Control IC	
	HCTL-2000	PDIP	CMOS Quadrature Decoder/Counter IC, 12-bit Counter	1-86
	HCTL-2016	PDIP	CMOS Quadrature Decoder/Counter IC, 16-bit Counter	
	*New* HCTL-2016 OPT PLC	PLCC	CMOS Quadrature Decoder/Counter IC, 16-bit Counter	1-102
	HCTL-2020	PDIP	CMOS Quadrature Decoder/Counter IC, 16-bit Counter, Quadrature Decoder Output Signals, Cascade Output Signals	1-86
	*New* HCTL-2020 OPT PLC	PLCC	CMOS Quadrature Decoder/Counter IC, 16-bit Counter, Quadrature Decoder Output Signals, Cascade Output Signals	1-102

Accessories for Encoders and Encoder Modules

Package Outline Drawing	Part No.	Description	Page No.
	HEDS-8902	4-wire connector with 15.5 cm (6.1 in.) flying leads. Locks into HEDS-5500 and HEDS-5600 2 channel encoders. Also fits HEDS-9000, HEDS-9100, and HEDS-9200 2 channel encoder modules.	1-61 1-22 1-28
	HEDS-8903	5-wire connector with 15.5 cm (6.1 in.) flying leads. Locks into HEDS-5540 and HEDS-5640 three channel encoders. Also fits HEDS-9040 and HEDS-9140 three channel encoder modules.	1-61 1-32
	HEDS-8905	Alignment Tool for HEDS-9140	1-32
	HEDS-8906	Alignment Tool for HEDS-9040	1-32
	HEDS-8901	Gap Setting shown for film codewheels	1-51
	HEDS-8932	Gap Setting shown for glass codewheels	1-51
	HEDS-8910 OPT 0 □□	Alignment Tool for HEDS-5540/5545 and HEDS-5640/5645. Order in appropriate shaft size.	1-61