

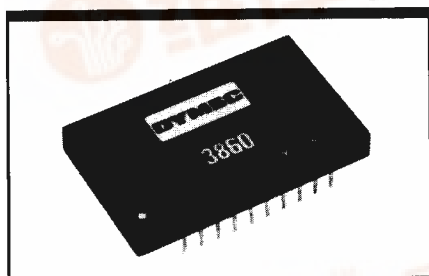
DYMEC

A Subsidiary of
SILICON TRANSISTOR CORP.

MODEL:

3860

Signal Conditioning 10MHz V/F Converter



Description

The **3860** is a high performance, precision 10MHz full scale voltage-to-frequency converter with integral low noise, user-configurable high input impedance buffer and gain stage amplifiers. Each functional block may be used independently or in combination to obtain a signal conditioning and V/F converter subsystem. By integrating a high performance amplifier and V/F in the same package, users can

quickly implement a front-end/converter design with guaranteed end-to-end specifications, tailored to their application requirements, and save design time and pc board space, reduce potential ground loops and improve overall performance.

The input buffer stage provides an input impedance of 10^{12} ohms. The separate inverting gain stage offers user programmable gains by adding a pair of precision resistors. When used in combination, the input buffer/gain stage offer an extremely stable amplifier chain.

The V/F converter itself accepts a $-100\mu\text{V}$ to -10V full scale analog signal which is converted to an output frequency proportional to the input signal and 10MHz, within $\pm 0.05\%$ linearity. Buffered complementary TTL-compatible frequency outputs are provided that will drive

FEATURES

- ☐ **Integral High Input Impedance Buffer**
 10^{12} ohms
- ☐ **Integral User-Programmable Inverting Gain Stage**
Two-resistor Programming
- ☐ **Wide Dynamic Range**
 $10,000,000:1$
 $>142\text{dB}$
- ☐ **Precision V/F Converter**
 $\pm 0.05\%$ Linearity
- ☐ **Excellent Stability**
 $10\mu\text{V}/^\circ\text{C}$ offset
 $60\text{ppm}/^\circ\text{C}$ gain
- ☐ **Complementary Frequency Outputs**
TTL/CMOS Compatible
- ☐ **Small Size**
24-pin Double-width DIL Package
- ☐ **Low Power**
 $<1.25\text{W}$

APPLICATIONS

- ☐ Precision Integration
- ☐ Analytical Instrumentation
- ☐ Medical Instrumentation
- ☐ Weighing Systems
- ☐ Data Recording
- ☐ Data Transmission

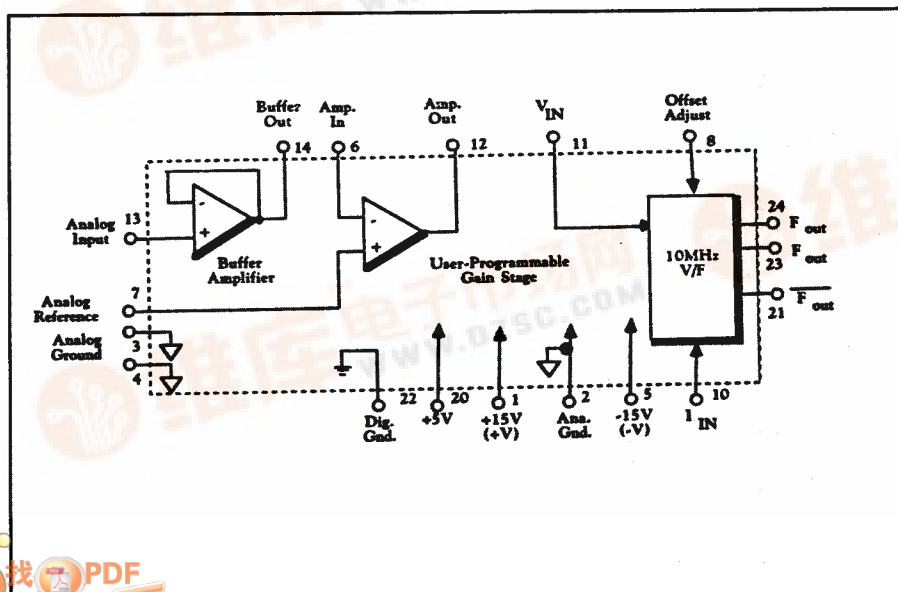


Figure 1. 3860 Block Diagram

Specifications

All Specifications Guaranteed at 25°C Unless Otherwise Noted

V/F CONVERTER

ANALOG INPUT

Input Range

-100 μ V to -10V

Overrange

5% minimum

Configuration

Single-ended

Impedance

6K Ω nominal

Offset Voltage

± 7 mV typical, ± 10 mV maximum;
adjustable to zero

Overvoltage Protection

$\pm V_S$ without damage

TRANSFER CHARACTERISTICS

Full Scale Frequency Output (Fout)

10.000MHz; $\pm 5\%$ overrange minimum

V/F Transfer Characteristic

10MHz(Vin/10V)

Gain Error

$\pm 1\%$, trimmable to zero

Non-Linearity

$\pm 0.05\%$ FS, $\pm 0.05\%$ of input, maximum

Full Scale Step Response

2 cycles of new frequency, plus 5 μ s;
to $\pm 0.01\%$

Overload Recovery

12 cycles of new frequency

STABILITY

(Exclusive of external components)

Gain - Tempco

± 60 ppm/ $^{\circ}$ C typical, ± 100 ppm/ $^{\circ}$ C maximum

Gain - Power Supply Sensitivity

200ppm per 1% change in power supply voltage

Offset - Tempco

$\pm 10\mu$ V/ $^{\circ}$ C typical, $\pm 30\mu$ V/ $^{\circ}$ C maximum

Offset - Power Supply Sensitivity

$\pm 10\mu$ V per 1% change in power supply voltage

Warmup Time

< 2 minutes to specified accuracy

OUTPUT

Pulse Polarity

Positive and Negative

Pulse Width

50ns \pm 15ns

Logic Levels (V_{CC}=+5V)

Logic "1" (High) = +4.0V \pm 0.5V

Logic "0" (Low) = <0.4V @ 3mA sink

Load

≤ 50 pF for rated performance;

10 LSTTL loads

INPUT BUFFER

Input Offset Voltage

5mV typical, 10mV maximum

Input Offset Current

25pF typical, 100pA maximum;
doubles every 10 $^{\circ}$ C

Input Impedance

$10^{12}\Omega$

Common Mode Voltage Range

11V minimum

Gain

+1

Supply Voltage Rejection

70dB minimum, 100dB typical

Slew Rate

13V/ μ s typical

Bandwidth

4MHz typical

Equivalent Input Voltage Noise

25nV/ $\sqrt{\text{Hz}}$ typical; $R_S=100\Omega$, $f=1\text{kHz}$

Equivalent Input Current Noise

0.01pA/ $\sqrt{\text{Hz}}$ typical; $f=1\text{kHz}$

GAIN STAGE

Input Offset Voltage

5mV typical, 10mV maximum

Input Offset Current

25pA typical, 100pA maximum;
doubles every 10 $^{\circ}$ C

Input Impedance

$10^{12}\Omega$

Common Mode Voltage Range

11V minimum

Common Mode Rejection Ratio

100dB typical, 70dB minimum

Large Signal Voltage Gain

25V/mV minimum, 100V/mV typical;
 $V_O=10\text{V}$, $R_L=2.0\text{k}\Omega$

Supply Voltage Rejection

70dB minimum, 100dB typical

Slew Rate

13V/ μ s typical; gain = -1

Gain-Bandwidth Product

4MHz typical

Equivalent Input Voltage Noise

25nV/ $\sqrt{\text{Hz}}$ typical; $R_S=100\Omega$, $f=1\text{kHz}$

Equivalent Input Current Noise

0.01pA/ $\sqrt{\text{Hz}}$ typical; $f=1\text{kHz}$

TOTAL POWER REQUIREMENTS

(+V_S) +15V, $\pm 3\%$

40mA maximum

(-V_S) -15V, $\pm 3\%$

20mA maximum

Specifications (continued)

<p>(+V_{CC}) +5V, ±5% 50mA maximum Power Dissipation 1.25W maximum</p> <p>ENVIRONMENTAL AND MECHANICAL Operating Temperature 0°C to +70°C</p>	<p>Storage Temperature -55°C to +125° Dimensions 1.6"x0.69"x0.22" (40.6x17.5x5.5mm)</p>
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Description (continued)

up to 50pF capacitive loads. Stability of the V/F over temperature is excellent, with offset and gain temperature coefficients of 10μV/°C and

60ppm/°C typical respectively.

The **3860** is packaged in a 1.6"x0.69"x0.22" 24-pin DIL plastic package. Pin spacing is 0.1"x0.6".

Power dissipation is less than 1.25W. Operation to specified performance is over the 0°C to +70°C temperature range.

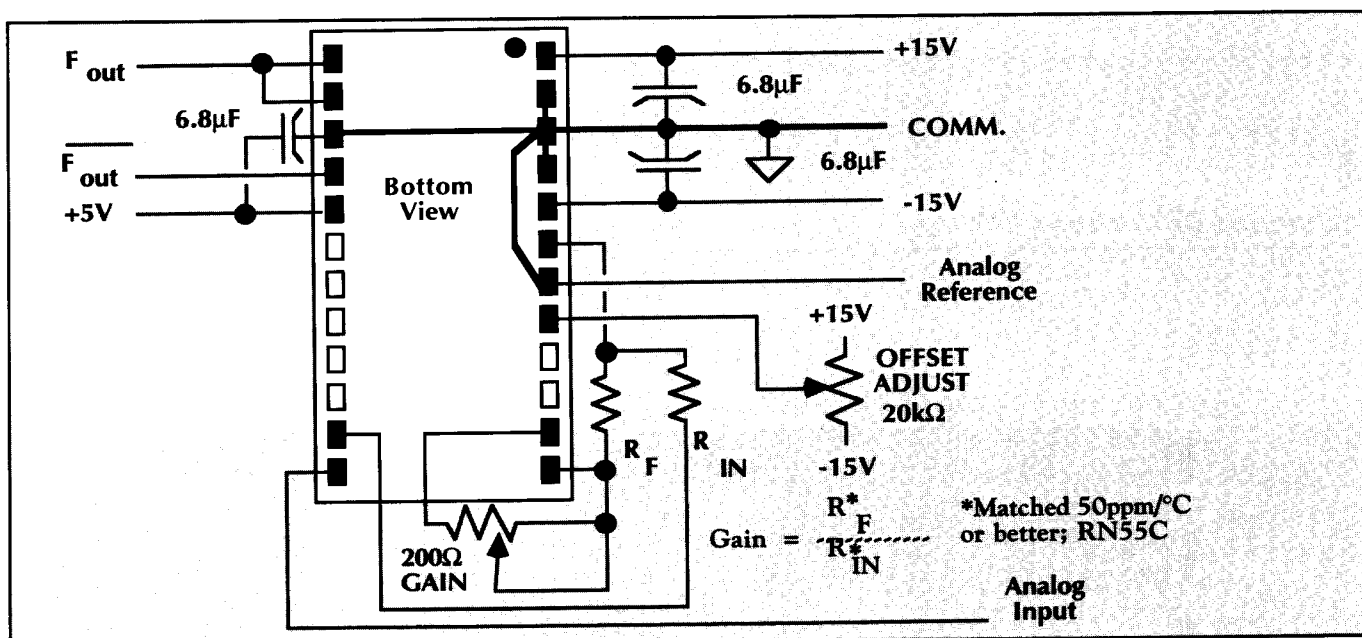


Figure 2. Recommended Interconnection and Signal Routing

Using the 3860

General Considerations

As with any high precision, signal conditioning and data acquisition and conversion circuitry, the use of a ground plane is strongly recommended. The layout should be clean, with output pulses routed as far away as possible from the input analog signals. As shown in Figure 2, bypass capacitors should be mounted as close as possible to the power supply pins of the **3860**.

Gain Stage

As shown in Figure 2, the gain stage is configured such that the gain can be set using a matched set of user-supplied, 50ppm or better, RN55C metal film resistors.

Improving the Offset TC Performance

Due to the offset voltage tracking and compensation scheme

employed in the **3860** design, an approximate 2:1 improvement in the offset TC is possible for the combination buffer/gain stage, over the gain stage alone. In circuit configurations that do not require the high impedance buffer, consideration should be given to using the buffer stage to improve the overall offset TC performance of the complete front-end.

