



VL16C45X • VL16C55X

PC/AT®-COMPATIBLE UART FAMILY

FAMILY FEATURES

- IBM PC/AT-compatible
- Individual modem control signals for each channel
- Programmable serial interface characteristics for each channel:
 - 5-, 6-, 7- or 8-bit characters
 - Even-, odd- or no-parity bit generation and detection
 - 1, 1-1/2, or 2 stop bit generation
- Independent control of transmit, receive, line status and data set interrupts on each channel
- Three-state TTL drive for the data and control bus on each channel

FAMILY DESCRIPTION

The universal asynchronous receiver/transmitter (UART) serves as serial input/output interfaces in microcomputer- or microprocessor-based systems.

It performs serial-to-parallel conversion on data characters received from peripheral devices or modems, and parallel-to-serial conversion on data characters transmitted by the CPU. The complete status of each channel of the UART can be read at any time during functional operation by the CPU. The information obtained includes the type and condition of the transfer operations being performed and error conditions.

Four UARTs provide the user with a fully bidirectional parallel data port that fully supports the parallel Centronics type printer. The parallel port, together with the serial port(s), provide IBM PC/AT-compatible computers with a single device to serve the system port(s).

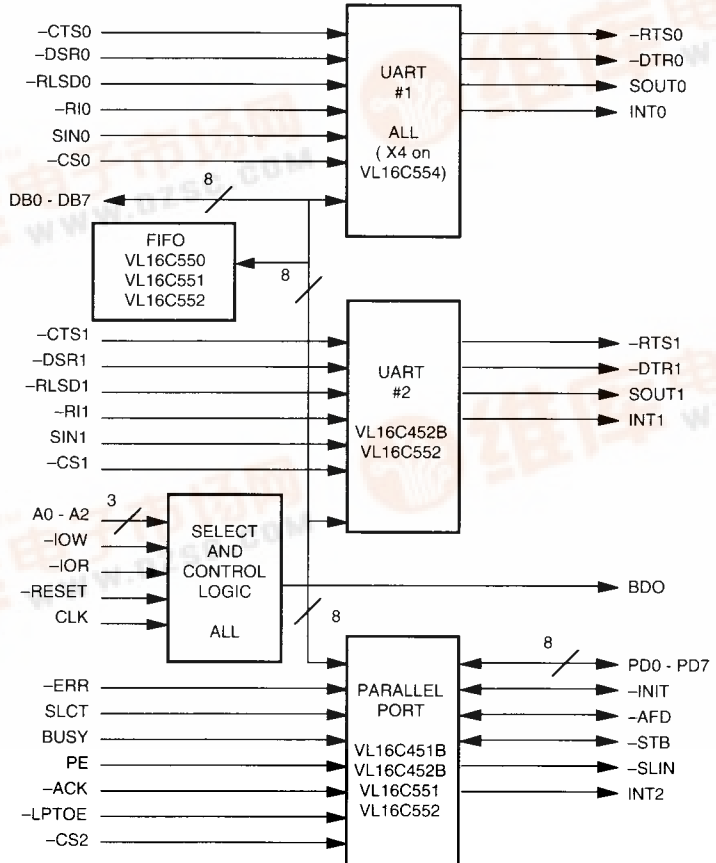
A programmable baud rate generator is included that can divide the timing reference clock input by a divisor between 1 and $(2^{16}-1)$.

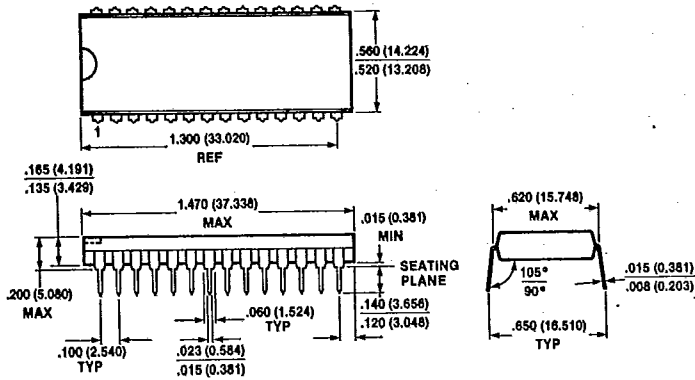
The VLSI family of UARTs is housed in 40-lead plastic DIPs, 44-lead PLCCs, 68-lead PLCCs, and 84-lead quad PLCCs.

INDIVIDUAL FEATURES

- VL16C450
 - Single UART
- VL16C451B
 - Single UART (enhanced VL16C451)
 - Parallel port
- VL16C452B
 - Dual UART (enhanced VL16C452)
 - Parallel port
- VL16C550
 - Single enhanced UART (NSC compatible)
 - FIFOs
- VL16C551
 - Single enhanced UART
 - FIFOs
 - Parallel port
- VL16C552
 - Dual enhanced UARTs
 - FIFOs
 - Parallel port
- VL16C554
 - Quad UART

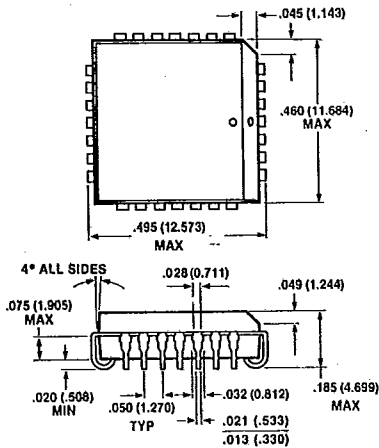
BLOCK DIAGRAM



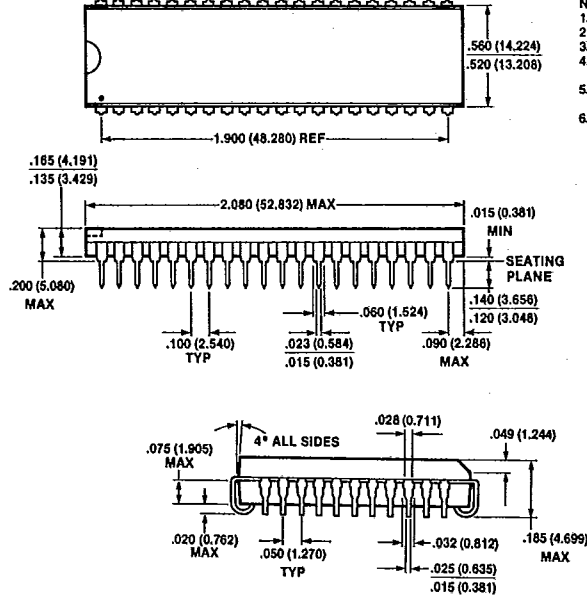


- NOTES: UNLESS OTHERWISE SPECIFIED.
1. LEAD FINISH: MATTE TIN PLATE OR LEAD/TIN SOLDER.
 2. LEAD MATERIAL: ALLOY 42 OR COPPER.
 3. PACKAGE LENGTH DOES NOT INCLUDE END FLASH BURR WHICH IS .010 (0.254) MAX. AT EACH END.
 4. TOLERANCE TO BE $\pm .005$ (0.127) UNLESS OTHERWISE NOTED.
 5. ALL METRIC DIMENSIONS ARE IN PARENTHESES.
 6. PIN 1 INDEX MARK MAY VARY IN SIZE AND SHAPE.

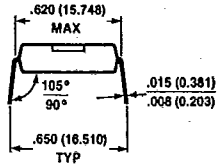
28-PIN PLASTIC LEADED CHIP CARRIER



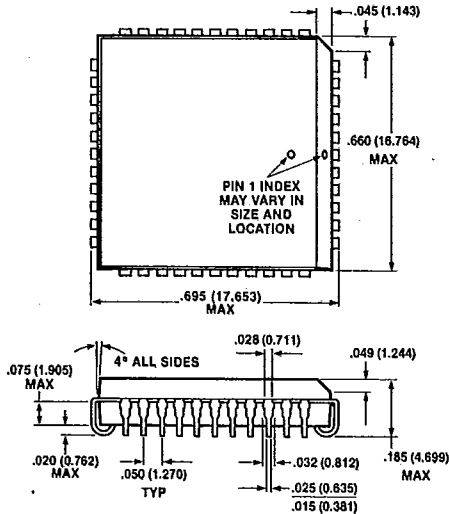
- NOTES: UNLESS OTHERWISE SPECIFIED.
1. TOLERANCE TO BE $\pm .005$ (0.127).
 2. LEADFRAME MATERIAL: COPPER.
 3. LEAD FINISH: MATTE TIN PLATE OR Sn Pb SOLDER DIP.
 4. SPACING TO BE MAINTAINED BETWEEN FORMED LEAD AND MOLDED PLASTIC ALONG FULL LENGTH OF LEAD.
 5. MOLDED PLASTIC DIMENSION DOES NOT INCLUDE SIDE FLASH BURR, WHICH IS .010 (0.254) MAX ON FOUR SIDES.
 6. ALL METRIC DIMENSIONS ARE IN PARENTHESES.



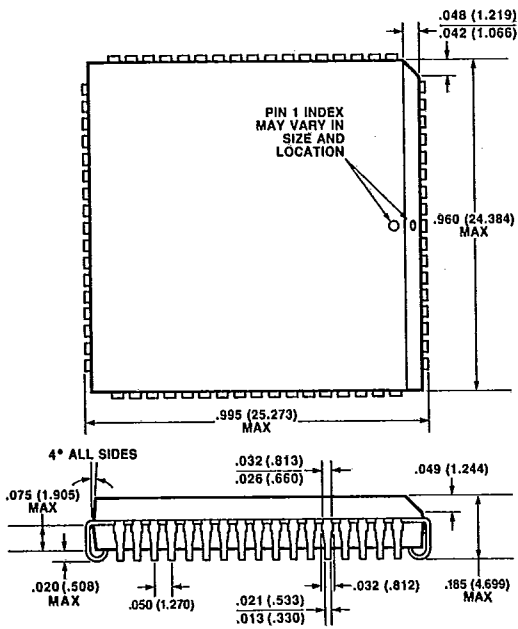
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 2. LEADFRAME MATERIAL: COPPER.
 3. LEAD FINISH: MATTE TIN PLATE OR SOLDER DIP.
 4. SPACING TO BE MAINTAINED BETWEEN FORMED LEAD AND MOLDED PLASTIC ALONG FULL LENGTH OF LEAD.
 5. MOLDED PLASTIC DIMENSION DOES NOT INCLUDE SIDE FLASH BURR, WHICH IS .010 (0.254) MAX ON FOUR SIDES.
 6. ALL METRIC DIMENSIONS ARE IN PARENTHESES.

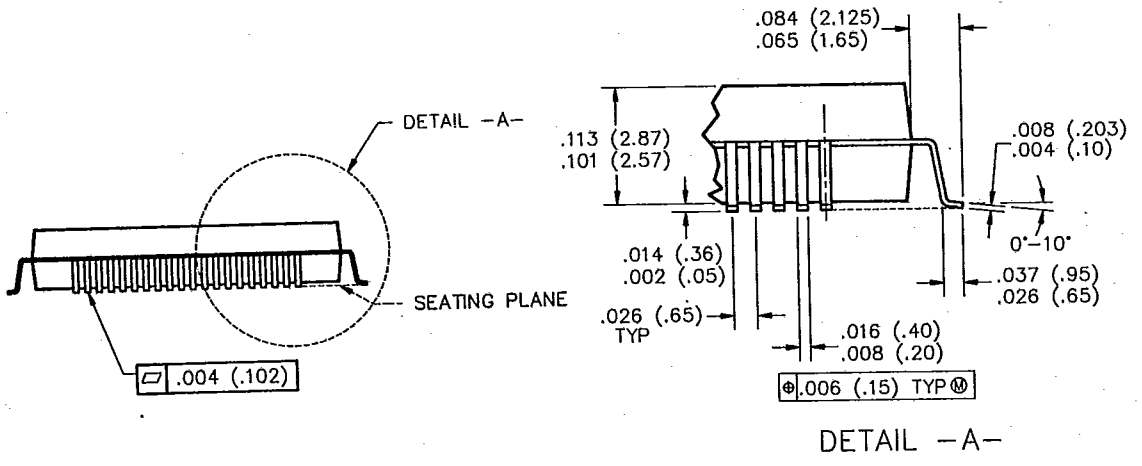
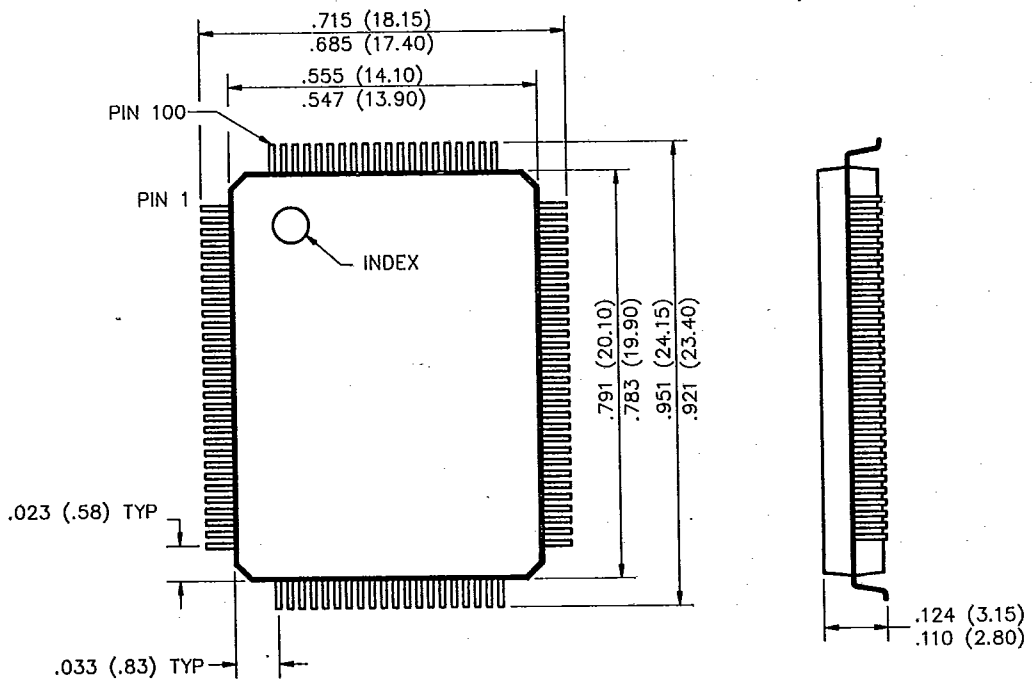


44-PIN PLASTIC LEADED CHIP CARRIER



- NOTES: UNLESS OTHERWISE SPECIFIED.
1. TOLERANCE TO BE $\pm .005$ (0.127).
 2. LEADFRAME MATERIAL: COPPER.
 3. LEAD FINISH: MATTE TIN PLATE OR SOLDER DIP.
 4. SPACING TO BE MAINTAINED BETWEEN FORMED LEAD AND MOLDED PLASTIC ALONG FULL LENGTH OF LEAD.
 5. MOLDED PLASTIC DIMENSION DOES NOT INCLUDE SIDE FLASH BURR, WHICH IS .010 (0.254) MAX ON FOUR SIDES.
 6. ALL METRIC DIMENSIONS ARE IN PARENTHESES.





NOTES:
 1. CONTROLLING DIMENSION IS MM.