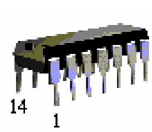
PJ324

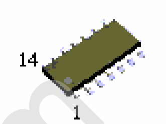
Quad Low Power Operational Amplifiers

The PJ324 series are low-cost , quad operational amplifiers with true differential inputs. These have several distinct advantage over standard operational amplifier types in single supply applications. The quad amplifiers can operate at supply voltages as low as 3.0V or as high as 32V with very low quiescent currents and eliminat the necessity for external biasing components in many applications. The output voltage range also includes the negative power supply voltage.

DIP-14



SOP-14



Pin:

1.Output 1	8.Output 3
2.Input 1 (-)	9.Input 3 (-)
3.Input 1(+)	10.Input 3 (+)
4.Vcc	11.Vee Gnd
5.Input 2(+)	12.Input 4 (+)
6.Input 2 (-)	13.Input 4 (-)
7.Output 2	14.Output 4

FEATURES

- Short circuited protected outputs
- True differential input stage
- Single supply operation:3.0V to 32V
- Low input bias currents:100nA Max
- Four amplifiers per package
- Internally compensated
- Common mode range extends to negative supply
- Industry standard pinouts
- ESD clamps on the inputs increase raggedness without affecting device operation

ORDERING INFORMATION

Device	Operating Temperature	Package
PJ324CD	-20℃ to +85℃	DIP-14
PJ324CS		SOP-14

MAXIMUM RATING(Ta=+25℃,unless otherwise noted.)

Rating	Symbol	PJ324	Unit
Power Supply Voltage Single Supply Split Supplies	V_{CC} V_{CC}, V_{EE}	±16	Vdc
Input Differential Voltage Range (1)	V_{IDR}	32	Vdc
Input Common Mode Voltage Range	V_{ICR}	-0.3 to 32	Vdc
Output Short Circuit Duration	t_{SC}	Continuous	
Junction Temperature Plastic Packages	T_J	150	℃
Storage Temperature Ceramic Package Plastic Packages	T_{stg}	- 65 to + 150	℃

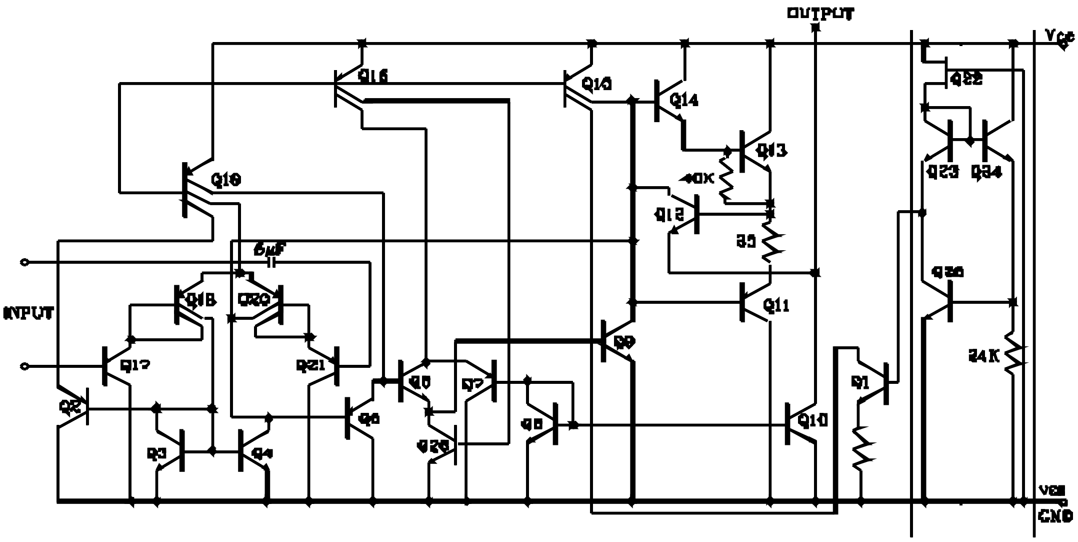
NOTE : 1. Split Power Supplies.

ELECTRICAL CHARACTERISTICS **(V_{CC}= 5.0V, V_{EE}=GND, T_A= 25 ℃ unless otherwise noted.)**

Characteristics	Symbol	PJ324 Min	PJ324 Typ	PJ324 Max	Unit
Input Offset Voltage V_{CC}=5.0V to 30V V_{ICR}=0 V to V_{CC}-0.7V, Vo=1.4V, Rs=0Ω T_A=25℃ T_A=T_{high} to T_{low} (Note 1)	V_{IO}	 - -	 2.0 -	 7.0 9.0	mV
Average Temperature Coefficient of Input Offset Voltage T_A=T_{hige} to T_{low} (Note 1)	△V_{IO} /△T	-	7.0	-	μ V/ ℃
Input Offset Current T_A=T_{hige} to T_{low} (Note 1)	I_{IO}	- -	5.0 -	50 150	nA
Average Temperature Coefficient of Input Offset Current T_A=T_{hige} to T_{low} (Note 1)	△I_{IO} /△T	-	10	-	pA/ ℃
Input Bias Current T_A=T_{hige} to T_{low} (Note 1)	I_{IB}	- -	-90 -	-250 -500	nA
Input Common Mode Voltage Range (Note 2) V_{CC}=30V V_{CC}=30V, T_A=T_{hige} to T_{low}	V_{ICR}	 0 0	 - -	 28.3 28	V
Differential Input Voltage Range	V_{IDR}	-	-	V_{CC}	V
Large Signal Open-Loop Voltage Gain R_L=2.0K , V_{CC}=15V, for Large Vo Swing T_A=T_{hige} to T_{low} (Note 1)	A_{VOL}	 25 15	 100 -	 - -	V/mV
Channel Separation 10KHz≤f≤20KHz, Input Referenced	CS	-	-120	-	dB
Common Mode Rejection Rs≤10KΩ	CMR	65	70	-	dB
Power Supply Rejection	PSR	65	100	-	dB
Output Voltage - High Limit (T_A=T_{hige} to T_{low}) (Note 1) V_{CC}=5.0V, R_L=10K ,T_A=25℃ V_{CC}=30V, R_L=2.0K V_{CC}=30V, R_L=10K	V_{OH}	 3.3 26 27	 3.5 - 28	 - - -	V
Output Voltage-Low Limit V_{CC}=5.0V, R_L=10K , T_A=T_{hige} to T_{low} (Note 1)	V_{OL}	-	5.0	20	mV
Output Source Current (V_{ID}=+1.0V, V_{CC}=15V) T_A=25℃ T_A=T_{hige} to T_{low} (Note 1)	I_O^+	 20 10	 40 20	 - -	mA
Output Sink Current (V_{ID}= -1.0V, V_{CC}=15V) T_A=25℃ T_A=T_{hige} to T_{low} (Note 1) (V_{ID}= -1.0V, V_{CC}=200mV, T_A=25℃)	Io^-	 10 5.0 12	 20 8.0 50	 - - -	mA μ A
Output Short Circuit Ground (Note 2)	Isc	-	40	60	mA
Power Supply Current (T_A=T_{hige} to T_{low}) (Note 1) V_{CC}=30V (26V for LM2902), Vo=0V, R_L=∞ V_{CC}=5.0V, Vo=0V, R_L=∞	Icc	 - -	 - -	 3.0 1.2	mA

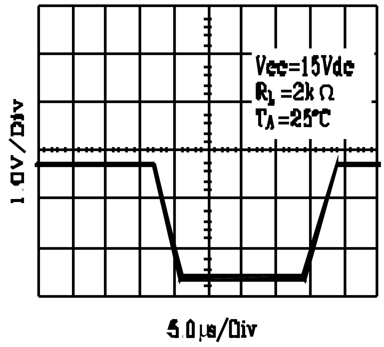
Note: 1. Short circuits from the output to Vcc can cause excessive heating and eventual destruction . Destructive dissipation can result from simultaneous shorts on all amplifiers.
2. The input common mode voltage or either input signal voltage should not be allowed to go negative by more than 0.3V The upper end of the common mode voltage range is Vcc-1.7V.

Representative Circuit Schematic
(One-Fourth of Circuit Shown)



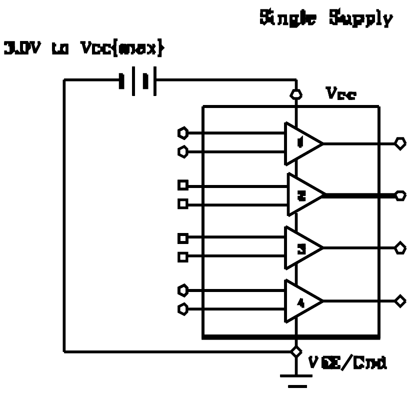
CIRCUIT DESCRIPTION

The PJ324 series is made using four internally compensated, two-stage operational amplifiers. The first stage of each consists of differential input devices Q20 and Q18 with input buffer transistors Q21 and Q17 and the differential to single ended converter Q3 and Q4 . The first stage performs not only the first stage gain function but also performs the level shifting and transconductance reduction functions. By reducing the transconductance a smaller compensation capacitor (only 5.0pF) can be employed , thus saving chip area. The transconductance reduction is accomplished by splitting the collectors of Q20 and Q18 . Another feature of this input stage is that the input common mode range can include the negative supply or ground, in single supply operation without saturating either the input devices or the differential to single-ended converter . The second stage consists of a standed current source load amplifier stage.



Large Signal Voltage Follower Response

Each amplifier is biased from an internal voltage regulator which has a low temperature coefficient thus giving each amplifier good temperature characteristics as will as excellent power supply rejection.



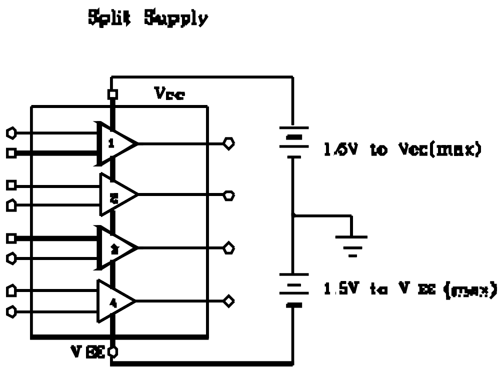


Figure 1.Input Voltage Range

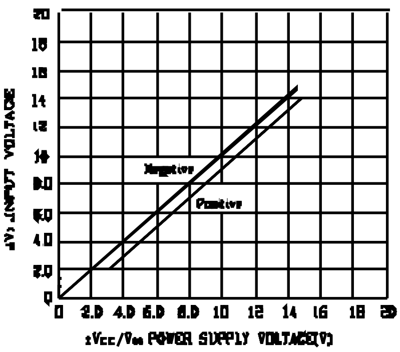


Figure 2.Open-Loop Frequency

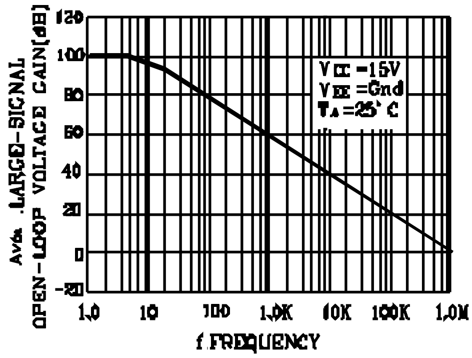


Figure 3.Large-Signal Frequency Response

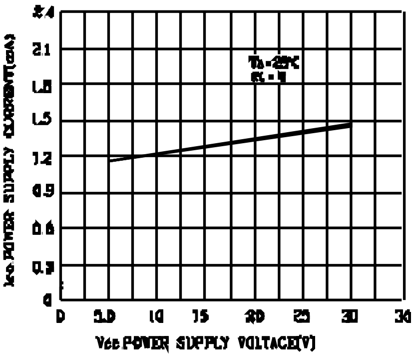


Figure 4.Small-Signal Voltage Follower
Pulse Response (Noninverting)

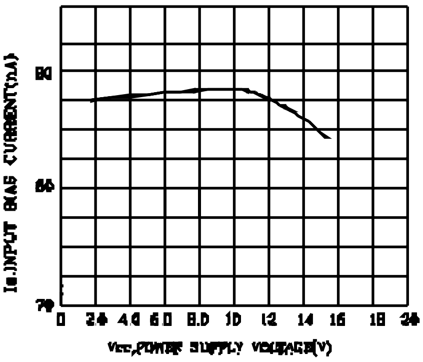


Figure 5.Power Supply Current versus
Power Supply Voltage

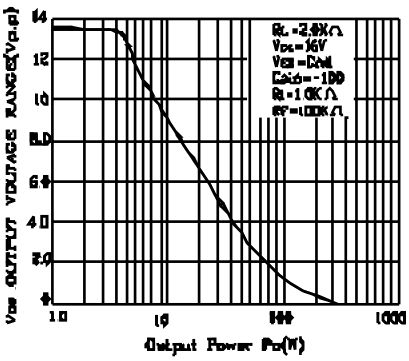


Figure 6.Input Bias Current versus
Power Supply Voltage

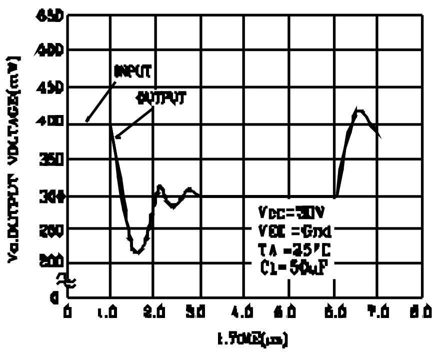
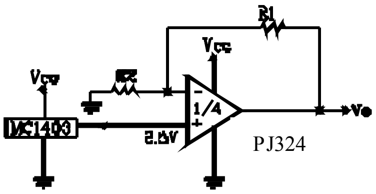
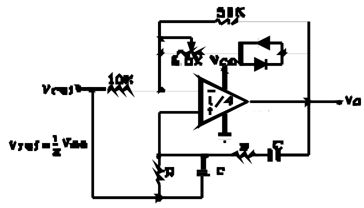


Figure 7.Voltage Reference



Vo = 2.5V (1+ R1/ R2)

Figure 8.Wlen Bridge Oscillator



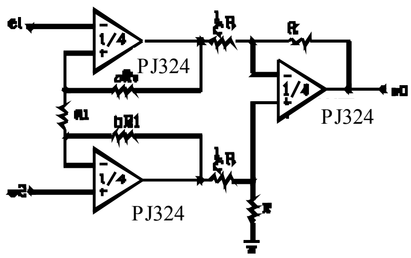
fo = 1/ (2 π RC)

For: fo =1.0KHz

R=16K Ω

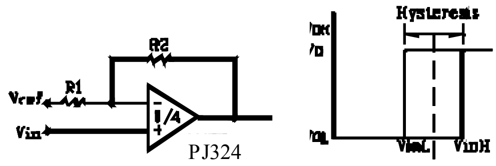
C =0.01 μ F

Figure 9.High Impedance Differential Amplifier



e_o =C (1+a+b) (e2- e1)

Figure 10.Comparator with Hysteresis

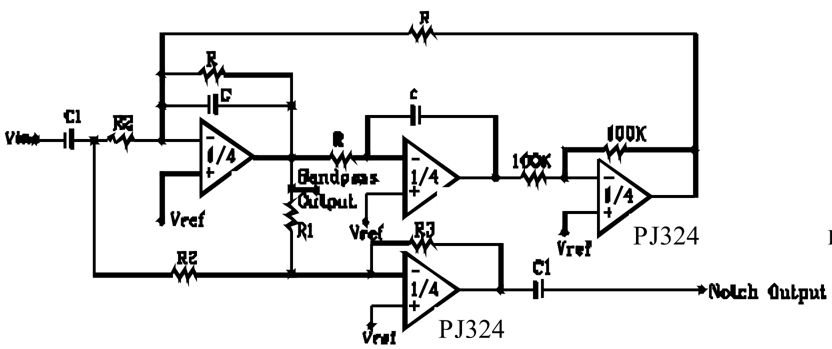


V_{inL} = R1/ (R1 + R2) (V_{OL}-V_{ref}) +V_{ref}

V_{inH} = R1 / (R1 + R2) (V_{OH} -V_{ref}) +V_{ref}

H = R1/ (R1 + R2) (V_{OH} -V_{OL})

Figure 11.Bi-Quad Filter



fo = 1/ (2 π RC)

R1 = OR

R2 = R1/ T_{BP} V_{ref} = 1/2

R3 =T_{NR2}

C1 =10C

For : fo =1.0 Khz

Q =10

T_{BP} =1

T_N =1

R =160 K Ω

C =0.001 μ F

R1 =1.6M Ω

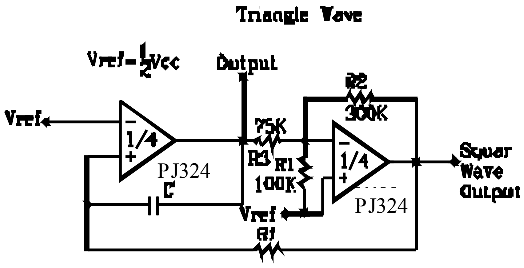
R2 =1.6M Ω

R3 =1.6M Ω

Where : T_{BP} =Center Frequency Gain

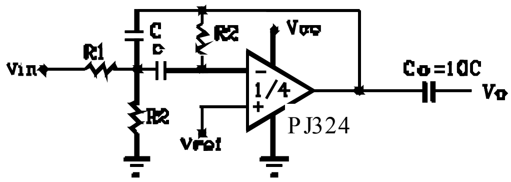
T_N = Passband Notch Gain

Figure 12.Function Generator



f= （R1+R2）/ （4CRfR1）
R3=（R2R1）/ （R2+R1）

Figure 13.Mulitiple Feedback Bandpass Filter

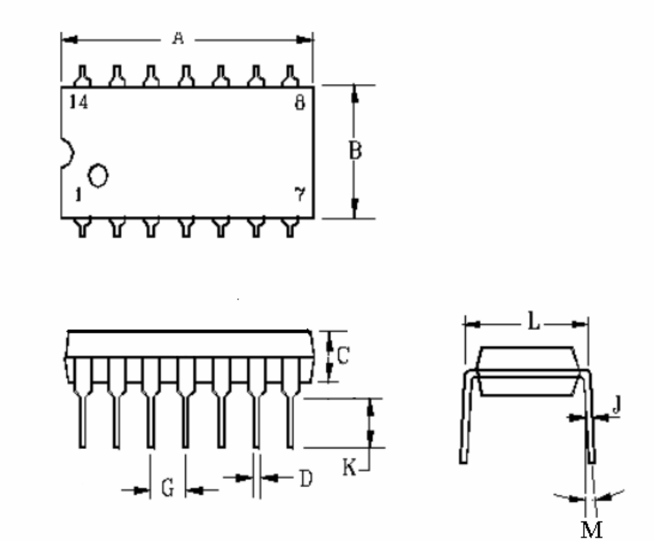


Given: fo=center frequency
A(fo)=gain at center frequency
Choose value fo C
Then:

R3= Q/（π fo C）
R1= R3/（2Afo）
R2=（R1R3）/（$4Q^2$R1-R3）

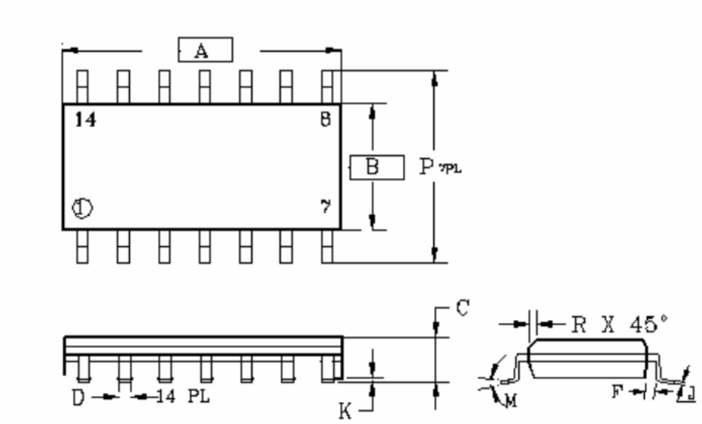
For less than 10% error operational amplifier
Qofo<0.1 where fo and BW are expressed in Hz
BW
If source impedance varies, filter may be preceded with voltage follow buffer to stabilize filter parameters.

DIP-14



DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	18.55	19.56	0.73	0.77
B	6.22	6.48	0.245	0.255
C	3.18	4.43	0.125	0.135
D	0.35	0.55	0.019	0.020
G	2.54BSC		0.10BSC	
J	0.29	0.31	0.011	0.012
K	3.25	3.35	0.128	0.132
L	7.75	8.00	0.305	0.315
M	-	10°	-	10°

SOP-14



DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	8.55	8.75	0.337	0.344
B	3.80	4.00	0.150	0.157
C	1.35	1.75	0.054	0.068
D	0.35	0.49	0.014	0.019
F	0.40	1.25	0.016	0.049
G	1.27BSC		0.05BSC	
K	0.10	0.25	0.004	0.009
M	0°	7°	0°	7°
P	5.80	6.20	0.229	0.244
R	0.25	0.50	0.010	0.019