查询HD64F3644H供应商 捷多邦，专业PCB打样工厂，24小时加急出货

Section 13 Electrical Characteristics

13.1 Absolute Maximum Ratings

Table 13-1 lists the absolute maximum ratings.

Table 13-1 Absolute Maximum Ratings

Item		Symbol	Value	Unit
Power supply voltage		V_{CC}	–0.3 to +7.0	V
Analog power supply voltage		AV_{CC}	–0.3 to +7.0	V
Programming voltage		V_{PP}	–0.3 to +13.0	V
Input voltage	Ports other than Port C	V_{in}	–0.3 to V_{CC} +0.3	V
	Port B	AV_{in}	–0.3 to AV_{CC} +0.3	V
Operating temperature	T_{opr}	–20 to +75	°C	
Storage temperature	T_{stg}	–55 to +125	°C	

Note: Permanent damage may occur to the chip if maximum ratings are exceeded. Normal operation should be under the conditions specified in Electrical Characteristics. Exceeding these values can result in incorrect operation and reduced reliability.

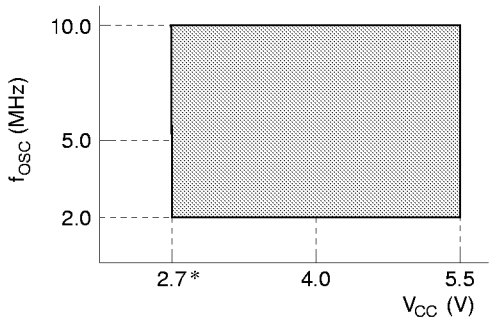
13.2 Electrical Characteristics

13.2.1 Power Supply Voltage and Operating Range

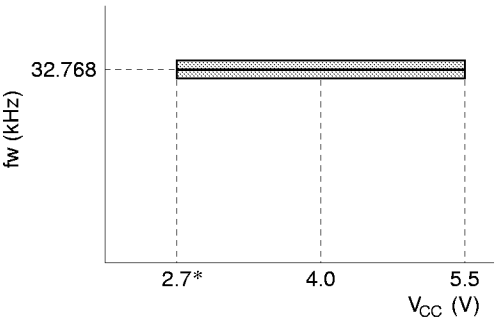
The power supply voltage and operating range are indicated by the shaded region in the figures below.

找PDF 维库一下 pdf.dzsc.com

1. Power supply voltage vs. oscillator frequency range

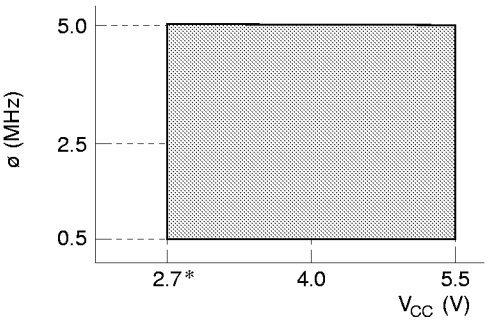


• Active mode (high speed)
• Sleep mode (high speed)

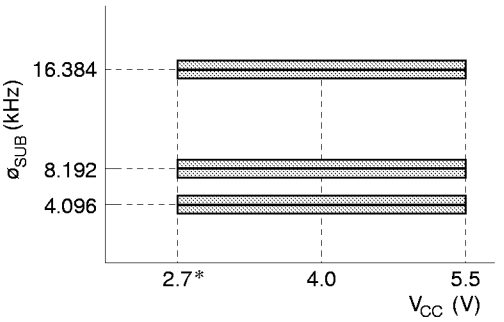


• All operating modes

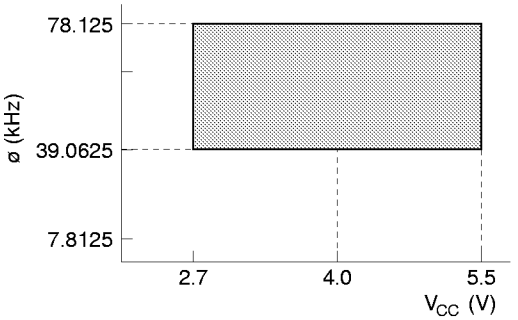
2. Power supply voltage vs. clock frequency range



• Active (high speed) mode
• Sleep (high speed) mode (except CPU)

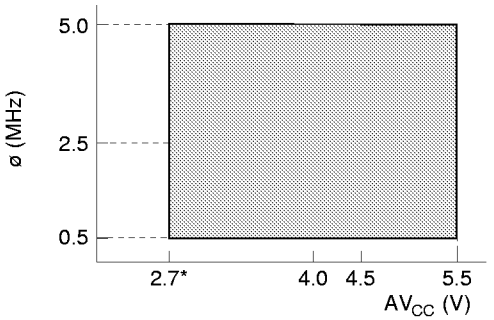


• Subactive mode
• Subsleep mode (except CPU)
• Watch mode (except CPU)



• Active (medium speed) mode
• Sleep (medium speed) mode (except CPU)

3. Analog power supply voltage vs. A/D converter operating range



Don't use in these modes.

- Active (medium speed) mode
- Sleep (medium speed) mode

- Active (high speed) mode
- Sleep (high speed) mode

Note: * 2.5 V for the HD6433644, HD6433643, HD6433642, HD6433641 and HD6433640.

13.2.2 DC Characteristics

Table 13-2 lists the DC characteristics of the HD6473644.

Table 13-2 DC Characteristics

$V_{C\ \ C} = 4.0$ V to 5.5 V, $V_{SS} = 0.0$ V, $T_a = -20°C$ to $+75°C$ unless otherwise indicated.

Item	Symbol	Applicable Pins	Values Min	Typ	Max	Unit	Test Condition	Notes
Input high voltage	V_{IH}	$\overline{RES}$, $\overline{INT_0}$ to $\overline{INT_7}$, $\overline{IRQ_0}$ to $\overline{IRQ_3}$, $\overline{ADTRG}$, TMIB,	0.8 V_{CC}	—	V_{CC} + 0.3	V		
		TMRIV, TMCIV, FTCI, FTIA, FTIB, FTIC, FTID, SCK_1, SCK_3 TRGV	0.9 V_{CC}	—	V_{CC} + 0.3		V_{CC} = 2.7 V to 5.5 V including subactive mode	
		SI_1, RXD $P1_0$, $P1_4$ to $P1_7$, $P2_0$ to $P2_2$, $P3_0$ to $P3_2$,	0.7 V_{CC}	—	V_{CC} + 0.3	V		
		$P5_0$ to $P5_7$, $P6_0$ to $P6_7$, $P7_3$ to $P7_7$, $P8_0$ to $P8_7$, $P9_0$ to $P9_4$	0.8 V_{CC}	—	V_{CC} + 0.3		V_{CC} = 2.7 V to 5.5 V including subactive mode	
		PB_0 to PB_7,	0.7 V_{CC}	—	AV_{CC} + 0.3			
			0.8 V_{CC}	—	AV_{CC} + 0.3		V_{CC} = 2.7 V to 5.5 V including subactive mode	
		OSC_1	V_{CC} – 0.5	—	V_{CC} + 0.3	V		
			V_{CC} – 0.3	—	V_{CC} + 0.3		V_{CC} = 2.7 V to 5.5 V including subactive mode	

Note: Connect the TEST pin to V_{SS}.

Table 13-2 DC Characteristics (cont)

V_{CC} = 4.0 V to 5.5 V, V_{SS} = 0.0 V, T_a = –20°C to +75°C unless otherwise indicated.

Item	Symbol	Applicable Pins	Values Min	Typ	Max	Unit	Test Condition	Notes
Input low voltage	V_{IL}	$\overline{RES}$,, $\overline{INT_0}$ to $\overline{INT_7}$ $\overline{IRQ_0}$ to $\overline{IRQ_3}$, $\overline{ADTRG}$, TMIB,	–0.3	—	0.2 V_{CC}	V		
		TMRIV, TMCIV, FTCI, FTIA, FTIB, FTIC, FTID, SCK_1, SCK_3, TRGV	–0.3	—	0.1 V_{CC}		V_{CC} = 2.7 V to 5.5 V including subactive mode	
		SI,, RXD, $P1_0$, $P1_4$ to $P1_7$, $P2_0$ to $P2_2$, $P3_0$ to $P3_2$, $P5_0$ to $P5_7$,	–0.3	—	0.3 V_{CC}	V		
		$P6_0$ to $P6_7$, $P7_3$ to $P7_7$, $P8_0$ to $P8_7$, $P9_0$ to $P9_4$, PB_0 to PB_7	–0.3	—	0.2 V_{CC}	V	V_{CC} = 2.7 V to 5.5 V including subactive mode	
		OSC_1	–0.3	—	0.5	V		
			–0.3	—	0.3		V_{CC} = 2.7 V to 5.5 V including subactive mode	

Note: Connect the TEST pin to V_{SS}.

Table 13-2 DC Characteristics (cont)

V_{CC} = 4.0 V to 5.5 V, V_{SS} = 0.0 V, T_a = –20°C to +75°C unless otherwise indicated.

Item	Symbol	Applicable Pins	Values Min	Typ	Max	Unit	Test Condition	Notes
Output high voltage	V_{OH}	$P1_0$, $P1_4$ to $P1_7$,	V_{CC} – 1.0	—	—	V	$-I_{OH}$ = 1.0 mA	
		$P2_0$ to $P2_2$,	V_{CC} – 1.0	—	—		$-I_{OH}$ = 1.5 mA	
		$P3_0$ to $P3_2$, P50 to P57, $P6_0$ to $P6_7$, $P7_3$ to $P7_7$, $P8_0$ to $P8_7$, $P9_0$ to $P9_4$	V_{CC} – 0.5	—	—		V_{CC} = 2.7 V to 5.5 V $-I_{OH}$ = 0.1 mA	
Output low voltage	V_{OL}	$P1_0$, $P1_4$ to $P1_7$, $P2_0$ to $P2_2$, $P3_0$ to $P3_2$, $P5_0$ to $P5_7$,	—	—	0.6	V	I_{OL} = 1.6 mA	
		$P7_3$ to $P7_7$, $P8_0$ to $P8_7$, $P9_0$ to $P9_4$	—	—	0.4		V_{CC} = 2.7 V to 5.5 V I_{OL} = 0.4 mA	
		$P6_0$ to $P6_4$	—	—	1.0	V	I_{OL} = 10.0 mA	
			—	—	0.4		I_{OL} = 1.6 mA	
			—	—	0.4		V_{CC} = 2.7 V to 5.5 V I_{OL} = 0.4 mA	
Input/ output leakage current	$\lvert I_{IL} \rvert$	OSC_1, $P1_0$, $P1_4$ to $P1_7$, $P2_0$ to $P2_2$, $P3_0$ to $P3_2$, $P5_0$ to $P5_7$, $P6_0$ to $P6_7$, $P7_0$ to $P7_7$, $P8_0$ to $P8_7$, $P9_0$ to $P9_4$	—	—	1.0	µA	V_{IN} = 0.5 V to (V_{CC} – 0.5 V)	
		PB_0 to PB_7	—	—	1.0		V_{IN} = 0.5 V to AV_{CC} – 0.5 V	

Table 13-2 DC Characteristics (cont)

V_{CC} = 4.0 V to 5.5 V, V_{SS} = 0.0 V, T_a = –20°C to +75°C unless otherwise indicated.

Item	Symbol	Applicable Pins	Values Min	Typ	Max	Unit	Test Condition	Notes
Input leakage current	$\lvert I_{IL} \rvert$	$\overline{RES}$, IRQ_0	—	—	20	µA	V_{IN} = 0.5 V to (V_{CC} – 0.5 V)	
Pull-up MOS current	$-I_P$	$P1_0$, $P1_4$ to $P1_7$, $P3_0$ to $P3_2$,	50	—	300	µA	V_{CC} = 5 V, V_{IN} = 0 V	
		P50 to P57	—	25	—		V_{CC} = 2.7 V, V_{IN} = 0 V	Reference value
Input capacitance	C_{IN}	All input pins except $\overline{RES}$,	—	—	15.0	pF	f = 1 MHz, V_{IN} = 0 V, T_a = 25°C	
		$\overline{RES}$	—	—	60.0			
		IRQ_n	—	—	30.0			
Active mode current dissipation	I_{OPE1}	V_{CC}	—	10	15	mA	Active (high- speed) mode V_{CC} = 5 V, f_{OSC} = 10 MHz	1, 2
			—	5	—		V_{CC} = 2.7 V, f_{OSC} = 10 MHz	
	I_{OPE2}	V_{CC}	—	2	3	mA	Active (medium-speed) mode V_{CC} = 5 V, f_{OSC} = 10 MHz	1, 2
			—	1	—		V_{CC} = 2.7 V, f_{OSC} = 10 MHz	
Sleep mode current dissipation	I_{SLEEP1}	V_{CC}	—	5	7	mA	Sleep (high-speed) mode V_{CC} = 5 V, f_{OSC} = 10 MHz	1, 2
			—	2	—		V_{CC} = 2.7 V, f_{OSC} = 10 MHz	
	I_{SLEEP2}	V_{CC}	—	2	3	mA	Sleep (medium-speed) mode V_{CC} = 5 V, f_{OSC} = 10 MHz	1, 2
			—	1	—		V_{CC} = 2.7 V, f_{OSC} = 10 MHz	
Subactive mode current dissipation	I_{SUB}	V_{CC}	—	10	20	µA	V_{CC} = 2.7 V 32-kHz crystal oscillator ($\phi_{SUB} = \phi_W/2$)	1, 2
			—	10	—	µA	V_{CC} = 2.7 V 32-kHz crystal oscillator ($\phi_{SUB} = \phi_W/8$)	1, 2 Reference value

Table 13-2 DC Characteristics (cont)

V_{CC} = 4.0 V to 5.5 V, V_{SS} = 0.0 V, T_a = –20°C to +75°C unless otherwise indicated.

Item	Symbol	Applicable Pins	Values Min	Typ	Max	Unit	Test Condition	Notes
Subsleep mode current dissipation	I_{SUBSP}	V_{CC}	—	5	10	µA	V_{CC} = 2.7 V 32-kHz crystal oscillator ($\phi_{SUB} = \phi_W/2$)	1, 2
Watch mode current dissipation	I_{WATCH}	V_{CC}	—	—	6	µA	V_{CC} = 2.7 V 32-kHz crystal oscillator	1, 2
Standby mode current dissipation	I_{STBY}	V_{CC}	—	—	5	µA	32-kHz crystal oscillator not used	1, 2
RAM data retaining voltage	V_{RAM}	V_{CC}	2	—	—	V		1, 2

Notes: 1. Pin states during current measurement are given below.
2. Excludes current in pull-up MOS transistors and output buffers.

Mode	$\overline{RES}$ Pin	Internal State	Other Pins	Oscillator Pins
Active (high-speed) mode	V_{CC}	Operates	V_{CC}	System clock oscillator ceramic or crystal:
Active (medium-speed) mode		Operates (ϕOSC/128)		Subclock oscillator: Pin X_1 = V_{CC}
Sleep (high-speed) mode	V_{CC}	Only timers operate	V_{CC}	
Sleep (medium-speed) mode		Only timers operate (ϕOSC/128)		
Subactive mode	V_{CC}	Operates	V_{CC}	System clock oscillator:
Subsleep mode	V_{CC}	Only timers operate, CPU stops	V_{CC}	ceramic or crystal Subclock oscillator:
Watch mode	V_{CC}	Only time base perates, CPU stops	V_{CC}	crystal
Standby mode	V_{CC}	CPU and timers both stop	V_{CC}	System clock oscillator: ceramic or crystal Subclock oscillator: Pin X_1 = V_{CC}

Table 13-2 DC Characteristics (cont)

V_{CC} = 4.0 V to 5.5 V, V_{SS} = 0.0 V, T_a = –20°C to +75°C, unless otherwise indicated.

Item		Values				
		Symbol	Min	Typ	Max	Unit
Allowable output low current (per pin)	Output pins except port 6	I_{OL}	—	—	2	mA
	Port 6		—	—	10	
Allowable output low current (total)	Output pins except port 6	ΣI_{OL}	—	—	40	mA
	Port 6		—	—	80	
Allowable output high current (per pin)	All output pins	$-I_{OH}$	—	—	2	mA
Allowable output high current (total)	All output pins	$\Sigma (-I_{OH})$	—	—	30	mA

13.2.3 AC Characteristics

Table 13-3 lists the control signal timing, and tables 13-4 and 13-5 list the serial interface timing of the HD6473644.

Table 13-3 Control Signal Timing

V_{CC} = 4.0 V to 5.5 V, V_{SS} = 0.0 V, T_a = –20°C to +75°C, unless otherwise specified.

Item	Symbol	Applicable Pins	Values Min	Typ	Max	Unit	Test Condition	Reference Figure
System clock oscillation frequency	f_{OSC}	OSC_1, OSC_2	2	—	10	MHz		
			2	—	5		V_{CC} = 2.7 V to 5.5 V	
OSC clock (ϕ_{OSC}) cycle time	t_{OSC}	OSC_1, OSC_2	100	—	1000	ns		1
			200	—	1000		V_{CC} = 2.7 V to 5.5 V	Figure 13-1
System clock (ϕ)cycle time	t_{cyc}		2	—	128	t_{OSC}	V_{CC} = 2.7 V to 5.5 V	1
			—	—	25.5	µs		
Subclock oscillation frequency	f_w	X_1, X_2	—	32.768	—	kHz	V_{CC} = 2.7 V to 5.5 V	
Watch clock (ϕ_w) cycle time	t_w	X_1, X_2	—	30.5	—	µs	V_{CC} = 2.7 V to 5.5 V	
Subclock (ϕ_{SUB}) cycle time	t_{subcyc}		2	—	8	t_w	V_{CC} = 2.7 V to 5.5 V	2
Instruction cycle time			2	—	—	t_{cyc} t_{subcyc}	V_{CC} = 2.7 V to 5.5 V	
Oscillation stabilization time (crystal oscillator)	t_{rc}	OSC_1, OSC_2	—	—	40	ms		
			—	—	60		VCC = 2.7 V to 5.5 V	
Oscillation stabilization time (ceramic oscillator)	t_{rc}	OSC_1, OSC_2	—	—	20	ms		
			—	—	40		VCC = 2.7 V to 5.5 V	
Oscillation stabilization time	t_{rc}	X_1, X_2	—	—	2	s	V_{CC} = 2.7 V to 5.5 V	
External clock high width	t_{CPH}	OSC_1	40	—	—	ns		Figure 13-1
			80	—	—		V_{CC} = 2.7 V to 5.5 V	
External clock low width	t_{CPL}	OSC_1	40	—	—	ns		Figure 13-1
			80	—	—		V_{CC} = 2.7 V to 5.5 V	
External clock rise time	t_{CPr}		—	—	15	ns		
			—	—	20		V_{CC} = 2.7 V to 5.5 V	
External clock fall time	t_{CPf}		—	—	15	ns		
			—	—	20		V_{CC} = 2.7 V to 5.5 V	
Pin $\overline{RES}$ low width	t_{REL}	$\overline{RES}$	10	—	—	t_{cyc}	V_{CC} = 2.7 V to 5.5 V	Figure 13-2

Notes: 1. A frequency between 1 MHz to 10 MHz is required when an external clock is input
2. Selected with SA1 and SA0 of system clock control register 2 (SYSCR2).

Table 13-3 Control Signal Timing (cont)

V_{CC} = 4.0 V to 5.5 V, V_{SS} = 0.0 V, T_a = –20°C to +75°C, unless otherwise specified.

Item	Symbol	Applicable Pins	Values Min	Typ	Max	Unit	Test Condition	Reference Figure
Input pin high width	t_{IH}	$\overline{IRQ_0}$ to $\overline{IRQ_3}$, $\overline{INT_0}$ to $\overline{INT_7}$, $\overline{ADTRG}$, TMIB, TMCIV, TMRIV, FTCI, FTIA, FTIB, FTIC, FTID, TRGV	2	—	—	t_{cyc} t_{subcyc}		Figure 13-3
Input pin low width	t_{IL}	$\overline{IRQ_0}$ to $\overline{IRQ_3}$, $\overline{INT_0}$ to $\overline{INT_7}$, $\overline{ADTRG}$, TMIB, TMCIV, TMRIV, FTCI, FTIA, FTIB, FTIC, FTID, TRGV	2	—	—	t_{cyc} t_{subcyc}	V_{CC} = 2.7 V to 5.5 V	Figure 13-3

Table 13-4 Serial Interface (SCI1) Timing

V_{CC} = 4.0 V to 5.5 V, V_{SS} = 0.0 V, T_a = –20°C to +75°C, unless otherwise specified.

Item	Symbol	Applicable Pins	Values Min	Typ	Max	Unit	Test Condition	Figure
Input serial clock cycle time	t_{scyc}	SCK_1,	2	—	—	t_{cyc}	V_{CC} = 2.7 V to 5.5 V	Figure 13-4
Input serial clock high width	t_{SCKH}	SCK_1,	0.4	—	—	t_{scyc}	V_{CC} = 2.7 V to 5.5 V	
Input serial clock low width	t_{SCKL}	SCK_1,	0.4	—	—	t_{scyc}	V_{CC} = 2.7 V to 5.5 V	
Input serial clock rise time	t_{SCKr}	SCK_1,	—	—	60	ns		
			—	—	80		V_{CC} = 2.7 V to 5.5 V	
Input serial clock fall time	t_{SCKf}	SCK_1,	—	—	60	ns		
			—	—	80		V_{CC} = 2.7 V to 5.5 V	
Serial output data delay time	t_{SOD}	SO_1,	—	—	200	ns		
			—	—	350		V_{CC} = 2.7 V to 5.5 V	
Serial input data setup time	t_{SIS}	SI_1,	180	—	—	ns		
			360	—	—		V_{CC} = 2.7 V to 5.5 V	
Serial input data hold time	t_{SIH}	SI_1,	180	—	—	ns		
			360	—	—		V_{CC} = 2.7 V to 5.5 V	

Table 13-5 Serial Interface (SCI3) Timing

V_{CC} = 2.7 V to 5.5 V, AV_{CC} = 2.7 V to 5.5 V, V_{SS} = 0.0 V, T_a = –20°C to +75°C, unless otherwise specified.

Item		Symbol	Values Min	Typ	Max	Unit	Test Conditions	Reference Figure
Input clock cycle	Asynchronous	t_{scyc}	4	—	—	t_{cyc}		Figure 13-5
	Synchronous		6	—	—			
Input clock pulse width		t_{SCKW}	0.4	—	0.6	t_{scyc}		Figure 13-5
Transmit data delay time(synchronous)		t_{TXD}	—	—	1	t_{cyc}	V_{CC} = 4.0 V to 5.5 V	Figure 13-6
			—	—	1			
Receive data setup time(synchronous)		t_{RXS}	200.0	—	1	ns	V_{CC} = 4.0 V to 5.5 V	Figure 13-6
			400.0	—	—			
Receive data hold time (synchronous)		t_{RXH}	200.0	—	—	ns	V_{CC} = 4.0 V to 5.5 V	Figure 13-6
			400.0	—	—			

13.2.4 DC Characteristics

Table 13-6 lists the DC characteristics of the HD6433644, the HD6433643, the HD6433642, the HD6433641 and the HD6433640.

Table 13-6 DC Characteristics

V_{CC} = 4.0 V to 5.5 V, V_{SS} = 0.0 V, T_a = –20°C to +75°C unless otherwise indicated.

			Values					
Item	**Symbol**	**Applicable Pins**	**Min**	**Typ**	**Max**	**Unit**	**Test Condition**	**Notes**
Input high voltage	V_{IH}	$\overline{RES}$, $\overline{INT}_0$ to $\overline{INT}_7$, $\overline{IRQ}_0$ to $\overline{IRQ}_3$, $\overline{ADTRG}$, TMIB,	0.8 V_{CC}	—	V_{CC} + 0.3	V		
		TMRIV, TMCIV, FTCI, FTIA, FTIB, FTIC, FTID, SCK_1, SCK_3, TRGV	0.9 V_{CC}	—	V_{CC} + 0.3		V_{CC} = 2.5 V to 5.5 V including subactive mode	
		SI_1, RXD $P1_0$, $P1_4$ to $P1_7$, $P2_0$ to $P2_2$, $P3_0$ to $P3_2$,	0.7 V_{CC}	—	V_{CC} + 0.3	V		
		$P5_0$ to $P5_7$, $P6_0$ to $P6_7$, $P7_3$ to $P7_7$, $P8_0$ to $P8_7$ $P9_0$ to $P9_4$	0.8 V_{CC}	—	V_{CC} + 0.3		V_{CC} = 2.5 V to 5.5 V including subactive mode	
		PB_0 to PB_7,	0.7 V_{CC}	—	AV_{CC} + 0.3			
			0.8 V_{CC}	—	AV_{CC} + 0.3		V_{CC} = 2.5 V to 5.5 V including subactive mode	
		OSC_1	V_{CC} – 0.5	—	V_{CC} + 0.3	V		
			V_{CC} – 0.3	—	V_{CC} + 0.3		V_{CC} = 2.5 V to 5.5 V including subactive mode	

Note: Connect the TEST pin to V_{SS}.

Table 13-6 DC Characteristics (cont)

V_{CC} = 4.0 V to 5.5 V, V_{SS} = 0.0 V, T_a = –20°C to +75°C unless otherwise indicated.

Item	Symbol	Applicable Pins	Values Min	Typ	Max	Unit	Test Condition	Notes
Input low voltage,	V_{IL}	$\overline{RES}$,, $\overline{INT_0}$ to $\overline{INT_7}$ $\overline{IRQ_0}$ to $\overline{IRQ_3}$, $\overline{ADTRG}$, TMIB,	–0.3	—	0.2 V_{CC}	V		
		TMRIV, TMCIV, FTCI, FTIA, FTIB, FTIC, FTID, SCK_1, SCK_3, TRGV	–0.3	—	0.1 V_{CC}		V_{CC} = 2.5 V to 5.5 V including subactive mode	
		SI_1, RXD, $P1_0$, $P1_4$ to $P1_7$, $P2_0$ to $P2_2$, $P3_0$ to $P3_2$, $P5_0$ to $P5_7$,	–0.3	—	0.3 V_{CC}	V		
		$P6_0$ to $P6_7$, $P7_3$ to $P7_7$, $P8_0$ to $P8_7$, $P9_0$ to $P9_4$, PB_0 to PB_7	–0.3	—	0.2 V_{CC}	V	V_{CC} = 2.5 V to 5.5 V including subactive mode	
		OSC_1	–0.3	—	0.5	V		
			–0.3	—	0.3		V_{CC} = 2.5 V to 5.5 V including subactive mode	

Note: Connect the TEST pin to V_{SS}.

Table 13-6 DC Characteristics (cont)

V_{CC} = 4.0 V to 5.5 V, V_{SS} = 0.0 V, T_a = –20°C to +75°C unless otherwise indicated.

Item	Symbol	Applicable Pins	Values Min	Typ	Max	Unit	Test Condition	Notes
Output high voltage	V_{OH}	$P1_0$, $P1_4$ to $P1_7$,	V_{CC} – 1.0	—	—	V	$–I_{OH}$ = 1.0 mA	
		$P2_0$ to $P2_2$,	V_{CC} – 1.0	—	—		$–I_{OH}$ = 1.5 mA	
		$P3_0$ to $P3_2$, $P5_0$ to $P5_7$, $P6_0$ to $P6_7$, $P7_3$ to $P7_7$, $P8_0$ to $P8_7$, $P9_0$ to $P9_4$	V_{CC} – 0.5	—	—		V_{CC} = 2.5 V to 5.5 V $–I_{OH}$ = 0.1 mA	
Output low voltage	V_{OL}	$P1_0$, $P1_4$ to $P1_7$, $P2_0$ to $P2_2$, $P3_0$ to $P3_2$, $P5_0$ to $P5_7$,	—	—	0.6	V	I_{OL} = 1.6 mA	
		$P7_3$ to $P7_7$, $P8_0$ to $P8_7$, $P9_0$ to $P9_4$	—	—	0.4		V_{CC} = 2.5 V to 5.5 V I_{OL} = 0.4 mA	
		$P6_0$ to $P6_4$	—	—	1.0	V	I_{OL} = 10.0 mA	
			—	—	0.4		I_{OL} = 1.6 mA	
			—	—	0.4		V_{CC} = 2.5 V to 5.5 V I_{OL} = 0.4 mA	
Input/ output leakage current	$\lvert I_{IL} \rvert$	OSC_1, $P1_0$, $P1_4$ to $P1_7$, $P2_0$ to $P2_2$, $P3_0$ to $P3_2$, $P5_0$ to $P5_7$, $P6_0$ to $P6_7$, $P7_0$ to $P7_7$, $P8_0$ to $P8_7$, $P9_0$ to $P9_4$	—	—	1.0	µA	V_{IN} = 0.5 V to (V_{CC} – 0.5 V)	
		PB_0 to PB_7	—	—	1.0		V_{IN} = 0.5 V to AV_{CC} – 0.5 V	

Table 13-6 DC Characteristics (cont)

V_{CC} = 4.0 V to 5.5 V, V_{SS} = 0.0 V, T_a = –20°C to +75°C unless otherwise indicated.

Item	Symbol	Applicable Pins	Values Min	Typ	Max	Unit	Test Condition	Notes
Input leakage current	$\lvert I_{IL} \rvert$	$\overline{RES}$, IRQ_0	—	—	1	µA	V_{IN} = 0.5 V to (V_{CC} – 0.5 V)	
Pull-up MOS current	$-I_P$	$P1_0$, $P1_4$ to $P1_7$, $P3_0$ to $P3_2$	50	—	300	µA	V_{CC} = 5 V, V_{IN} = 0 V	
		P50 to P57	—	25	—		V_{CC} = 2.7 V, V_{IN} = 0 V	Reference value
Input capacitance	C_{IN}	All input pins except $\overline{RES}$,	—	—	15.0	pF	f = 1 MHz, V_{IN} = 0 V, T_a = 25°C	
		$\overline{RES}$	—	—	15.0			
		IRQ_0	—	—	15.0			
Active mode current dissipation	I_{OPE1}	V_{CC}	—	10	15	mA	Active (high-speed) mode V_{CC} = 5 V, f_{OSC} = 10 MHz	1, 2
			—	5	—		V_{CC} = 2.5 V, f_{OSC} = 10 MHz	
	I_{OPE2}	V_{CC}	—	2	3	mA	Active (medium-speed) mode V_{CC} = 5 V, f_{OSC} = 10 MHz	1, 2
			—	1	—		V_{CC} = 2.5 V f_{OSC} = 10 MHz	
Sleep mode current dissipation	I_{SLEEP1}	V_{CC}	—	5	7	mA	Sleep (high-speed) mode V_{CC} = 5 V, f_{OSC} = 10 MHz	1, 2
			—	2	—		V_{CC} = 2.5 V f_{OSC} = 10 MHz	
	I_{SLEEP2}	V_{CC}	—	2	3	mA	Sleep (medium-speed) mode V_{CC} = 5 V, f_{OSC} = 10 MHz	1, 2
			—	1	—		V_{CC} = 2.5 V, f_{OSC} = 10 MHz	
Subactive mode current dissipation	I_{SUB}	V_{CC}	—	10	20	µA	V_{CC} = 2.5 V 32-kHz crystal oscillator ($\phi_{SUB} = \phi_W/2$)	1, 2
			—	10	—	µA	V_{CC} = 2.5 V 32-kHz crystal oscillator ($\phi_{SUB} = \phi_W/8$)	1, 2 Reference value

Table 13-6 DC Characteristics (cont)

V_{CC} = 4.0 V to 5.5 V, V_{SS} = 0.0 V, T_a = –20°C to +75°C unless otherwise indicated.

Item	Symbol	Applicable Pins	Values Min	Typ	Max	Unit	Test Condition	Notes
Subsleep mode current dissipation	I_{SUBSP}	V_{CC}	—	5	10	µA	V_{CC} = 2.5 V 32-kHz crystal oscillator ($\phi_{SUB} = \phi_W/2$)	1, 2
Watch mode current dissipation	I_{WATCH}	V_{CC}	—	—	6	µA	V_{CC} = 2.5 V 32-kHz crystal oscillator	1, 2
Standby mode current dissipation	I_{STBY}	V_{CC}	—	—	5	µA	32-kHz crystal oscillator not used	1, 2
RAM data retaining voltage	V_{RAM}	V_{CC}	2	—	—	V		1, 2

Notes: 1. Pin states during current measurement are given below.
2. Excludes current in pull-up MOS transistors and output buffers.

Mode	$\overline{RES}$ Pin	Internal State	Other Pins	Oscillator Pins
Active (high-speed) mode	V_{CC}	Operates	V_{CC}	System clock oscillator: ceramic or crystal
Active (medium-speed) mode		Operates (ϕOSC/128)		Subclock oscillator: Pin X_1 = V_{CC}
Sleep (high-speed) mode	V_{CC}	Only timers operate	V_{CC}	
Sleep (medium-speed) mode		Only timers operate (ϕOSC/128)		
Subactive mode	V_{CC}	Operates	V_{CC}	System clock oscillator:
Subsleep mode	V_{CC}	Only timers operate, CPU stops	V_{CC}	ceramic or crystal Subclock oscillator:
Watch mode	V_{CC}	Only time base perates, CPU stops	V_{CC}	crystal
Standby mode	V_{CC}	CPU and timers both stop	V_{CC}	System clock oscillator: ceramic or crystal Subclock oscillator: Pin X_1 = V_{CC}

Table 13-6 DC Characteristics (cont)

V_{CC} = 4.0 V to 5.5 V, V_{SS} = 0.0 V, T_a = –20°C to +75°C, unless otherwise indicated.

Item		Values				
		Symbol	Min	Typ	Max	Unit
Allowable output low current (per pin)	Output pins except port 6	I_{OL}	—	—	2	mA
	Port 6		—	—	10	
Allowable output low current (total)	Output pins except port 6	ΣI_{OL}	—	—	40	mA
	Port 6		—	—	80	
Allowable output high current (per pin)	All output pins	$-I_{OH}$	—	—	2	mA
Allowable output high current (total)	All output pins	$\Sigma(-I_{OH})$	—	—	30	mA

13.2.5 AC Characteristics

Table 13-7 lists the control signal timing, and tables 13-8 and 13-9 list the serial interface timing of the HD6433644, the HD6433643, the HD6433642, the HD6433641 and the HD6433640.

Table 13-7 Control Signal Timing

V_{CC} = 4.0 V to 5.5 V, V_{SS} = 0.0 V, T_a = –20°C to +75°C, unless otherwise specified.

Item	Symbol	Applicable Pins	Values Min	Typ	Max	Unit	Test Condition	Reference Figure
System clock oscillation frequency	f_{OSC}	OSC_1, OSC_2	2	—	10	MHz		
			2	—	5		V_{CC} = 2.5 V to 5.5 V	
OSC clock (ϕ_{OSC}) cycle time	t_{OSC}	OSC_1, OSC_2	100	—	1000	ns		*1
			200	—	1000		V_{CC} = 2.5 V to 5.5 V	Figure 13-1
System clock (ϕ)cycle time	t_{cyc}		2	—	128	t_{OSC}	V_{CC} = 2.5 V to 5.5 V	*1
			—	—	25.5	µs		
Subclock oscillation frequency	f_W	X_1, X_2	—	32.768	—	kHz	V_{CC} = 2.5 V to 5.5 V	
Watch clock (ϕ_W) cycle time	t_W	X_1, X_2	—	30.5	—	µs	V_{CC} = 2.5 V to 5.5 V	
Subclock (ϕ_{SUB}) cycle time	t_{subcyc}		2	—	8	t_W	V_{CC} = 2.5 V to 5.5 V	2
Instruction cycle time			2	—	—	t_{cyc} t_{subcyc}	V_{CC} = 2.5 V to 5.5 V	
Oscillation stabilization time(crystal oscillator)	t_{rc}	OSC_1, OSC_2	—	—	40	ms		
			—	—	60		VCC = 2.5 V to 5.5 V	
Oscillation stabilization time(ceramic oscillator)	t_{rc}	OSC_1, OSC_2	—	—	20	ms		
			—	—	40		VCC = 2.5 V to 5.5 V	
Oscillation stabilization time	t_{rc}	X_1, X_2	—	—	2	s	V_{CC} = 2.5 V to 5.5 V	
External clock high width	t_{CPH}	OSC_1	40	—	—	ns		Figure 13-1
			80	—	—		V_{CC} = 2.5 V to 5.5 V	
External clock low width	t_{CPL}	OSC_1	40	—	—	ns		Figure 13-1
			80	—	—		V_{CC} = 2.5 V to 5.5 V	
External clock rise time	t_{CPr}		—	—	15	ns		
			—	—	20		V_{CC} = 2.5 V to 5.5 V	
External clock fall time	t_{CPf}		—	—	15	ns		
			—	—	20		V_{CC} = 2.5 V to 5.5 V	
Pin $\overline{RES}$ low width	t_{REL}	$\overline{RES}$	10	—	—	t_{cyc}	V_{CC} = 2.5 V to 5.5 V	Figure 13-2

Notes: 1. A frequency between 1 MHz to 10 MHz is required when an external clock is input.
2. Selected with SA1 and SA0 of system clock control register 2 (SYSCR2).

Table 13-7 Control Signal Timing (cont)

V_{CC} = 4.0 V to 5.5 V, V_{SS} = 0.0 V, T_a = –20°C to +75°C, unless otherwise specified.

Item	Symbol	Applicable Pins	Values Min	Typ	Max	Unit	Test Condition	Figure
Input pin high width	t_{IH}	$\overline{IRQ_0}$ to $\overline{IRQ_3}$, $\overline{INT_0}$ to $\overline{INT_7}$, $\overline{ADTRG}$, TMIB, TMCIV, TMRIV, FTCI, FTIA, FTIB, FTIC, FTID, TRGV	2	—	—	t_{cyc} t_{subcyc}	V_{CC} = 2.5 V to 5.5 V	Figure 13-3
Input pin low width	t_{IL}	$\overline{IRQ_0}$ to $\overline{IRQ_3}$, $\overline{INT_0}$ to $\overline{INT_7}$, $\overline{ADTRG}$, TMIB, TMCIV, TMRIV, FTCI, FTIA, FTIB, FTIC, FTID, TRGV	2	—	—	t_{cyc} t_{subcyc}	V_{CC} = 2.5 V to 5.5 V	Figure 13-3

Table 13-8 Serial Interface (SCI1) Timing

V_{CC} = 4.0 V to 5.5 V, V_{SS} = 0.0 V, T_a = –20°C to +75°C, unless otherwise specified.

			Values					
Item	Symbol	Applicable Pins	Min	Typ	Max	Unit	Test Condition	Figure
Input serial clock cycle time	t_{scyc}	SCK_1,	2	—	—	t_{cyc}	V_{CC} = 2.5 V to 5.5 V	Figure 13-4
Input serial clock high width	t_{SCKH}	SCK_1,	0.4	—	—	t_{scyc}	V_{CC} = 2.5 V to 5.5 V	
Input serial clock low width	t_{SCKL}	SCK_1,	0.4	—	—	t_{scyc}	V_{CC} = 2.5 V to 5.5 V	
Input serial clock rise time	t_{SCKr}	SCK_1,	—	—	60	ns		
			—	—	80		V_{CC} = 2.5 V to 5.5 V	
Input serial clock fall time	t_{SCKf}	SCK_1,	—	—	60	ns		
			—	—	80		V_{CC} = 2.5 V to 5.5 V	
Serial output data delay time	t_{SOD}	SO_1,	—	—	200	ns		
			—	—	350		V_{CC} = 2.5 V to 5.5 V	
Serial input data setup time	t_{SIS}	SI_1,	180	—	—	ns		
			360	—	—		V_{CC} = 2.5 V to 5.5 V	
Serial input data hold time	t_{SIH}	SI_1,	180	—	—	ns		
			360	—	—		V_{CC} = 2.5 V to 5.5 V	

Table 13-9 Serial Interface (SCI3) Timing

V_{CC} = 2.7 V to 5.5 V, AV_{CC} = 2.5 V to 5.5 V, V_{SS} = 0.0 V, T_a = –20°C to +75°C, unless otherwise specified.

Item		Symbol	Values Min	Typ	Max	Unit	Test Conditions	Reference Figure
Input clock cycle	Asynchronous	t_{scyc}	4	—	—	t_{cyc}		Figure 13-5
	Synchronous		6	—	—			
Input clock pulse width		t_{SCKW}	0.4	—	0.6	t_{scyc}		Figure 13-5
Transmit data delay time (synchronous)		t_{TXD}	—	—	1	t_{cyc}	V_{CC} = 4.0 V to 5.5 V	Figure 13-6
			—	—	1			
Receive data setup time (synchronous)		t_{RXS}	200.0	—	1	ns	V_{CC} = 4.0 V to 5.5 V	Figure 13-6
			400.0	—	—			
Receive data hold time (synchronous)		t_{RXH}	200.0	—	—	ns	V_{CC} = 4.0 V to 5.5 V	Figure 13-6
			400.0	—	—			

13.2.6 A/D Converter Characteristics

Table 13-10 shows the A/D converter characteristics of the HD6473644, the HD6433644, the HD6433643, the HD6433642, the HD6433641 and the HD6433640.

Table 13-10 A/D Converter Characteristics

V_{CC} = 2.7 V to 5.5 V, V_{SS} = AV_{SS} = 0.0 V, T_a = –20°C to +75°C, unless otherwise specified.

			Values					
Item	Symbol	Applicable Pins	Min	Typ	Max	Unit	Test Condition	Reference Figure
Analog power supply voltage	AV_{CC}	AV_{CC}	2.7	—	5.5	V		*1
Analog input voltage	AV_{IN}	AN_0 to AN_7	AV_{SS} – 0.3	—	AV_{CC} + 0.3	V		
Analog power supply current	AI_{OPE}	AV_{CC}	—	—	1.5	mA	AV_{CC} = 5 V	
	AI_{STOP1}	AV_{CC}	—	150	—	µA		*2 Reference value
	AI_{STOP2}	AV_{CC}	—	—	5	µA		*3
Analog input capacitance	C_{AIN}	AN_0 to AN_7	—	—	30	pF		
Allowable signal source impedance	R_{AIN}		—	—	5.0	kΩ		
Resolution			—	—	8	bit		
Nonlinearity error			—	—	±2.0	LSB		
Quantization error			—	—	±0.5	LSB		
Absolute accuracy			—	—	±2.5	LSB		
			—	—	—	LSB		
Conversion time			12.4	—	124	µs		

Notes: 1. Set AV_{CC} = V_{CC} when the A/D converter is not used.
2. AI_{STOP1} is the current in active and sleep modes while the A/D converter is idle.
3. AI_{STOP2} is the current at reset and in standby, watch, subactive, and subsleep modes while the A/D converter is idle.

13.3 Operation Timing

Figures 13-1 to 13-9 show timing diagrams.

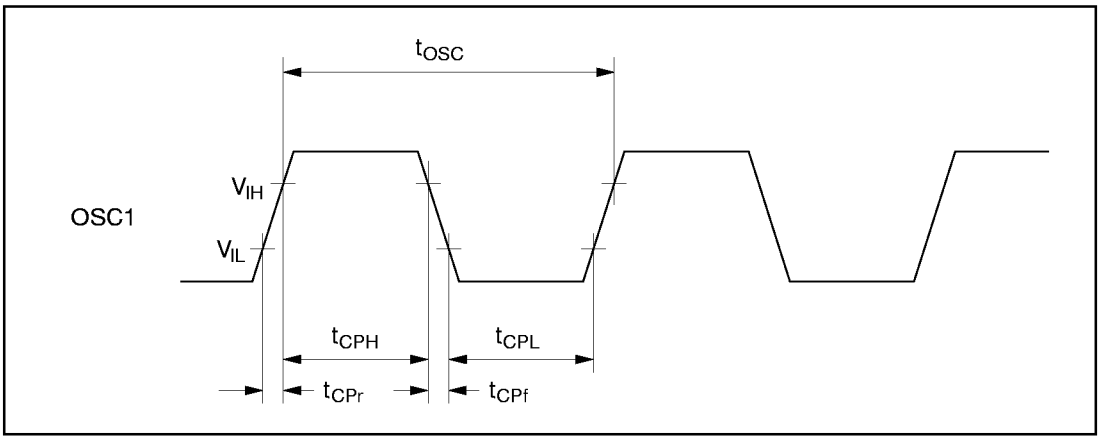


Figure 13-1 System Clock Input Timing

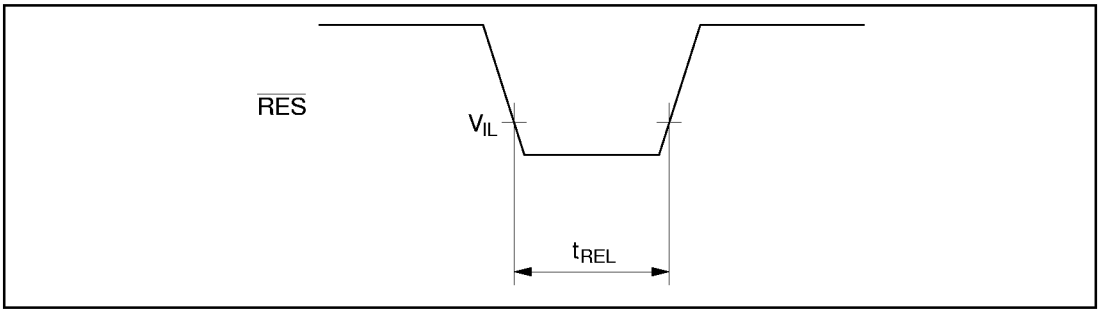


Figure 13-2 $\overline{RES}$ Low Width

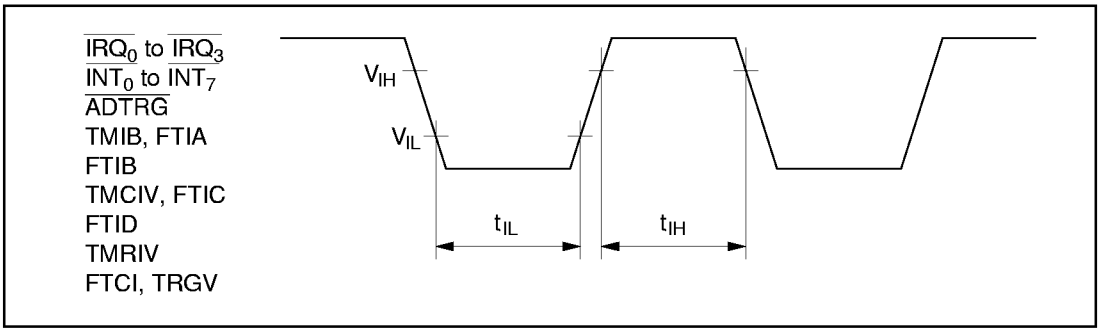
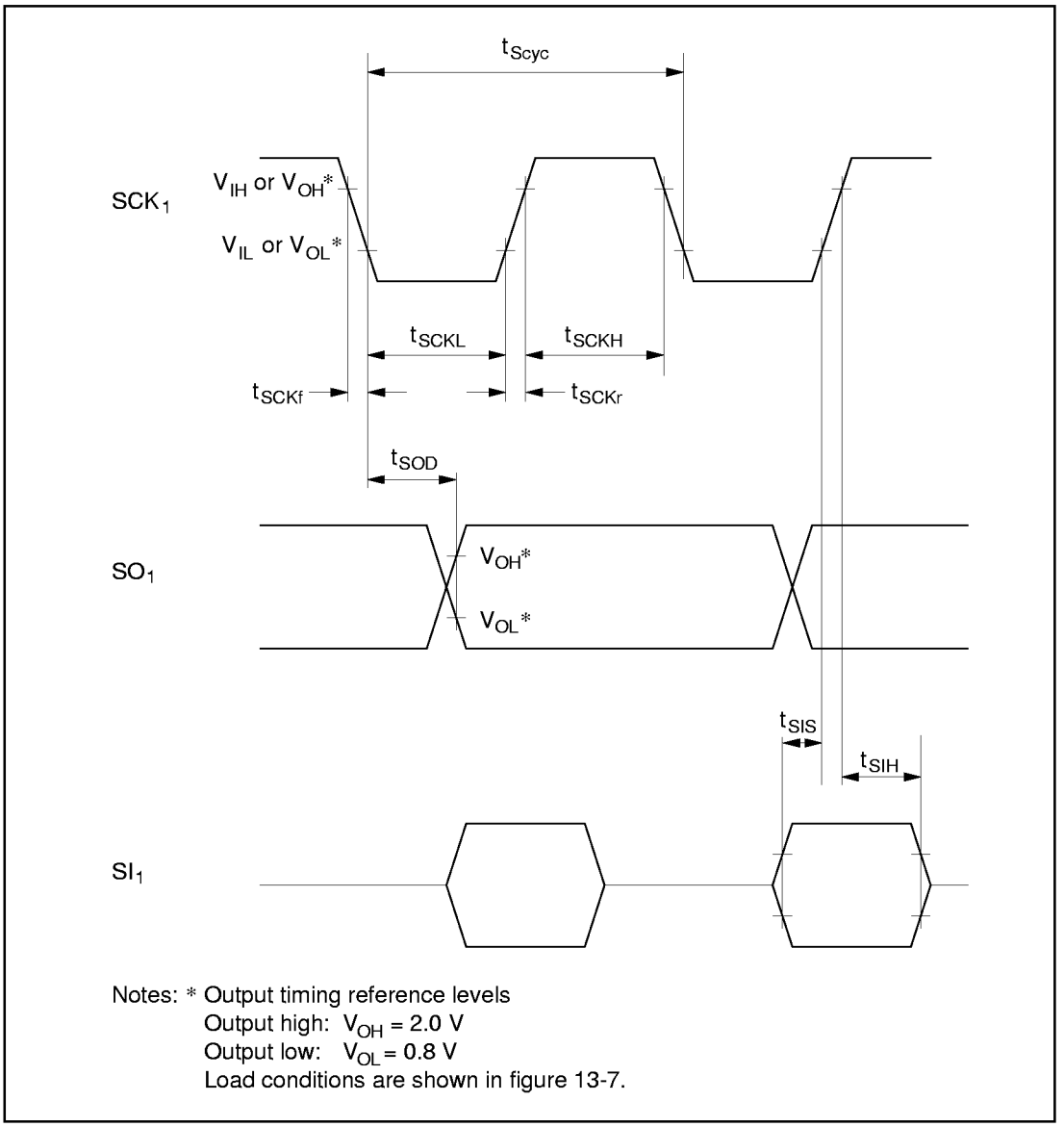


Figure 13-3 Input Timing



Notes: * Output timing reference levels
Output high: V_{OH} = 2.0 V
Output low: V_{OL} = 0.8 V
Load conditions are shown in figure 13-7.

Figure 13-4 Serial Interface 1 Input/Output Timing

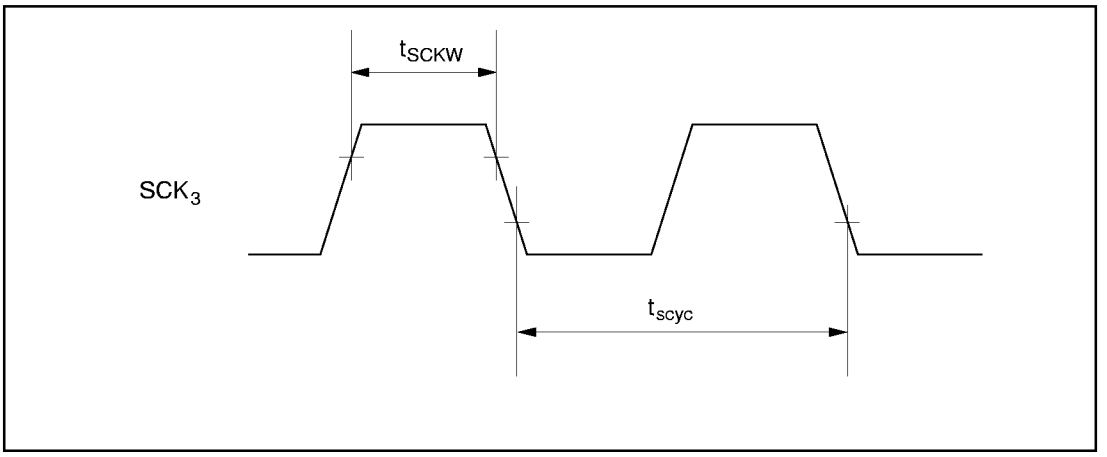
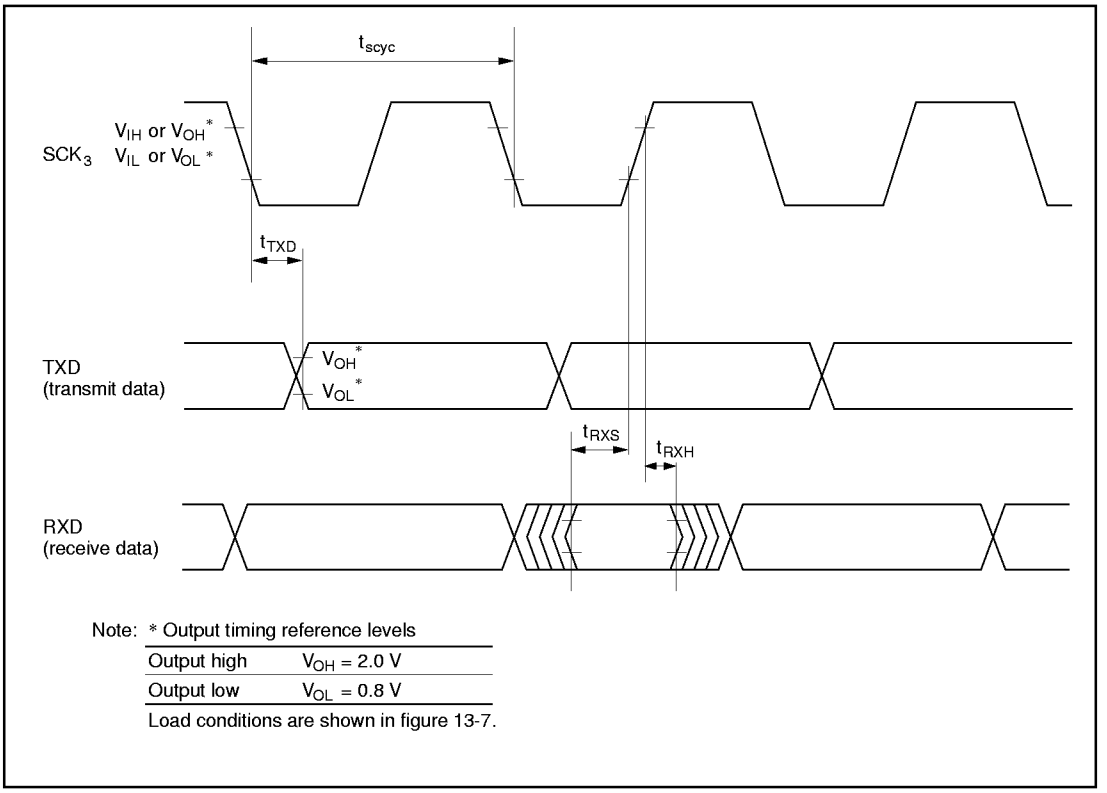


Figure 13-5 SCK_3 Input Clock Timing



Note: * Output timing reference levels

Output high	V_{OH} = 2.0 V
Output low	V_{OL} = 0.8 V

Load conditions are shown in figure 13-7.

Figure 13-6 Serial Interface 3 Synchronous Mode

13.4 Output Load Circuit

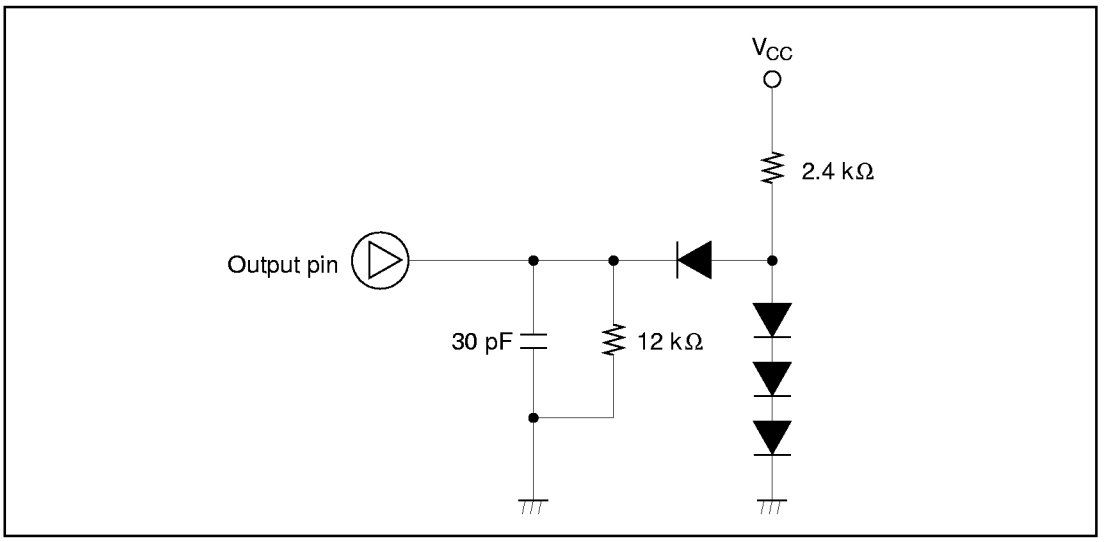


Figure 13-7 Output Load Condition