Dual VCO/PLL Synthesizer With IF Up-Converter

FEATURES

- **Low Phase Noise**
- **Image Reject Upconverter**
- **Dual VCO/PLL For Double Up Conversion Architecture**
- **On-Chip VCO, Resonator and PLL Only Requires Off-Chip Loop Filter**
- **External S-Band VCO Option**
- **5-Bit Transmit Level Control, 32 dB in 1 dB Steps**

SPECIFICATIONS

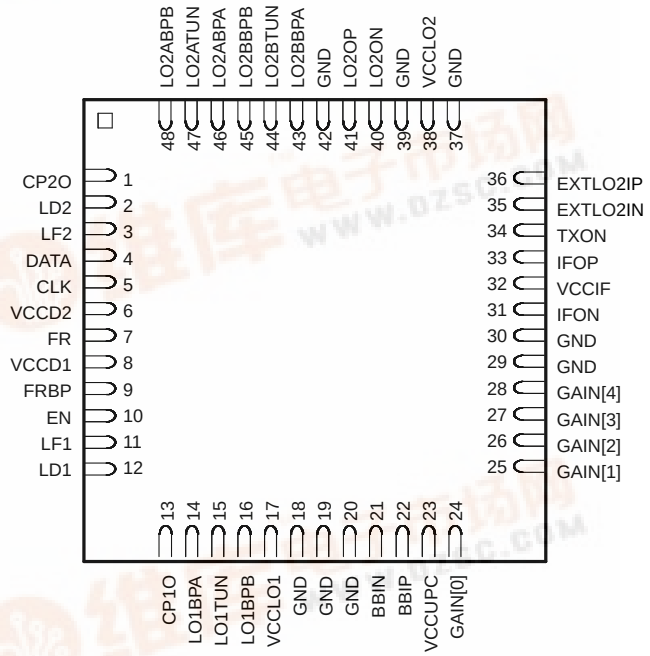
- **S-Band LO Frequency Range:**
  - **– TRF1121: 1500 to 2500 MHz**
  - **– TRF1221: 1700 to 3600 MHz**
- **UHF LO Frequency Range: 250 to 350 MHz**
- **Input Frequency Range: 10 MHz to 70 MHz**
- **S-Band LO Phase Noise Typical 0.5 rms (100 Hz to 1 MHz)**
- **Output Power Range From –32 dBm to 0 dBm in 1 dB Steps (500-mVpp Diff Input)**
- **Minimum UHF LO Step Size of 50 kHz For TRF1121 and 62.5 kHz for TRF1221**
- **Image Rejection: –50 dBc, Typical (20–40 MHz Tx IF Input)**
- **LO Leakage: –36 dBm, Typical**
- **3rd Order IMD: < –60 dBc In Max Gain**

DESCRIPTION

The TRF1121/TRF1221 are VHF-UHF upconverters with integrated UHF and S-band frequency synthesizers for radio applications in the 2GHz to 4 GHz range. The IC performs the first up-conversion and generates the local oscillator (LO) for the second up-conversion. The device uniquely integrates an image reject mixer, IF gain blocks, 5-bit gain control, and two complete phase locked loop (PLL) circuits including: VCOs, resonator circuit, varactors, dividers, and phase detectors.

The TRF1121/TRF1221 are designed to function as part of complete 2.5-GHz and 3.5-GHz radio chipsets, respectively. In the chipset, the transmit chain operates as a double up converter from an IF frequency input (typically from a baseband modem's DAC) to an RF output frequency. The TRF1121/ TRF1221 performs the first up conversion from IF signals in the range of 10 MHz to 60 MHz to a second IF frequency in the range of 300 MHz to 360 MHz. The radio chipset features sufficient linearity, phase noise, and dynamic range to work in either single carrier or multi-carrier, line-of-sight or non-line-of-sight, standard (IEEE 802.16), or proprietary systems. Due to the modular nature of the chipset, it is ideal for use in systems that employ transmit or receive diversity.

LPCC–48 PACKAGE
(TOP VIEW)

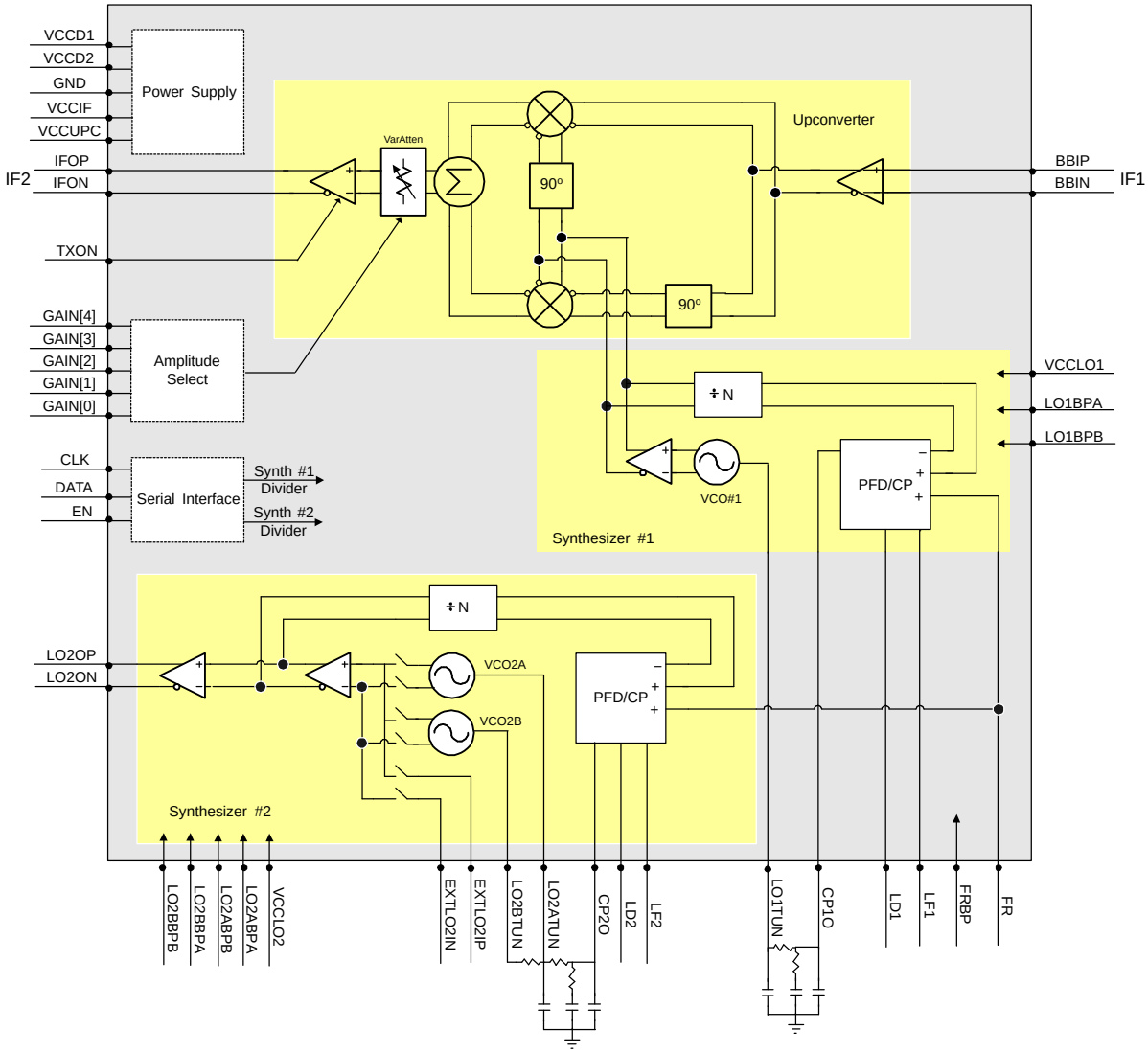


This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

BLOCK DIAGRAM

The detailed block diagram and the pin-out of the ASIC are shown in Figure 1 and Table 1.



TERMINAL FUNCTIONS

TERMINAL		I/O	TYPE	DESCRIPTION
NO.	NAME			
1	CP2O	O	Analog	Synthesizer 2 charge pump output
2	LD2	O	Digital	Synthesizer 2 lock detect output, High is locked.
3	LF2	O	Analog	Lock detect filter capacitor for LO2, 0.01 µF typical 100 kΩ pull-up(1)
4	DATA	I	Digital	Serial interface data input
5	CLK	I	Digital	Serial interface clock input
6	VCCD2	I	Power	+5 V power for digital
7	FR	I	Analog	18-MHz reference clock input, HCMOS input. (DC level = 2.5 V)
8	VCCD1	I	Power	+5 V power for digital
9	FRBP	O	Analog	Reference frequency bypass. Internally biased to 2.5 V.
10	EN	I	Digital	Serial interface load enable (active high)
11	LF1	O	Analog	Lock detect filter capacitor for LO1, 0.01 µF typical 100 kΩ(1)
12	LD1	O	Digital	Synthesizer 1 lock detect output, High is locked.
13	CP1O	O	Analog	Synthesizer 1 charge pump output
14	LO1BPA	O	Analog	Not connected for normal operation. DC bias nominal 1.8 V. Do not ground or connect to any other pin.
15	LO1TUN	I	Analog	VCO synthesizer 1 tuning port
16	LO1BPB	O	Analog	Bypass capacitor for LO1 0.1 µF (min) DCV =1.0 V
17	VCCLO1	I	Power	VCC for LO1
18, 19, 20, 29, 30, 37, 39, 42	GND		Power	Ground
21	BBIN	I	Analog	Baseband IF input (2 kΩ diff) negative, dc-coupled, Internal voltage is 4 V DC
22	BBIP	I	Analog	Baseband IF input (2 kΩ diff) positive, dc-coupled, Internal voltage is 4 V DC
23	VCCUPC	I	Power	+5V power Analog
24	GAIN[0]	I	Digital	Gain control bit 0 (LSB) – Logic low induces 1-dB attenuation
25	GAIN[1]	I	Digital	Gain control bit 1 – Logic low induces 2-dB attenuation
26	GAIN[2]	I	Digital	Gain control bit 2 – Logic low induces 4-dB attenuation
27	GAIN[3]	I	Digital	Gain control bit 3 – Logic low induces 8-dB attenuation
28	GAIN[4]	I	Digital	Gain control bit 4 (MSB) – Logic low induces 16-dB attenuation
31	IFON	O	Analog	IF analog output (100 Ω diff) negative, dc-coupled, Internal voltage is 2.1 V DC
32	VCCIF	I	Power	+5 V power Analog
33	IFOP	O	Analog	IF analog output (100 Ω diff) positive, dc-coupled, Internal voltage is 2.1 V DC
34	TXON	I	Digital	IF amplifier enable active high
35	EXTLO2IN	I	Analog	External input for LO2 (differential) negative and logic level for VCO select.
36	EXTLO2IP	I	Analog	External input for LO2 (differential) positive and logic level for VCO select.
38	VCCLO2	I	Power	VCC for LO2 A and B
40	LO2ON	O	Analog	LO2 output (differential) Negative and positive VCC bias (+5 V) for LO buffer amp.
41	LO2OP	O	Analog	LO2 output (differential) Positive and positive VCC bias (+5 V) for LO buffer amp.
43	LO2BBPA	O	Analog	Not connected for normal operation. DC bias nominal 1.8 V. Do not ground or connect to any other pin.
44	LO2BTUN	I	Analog	LO2B Tune Port
45	LO2BBPB	O	Analog	Bypass cap. for LO2B 0.1 µF (min) DCV = 1 V
46	LO2ABPA	O	Analog	Not connected for normal operation. DC bias nominal 1.8 V. Do not ground or connect to any other pin.
47	LO2ATUN	I	Analog	LO2A tune port
48	LO2ABPB	O	Analog	Bypass capacitor for LO2A 0.1 µF (min) DCV = 1 V
Back	Back side of package has metal base that must be grounded for thermal and RF performance			

(1) Current leakage on the order of 10µA through the capacitor or by any other means from either LF pin can cause false loss of lock signals. The two pullup resistors (R16 and R17) in Figure 23 reduce this sensitivity.

ABSOLUTE MAXIMUM RATINGS

over operating free-air temperature range (unless otherwise noted)

		VALUE	UNIT
V_{CC}	DC supply voltage	0 to 5.5	V
I_{CC}	DC supply current	270	mA
P_{in}	RF input power	20	dBm
T_J	Junction temperature	150	°C
P_{diss}	Power dissipation	1.5	W
	Digital input voltage	–0.3 to V_{CC}+0.3	V
	Analog input voltage	V_{CC}	V
θ_{JC}	Thermal resistance junction-to-ambien(1)	25	°C/W
T_{stg}	Storage temperature	–40 to 105	°C
T_{op}	Operating temperature	–40 to 85	°C
	Lead temperature, 40 Sec Max	260	°C

(1) Thermal resistance is junction-to-ambient assuming thermal pad with nine thermal vias under package metal base. See the recommended PCB layout.

ELECTRICAL CHARACTERISTICS

The characteristics listed in the following tables are at V_{CC} = 5 V, T_A = 25°C(unless otherwise noted)

DC CHARACTERISTICS						
PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{CC}	DC supply voltage	T_A = 25°C	4.8		5.2	V
I_{CC_TxON}	Supply current	T_A = 25°C, TXON enabled		180		mA
I_{CC_TxOFF}		T_A = 25°C, TXON disabled		130		

UPCONVERTER CHARACTERISTICS

Input signal 500 mVpp, V_{CC} = 5 V, 25°C, IF1 = 26 MHz, IF2 = 325 MHz unless otherwise stated

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
F_{IF1}	Input center frequency	See Figure 3		26		MHz
F_{IF2}	Output frequency range		270		400	MHz
V_{BB}	Input signal level	Peak-to-peak differential		500	1000	mV
Z_{IF1}	Input IF1 differential impedance	See Application Note TDB		2		kW
P_{out}	Output power (maximum gain)	Measured at IF2 (IF2OP,IF2ON) With 500-mVpp differential input to IF1(BBIP,BBIN) and GAIN[4:0] = 11111		0		dBm
	Output power (minimum gain)	Measured at IF2 (IF2OP,IF2ON) With 500-mVpp differential input to IF1(BBIP,BBIN), GAIN[4:0] = 00000		–32		dBm
ΔG_{max}	Gain flatness	300 MHz < IF2 < 330 MHz		±0.3		dB
ΔP_{STEP}	Gain step size		0.7	1	1.3	dB
OP1dB	Output power a 1-dB gain compression	GAIN[4:0] = 11111		12		dBm
OIP3	Output third order intercept	For any gain setting		24		dBm
IR	Image rejection	IF1 = 15 to 45 MHz			–30	dBc
P_{LO1}	LO1 leakage	At GAIN[4:0] = 11111 decreases dB for dB as gain state is changed		–36		dBm
NF	Input noise figure	At max gain (GAIN[4:0]=11111), no worse then 1-dB degradation per 1 dB of attenuation		27		dB
Z_{IF2}	Output RF impedance	Differential		100		Ω

SYNTHESIZER #1 (UHF-BAND PLL) CHARACTERISTICS

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
f_{Ref}	Reference frequency	See Table 7		18		MHz
f_{VCO1}	Frequency	TRF1121 and TRF1221	250		350	MHz
$£_{FRVCO1}$	Free running VO1 SSB phase noise at 100 kHz			–115		dBc/Hz
$£_{LD\ LO1}$	Locked synthesizer 1 SSB phase noise at 10 kHz			–115		dBc/Hz
$£_{LD\ LO1}$	Locked synthesizer 1 SSB phase noise at 100 kHz			–115		dBc/Hz
$f_{LD\ LO1}$	Locked synthesizer 1 integrated RMS phase noise	100 Hz to 1 MHz			0.2	deg
MS_{LO1}	Tuning sensitivity	For V_{LO1TUN} > 2 V	30		60	MHz/V
Δf_{LO1}	Step Size	TRF1121, 18-MHz reference input	50			kHz
		TRF1221, 18-MHz reference input	62.5			
$R_{RS\ LO1}$	Reference spur rejection		–70			dBc
$R_{FS\ LO1}$	Fractional spurs rejection			-60		dBc

SYNTHESIZER #2 (S-BAND PLL) CHARACTERISTICS

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
f_{Ref}	Reference frequency	See Table 7		18		MHz
f_{LO2A}	Output frequency, VCO#2A	TRF1121	1500		2100	MHz
		TRF1221	1700		2450	
f_{LO2B}	Output frequency, VCO#2B	TRF1121	1700		2500	MHz
		TRF1221	2400		3600	
MS_{LO2A}	Tuning sensitivity, VCO#2A	TRF1121 For VLO1TUN >2 V	150		350	MHz/V
		TRF1221 For VLO1TUN >2 V	200		400	
MS_{LO2B}	Tuning sensitivity, VCO#2B	TRF1121 For VLO1TUN >2 V	200		400	MHz/V
		TRF1221 For VLO1TUN >2 V	350		550	
Δf_{LO2}	Step size	For 18-MHz ref input	1			MHz
P_{LO2}	Output power level	Measured into a 100-Ω differential load at the LO1OP/N port		-3		dBm
$£_{FR\ VCO2}$	Free running SSB phase noise at 100 kHz	Measured into a 100-Ω differential load at the LO1OP/N port		–100		dBc/Hz
$£_{LD\ LO2}$	Locked synthesizer SSB phase noise at 10 kHz	Measured into a 100-Ω differential load at the LO2OP/N port with loop filter set to 400 kHz nominal		– 102	–97	dBc/Hz
	Locked synthesizer SSB phase noise at 100 kHz			–100	–95	
$\phi_{LD\ LO2}$	Integrated RMS phase noise	Locked, 100 Hz to 1 MHz		0.5	1	Deg
$R_{RS\ LO2}$	Reference sideband suppression	Measured into a 100-Ω differential load at the LO1OP/N port. PLL loop bandwidth ~ 400 kHz		–65	–60	dBc
$R_{FS\ LO2}$	Fractional spur suppression	At 1 MHz offset (Loop BW ~400 kHz)		–50	–45	dBc
		At 2 MHz offset (Loop BW ~400 kHz)		–65	–60	
		All others		–70	–70	
$R_{H\ LO2}$	Harmonics suppression	Measured into a 100-Ω differential load at the LO1OP/N port			–20	dBc
RL_{LO2}	Output return loss	Measured into a 100-Ω differential load at the LO1OP/N port	–11	–16		dB
P_{extVCO}	Ext VCO input power			–13		dBm
RL_{extVCO}	Ext VCO port input ret. loss	Differential mode	–10	–15		dB
$Z_{in\ extVCO}$	Ext VCO port input impedance	Differential mode		100		Ω

INPUT REFERENCE REQUIREMENTS

Conditions: Signal BW = 6 MHz nom, 15 dB maximum loss IF2 SAW filter. See Figure 19

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
f_{Ref}	Reference frequency			18		MHz
	Temperature stability	Customer requirements				PPM
V_{FR}	Ref. source input voltage(1)	HCMOS Output	4	4.5	5	Vpp
DC_{fref}	Reference Input Symmetry	Waveform Duty Cycle	40%		60%	
t_{FR}	Reference source pulse rise time	10% to 90% of maximum voltage transition		1	4	nsec
f_{FR}	Reference Phase Noise at 10 kΩ offset			–153	–150	dBc/Hz

(1) Note that for source peak-to-peak voltages of less than 4 V and dc-component other than 2.5-V degradation of the close-in phase noise may occur. For oscillators with no dc-component, a dc-voltage may be applied using a voltage divider (see the schematic) .

AC TIMING, SERIAL BUS INTERFACE

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
CD_I	Clock to data invalid	See Figure 7	10			ns
D_VC	Data valid to clock	See Figure 7	10			ns
C_{PWH}	Clock pulse width high	See Figure 7	50			ns
C_{PWL}	Clock pulse width low	See Figure 7	50			ns
CE_L	Clock to enable low	See Figure 7	10			ns
E_LC	Enable low to clock	See Figure 7	10			ns
E_{PWH}	Enable pulse width	See Figure 7	10			ns

DIGITAL INTERFACE CHARACTERISTICS

Conditions: Signal BW = 6 MHz nom, 15 dB maximum loss IF2 SAW filter. See Figure 19

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_IH	Input high voltage		2.1		5	V
V_{IL}	Input low voltage		0		0.8	V
I_{IH}	Input high current		0		50	µA
I_{IL}	Input low current		0		–50	µA
C_I	Input capacitance			3		pF
V_{OH}	Output logic 1 voltage	0 to 100-µA load	2.4		3.6	V
R_{OH}	Output logic 1 impedance			18		kΩ
V_{OL}	Output low voltage	0 to –100-µA load	0		0.4	V

AUXILIARY AND CONTROL

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{VCOenb}	External VCO enable voltage	CMOS compatible Input. See Table 9				V
V_{LD1}	Lock detect voltage (PLL1)	CMOS compatible output (active high). See Table 9				V
VLD2	Lock Detect Voltage (PLL2)	CMOS compatible output (active high). See Table 9				V
TXON	IF Amp Enable	IF Output On		High		
		IF Output Off		Low		
EXTLO2IP	On-chip VCO2A selection	Logic level applied to EXTLOIP and EXTLOIN pins to select either on chip VCO 2A or 2B. Pullup resistor = 200 Ω and pulldown resistor = 1 kΩ.		High		
EXTLO2IN				Low		
EXTLO2IP	On-chip VCO2B selection			Low		
EXTLO2IN				High		
EXTLO2IP	On-chip VCO2 selection	Logic Level applied to EXTLOIP and EXTLOIN pins to select the external VCO2 input		Low		
EXTLO2IN				Low		

FREQUENCY PLAN

The TRF1121/TRF1221 allow a variety of frequency plans. Figure 1 illustrates the allowable combinations of first and second IFs. However, due to the fact that the chip features image reject mixers, significant changes in the frequency plan can result in degradation of the image rejection as shown in Figure 2. LO leakage vs LO1 frequency is shown in Figure 3.

In order to maintain maximum image rejection and LO suppression, a recommended frequency plan is TxIF1 = 26 MHz, TxIF2 = 325 MHz.

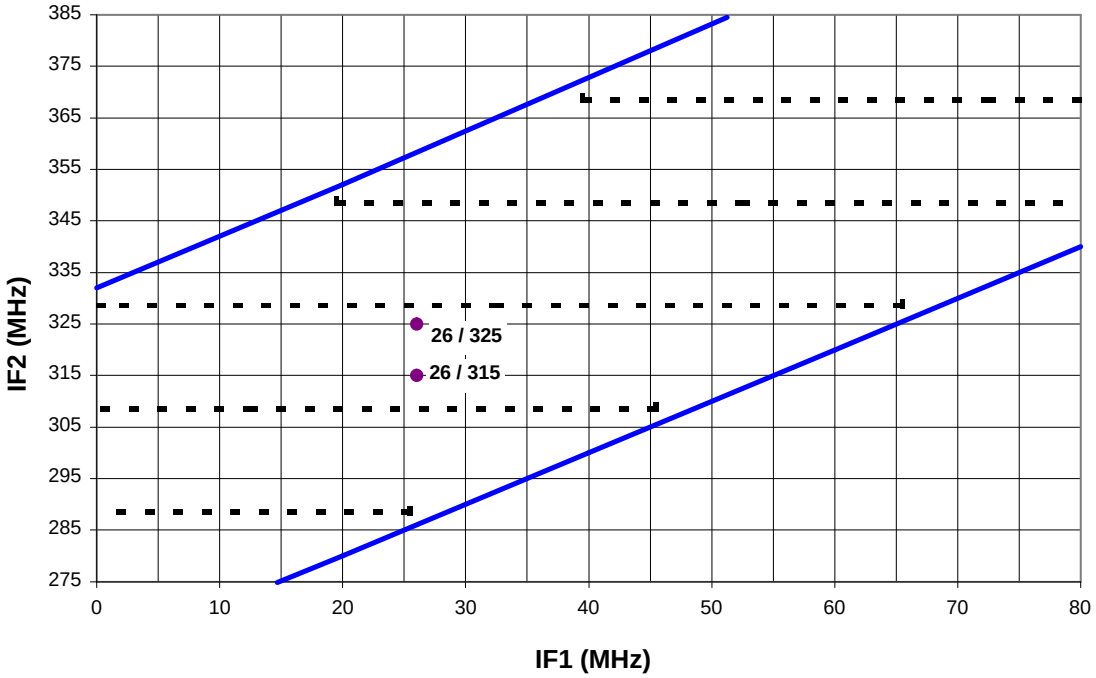


Figure 1. Potential IF Combinations (TRF1121/1221)

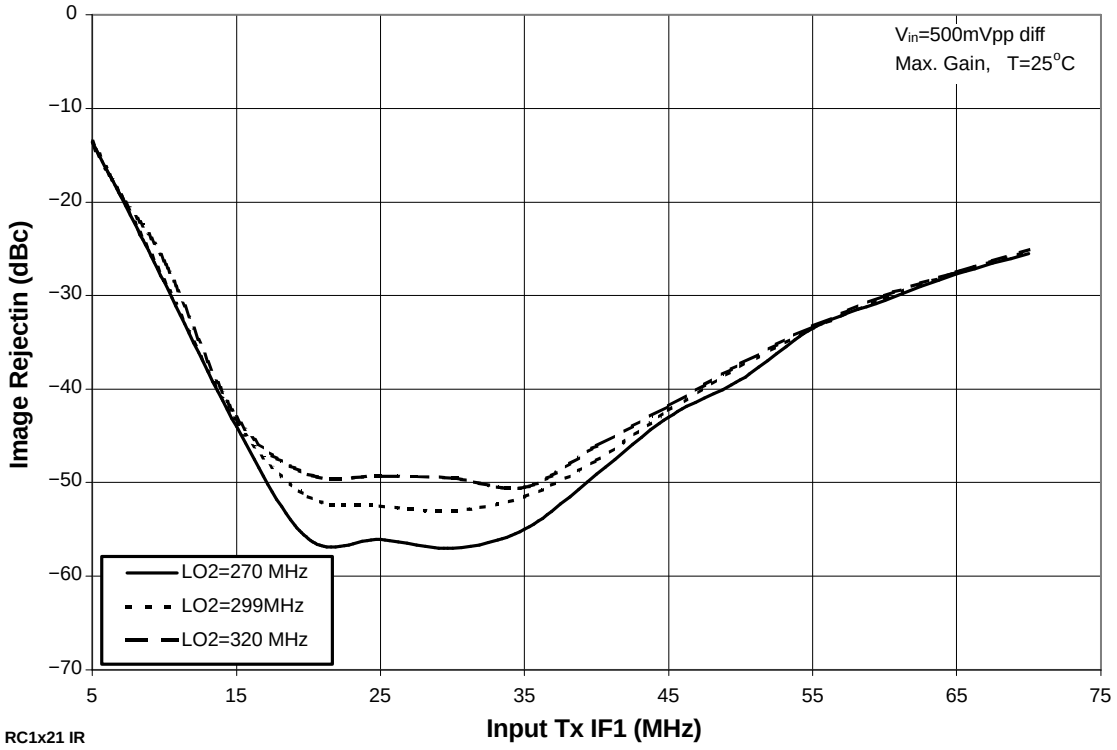


Figure 2. . Image Rejection vs IF1, Transmit Chain

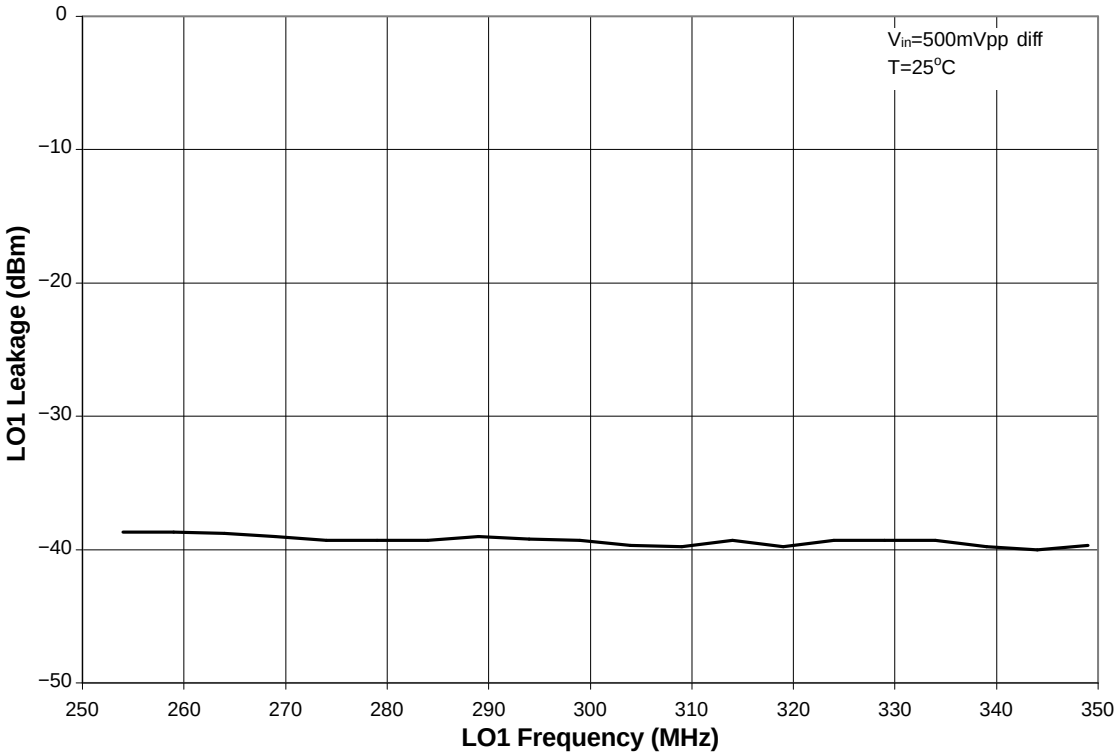


Figure 3. LO1 Leakage at IF2 Port, Maximum Gain

TRANSMIT LEVEL CONTROL

The TRF1121 / TRF1221 offer 32 dB of gain control through a five wire parallel bus. When driven with a 500-mVpp differential baseband IF signal, the transmit level can be programmed between –32 dBm and 0 dBm in 1 dB steps.

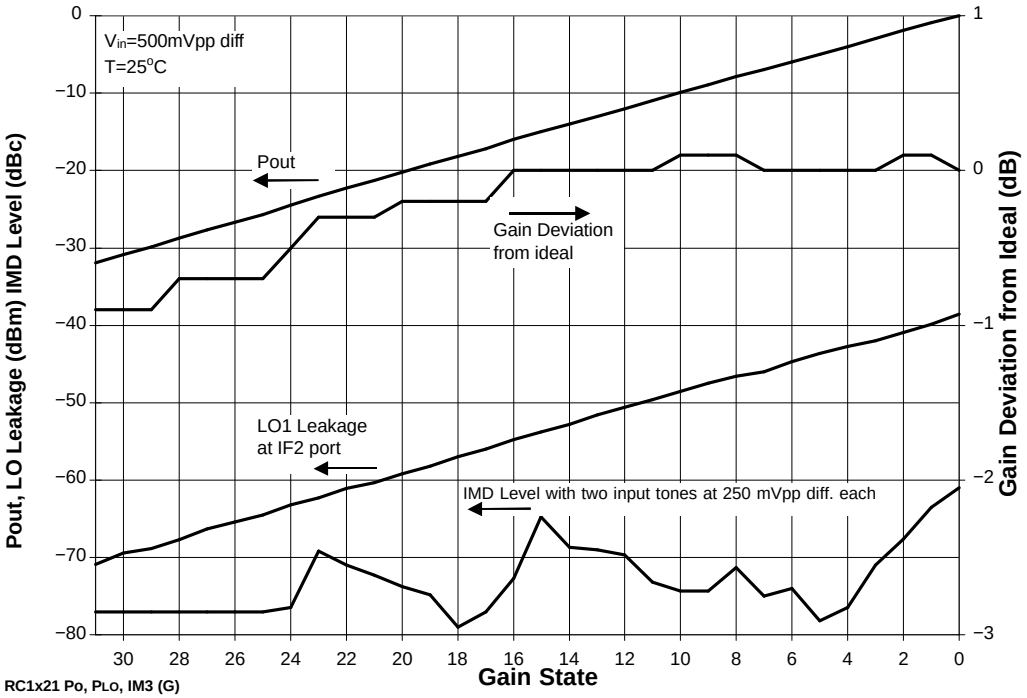


Figure 4. Output Power, LO Leakage and IMD Level vs Gain State

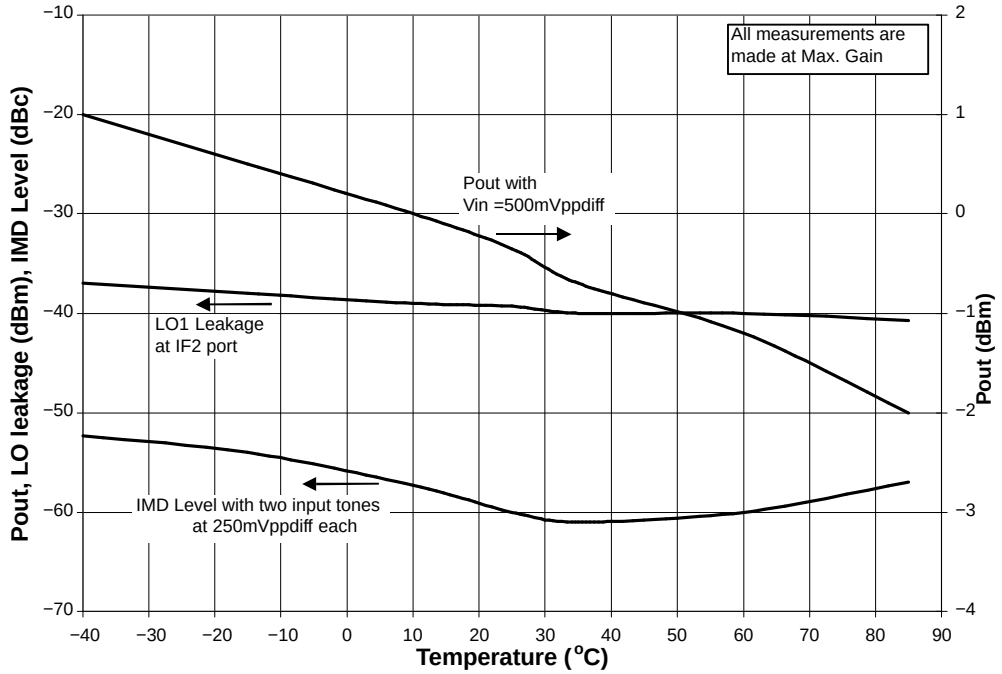
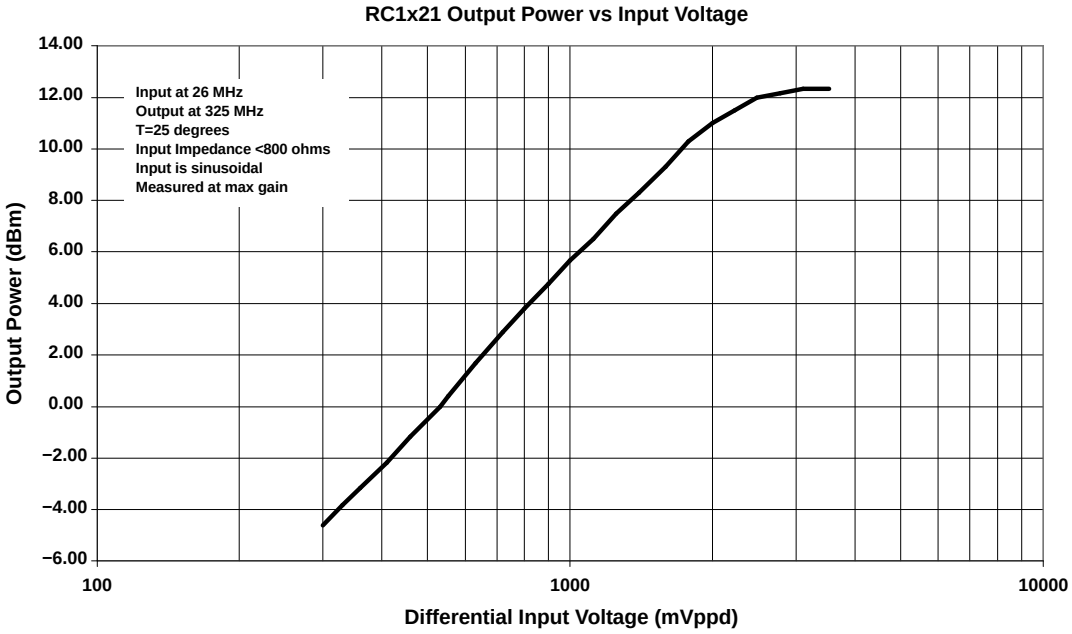


Figure 5. Power Level, IMD and LO1 Leakage Variation vs Temperature at Maximum Gain Setting

Figure 4 shows the output power, two-tone imtermodulation level, LO leakage and gain deviation from ideal vs gain state while Figure 5 shows the upconverter gain variation vs temperature.



NOTE: If left unconnected, the GAIN[0], GAIN[1], GAIN[2], GAIN[3], GAIN[4], and TXEN pins rest on logic Low.

Figure 6. Output Power vs Input Voltage

INTEGRATED SYNTHESIZERS

PLL Programming

Synthesizer #1 (UHF) and synthesizer #2 (S-band) are both integrated in the TRF1121/TRF1221. These two PLLs can be programmed via a 3-wire serial bus (CLK, DATA, and EN) from the baseband processor. The timing specs are given in the AC Timing table.

Synthesizer #2 has a step size of 1 MHz, while Synthesizer #1 offers a step size of 50 kHz, both assuming an 18-MHz reference frequency. Different reference frequencies yield different step sizes, many of which may be non-integer.

NOTE:

If left unconnected, the DATA, CLK and EN pins rest on logic *High*. EN is level sensitive.

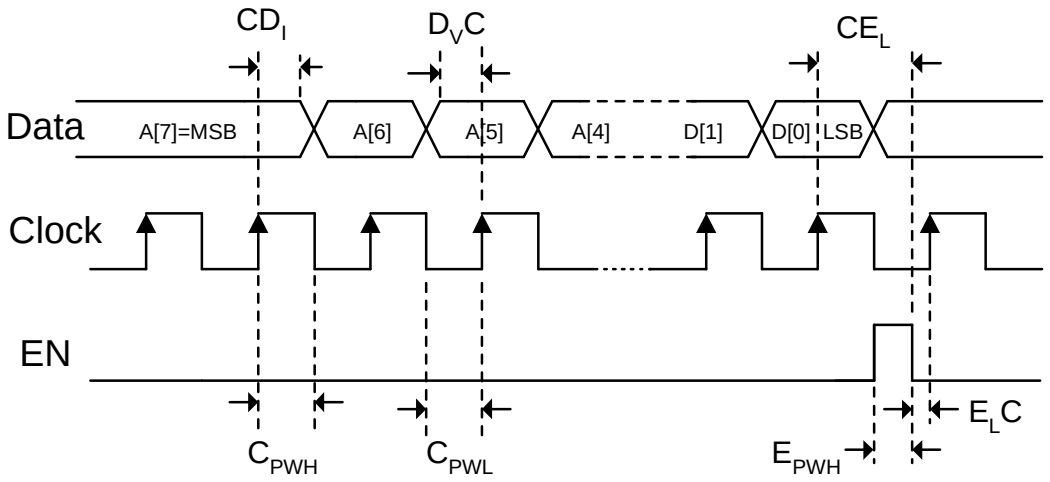


Figure 7. Serial Interface Timing Diagram

Data is written to the PLLs according to the format in Figure 8.

MSB				Byte 1			LSB	MSB				Byte 2			LSB	MSB			Byte 3				LSB
Address								Data															
A[7]	A[6]	A[5]	A[4]	A[3]	A[2]	A[1]	A[0]	D[15]	D[14]	D[13]	D[12]	D[11]	D[10]	D[9]	D[8]	D[7]	D[6]	D[5]	D[4]	D[3]	D[2]	D[1]	D[0]
1	0	0	0	0	0	0	0	0	0	Synth #1 N divider						Synth #1 S counter			Synth #1 F counter				
1	0	0	0	0	0	0	1	0	0	Synth #2 N divider						Synth #2 S counter			Synth #2 F counter				
1	0	0	0	0	1	0	0	0	0	0	0	0	0	0	PS	0	0	0	0	0	0	0	0
all other addresses reserved for future expansion																							

Figure 8. Serial Interface Data Format

The first eight bits are the appropriate address for the instruction set and the remaining 16 bits are the instructions. The data is 24 bits long (3 bytes). Byte 1 is the address with A[7] being the MSB and A[0] being the LSB. Byte 2 and 3 program the IC with synthesizer information and PS (Polarity Select Bit) information. D[15] is the MSB and D[8] the LSB. The PS bit selects which edge of the reference is used for frequency comparison. Improved spurious and phase noise is achieved by selecting the edge with the fastest rise or fall time. If PS = 1 the rising edge is used as the reference. If PS = 0, the falling edge is used.

Figure 7 needs to be sent to the TRF1121 / TRF1221 to fully program the Synthesizers #1 and #2 and the PS bit. Once the synthesizers and the PS bit are fully programmed, the clock signal should be turned off to eliminate any clock-related spurious signals.

The LO1 (UHF oscillator) frequency of oscillation is set by Equation 1:

$$Fout = REFIN \times \left[8 \times (N + 3) - S - \frac{F}{18}\right] / [2 \times M] \quad (1)$$

where M = 10 for TRF1121 and 8 for 1221

The TRF1121/TRF1221 contains two independent S-band VCOs and resonator circuits to provide additional frequency range from one IC, however only one VCO can be enabled at a time. These two VCOs are referred to as VCO2A and VCO2B (see the block diagram). The S-band PLL (LO2A or LO2B) frequency of oscillation is set by the following equation:

$$Fout = REFIN \times \left[8 \times (N + 3) - S - \frac{F}{18}\right] \quad (2)$$

where F has a range of 0 to 17. Both N and S have ranges that are limited more by the LO range than by their digital count.

Both synthesizers have a fractional architecture, which allows a high comparison frequency relative to the step size. The S-band PLL operates at a reference frequency of 18 MHz with a minimum phase accumulator frequency of 1 MHz. The UHF PLL operates at a 9-MHz reference with a minimum phase accumulator frequency of 0.5 MHz. The S-band PLL has a step size of 1 MHz and the UHF PLL has a step size of 50 kHz (TRF1121) or 62.5 kHz (TRF1221), when using an 18-MHz reference frequency. Different reference frequencies yield different step sizes, many of which are non-integer. If a different reference frequency is chosen, the step size is linearly related to the step size for 18 MHz.

Step size = step size 18 MHz x [REF FREQ / 18 MHz]

In addition to the normal reference spurious signals at the comparison frequency, fractional synthesizers have fractional spurs. The fractional spurs occur at an offset from the LO signal that is dependent on the difference between the LO frequency and integer multiples of the reference frequency. They occur on both sides of the LO carrier. The spur locations can be found by the following process: divide the LO frequency by the reference frequency, take the remainder (fraction to the right of the whole number) and multiply it by the reference frequency. This frequency is the difference between the actual LO frequency and an integer-multiple of the reference frequency. Fractional spurs occur at this frequency and the reference frequency minus this frequency.

The following example best explains the process: if LO2 is set to 2206 MHz and we are using an 18 MHz reference frequency, then 2206/18 is 122.55556. The difference between the LO and 122 x 18 MHz is:

0.55556 x 18 MHz = 10 MHz

The fractional spurs occur at this frequency offset (10 MHz) from LO2 and:

18–10 MHz or 8 MHz offset from LO2.

The fractional spurious level varies with the offset from the LO since the spurs are attenuated by the loop filter response. The larger the offset from the LO, the lower the spur level. In general, spurs at offsets greater than 3 MHz or 4 MHz are below -75 dBc and are not a concern. The worst fractional spur levels occur when they are located at 1 MHz offsets from the LO2. (Note: the fractional spurs are offset from the LO2 by 1 MHz when the difference between the LO2 and an integer multiple of the reference frequency is 1 MHz or 17 MHz).

Although both synthesizers have fractional spurs, for most applications the spurious signals from the UHF synthesizer can be ignored because the LO1 spurs are filtered by the IF2 filter and attenuated by frequency dividers that are located after the LO1 generation. In some frequency plans it is possible to offset LO1 and LO2 to avoid worst case fractional spurs (at 1-MHz offsets) on LO2.

VCO Tuning Characteristics

The TRF1121 / TRF1221 have internal VCOs with the following frequency vs tuning voltage characteristics.

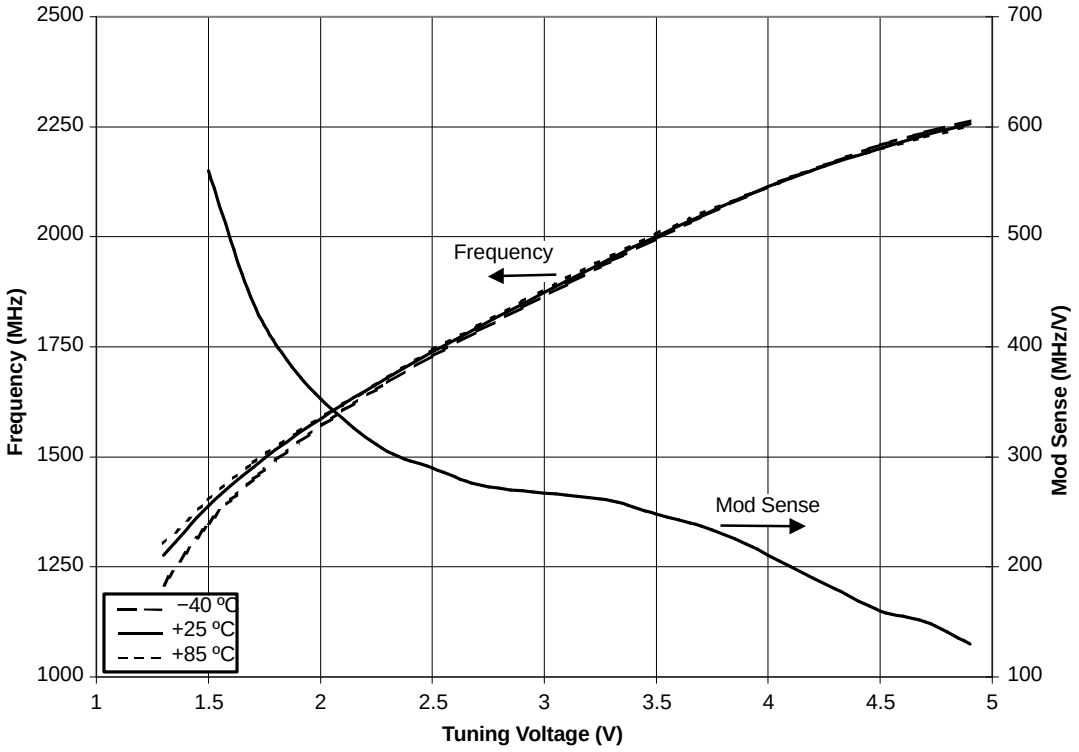


Figure 9. TRF1121 LO2A Frequency LO2ATUN Voltage

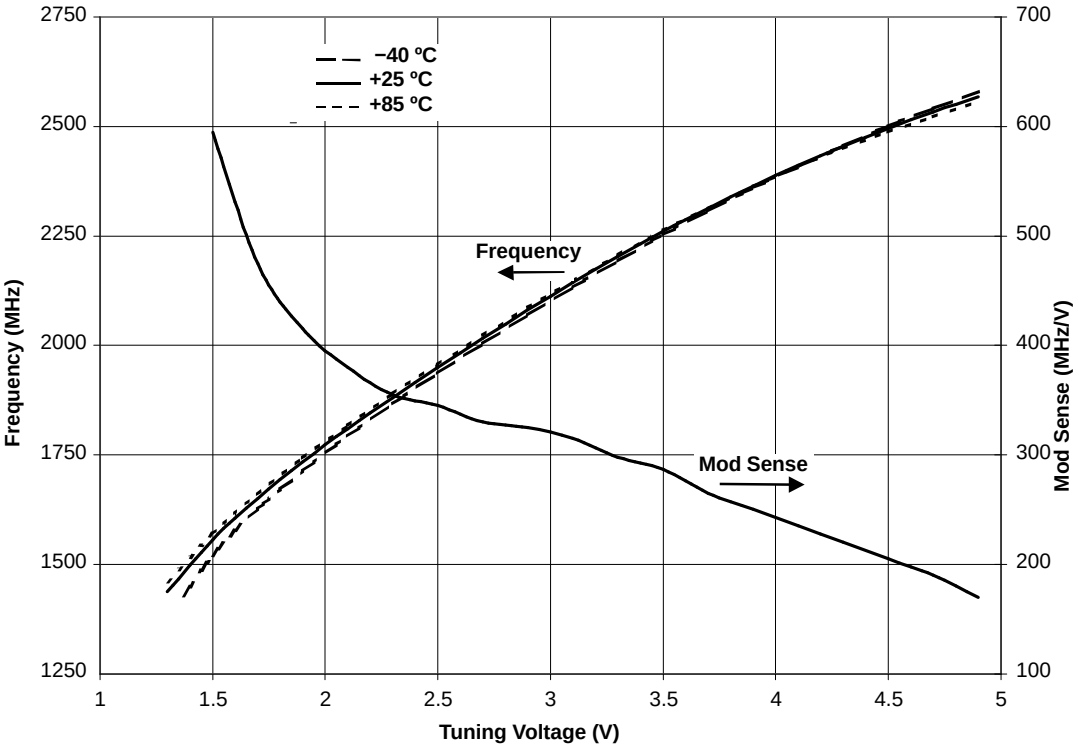


Figure 10. TRF1121 LO2B Frequency vs LO2BTUN Voltage

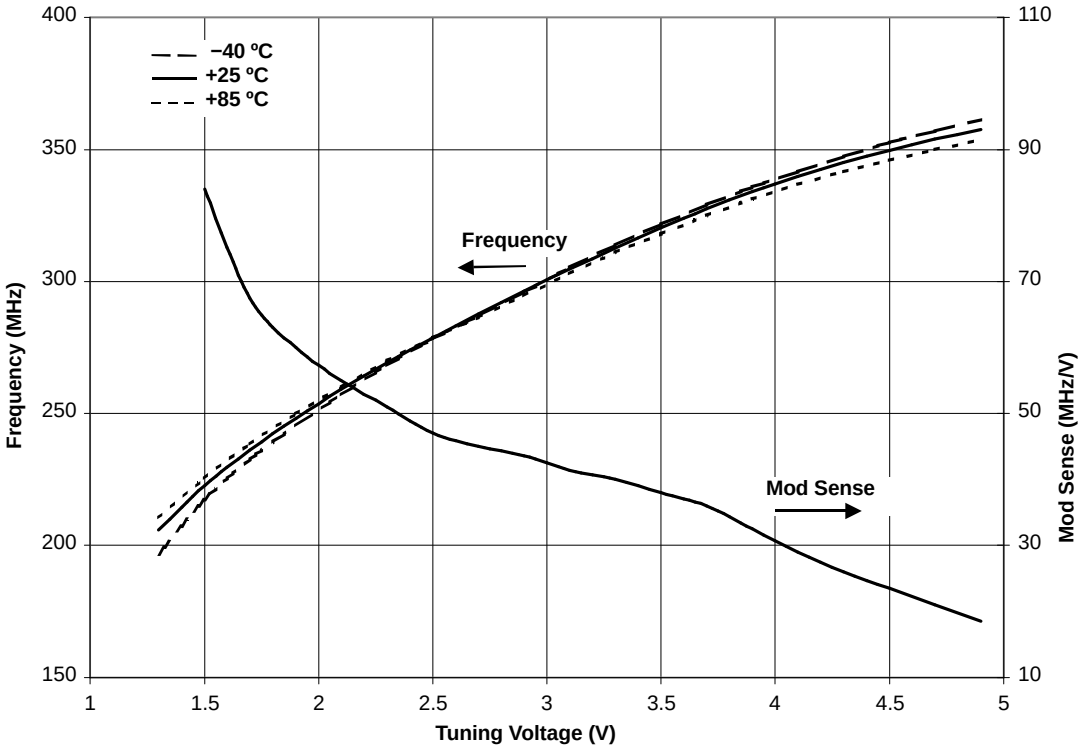


Figure 11. TRF1121 LO1 Frequency vs LO1TUN Voltage

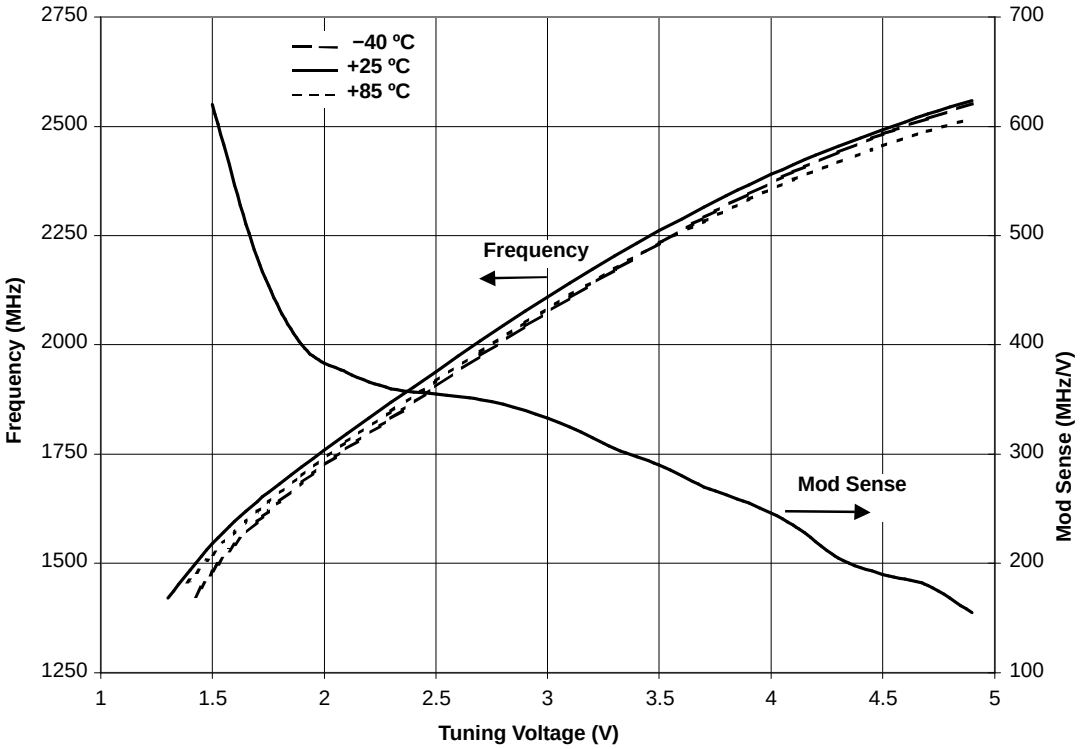


Figure 12. TRF1221 LO2A Frequency vs LO2ATUN Voltage

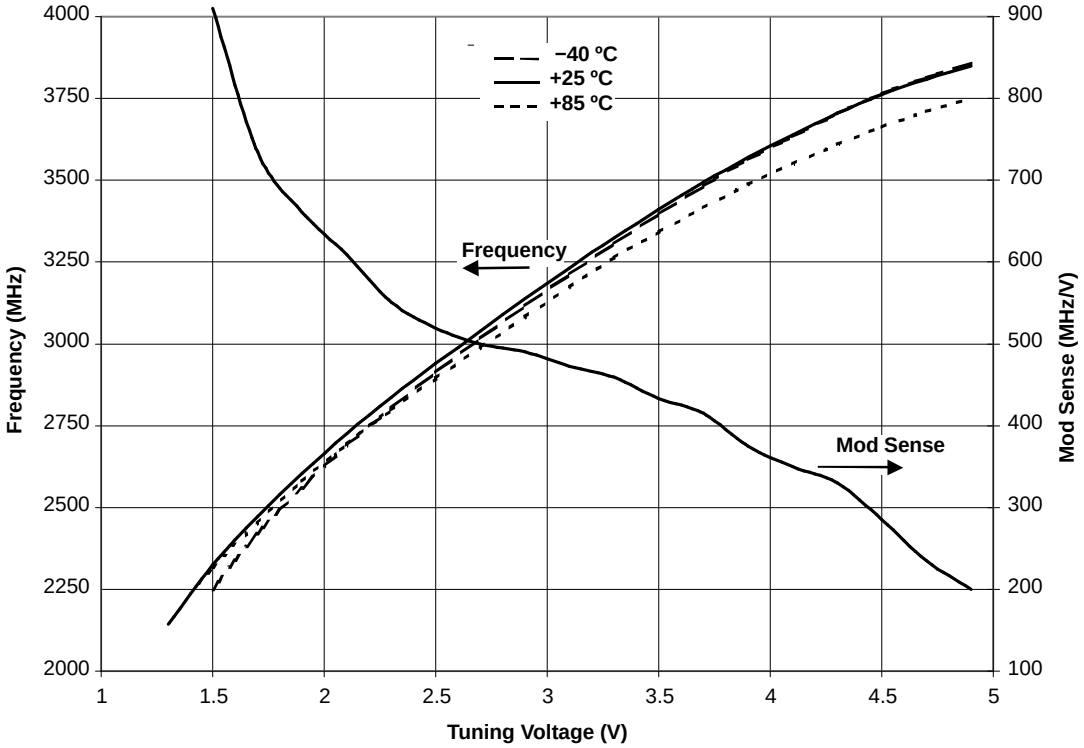


Figure 13. TRF1221 LO2B Frequency vs LO2BTUN Voltage

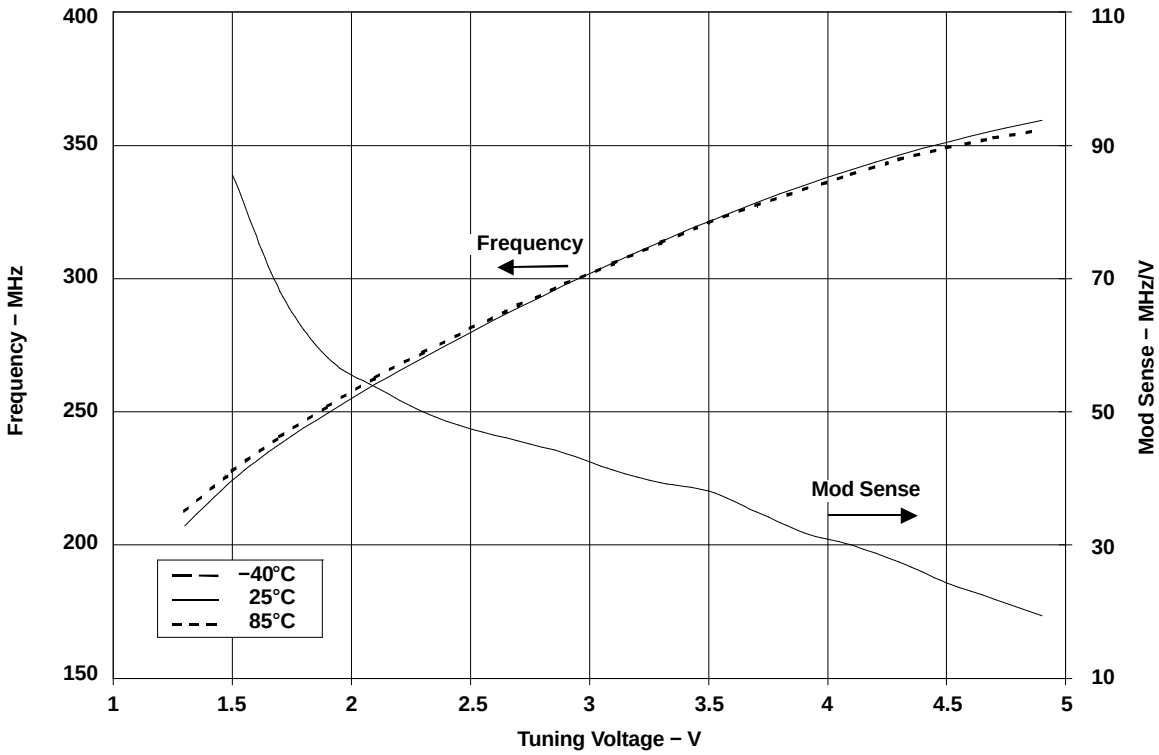


Figure 14. TRF1221 LO1 Frequency vs LO1TUN Voltage

Phase Noise

The TRF1121 / TRF1221 achieve superior phase noise performance with on-chip resonators and varactors. It is designed to meet the phase noise requirements of both single-carrier and multi-carrier systems. Due to the chip architecture, the phase noise and spurious performance of the LO1 PLL is about 15 dB better than the LO2 PLL. The typical phase noise of the TRF1121 and TRF1221 S-band PLL (LO2) with the PLL locked is shown in Figure 15 and Figure 16 respectively. The phase noise plots of the TRF1221 S-band PLL at the min and max range are shown in Figure 20 and Figure 21 respectively. These plots were taken at room temperature and typical voltage conditions.

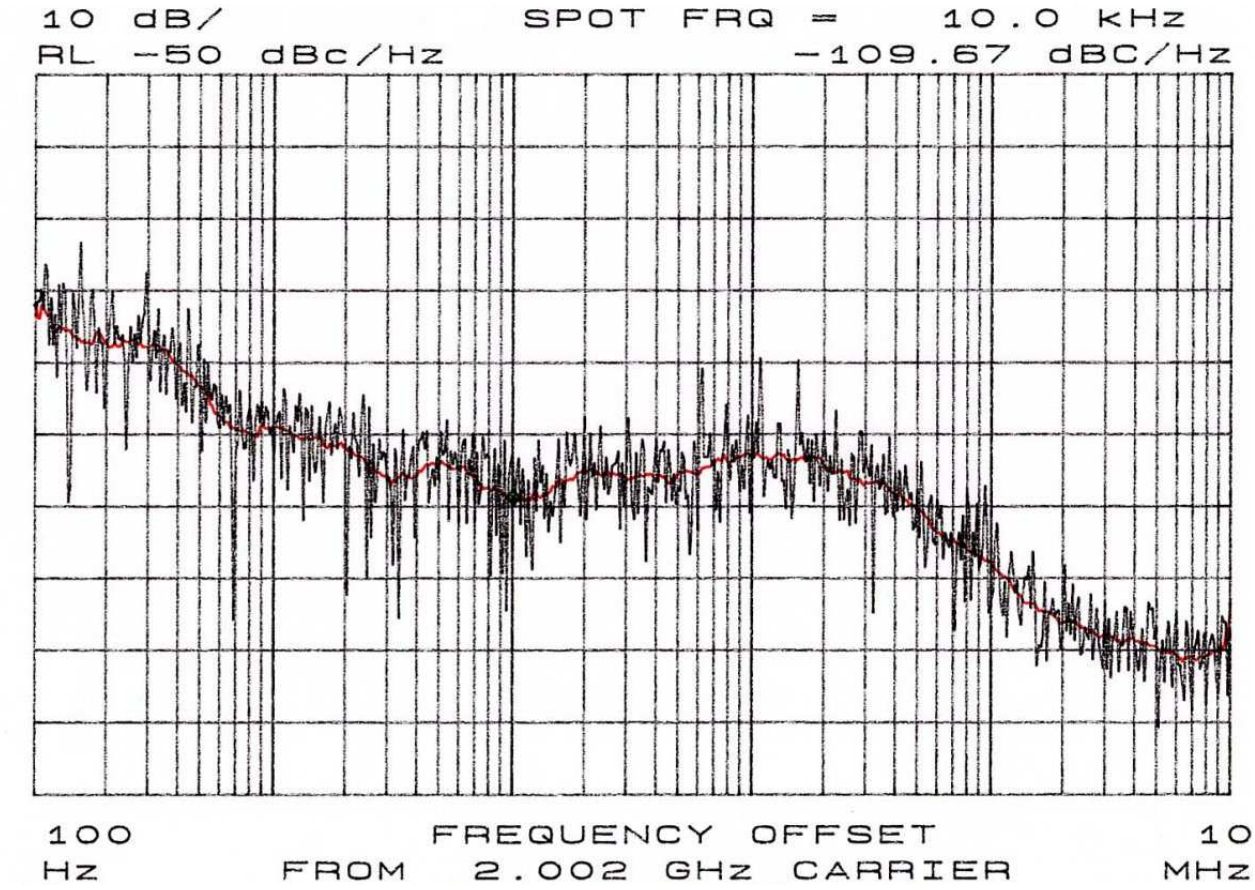


Figure 15. TRF1121 Typical Integrated LO1 (S-band) Phase Noise is 0.35 rms (100 Hz to 1 MHz)

When designing full duplex radios that employ narrow T to R spacing, one must consider impact of wide-band phase noise since it can degrade Rx sensitivity. (See Application Note TDB). Figure 17 shows typical wide-band composite phase noise performance of the combination of the two integrated PLLs. At 50-MHz offset typical performance is –145 dBc/Hz.

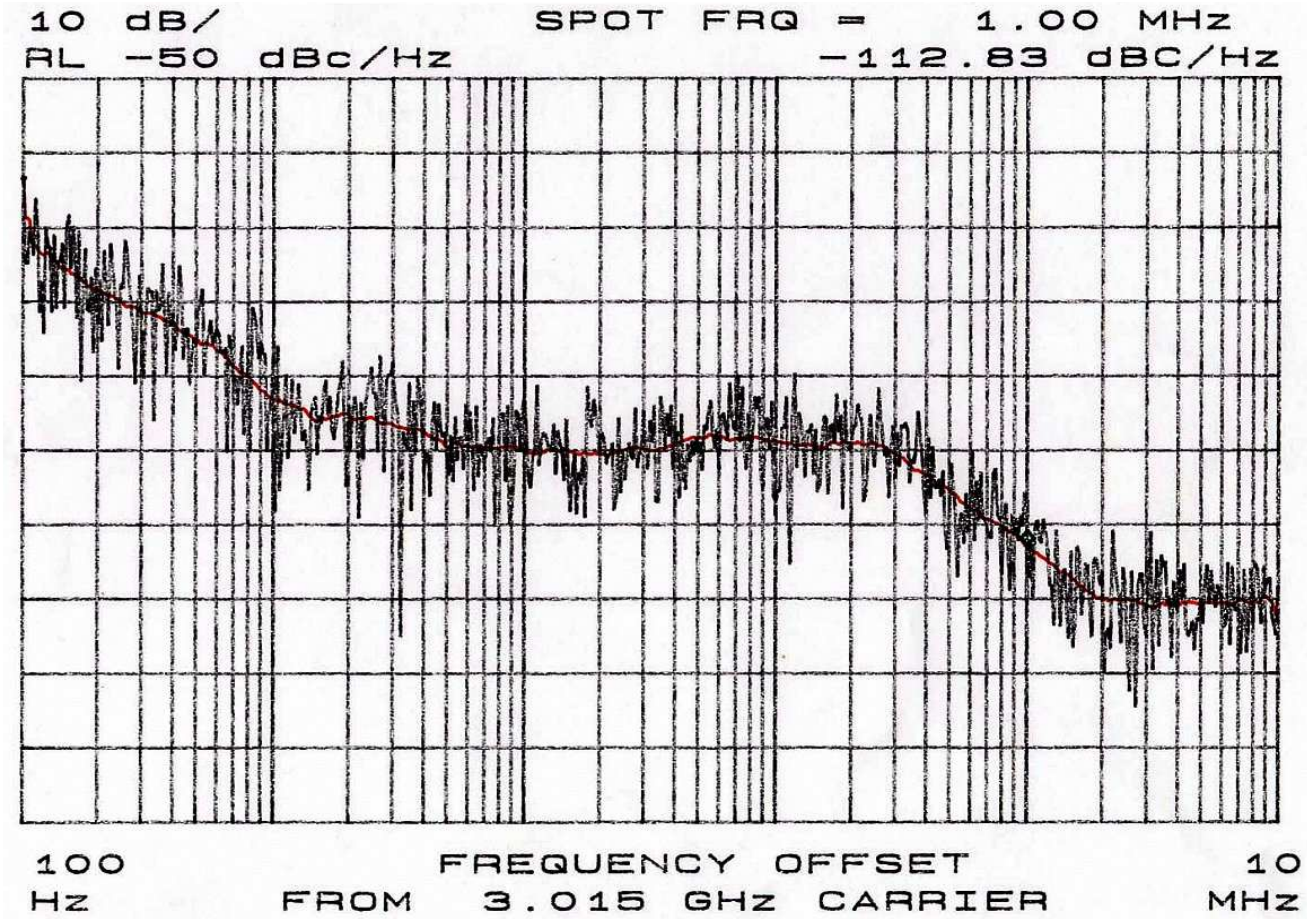


Figure 16. TRF1221 Typical Integrated LO2 (S-band) Phase Noise is 0.65 rms (100 Hz to 1 MHz)

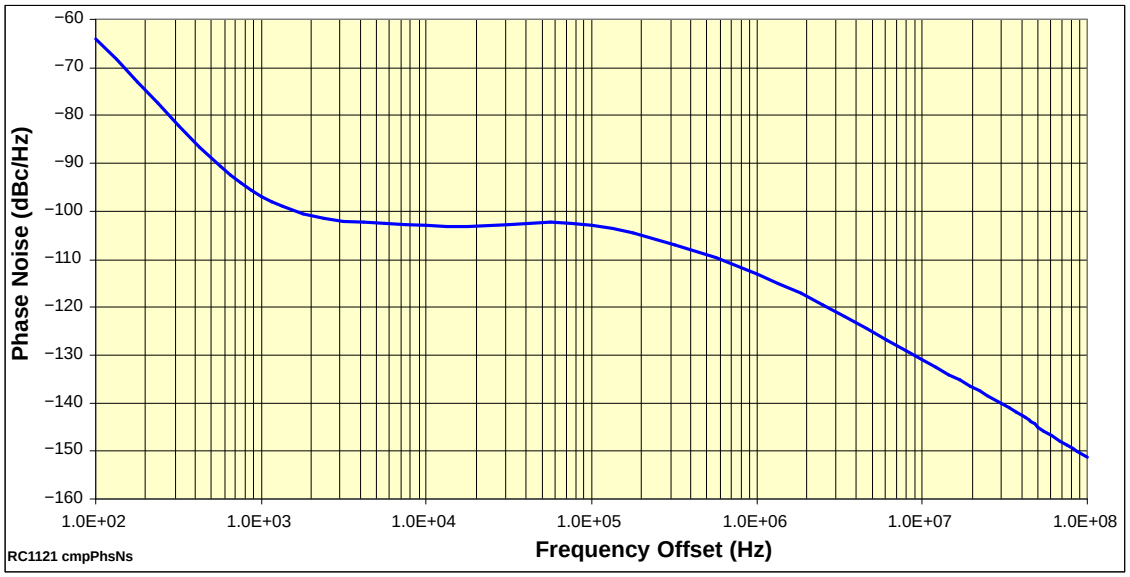


Figure 17. TRF1121 Typical Wide-Band Composite PLL Phase Noise Profile

Figure 18 shows reference spurs of the S-band (LO2) locked synthesizer and Figure 19 shows the fractional spurs of the same LO at 2-MHz offset from the carrier

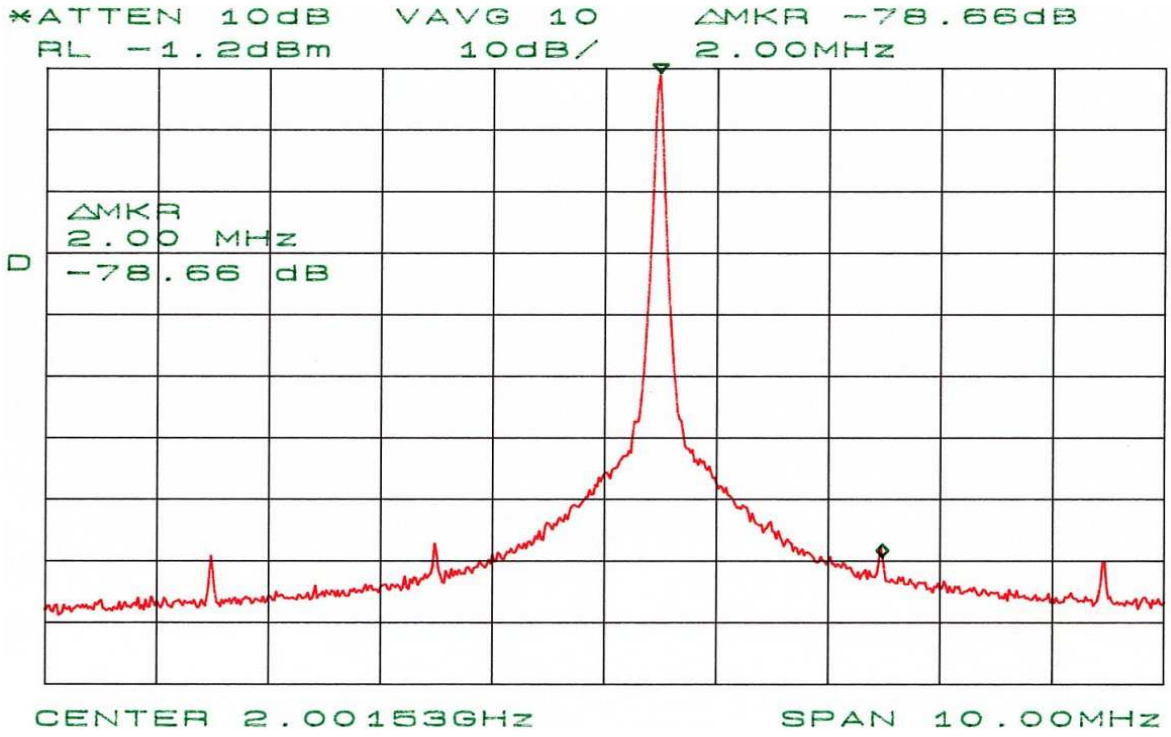


Figure 18. TRF1121 Reference Spurs on LO2 Output

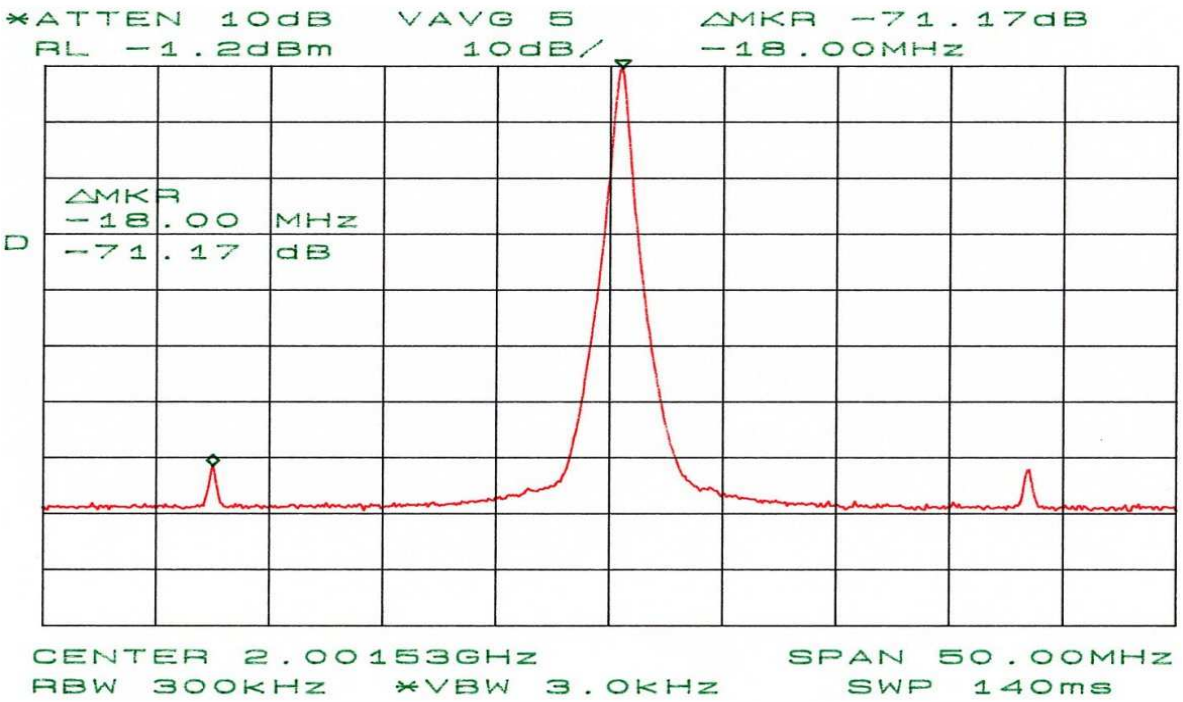


Figure 19. TRF1121 Fractional Spurs on LO2 (2-MHz Offset)

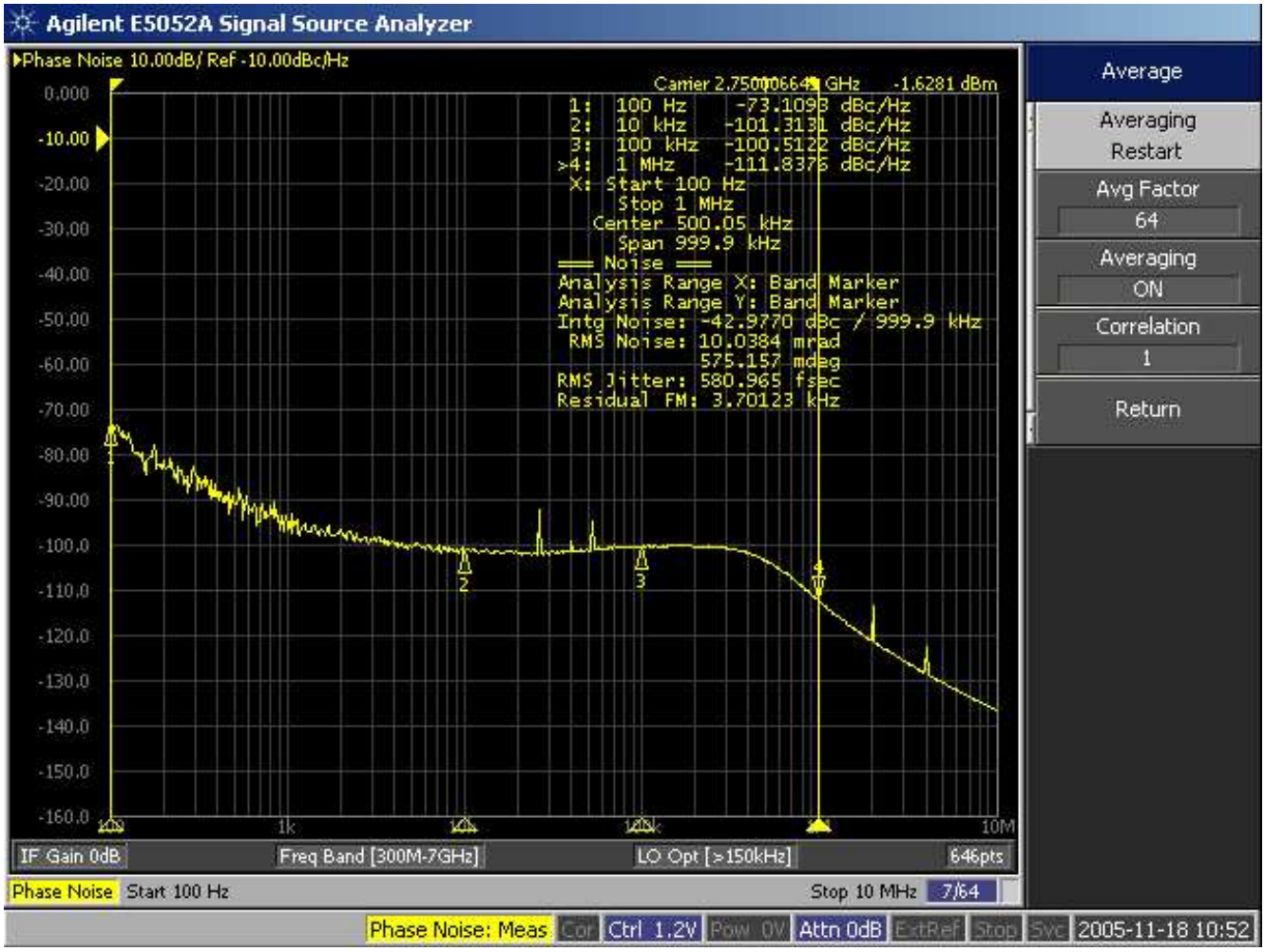


Figure 20. Phase Noise - 2750 MHz

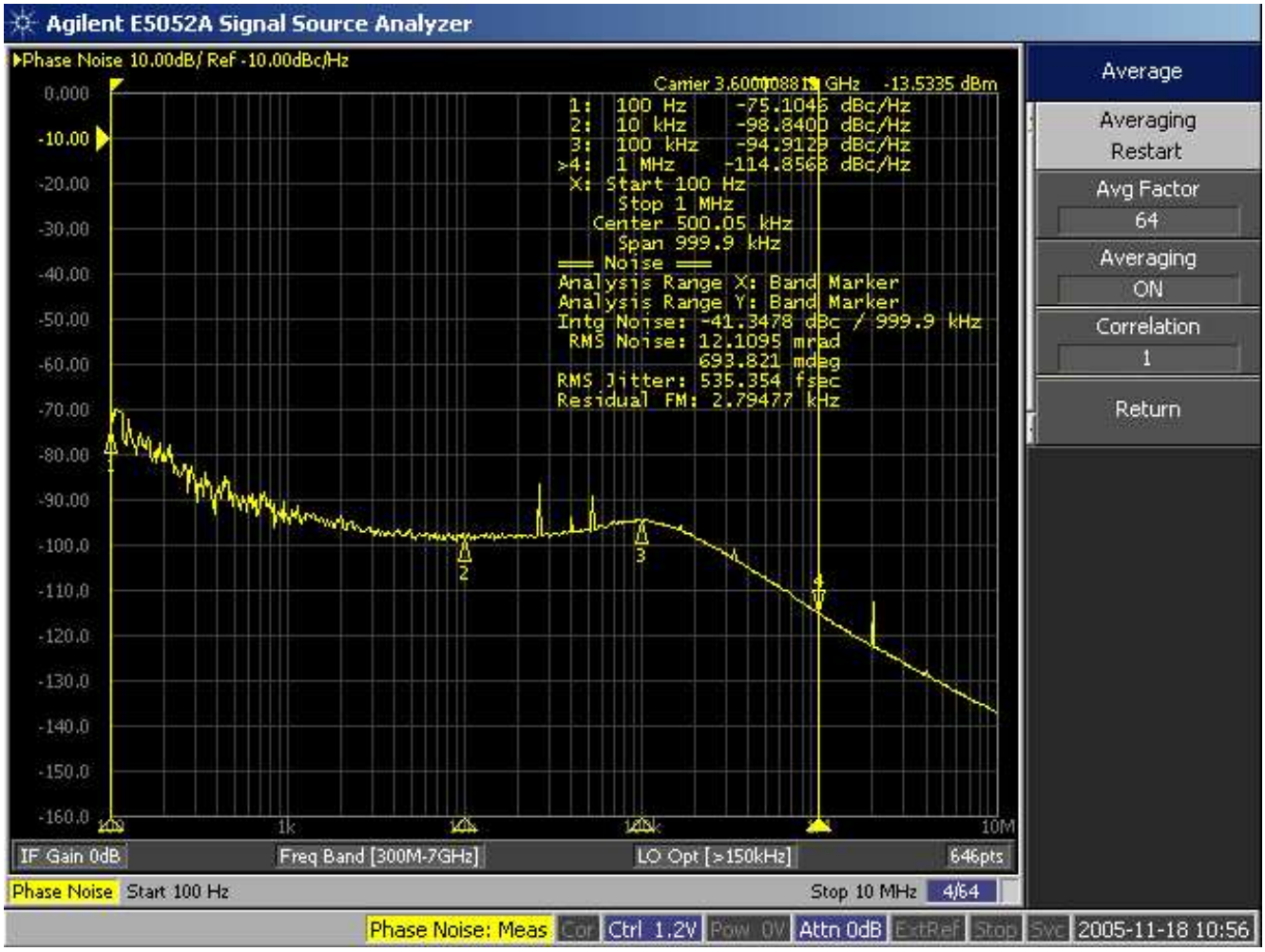


Figure 21. Phase Noise - 3600 MHz

For systems that demand tighter phase noise performance than that offered by Texas Instruments internal VCOs, a provision exists for connection of an external VCO. Texas Instruments PLL still locks the VCO to the reference frequency and the ASIC provides an external tuning voltage that drives the VCO.

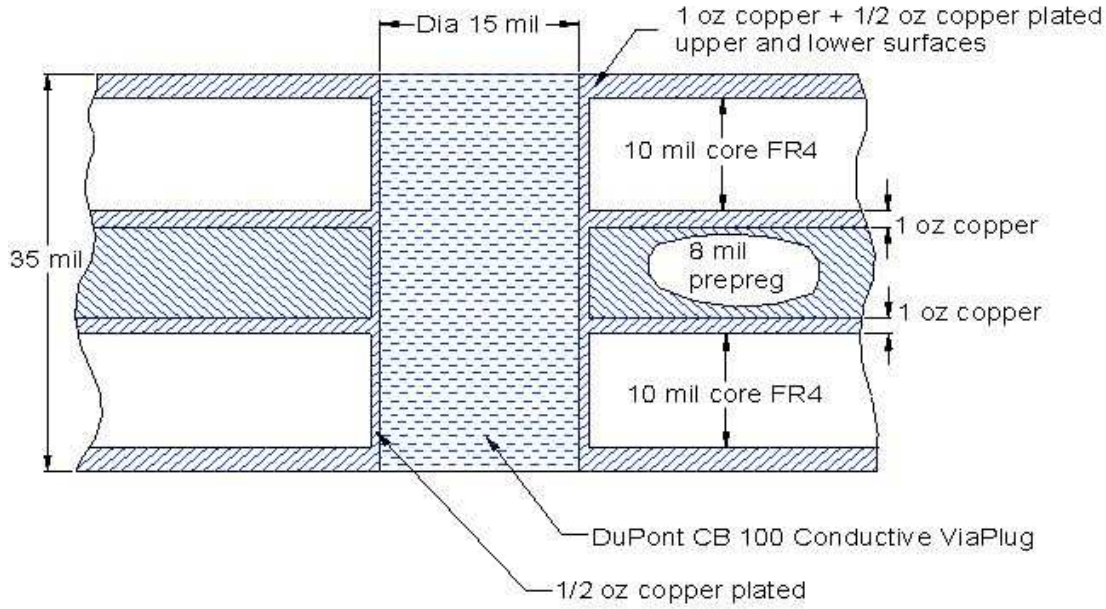
APPLICATION INFORMATION

A typical application schematic is shown in Figure 23, while a mechanical drawing of the package outline (LPCC Quad 7 mm × 7 mm, 48 pin) is presented in Figure 24.

The recommended PCB layout mask is shown in Figure 25. PCB material recommendations are shown in , Table 1and Figure 22.

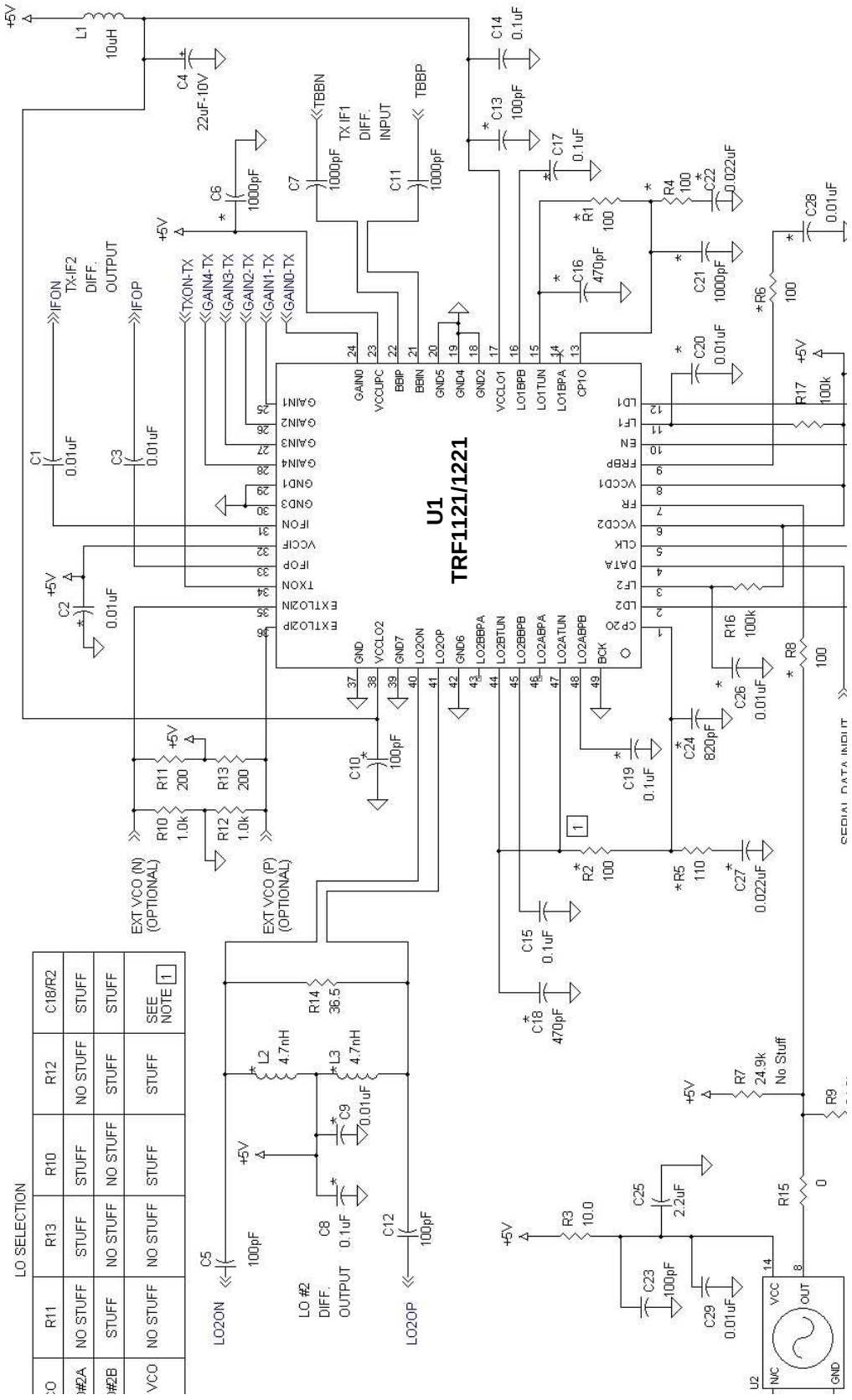
Table 1. PCB Recommendations

Board material	FR4
Board material core thickness	10 mil
Copper thickness (starting)	1 oz
Prepreg thickness	8 mil
Recommended number of layers	4
Via plating thickness	0.5 oz
Final plate	White immersion tin
Final board thickness	33–37 mil



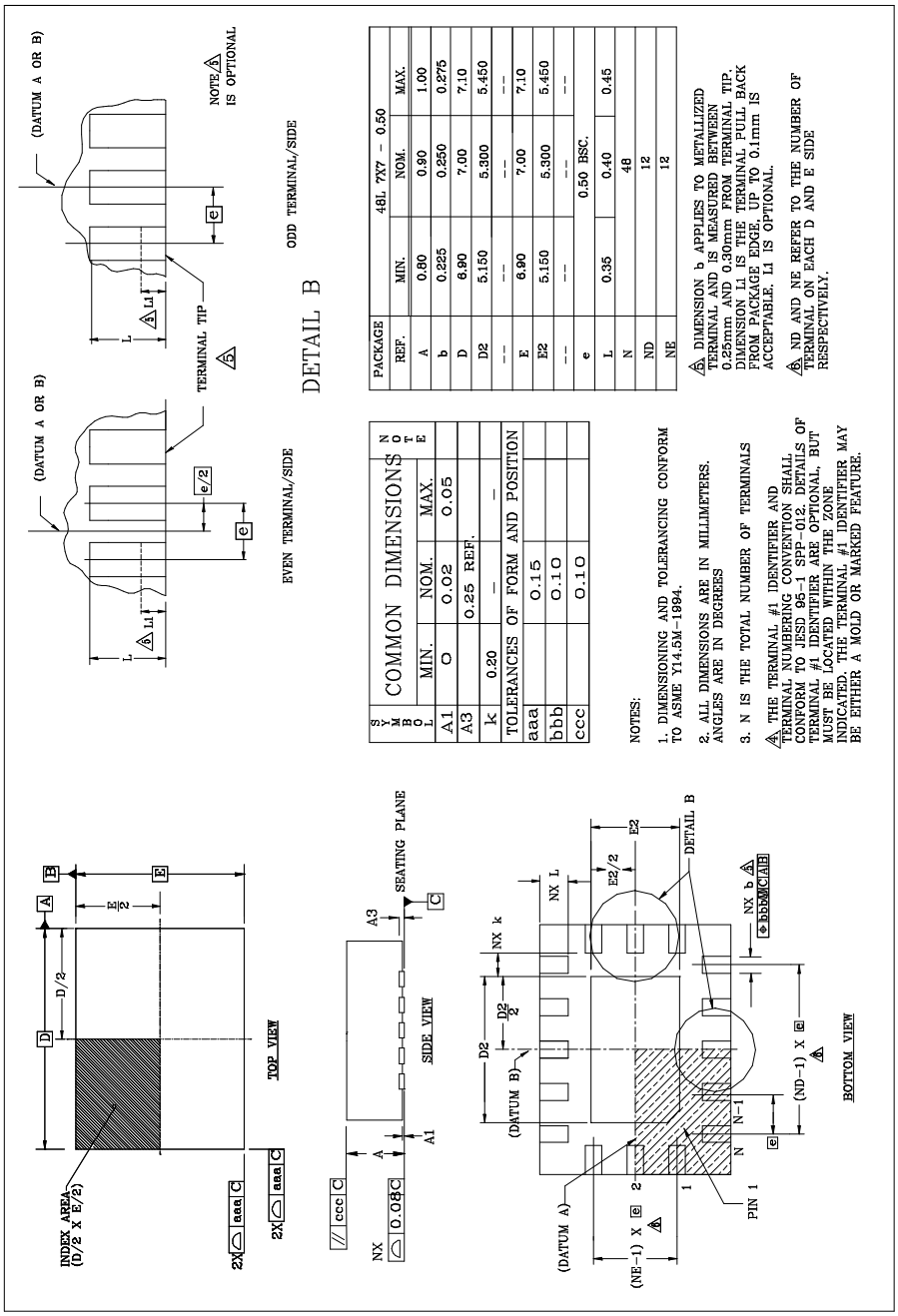
Note 1. Top and bottom surface finish: copper flash with 50-70 µin white tin immersion

Figure 22. PCB Construction and Via Cross Section



LO SELECTION						
VCO	R11	R13	R10	R12	C18/R2	
VCO	NO STUFF	NO STUFF	STUFF	STUFF	STUFF	SEE NOTE 1
LO #2B	STUFF	NO STUFF	NO STUFF	STUFF	STUFF	
LO #2A	NO STUFF	STUFF	STUFF	NO STUFF	STUFF	

Figure 23. Typical Application Schematic



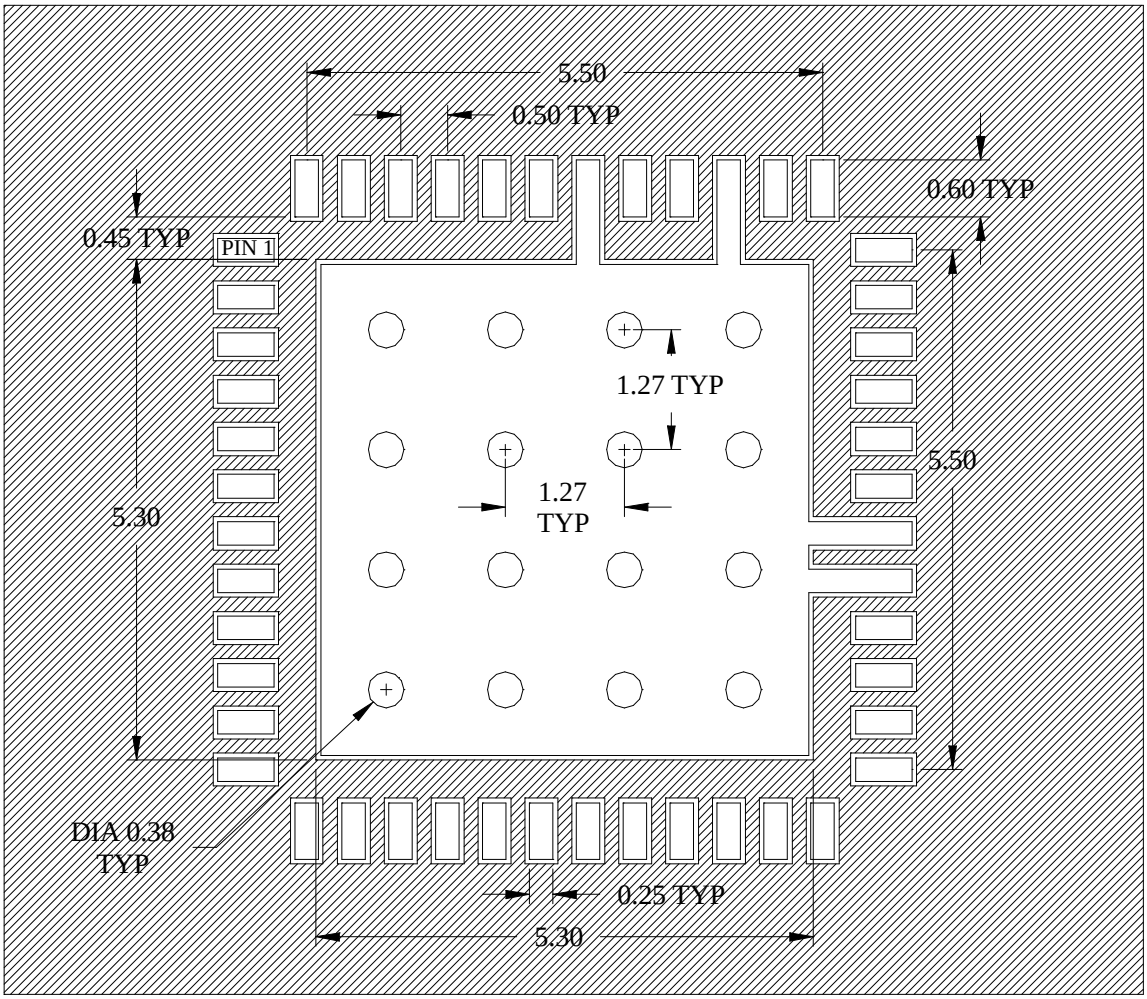
SYMBOL	COMMON DIMENSIONS MIN.	NOM.	MAX.	NOTE
A1	0	0.02	0.05	
A3		0.25 REF.		
k	0.20	—	—	
TOLERANCES OF FORM AND POSITION				
aaa		0.15		
bbb		0.10		
ccc		0.10		

PACKAGE REF.	48L 7X7 – 0.50 MIN.	NOM.	MAX.
A	0.80	0.90	1.00
b	0.225	0.250	0.275
D	6.90	7.00	7.10
D2	5.150	5.300	5.450
—	—	—	—
E	6.90	7.00	7.10
E2	5.150	5.300	5.450
—	—	—	—
e		0.50 BSC.	
L	0.35	0.40	0.45
N		48	
ND		12	
NE		12	

NOTES:

1. DIMENSIONING AND TOLERANCING CONFORM TO ASME Y14.5M–1994.
2. ALL DIMENSIONS ARE IN MILLIMETERS. ANGLES ARE IN DEGREES
3. N IS THE TOTAL NUMBER OF TERMINALS
4. THE TERMINAL #1 IDENTIFIER AND TERMINAL NUMBERING CONVENTION SHALL CONFORM TO JESD 95–1 SPP–012. DETAILS OF TERMINAL #1 IDENTIFIER ARE OPTIONAL, BUT MUST BE LOCATED WITHIN THE ZONE INDICATED. THE TERMINAL #1 IDENTIFIER MAY BE EITHER A MOLD OR MARKED FEATURE.
5. DIMENSION b APPLIES TO METALLIZED TERMINAL AND IS MEASURED BETWEEN 0.25mm AND 0.30mm FROM TERMINAL TIP. DIMENSION L1 IS THE TERMINAL PULL BACK FROM PACKAGE EDGE, UP TO 0.1mm IS ACCEPTABLE. L1 IS OPTIONAL.
6. ND AND NE REFER TO THE NUMBER OF TERMINAL ON EACH D AND E SIDE RESPECTIVELY.

Figure 24. ASIC Package Outline



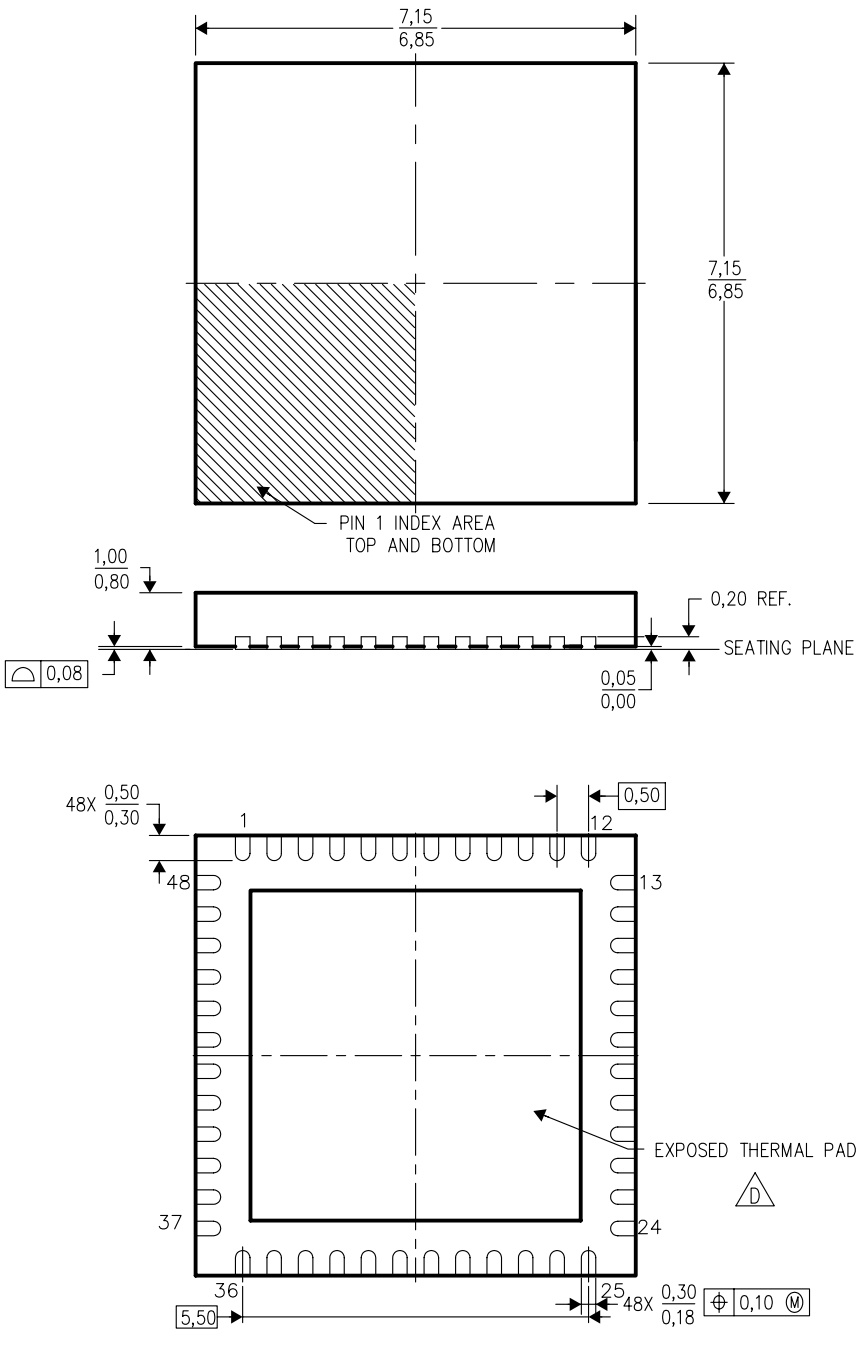
SOLDER MASK: NO SOLDERMASK UNDER CHIP, ON LEAD PADS OR ON GROUND CONNECTIONS.

16 VIA HOLES, EACH 0.38 mm.

DIMENSIONS in mm

Figure 25. PCB Layout Mask for TRF1121/TRF1221

RGZ (S–PQFP–N48) PLASTIC QUAD FLATPACK



NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. Quad Flatpack, No–leads (QFN) package configuration.
D. The package thermal pad must be soldered to the board for thermal and mechanical performance. See the Product Data Sheet for details regarding the exposed thermal pad dimensions.
E. Falls within JEDEC MO–220.

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