SKHI 61 ...

SEMIDRIVER™

Sixpack IGBT and MOSFET Driver

SKHI 61

Features

- CMOS-compatible input buffers at V_{DD}=5V
- Short-circuit protection by V_{CE}-monitoring and Soft-turn-Off
- Drive interlock top/bottom
- Signal transmission by opto-couplers
- Supply undervoltage protection (13V)
- Error latch / output

Typical Applications

- Driver for IGBT and MOSFET modules in three-phase-bridge circuits, inverter drives, UPS-facilities, etc.

[1] At T_a < -25℃ the current consumption can be 1,6 times the rated maximum current for the first three operating minutes.

Absolute Maximum Ratings

Symbol	Conditions	Values	Units
V_S	Supply voltage primary	15,6	V
V_{iH}	Input signal voltage	V_S + 0,3	V
$Iout_{PEAK}$	Output peak current	2	A
$Iout_{AVmax}$	Output average current (T_a = 85 ℃)	20	mA
f_{max}	Max. switching frequency (C_{GE} < 9nF)	50	kHz
V_{CE}	Collector emitter voltage sense across the IGBT (for 1200V-IGBTs)	900	V
dv/dt	Rate of rise and fall of voltage (secondary to primary side)	15	kV/µs
V_{isolIO}	Isolation test voltage input - output (2 sec. AC)	2500	V
V_{isol12}	Isolation test voltage output 1 - output 2 (2 sec. AC)	1500	V
R_{Gonmin}	Minimum rating of R_{Gon}	10	Ω
$R_{Goffmin}$	Minimum rating for R_{Goff}	10	Ω
$Q_{out/pulse}$	Max. rating for gate T_a = 85 ℃	0,7	µC
	charge per pulse T_a = 55 ℃	1	µC
T_{op}	Operating temperature	- 40 ... + 85	℃
T_{stg}	Storage temperature	- 40 ... + 85	℃

Characteristics T_a = 25℃, unless otherwise specified

Symbol	Conditions	min.	typ.	max.	Units
V_S	Supply voltage primary	14,4	15,0	15,6	V
I_{SO} [1]	Supply current no load	160		200	mA
	primary side normal op.			450	mA
V_{iT+}	Input threshold voltage (High)	4,0			V
V_{iT-}	Input threshold voltage (LOW)			1,5	V
R_{in}	Input resistance		60		kΩ
$V_{G(on)}$	Turn on gate voltage output		14,9		V
$V_{G(off)}$	Turn off gate voltage output		-6,5		V
R_{GE}	Internal gate-emitter resistance		20		kΩ
f_{ASIC}	ASIC system switching frequency		8		MHz
$td(on)_{IO}$	Input-output turn-on propagation time	0,3	0,45	0,6	µs
$td(off)_{IO}$	Input-output turn-off propagation time	0,3	0,45	0,6	µs
$t_{d(err)}$	Error input-output propagation time	1,15	1,3	1,5	µs
$t_{pERRRESET}$	Error memory reset time	7	15	27	µs
t_{TD}	Interlock dead time adjustable	no interlock		4,1	µs
V_{CEstat}	Reference voltage for V_{CE}-monitoring		5,8		V
t_{blank}	Blanking time		3,5		µs
C_{ps}	Coupling capacitance primary-secondary		40		pF
MTBF	Mean Time Between Failure T_a = 40℃		1		10^6 h
w	weight		95		g
H x B x T	Dimensions		20x57x 114		mm

SKHI 71 ...

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Sevenpack IGBT and MOSFET Driver

SKHI 71

Preliminary Data

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	primary side normal op.			550	mA
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V_{iT-}	Input threshold voltage (LOW)			1,5	V
R_{in}	Input resistance		60		kΩ
$V_{G(on)}$	Turn on gate voltage output		14,9		V
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t_{blank}	Blanking time		3,5		µs
C_{ps}	Coupling capacitance primary-secondary		40		pF
MTBF	Mean Time Between Failure T_a = 40℃		1		10^6 h
w	weight		99		g
H x B x T	Dimensions		20x57x 114		mm

PIN array

Primary side PIN array

Pin	Symbol	Function	Pin	Symbol	Function
01	BS	Auxiliary earth connection	11	+15V	Supply voltage
02	BOT3	Driver signal BOT HB3	12	+15V	Supply voltage
03	TOP3	Driver signal TOP HB3	13	TDT1	Deadtime bit #1
04	BOT2	Driver signal BOT HB2	14	TDT2	Deadtime bit #2
05	TOP2	Driver signal TOP HB2	15	SEL	Deadtime on/off
06	BOT1	Driver signal BOT HB1	16	BSTD	Aux. earth for deadtime adjustment
07	TOP1	Driver signal TOP HB1	17	_ERRIN	_External error signal input
08	_ERR	_Error output Sixpack-driver	18	NC	reserved
09	BSS	System earth connection	19	BRK	Driver signal additional switch
10	BSS	System earth connection	20	_BERR	_Error output additional switch

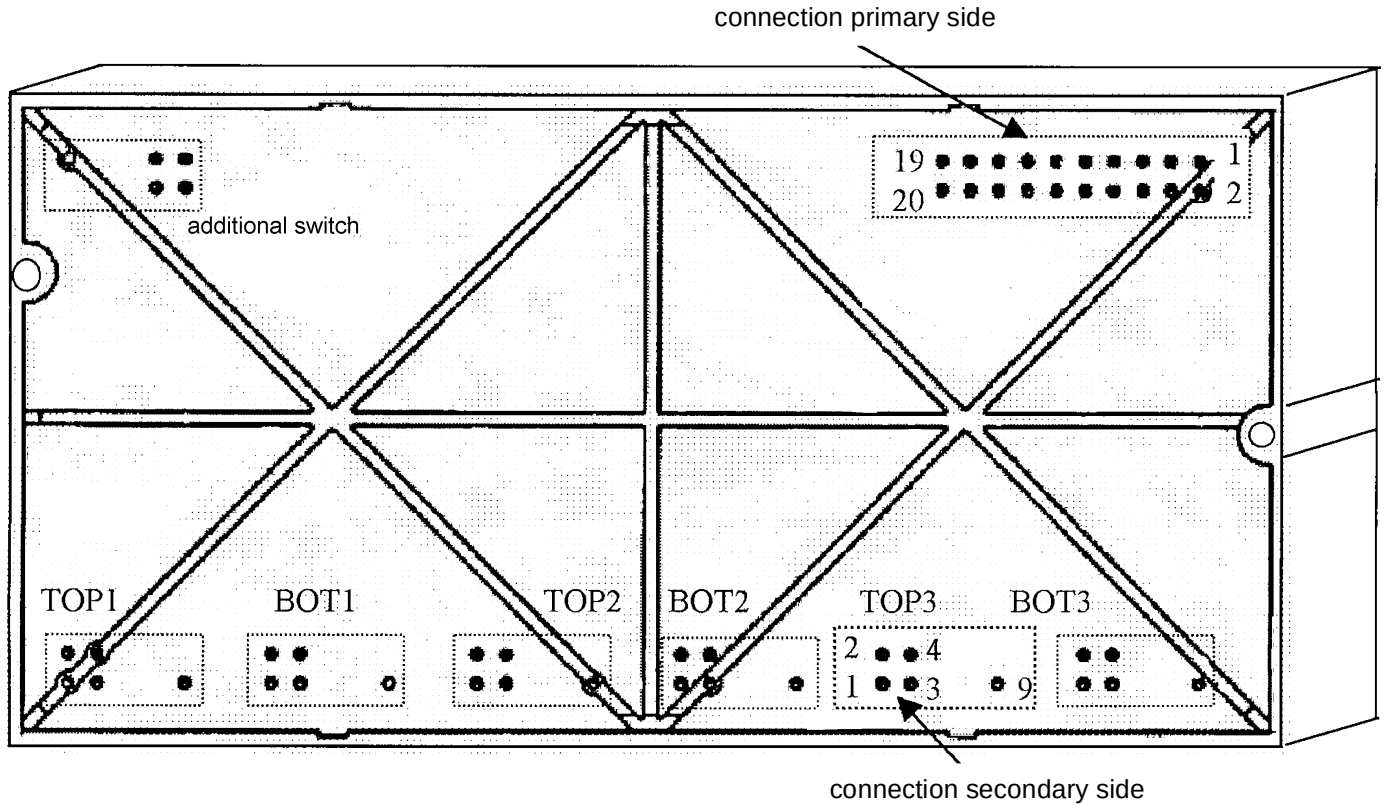

Fig. 1 Bottom view of the SKHI 61 / SKHI 71

Secondary side PIN array

Pin	Symbol	Function	Pin	Symbol	Function
01	R_{Gate}	Gate resistor input	04	$V_{CET}2$	VCE-threshold #2
02	$V_{CET}1$	VCE-threshold #1			
03	E	Emitter input	09	V_{CE}	Collector input

SEMIDRIVER™

SKHI 61 and SKHI 71

General properties and functions

The SKHI 61 and SKHI 71 are 6- and 7-channel drivers for IGBT- and MOSFET-modules and can be soldered directly onto the PCB. The drivers are physically separated.

Since all subassemblies necessary for operation have been integrated, there is no need for external components except for the gate resistors and the V_{CE}-circuitry. V_{CE}-thresholds and the blanking time are adjustable by integrating additional resistors and capacitors according to the customer's specifications.

Interlocking time can be adjusted by simple bridging of connector pins. The driver is equipped with a separate error input for immediate turn-off when receiving error signals from external components (e.g. over-temperature).

The independent seventh driver channel of the SKHI 71 guarantees for simple realisation of brake chopper, boost converter or PFC-circuit applications. By bridging of connector pins the driver error signal is transmitted directly to the SIXPACK-driver for turn-off.

Technical information

I. Primary side

The driver input signals may be transmitted directly to the driver inputs by the controller. The input signal circuit was designed to accept a wide voltage range (see table 1). The typical voltage level is at HCMOS level of V_{DD}=5V (0V=Off, +5V=On).

However, also 15V-signals may be applied with the same turn-on/turn-off thresholds without additional requirements. In this case the input resistance will be different (see table 1).

Status	Level / V			Input Impedance	
	min	typ	max	Ch. 1-6	Ch7
ON 5V	4,0	5,0	5,5	60 kΩ	2,4 kΩ
ON 15V	4,0	15,0	15,6	7 kΩ	1,6 kΩ
OFF 0V	-0,7	0	1,5	60 kΩ	2,4kΩ

Table 1: Input voltage level and input impedances

Error input signal

The error input signal can gather error signals of other hardware components, such as temperature sensors, in a "wired-or"-connection for direct turn-off of the driver. In this case an external pull-up resistor must not be connected.

Note: It is not possible to connect the error output of the SKHI 61/71 to an error input of the SKHI 61/71. But the error output of the chopper driver (SKHI 71) can be connected directly to the error input.

Error output signals

i) 6pack - driver

The error signal of the 6-PACK driver is equipped with an active push-pull output buffer which switches towards zero Volt in case of an error and actively towards + 5 V under operating conditions. The error memory may only be reset, if no error is pending and all cycle signal inputs are set to LOW for t > 9 µs at the same time. If any other external signals are intended to be connected to the error signal _ERR, the _ERR-signal must be uncoupled (see Figure 2) .

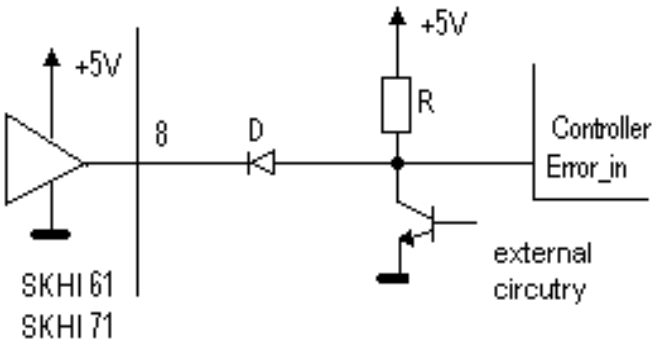

Fig. 2 _ERR-Signal in an „open-collector“-circuit

State _ERROR	Level / V		I / mA	Typical error memory set back time	
	min	max	max	6-PACK	seventh driver
Error	0	0.8	5	16µs	7µs
No error	4	5	5		

Table 2: Error output signal ratings

ii) chopper driver (only SKHI 71)

The error output signal of the additional driver has been designed as an open collector output. A pull-up resistor against the controller's +V_{CC} has to be connected to the controller input for error indication. In case of error, the signal is turned towards earth (zero Volt/ active LOW), otherwise the output will be highly resistive. The error signal of the additional switch will only be active as long as the input signal is on High-level. It is not logically connected to the other six input signals. The error signal of the additional switch may also be directly connected to the error input of the SIXPACK-driver, without requiring an external pull-up resistor. This may be advantageous, if the SIXPACK-driver has to be turned off in case of e.g. a brake chopper error or if only one error signal is evaluated by the controller.

Configuration pins

The configuration pins serve to adjust the TOP/BOTTOM interlocking time of all halfbridges. Due to the special pin design the interlocking time can be adjusted by a simple connection to the BSTD terminal (BSS potential) on the PCB without requiring external components.

Pin	4µs (factory set)	3 µs	2 µs	1 µs	no inter-lock)+
TDT1	open	open	GND	GND	X
TDT2	open	GND	open	GND	X
SEL	open	open	open	open	GND

Table 3: Values for interlocking time adjustment „X“ = no effect

)+ TOP and BOTcan be switched simultaneously!

II. Secondary side

We have provided for five terminals per input. Two of them are required for driving the IGBT, one is for short-circuit protection. The remaining two have been designed for optional adjustment of the V_{CE}-threshold.

IGBT-driver signals

We have provided for one gate- and one emitter input pin per power switch, i.e. there is one gate resistor for turn-on and turn-off each. The earth connection of the driver is directly connected to the IGBT's emitter via the emitter input, whereas a resistor of at least 10 Ω has to be connected to the gate circuit. This resistance is the minimum limit value controlled by the driver output buffer in order to limit the pulse currents to their peak value.

A 20 kΩ-resistor has been interconnected between gate and emitter (for the case that the supply voltage breaks down).

Gate-Emitter-voltage	min	Typ	max	Unit
OFF (neg.)	-10	-6.5	-5	V
ON	14,4	14,9	15,4	V
Temperature drift	12	14	16	mV/K

Table 4: Gate-emitter-voltage at T_A = 25 ℃

V_{CE} -threshold and V_{CE} -monitoring

V_{CE}-monitoring is done by connection of the driver collector pin to the collector of the power semiconductor.

If the turn-off threshold for short-circuit protection is to be reduced (standard 5,8 V), a resistor has to be connected between the V_{CET1}-threshold#1 pin 2 and V_{CET2}-threshold#2 pin 4 (see fig. 4; Value to be calculated by equation 1). Please do not forget to adapt the blanking time[1] accordingly.

This can be done by attaching a capacitor (value to be calculated by equation 2) between V_{CE}-threshold (pin 2) and earth (pin 3). The V_{CE}-threshold may be adjusted to a minimum value of about 3 V (R_{VCE} = 0 Ω).

1. Blanking time: time between turn-on of the power semiconductor and V_{CE}-registration

$$C_{VCE}[nF] = \frac{t_{blank}[\mu s] \cdot (72{,}75 + R_{VCE}[k\Omega])}{(R_{VCE}[k\Omega] + 4{,}75) \cdot 36{,}08} - 0{,}1$$

Equation 1

$$R_{VCE}[k\Omega] = \frac{11{,}86}{5{,}4 - 0{,}93\, V_{CE}} - 4{,}75$$

Equation 2

The V_{CE}-threshold cannot be increased, so that the preset value of 5,8 V is the maximum value.

V_{CE}-monitoring can also be suppressed by connecting the collector pin V_{CE} of one driver to the belonging emitter pin E and not to the collector of the power semiconductor.

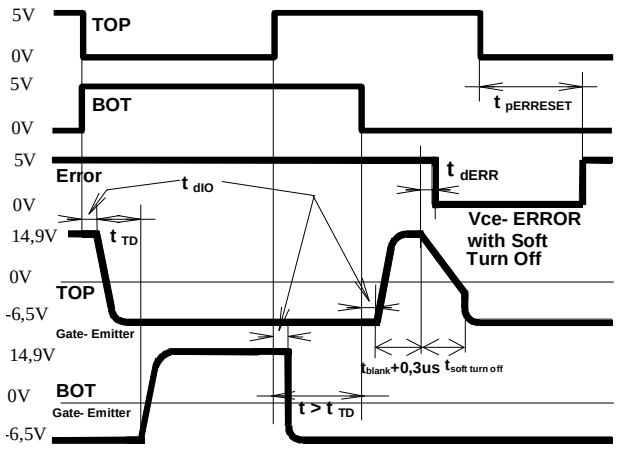

Fig. 3 Course diagram: TOP and BOT-inputs and signal Error compared to TOP and BOT-Gate-Emitter-signal (valid for all halfbridges).

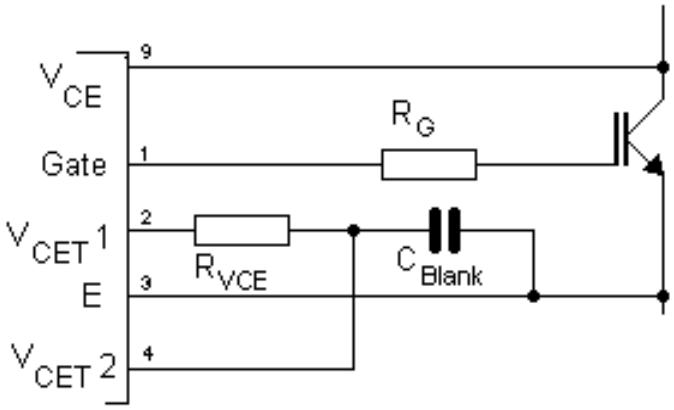

Fig. 4 Connection principle of a power switch with a specifically adjusted V_{CE}-threshold

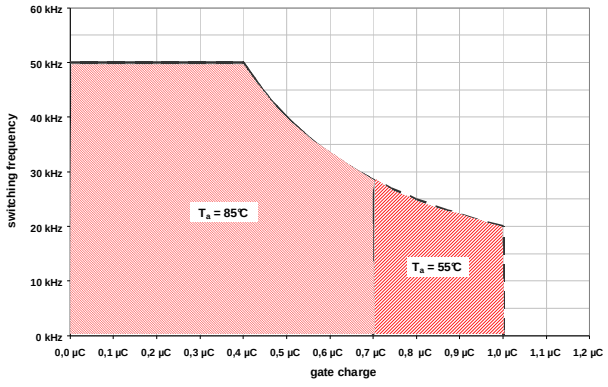

Fig. 5 Maximum rating for output gate charge per pulse

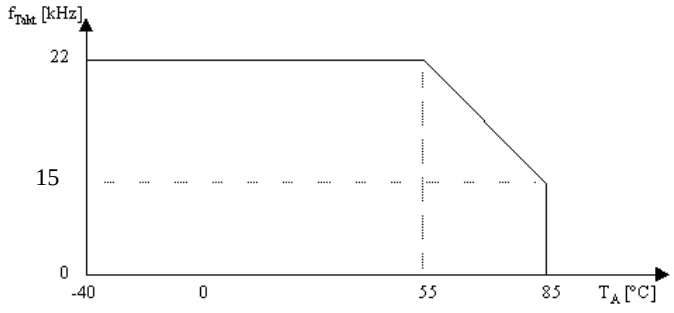

Fig. 6 Maximum cycling frequency at Q_{GE} = 1000 nC vs temperature

The application range can be calculated by the average output current of 20 mA and the repetetive acceptable peak current of 2 A. It has to be considered that the curves are valid for Q_{gmax} = 1 µC only.

The maximum switching frequency f_{max} may be calculated with the following formula, the maximum value however being 50 kHz due to switching reasons:

fmax (kHz) = $2*10^4$ / Q_{GE} (nC)

operating the SKHI 61: besides the operating voltage only the six driver signals TOP1...BOT3 and the driver error output signal are connected to the controller on the primary side. The secondary side is working with the preset V_{CE}-threshold of 5,8 V.

Fig. 7 and 8 show examples for connection of a SKHI 71 for the application with MiniSKiiP (SKiiP 32 NAB 12) and the following adjustments:

- Temperature monitoring of the power semiconductor
- V_{CE}-threshold : 4,8 V
- Interlocking time : 2 µs
- Error blanking time for V_{CE}-threshold : 4 µs

Application Hints

To adjust different V_{CE} thresholds there is needed an additional resistor R_{VCE} and a capacitor C_{VCE} for each switch.

Gate resistor : R_G = 33 Ω

V_{CE}-threshold resistor: intended U_{VCE} = 4,8 V

Applying equation 1 R_{VCE} will result in

$$R_{VCE}[k\Omega] = \frac{11,86}{5,4 - 0,93 \cdot 4,8} - 4,75[k\Omega] = 7,9k\Omega$$

Next value taken from the E24-range: 8,25 k. The threshold voltage is recalculated with 8,25 kΩ.

V_{CE}-threshold at 4,82 V.

For the capacitor the blanking time may be calculated as: $t_{blanking}$ = 4 µs

$$C_{VCE}[nF] = \frac{4 \cdot (72,75 + 8,25)}{(8,25 + 4,75) \cdot 36,08} - 0,1 = 590pF$$

Thus there can be chosen a capacitor of 680 pF.

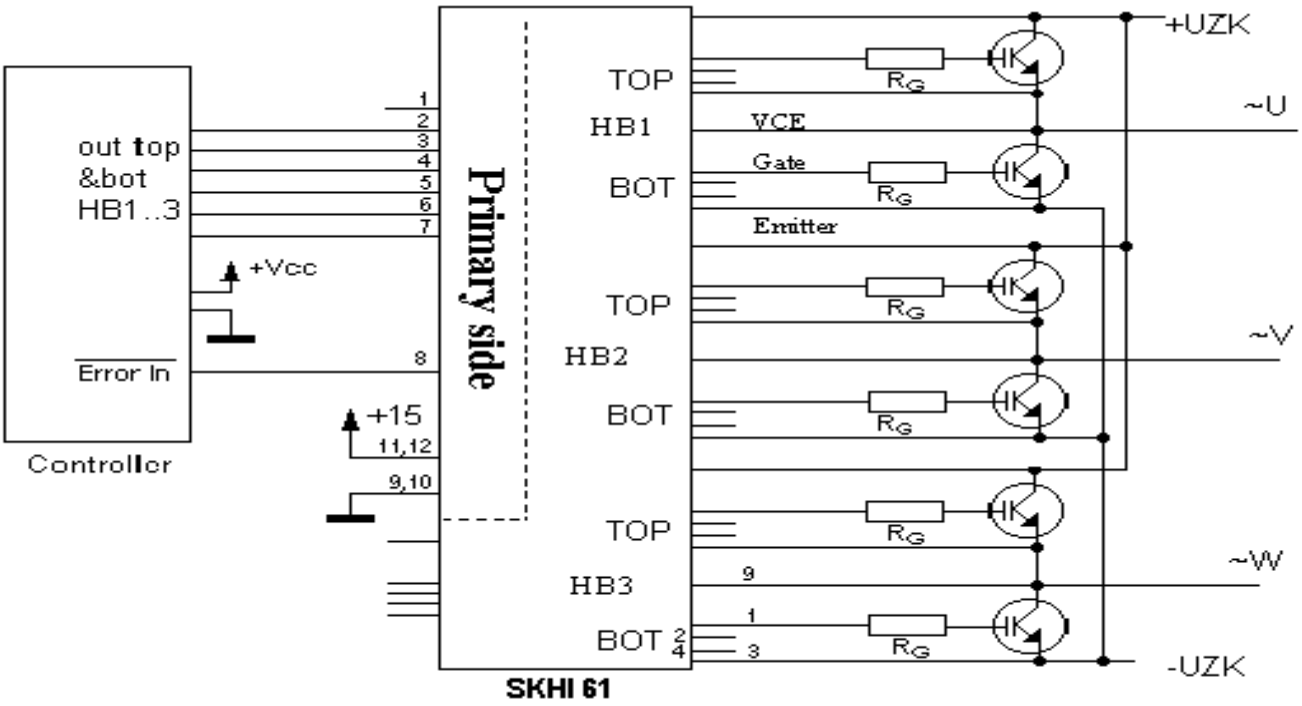

Fig. 7 SKHI 61 block diagram

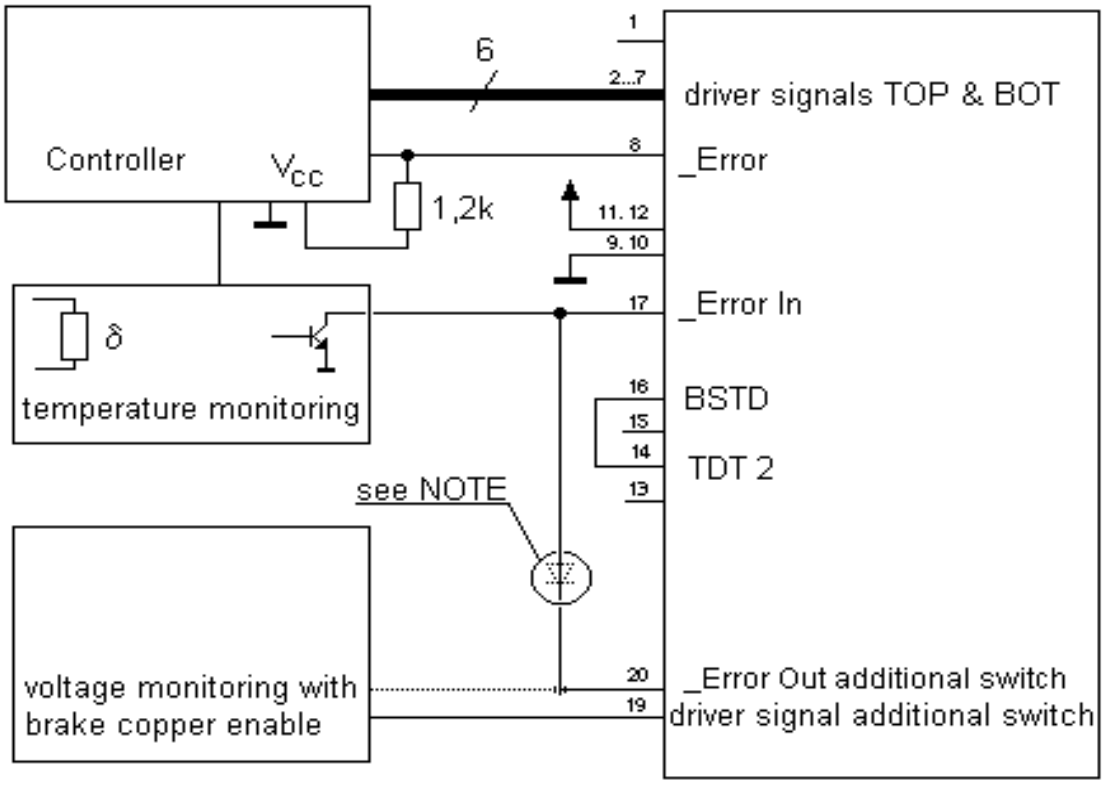

Fig. 8 Examply circuit for a SKHI 71 connected to the primary side

NOTE: If the _ErrorOut-signal of the additional switch (here brake chopper) is also needed for other evaluations, a Schottky diode has to be connected as shown in the figure above to uncouple the signal. Furthermore there has to be connected a pull-up resistor to the additional error output. It is useful to use a capacitor (typ. 100 pF, absolute maximum 2,2 nF) at the _ErrorIn to avoid undesired couplings.

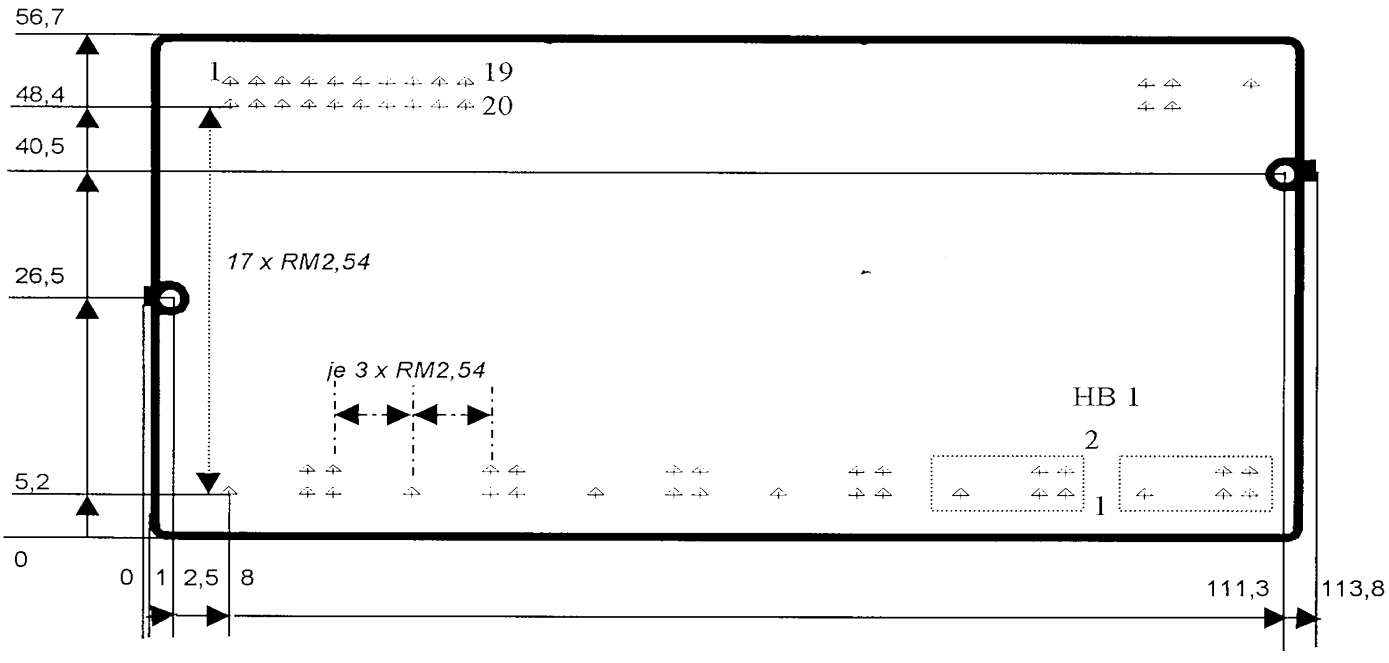

Fig. 9 Dimensional drawing, layout

View: tooling side (top view, driver put on top of the PCB)
Measurements taken in [mm]
Grid of connector pins; gaps between pins: RM2,54
Pin dimensions : 0,64 mm x 0,64 mm ; length 3,2 mm

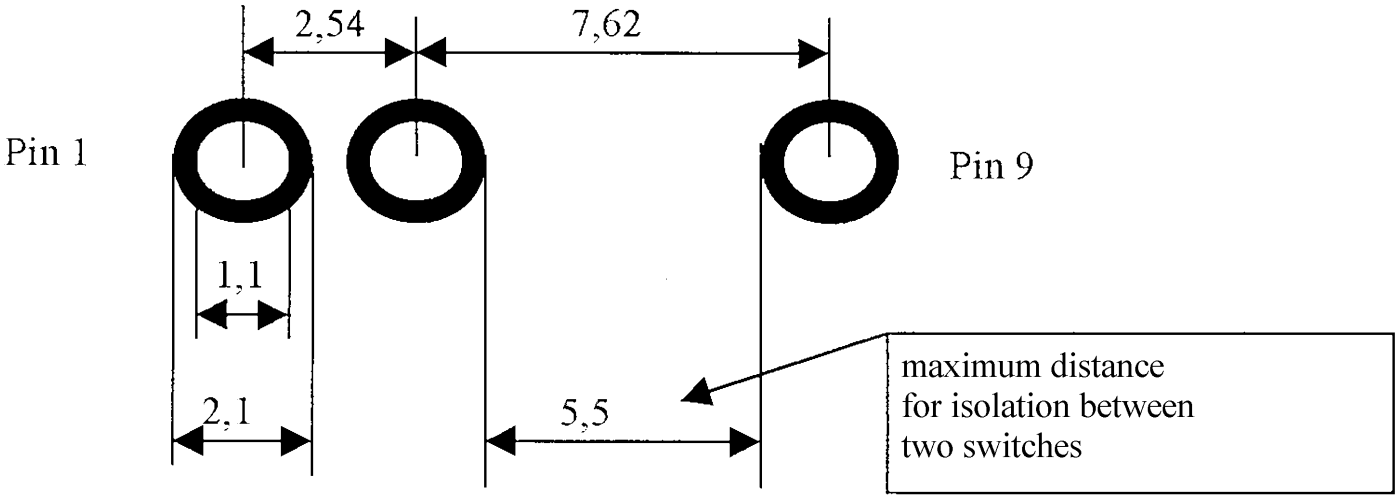

Fig. 10 Measurements in [mm] for solder pads (as a proposal for the design) and solder pad gaps (partial drawing)