Introduction

The 65520 and 65530 High Performance VGA Flat Panel / CRT controllers provide a powerful, yet versatile, feature set optimized for portable PC requirements. The 65520 / 530, which integrates the VGA controller, industry standard RAMDAC, and monitor sense circuitry, enable a complete VGA sub-system to be implemented with just four chips: CHIPS' 65520 or 65530 VGA Controller, CHIPS' 82C404 Programmable Clock Synthesizer, and two memory devices. The 65520 / 530 employs separate address and data buses and direct panel drive outputs so that no external buffers are required. Pinouts are optimized for PCB board layout such that the VGA sub-system can be implemented in less than 4 square inches (2580 sq mm). The 65520 / 530 can use a variety of video memory configurations, enabling OEMs to differentiate their portable PC products by modifying video memory (e.g., two 256Kx4 DRAMs for low-cost systems; four 256Kx4 VRAMs for high-performance systems; and an optional VRAM frame buffer / accelerator for additional features / performance).

The 65520 / 530 provides high performance by use of zero wait-state writes (write buffer), minimum wait-state reads (internal asynchronous FIFO design), 16-bit CPU and I/O interfaces, and 8/16-bit internal video data paths. The 65520 / 530 may use dual-port VRAMs, which provide higher performance than single-port DRAMs, for video memory. The 65520 / 530 fully supports the ISA, EISA, MC and PI (Peripheral Interface) buses. In addition, the 65530 provides a direct connection to a 386 SX CPU Local Bus.

The 65520 / 530 provides a variety of programmable features to optimize display quality, such as simultaneous LCD/CRT display capability (with the optional frame buffer), Vertical and Horizontal Compensation, SMARTMAP™, Text Enhancement, three selectable RGB color-to-gray-scale reduction techniques, and a polynomial FRC gray scale algorithm which reduces flicker on fast response "mouse quick" displays without increasing the panel's vertical refresh rate.

The 65520 and 65530 produce up to 64 gray scales on a wide variety of monochrome LCD, EL and plasma flat panels with resolutions up to 1280x1024. The 65520 supports color TFT LCD panels with a 24,389-color palette. The 65530, which is pin-compatible with the 65520 and contains a superset of the 65520's features, supports color TFT LCD panels with a 185,193-color palette and color STN LCD panels with a 226,981-color palette. The 65520 and 65530 directly support analog and digital CRT monitors -- interlaced monitors up to 1024 x 768 x 16 colors and non-interlaced monitors up to 800 x 600 x 256 colors.

The 65520 / 530's advanced power management features, which are tightly coupled with CHIPS' 82C404 Programmable Clock Synthesizer, reduce power consumption of the display subsystem and extend battery life in portable applications. The 65520 / 530 provides CAS-before-RAS refresh cycles for DRAMs. 65520 / 530-based systems may be implemented using VRAMs, which consume significantly less power while increasing performance, for video memory. 65520 / 530-based systems may also employ an optional VRAM frame accelerator which serves to lower power consumption by decreasing the dot clock required for a given panel shift clock.

The 65520 / 530 are fully compatible with IBM's VGA standard at the register, gate and BIOS levels. Enhanced backwards compatibility is provided with the EGA, CGA, Hercules™, and MDA standards without using NMIs. Also available from CHIPS and third-party vendors are a fully VGA-compatible BIOS, end-user utilities, and drivers for Super-VGA modes, Windows™ panning, and portrait / landscape rotation.

MINIMUM CHIP COUNT / BOARD SPACE

The 65520 / 530 was designed to integrate as many functions as economically as possible to minimize chip count and board space. The 65520 / 530 integrates the VGA controller, industry standard RAMDAC, monitor sense circuitry, and buffers with sufficient drive capability to directly drive most flat panels. The 65520 / 530 employ separate address and data buses so that no external buffers are required.

Using a 65520 or 65530, a complete VGA-compatible 16-bit video subsystem for motherboard applications can be built with just 4 ICs, including display memory and clock synthesizer, as shown in the following bill of materials table:

Qty	Chip Type
1	65520 or 65530 VGA Controller
1	82C404 Programmable Clock Synthesizer
2	256Kx4 DRAMs
4	Total

In some applications, external driver chips may be required for additional signal drive. Improved performance or other optional features may require implementation of more than the minimum two memory chips, such as support of simultaneous display capability on certain types of panels, support of high-resolution 256-color display modes (which require more than 256K of display memory), or ability to drive high-resolution (up to 1280x1024) monochrome panels.

DISPLAY MEMORY INTERFACE

The 65520 and 65530 pin-compatible VGA controllers can employ multiple video memory configurations providing the OEM with flexibility to use the same VGA controllers in several designs with differing cost, power consumption, and performance criteria.

The 65520 and 65530 offer a low cost system implementation by supporting operation with two or four 256Kx4 DRAMs, and a high performance and lower power system with two or four VRAMs.

The 65520 and 65530 support the following video memory configurations:

- Two 128Kx8 PSRAMs (256 KBytes)
- Two 256Kx4 DRAMs (256 KBytes)
- Four 256Kx4 DRAMs (512 KBytes)
- Two 256Kx4 VRAMs (256 KBytes)
- Four 256Kx4 VRAMs (512 KBytes)
- Two 256Kx8 VRAMs (512 KBytes)
- Two 512Kx8 DRAMs (1 MByte)

Implementing a 65520 / 530 Video Subsystem with two 256Kx4 DRAMs results in a cost-efficient system. In this configuration the 65520 / 530 support all standard VGA display modes.

Performance is significantly improved when the 65520 / 530 is configured with four 256Kx4 DRAMs. Standard VGA display modes are achieved along with high resolution 800x600 pixels 256 colors, 1024x768 pixels in 16 colors, and 132-column text modes.

A 65520 or 65530-based Video Subsystem implemented with two or four 256Kx4 VRAMs offers superior performance and considerable power savings in normal operating modes. High resolution CRT monitor support up to 1024x768 pixels in 16 colors and 800x600 pixels in 256 colors are achieved.

The entire display memory (256 Kbytes or 512 Kbytes) is always available to the CPU in regular four-plane mode, chained two-plane mode, and super-chained one-plane mode.

Display memory control signals are derived from the memory clock (MCLK) input.

The 65520 / 530 serves as a DRAM controller for the system's display memory. It handles DRAM refresh, fetches data from display memory as required to refresh the screen, interfaces the CPU to display memory and supplies all necessary DRAM control signals. The display memory is arranged as four planes of 64 Kbytes each. Each plane is eight bits wide for a total of 32 bits. Planes 0 and 1 share a common address bus, as do Planes 2 and 3. Each plane has a separate CAS signal and share a common RAS and write enable. 120ns DRAMS are required for clock inputs to up 30 MHz. Pseudo-Static and SRAMS can be supported with external address latches.

CPU BUS INTERFACE

The 65520 / 530 provides on-chip support for interface to EISA/ISA (PC/AT), MC (Micro Channel), 386 SL PI ('Peripheral Interface'), and (in the 65530) 386 SX Local Bus. Strap options allow the user to configure the chip for the type of interface desired. Control signals for all interface types are integrated on chip. Support is provided for 8-bit and 16-bit cycles for both memory and I/O. All operations necessary to ensure proper operation in these various environments are handled in a fashion transparent to the CPU. These include internal decoding of all memory and I/O addresses, bus width translations, and generation of the necessary control signals. The 65530 also provides a 'linear addressing' feature which allows display memory to be accessed in any area of upper memory up to 1MB in size.

EARLY MEMORY R/W INDICATION

In the ISA bus interface configuration, the 65520 / 530 provide an output called ERMEN/. When the CPU executes a memory read or write cycle in text mode, ERMEN/ goes low two MCLK cycles prior to the fall of RAS/ and stays active until RAS/ is asserted. ERMEN/ is driven high in graphics modes and during all display refresh accesses.

DISPLAY INTERFACE

The 65520 / 530 is designed to support a wide variety of flat panel and CRT displays of all different types and resolutions.

Flat Panel Displays

The 65520 / 530 supports all flat panel display technologies including plasma, electroluminescent (EL) and liquid crystal displays (LCD). LCD panel interfaces are provided for single panel-single drive (SS), dual panel-single drive (DS) and dual panel dual drive (DD) configurations. A single panel sequences data similar to a CRT (i.e., sequentially from one area of video memory). In contrast, a dual panel requires video data to be provided alternating between two separate areas of memory. In addition, a dual drive panel requires the data from the two areas to be provided simultaneously. Due to its integrated line buffer, the 65520 / 530 supports all panels directly. Support for LCD-DD panels does not require external hardware (such as a frame buffer). The 65520 / 530 handles display data sequencing transparently to application software providing full compatibility on both CRT and flat panel displays.

The 65520 / 530 supports panel resolutions up to 1280x1024, including the popular panel resolutions of 640x200, 640x400, 640x480, 800x600, 1024x768, and 1280x1024. For non-standard applications additional resolutions are supported.

There is currently no standard interface for flat panel displays. Interface signals and timing requirements vary between panel technologies and manufacturers. The 65520 / 530 provides register programmable features to allow interfacing to the widest possible range of flat panel display units. The 65520 / 530 provides a direct interface to panels from vendors such as Sharp, Sanyo, Epson, Seiko Instruments, Oki, Toshiba, Hitachi, Fujitsu, NEC, Matsushita/Panasonic, and Planar.

CRT Displays

The 65520 / 530 supports high resolution fixed frequency and variable frequency analog monitors in interlaced and non-interlaced modes of operation. Digital monitor support is also built in.

The 65520 / 530 supports resolutions up to 800x600 pixels with 16 colors in a 256 KB display memory configuration and supports Super-VGA resolutions such as 800x600 256 colors and 1024x768 16 colors in 512KB or 1MB display memory configurations.

Simultaneous Flat Panel / CRT Display

The 65520 / 530 provides simultaneous display operation with Multi-Sync variable frequency or PS/2 fixed frequency CRT monitors and single panel-single drive LCDs (LCD-SS), dual panel-single drive LCDs (LCD-DS), dual panel-dual drive LCDs (LCD-DD) and plasma and EL panels (which employ single panel-single drive interfaces). Single drive panels sequence data in the same manner as CRTs, so the 65520 / 530 provides simultaneous display with CRTs and LCD-SS, LCD-DS, plasma or EL panels by driving the panels with CRT timing. No external hardware is required. In contrast, LCD-DD panels require video data alternating between separate locations in memory. In addition, a dual-drive panel requires data from both locations simultaneously. The 65520 / 530 provides simultaneous display with LCD-DD and CRT monitors by employing a 64Kx4 VRAM as a frame buffer for panel sizes up to 640x480 and a 256Kx4 VRAM for higher resolution panels.

VRAM frame buffers offer significant advantages relative to competitors' DRAM frame buffers. A DRAM frame accelerator requires that the flat panel be refreshed at double the CRTs vertical refresh rate. Therefore, an expensive 6.3 MHz LCD (with 120 Hz panel vertical refresh rate) is required for simultaneous display with 60 Hz CRT monitors when a DRAM frame buffer is used. Due to its higher bandwidth relative to DRAMs, a VRAM frame buffer can refresh both the flat panel and CRT at the same vertical refresh rate. Therefore, inexpensive 3 MHz and 6 MHz LCDs (in addition to 6.3 MHz LCDs) can be used for simultaneous display with 60 Hz and 72 Hz CRT monitors when a VRAM frame buffer is used.

DISPLAY ENHANCEMENT FEATURES

Display quality is one of the most important considerations in the success of any flat-panel-based system design. The 65520 / 530 provides many features to enhance flat panel display qulaity.

Superior Display Quality

The 65520 / 530 produces up to 64 flicker-free gray scales on monochrome or grayscale panels. Because most application software is written for color CRT monitors, the 65520 / 530 provides several proprietary features to maximize display quality on monochrome flat panels. Via its Extension Registers, the 65520 / 530 provides the flexibility to interface to a wide range of flat panels

and provide full compatibility transparently to the application software. The 65520 / 530 enables flat panel display operation simultaneously with the CRT monitor.

RGB Color To Gray Scale Reduction

The 18 bits of color palette data from the VGA standard color lookup table (CLUT) are reduced to 6 bits for 64 gray scales via one of three selectable RGB color to gray scales reduction techniques:

1) NTSC Weighting: 59% Red 30% Green 11% Blue
2) Equal Weighting: 5/16 Red 6/16 Green 5/16 Blue
3) Green Only: 6 bits of Green only

NTSC is the most common weighting, which is used in television broadcasting. Equal weighting increases the weighting for Blue, which is important for Applications such as Microsoft Windows 3.0 which often uses Blue for background colors. Green Only is useful for replicating on a flat panel the display of software optimized for IBM's monochrome monitors which use the six Green bits of palette data.

Gray Scale Algorithm

A proprietary polynomial-based Frame Rate Control (FRC) and dithering algorithm in the 65520 / 530's hardware generates 64 gray levels on monochrome panels. The FRC technique simulates 16 gray levels on monochrome panels by turning the pixels on and off over several frames in time. The dithering technique increases the number of gray scales from 16 to 64 by altering the pattern of gray scales in adjacent pixels. By programming the polynomial (an 8-bit value in Extension Register XR6E), the FRC algorithm may be adjusted to reduce flicker without increasing the panel's vertical refresh rate. The persistence (response time) of the pixels varies among panel manufacturers and models. By re-programming the polynomial by trial-and-error while viewing the display, the FRC algorithm can be adjusted to match the persistence of the particular panel. With this technique, the 65520 / 530 produces 64 flicker-free gray scales on the latest fast response "mouse quick" film compensated monochrome STN LCDs. The alternate method of reducing flicker -- increasing the panel's vertical refresh rate -- has several drawbacks. As the vertical refresh rate increases, the panel's power consumption increases, ghosting (cross-talk) increases, and contrast decreases. The maximum vertical refresh rate specified by panel manufacturers is often well below 100 Hz. CHIPS' polynomial FRC gray scale algorithm reduces flicker without increasing the vertical refresh rate.

Vertical & Horizontal Compensation

Vertical & Horizontal Compensation are programmable features that adjust the display to completely fill the flat panel display. Vertical Compensation increases the usable display area when running lower resolution software on a higher resolution panel. Unlike CRT monitors, flat panels have a fixed number of scan lines (e.g., 200, 400, 480 or 768 lines). Lower resolution software run on a higher resolution panel only partially fills the usable display area. For instance, 350-line EGA software displayed on a 480-line panel would leave 130 blank lines at the bottom of the display and 400-line VGA text or Mode 13 images would leave 80 blank lines at the bottom. The 65520 / 530 offers the following Vertical Compensation techniques to increase the useable screen area:

Vertical Centering displays text or graphics images in the center of the flat panel, with a border of unused area at the top and bottom of the display. Automatic Vertical Centering automatically adjusts the Display Start address such that the unused area at the top of the display equals the unused area at the bottom. Non-Automatic Vertical Centering enables the Display Start address to be set (via programming the Extension Registers) such that text or graphics images can be positioned anywhere on the display.

Line replication (referred to as "stretching") duplicates every Nth display line (where N is programmable), thus stretching text characters and graphic images an adjustable amount. The display can be stretched to completely fill the flat panel area. Double scanning, a form of line replication where every line is replicated, is useful for running 200 line software on a 400 line panel or 480 line software on a 1024 line panel.

Blank line insertion, inserts N blank lines (where N is programmable) between each line of text characters. Thus text can be evenly spaced to fill the entire panel display area without altering the height and shape of the text characters. Blank line insertion can be used in text mode only.

Tall Fonts™ uses a non-VGA standard font such that text fills almost all lines on the flat panel and all lines of text are the same size. For example, an 8x19 font would fill 475 lines on a 480-line panel, or an 8x30 font would fill 750 lines on a 768-line panel. TallFonts can be used in text mode only.

Each of these Vertical Compensation techniques can be controlled by programming the Extension Registers. Each Vertical Compensation feature can be individually disabled, enabled and adjusted. A

combination of Vertical Compensation features can be used by adjusting the features' priority order. For example, text mode vertical compensation consists of four priority order options:

- Double Scanning+Line Insertion, Double Scanning, Line Insertion
- Double Scanning+Line Insertion, Line Insertion, Double Scanning
- Double Scanning+Tall Fonts, Double Scanning, Tall Fonts
- Double Scanning+Tall Fonts, Tall Fonts, Double Scanning

Text and graphics modes offer two Line Replication priority order options:

- Double Scanning+ Line Replication, Double Scanning, Line Replication
- Double Scanning+ Line Replication, Line Replication, Double Scanning

Horizontal Compensation techniques include Horizontal Compression, Horizontal Centering, and Horizontal Doubling. Horizontal Compression will compress 9-dot text to 8-dots such that 720-dot text in Hercules modes will fit on a 640-dot panel. Automatic Horizontal Centering automatically centers the display on a larger resolution panel such that the unused area at the left of the display equals the unused area at the right. Non-Automatic Horizontal Centering enables the left border to be set (via programming the Horizontal Centering Extension Register) such that the image can be positioned anywhere on the display. Automatic Horizontal Doubling will automatically double the display in the horizontal direction when the horizontal display width is equal to or less than half of the horizontal panel size.

SmartMap™

SmartMap™ is a proprietary feature that can be invoked to intelligently map colors to gray levels in text mode. SmartMap™ improves the legibility of flat panel displays by solving a common problem:

Most application programs are optimized for color CRT monitors using multiple colors. For example, a word processor might use a blue background with white characters for normal text, underlined text could be displayed in green, italicized text in yellow, and so on. This variety of colors, which is quite distinct on a color CRT monitor, can be illegible on a monochrome flat panel display if the colors are mapped to adjacent grayscale values. In the example, underlined and italicized text would be illegible if yellow is mapped to grayscale 4, green to grayscale 6 with the blue background mapped to grayscale 5.

SmartMap™ compares and adjusts foreground and background grayscale values to produce adequate display contrast on flat panel displays. The minimum contrast value and the foreground / background grayscale adjustment values are programmed in the 65520 / 530's Extension Registers. This feature can be disabled if desired.

Text Enhancement

Text Enhancement is another feature of the 65520 / 530 that improves image quality on flat panel displays. Many applications, such as MS-DOS, use Dim White for normal text characters, which results in non-optimal contrast on flat panels. When turned "on," the Text Enhancement feature displays Dim White as Bright White, thereby optimizing the contrast level on flat panels. This feature inverts the functionality of the Intensity Bit for White only. Highlighted white, which is displayed as Bright White when Text Enhancement is "off," is shown as Dim White with Text Enhancement "on," thus maintaining a difference between normal and highlighted text. Text Enhancement can be turned "on" and "off" by changing a bit in one of the Extension Registers.

Inverse Video

Inverse video can be enabled in text modes only on the flat panel (normal video is displayed on the CRT and in graphics modes on the flat panel), in graphics modes only on the flat panel (normal video is displayed on the CRT and in text modes on the flat panel), or in both text and graphics modes on flat panel.

ADVANCED POWER MANAGEMENT

The 65520 / 530 provides a number of advanced power management features to minimize power consumption during normal flat panel operation in addition to Standby/Sleep modes. In addition, the 65520 / 530 addresses the specific requirements of notebook design by providing different modes of operation to optimize power usage. The table at the bottom of the page summarizes these modes and display memory access in each.

Normal Operating Mode

The 65520 / 530 are full custom, low power CMOS integrated circuits which have a number of features to minimize power consumption during normal operation. The highly modular design enables entire functions in the chip to be powered down when not in use (e.g. such as the DACs during panel-only operation). Second, CAS before RAS video memory refresh is supported, which results in additional power savings. Third, the 65520 / 530 can employ an optional frame accelerator (a 64Kx4 or 256Kx4 VRAM) which can lower power consumption by lowering the dot clock for a given panel shift clock. For example, a 4 MHz shift clock requires only a 16 MHz dot clock with a frame accelerator versus a 32 MHz dot clock without a frame accelerator. Fourth, the optional use of VRAMs (which consume significantly less power than DRAMs during normal operation due to the serial nature of the data and less address accessing) or pseudo-static RAMs for video memory. Fifth, the 65520 / 530 generate gray scales using a proprietary polynomial based FRC algorithm which produces flicker free display without utilizing very high vertical refresh rates which exceed panel specifications. (Note: the current drawn by the LCD alone increases by approximately 20% when the vertical refresh rate is increased from 85 Hz to 120 Hz). Lastly, the serially programmable 82C404 clock synthesizer can slow down the memory clock input to the 65520/530 to conserve power consumption in various modes (e.g., text modes).

Screen Blanking

The flat panel display and its backlight are typically the largest consumers of power in a portable PC. The 65520 / 530 permits blanking of the display by writing to bit-5 of the Sequencer Clocking Mode Register (SR01). With the screen blanked, all memory cycles are available to the CPU except those used for display memory refresh.

Panel Off Mode

The 65520 / 530 provides a dedicated input pin, PNLOFF/ to go to the Panel Off Mode. In Panel Off mode, the video section and internal RAMDAC are inactive but the CPU interface and display memory refresh are still active. Additionally, the video data and control signals may be driven or tri-stated through software control. The 65520 / 530 initiates panel power sequencing to turn off the flat panel.

Standby (Sleep) Mode

The 65520 / 530 enters the Standby power-down mode when the STNDBY/ input is low. During standby mode, the 65520/530 draws less than 1 mA.

While the 65520 / 530 is in Standby mode, the display is blanked, the display timing signals are halted, and the 65520 / 530 initiates panel power sequencing to turn off the flat panel. While in Standby mode the 65520 / 530 is invisible to the system. The CPU cannot access any internal registers or display memory.

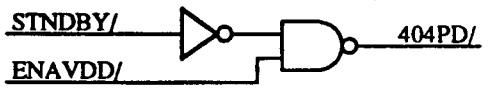
During Standby, the 65520 / 530 continues to refresh the DRAMs at a programmable rate to conserve power in display memory while preventing data loss. Refresh cycles can be turned off when pseudo-static RAMs or self refresh DRAMs are used. The 65520 / 530 may use 32 KHz input from the system real time clock for display memory refresh. This mode is useful when system operation is suspended. Extension registers XR52 and XR5F define the memory refresh cycle interval during Standby mode. The 65520 / 530 provides for very low refresh intervals from 16 usec (standard DRAMs) to 128 usec (slow refresh DRAMs), thereby extending battery life.

The 65520, when entering standby mode, requires MCLK to be active for at least 32 milliseconds. Therefore, the STNDBY/ pin of the 65520 and the PWRDN/ pin of the 82C404 should not be tied together. The signal used to power down the 82C404 must be delayed from the signal used to initiate the 65520 into standby mode. The PWRDN/ signal to the 82C404 can be generated simply by determining the status of the ENAVDD/ signal from the 65520. Please refer to the table below:

STNDBY/	ENAVDD/	404 PWRDN/
0	0	1
0	1	0
1	0	1
1	1	1

The 82C404 PWRDN/ signal should be forced low only when the status of the STNDBY/ input to the 65520 is low and the ENAVDD/ output from the

65520 is high. A simple circuit, using an inverter and a 2-input NAND gate, can be used to generate the '404PD/' signal as shown below:



The 65530 generates the output signal 404PD/, an alternate signal on pin 109, to be tied directly to the 82C404 PWRDN/ input signal. The 404PD/ is an alternate function on pin 109 and thereby this functionality cannot be used when the 65530 is in 4 VRAM mode.

Mode of Operation	RESET Pin	STNDBY/ Pin	PNLOFF/ Pin	Display Memory Access	Video Output
Normal	Low	High	High	Yes	Yes
Standby	Low	Low	High	No	No
Panel Off	Low	High	Low	Yes	No

Note: Combinations of pin levels not shown in the table above are illegal and should not be used.

3.3V OPERATION

The 65520 / 530 supports operation at either 5.0V ±10% or 3.3V ±0.3V. The 65520 requires that all VCC inputs be either 5V or 3.3V. In contrast, the 65530 provides "mixed" 5V and 3.3V operation by providing dedicated VCC pins for the 65530's internal logic, bus interface, memory interface, and display interface. Each dedicated VCC can be either 5V or 3.3V, such that the 65530 internal logic operates at 3.3V and the various interfaces at either 3.3V or 5V. The following table shows the relationship between the VCC inputs to the 65530 and the interface pins controlled by each VCC input. In "mixed" voltage mode, the VCC input on pin 80 must be 5V. The VCC input on pin 80 can only be 3.3V if all other VCC inputs are 3.3V.

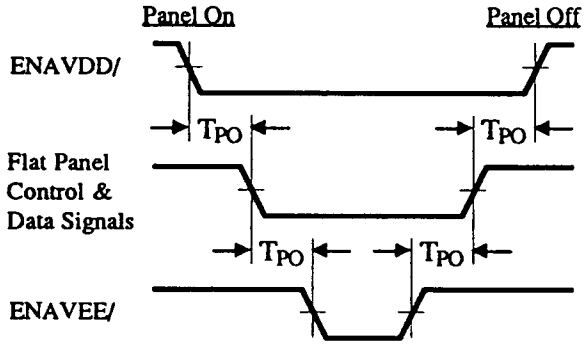
VCC Pins	Interface	Pins Affected
20	Internal Logic	--
100	Internal Logic	100-111
140	Memory	1-12, 116-160
60	Bus	13-19, 22-68
80	Video	69-99, 112-115

SELF REFRESH DRAMs

The 65520 / 530 support the self-refresh feature of certain 256Kx4 and 512Kx8 DRAMs during STANDBY mode thus enabling the 65520 / 530 to be powered down completely during STANDBY mode, extending battery life in portable computer applications.

PANEL POWER SEQUENCING

Flat panel displays are extremely sensitive to conditions where full biasing voltage VEE is applied to the liquid crystal material without enabling the control and data signals to the panel. This results in severe damage to the panel and may disable the panel permanently. The 65520 and 65530 provide a simple and elegant method to sequence power to the flat panel display during various modes of operation to conserve power and provide safe operation to the flat panel. The 65520 / 530 provides two pins called ENAVEE/ and ENAVDD/ to regulate the LCD Bias Voltage (VEE) and the driver electronics logic voltage (VDD), to provide intelligent power sequencing to the panel. The timing diagram below illustrates the power sequencing cycle. In the 65520, the power on/off delay time (TPO) is fixed at 32 mS; in the 65530 it is programmable (with a default of 32 mS).



Panel Power Sequencing

The 65520 / 530 initiates a 'panel off' sequence if either the PNLOFF/ or STNDBY/ input is asserted (low), if the chip is programmed to enter 'panel off' mode (by setting extension register XR52 bit-3=1), or if the 'Display Type' is programmed to 'CRT' (extension register XR51 bit-2 = 0). The 65520 / 530 initiates a 'panel on' sequence if both PNLOFF/ and STNDBY/ inputs are high and the chip is programmed to 'panel on' (XR52 bit-3=0) and 'flat panel display' (XR51 bit-2=1).

FULL COMPATIBILITY

The 65520 and 65530 are fully compatible with the IBM™ VGA standard at the hardware, register, and BIOS level. The 65520 and 65530 also provide enhanced backward compatibility to EGA™, CGA™, Hercules™, and MDA™ standards without using NMIs. These controllers include a variety of features to provide compatibility on flat panel displays in addition to CRT monitors. Internal compensation techniques ensure that industry-standard software designed for different displays can be executed on the single flat panel used in an implementation. Mode initialization is supported at the BIOS and register levels, ensuring compatibility with all application software.

Write Protection

The 65520 / 530 has the ability to write protect most of the standard VGA registers. This feature is used to provide backwards compatibility with software written for older generation display types. The write protection is grouped into register sets and controlled by the Write Protect Register (XR15).

Extension Registers

The 65520 / 530 employs an "Extension" Register set to control its enhanced features. These Extension Registers provide control of the flat panel interface, flat panel timing, vertical compensation, SMARTMAP™, and Backwards Compatibility. These registers are always accessable as an index/data register set at port addresses 3D6-3D7h. None of the unused bits in the regular VGA registers are used for extensions.

Panel Interface Registers

The Flat Panel Interface characteristics are controlled by a subset of the Extension Registers. These Registers select the panel type, data formatting, panel configuration, panel size, clock selection and video polarity. Since the 65520 / 530 is designed to support a wide range of panel types and sizes, the control of these features is fully programmable. The video polarity of text and graphics modes is independently selectable to allow black text on a white background and still provide normal graphics images.

Alternate Panel Timing Registers

Flat panel displays usually require sync signal timing that is different from a CRT. To provide full compatibility with the IBM VGA standard, alternate timing registers are used to allow independent timing of the sync signals for flat panel displays. Unlike the values programmed into the standard CRT timing registers, the value programmed into the alternate timing registers is dependent on the panel type used and is independent of the display mode.

Context Switching

For support of multi-tasking, windowing, and context switching, the entire state of the 65520 / 530 (internal registers) is readable and writable. This feature is fully compatible with IBM's VGA. Additional registers are provided to allow read back of internal latches not readable in the IBM VGA.

RESET, SETUP, AND TEST MODES

Reset Mode

When this mode is activated by pulling the RESET pin high, the 65520 / 530 is forced to VGA-compatible mode and the CRT is selected as the active display. In addition, the 65520 / 530 is disabled; it must be enabled after deactivating the RESET pin by writing to the Global Enable Register (102h in Setup Mode for PC and MC bus configurations) or to port 3C3h in PI bus or Local Bus configurations). Access to all Extension Registers is always enabled after reset (at 3D6/3D7h). The RESET pin must be active for at least 64 clock cycles.

Setup Mode

In this mode, only the Global Enable register is accessible. In PC bus configurations, setup mode is entered by writing a 1 to bit-4 of port 46E8h. This port is incorporated in the 65520 / 530. While in Setup mode, the video output is active if it was active prior to entering Setup mode and inactive if it was inactive prior to entering Setup mode. In MC bus configurations, setup mode may be entered by activating the 65520 / 530 SETUP/ pin (typically connected to signals driven by bits in port 94h in MC bus systems). After power up, video BIOS can optionally disable the video 46E8 or 3C3 registers (via XR70) for compatibility in case other non-IBM-compatible peripheral devices use those ports.

Tri-State Mode

In this mode, all output pins of the 65520 / 530 chip may be disabled for testing of circuitry external to the chip. The 65520 / 530 will enter Tri-State mode if it sees a rising edge on CLK0 during RESET with two of the display memory data pins pulled low (MAD0 and MBD0). The 65520 / 530 will exit Tri-State mode with either of the two enabling memory data pins high or RESET low.

ICT (In-Circuit Test) Mode

In this mode, all pins of the 65520 / 530 chip may be tested individually to determine if they are properly connected. The 65520 / 530 will enter ICT mode if it sees a rising edge on CLK0 during RESET with two of the display memory data pins pulled low (a different two pins from those used to enable Tri-state mode: MAD1 and MBD1). In ICT mode, all digital signal pins become inputs which are part of a long path starting at FLM (pin 72) and proceeding to lower pin numbers around the chip to pin 1 then to pin 160 and ending at VSYNC (pin 73). If all pins in the path are high, the VSYNC output will be high. If any pin is low, the VSYNC output will be low. Thus the chip can be checked in circuit to determine if all pins are connected properly by toggling all pins one at a time (CLK0 last) and observing the effect on VSYNC. CLK0 must be toggled last because rising edges on CLK0 with either of the enabling memory data pins high or RESET low will exit ICT mode. As a side effect, ICT mode effectively Tri-states all pins except VSYNC.

Mode of Operation	RESET Pin	STNDBY/ Pin	PNLOFF/ Pin	Display Memory Access	Video Output
Reset	High	xxx	xxx	-----	-----
Setup	-----	-----	-----	No	Yes
Test	-----	-----	-----	No	Yes

Note: Combinations of pin levels not shown in the table above are illegal and should not be used.

CHIP ARCHITECTURE

The 65520 / 530 integrates five major internal modules:

Sequencer

The Sequencer generates all CPU and display memory timing. It controls CPU access of display memory by inserting cycles dedicated to CPU access. It also contains mask registers which can prevent writes to individual display memory planes.

CRT Controller

The CRT Controller generates all the sync and timing signals for the display and also generates the multiplexed row and column addresses used for both display refresh and CPU access of display memory.

Graphics Controller

The Graphics Controller interfaces the 8 or 16-bit CPU data bus to the 32-bit internal data bus used by the four planes (Maps) of display memory. It also latches and supplies display memory data to the Attribute Controller for use in refreshing the screen image. For text modes this data is supplied in parallel form (character generator data and attribute code); for graphics modes it is converted to serial form (one bit from each of four bytes form a single pixel). The Graphics Controller can also perform any one of several types of logical operations on data while reading it from or writing it to display memory or the CPU data bus.

Attribute Controller

The Attribute Controller generates the 4-bit-wide video data stream used to refresh the display. This is created in text modes from a font pattern and an attribute code which pass through a parallel to serial conversion. In graphics modes, the display memory contains the 4-bit pixel data. In text and 16 color graphic modes the 4-bit pixel data acts as an index into a set of 16 internal color look-up registers which generate a 6-bit color value. Two additional bits of color data are added to provide an 8-bit address to the VGA color palette. In 256-color modes, two 4-bit values may be passed through the color look-up registers and assembled into one 8-bit video data value. In high-resolution 256-color modes, an 8-bit video data value may be provided directly, bypassing the attribute controller color lookup registers. Text and cursor blink, underline and horizontal scrolling are also the responsibility of the Attribute Controller.

VGA Color Palette/DAC

The 65520 / 530 contains an industry standard VGA-compatible RAMDAC on-chip for support of analog-output CRT displays. An external Palette DAC such as the Brooktree BT473 or Sierra SC1148x HiColor DACs would not normally be required, but is supported by the 65520 / 530 in case enhanced features are desired which are not provided by the internal RAMDAC. If an external RAMDAC is used, CPU access to the device is controlled by the 65520 / 530, which decodes CPU accesses and generates the PALRD/ and PALWR/ signals to the RAMDAC. I/O addresses 3C6-3C9h are valid external palette addresses, but the 65520 / 530 may be configured to additionally decode 83C6-83C9 port addresses for Brooktree RAMDAC extension registers (system bus address bit A15 is connected to the RAMDAC RS2 input).

The on-board VGA color palette contains a pixel mask register, 256x18 color lookup table, and triple 6-bit DACs for driving analog CRTs directly. The 'LM339' comparator function is implemented internally to generate the SENSE signal (the chip may be programmed to select either the internal comparator or a SENSE input pin if using an external RAMDAC). The analog reference for the internal DACs is also implemented on-chip.

The internal VGA color look-up table is always used in CRT modes and can be optionally used in flat panel modes, even if an external RAMDAC is used (the internal palette tracks CPU palette writes to match its contents to the external palette). An external palette would only be required for driving analog CRTs, it would not be needed for digital CRTs and flat panels.

65,536 and 32,768 Color Support

Each RAMDAC analog output provides 6-bit resolution (64 shades of color on each of the analog R, G, and B outputs). The internal RAMDAC supports generation of 15 bit/pixel (5R + 5G + 5B + 1 unused) and 16 bit/pixel (5R + 6G + 5B) graphics output to analog CRT displays. 15bpp (also called '555' mode) is compatible with Sierra RAMDACs and 16 bpp (also called '565' mode) is compatible with XGA high-color standards.

CONFIGURATION SWITCHES

The 65520 / 530 can read up to eight configuration bits. These signals are sampled on memory address bus bits AA0–AA7 on the falling edge of RESET. The state of AA0 and AA1 on RESET determine EISA/ISA bus (default), MC bus, PI bus, or 386 SX CPU interface. AA2 determines the pixel clock source as either clock chip (default) or external discrete oscillators. AA3 determines whether memory timing comes from 50.350 MHz (default) or 56.644 MHz. AA4-7 and BA0-7 are currently reserved for future use. All eight bits are latched into an extension register on RESET so software may determine the hardware configuration. Also, the reserved bits may optionally be used to read external switches or status bits (such as monitor sense bits MS0-2 from the VGA Analog Video connector).

Address lines AA0-7 for the corresponding bits should be externally connected to 4.7K pulldown (or driven to the desired 0 or 1 level while RESET is high) in order to be clear on the falling edge of RESET. The 65520 / 530 implements pullup resistors on these inputs.

VIRTUAL SWITCH REGISTER

The 65520 / 530 implements a 'virtual switch register'. In 'EGA' mode, the sense bit of the Feature control register (3C2 bit 4) may be set up to read a selected bit from the 'virtual switch register' (an extension register set up by BIOS at initialization time) instead of reading the state of the SENSE pin (or internal comparator output). This reduces overall video subsystem chip count by eliminating the external multiplexers otherwise required on the sense pin to implement TTL monitor support.

CLOCK SELECTION

The 65520 / 530 provide separate inputs for dot clock selections 0, 1, 2, and 3 (called CLK0, CLK1, CLK2, and CLK3) which are normally selected by Misc Output Register bits 2 and 3. By default, CLK0 and CLK1 are inputs which must be connected to 50.350 MHz and 28.322 MHz for implementation of standard VGA resolutions. The CLK0 input provides the memory clock (the CLK0 input is internally divided by two in the 65520 / 530 for the required 25.175 MHz dotclock). Alternately a 56.644 MHz memory clock can be provided on the CLK1 pin, with 50.35 MHz on CLK0 (both are internally divided by two). 50.35 MHz memory clock is used with 100ns DRAMs. 56.644 MHz memory clock is used with 80ns DRAMs. If desired, extended capabilities may be implemented, such as 800x600 sixteen-color graphics mode and 132-column text mode, by connecting a 40.000 MHz oscillator to CLK2. Interlaced 1024x768 sixteen-color mode can be implemented by connecting 44.9 MHz to the CLK3 input. The 65520 / 530 internally selects between these inputs so no additional circuitry is required.

Alternately, the CLK2 and CLK3 pins may be selected as outputs to provide Misc Output Register bits 2 and 3 externally to the chip. This allows clock selection to be implemented externally with 50.350 MHz on CLK0 or 56.644 MHz on CLK1. Either CLK0 or CLK1 may be selected as the memory clock (using the configuration option); the 65520 / 530 divides the clock by 2 as required to get the proper dot clock frequency. This allows an external clock synthesizer chip to be used which also allows additional user-defined frequencies to be selected.

The 82C404 Programmable Clock Synthesizer was designed to be tightly coupled to the 65520 / 530 controller and provide all the requisite clock frequencies. Refer to the application schematic examples to see an interface schematic detailing the 82C404 interface to the 65520 / 530.

LIGHT PEN REGISTERS

In the CGA and Hercules modes, the contents of the Display Address counter are saved at the end of the frame before being reset. The saved value can be read in the CRT Controller Register space at indices 10h and 11h. This allows simulation of a light pen hit in CGA and Hercules modes.

BIOS ROM INTERFACE

In typical ISA bus applications, the 65520 / 530 is placed on the motherboard and the video BIOS is integrated with the system BIOS (in local bus, Micro Channel, and PI-bus-based systems, the video BIOS is always included in the system BIOS). A separate signal (ROMCS/) may be created external to the 65520 / 530 for implementing a separate external ROM BIOS.

Typically, an 8-bit BIOS is implemented with one external ROM chip. A 16-bit dedicated video BIOS ROM could be implemented with the 65520 / 530 if required using two BIOS ROM chips, an external PAL, and a 74LS244 buffer. However, a higher-performance and lower-cost video system will result from implementation of the video BIOS as either an 8-bit dedicated video BIOS ROM or as

part of the system BIOS and having the video BIOS be copied into system RAM by the system BIOS on startup.

Chips and Technologies, Inc. supplies a video BIOS that is optimized for the 65520 / 530 hardware. The BIOS supports the extended functions of the 65520 / 530, such as switching between the flat panel and the CRT, SMARTMAP™, Vertical Compensation, and palette load/save. The BIOS Modification Program (BMP) enables OEMs to tailor their feature set by programming the extended functions. CHIPS offers the BIOS as a standard production version, a customized version, or as source code.

FLEXIBLE ARCHITECTURE

The 65520/530's flexible architecture enables OEMs to differentiate their products with enhanced features. OEMs can design one VGA sub-system and implement a wide range of features by selecting the controller (i.e., the 65520 or the 65530), the video display memory configuration, and the panel type and resolution. A single VGA sub-system design can provide:

- Monochrome and color TFT LCD panels (use the 65520)
- Monochrome and color TFT/STN LCD panels (use the pin-compatible 65530)
- Lowest cost: use two 256Kx4 DRAMs (256 Kbytes) for a minimum VGA subsystem
- Simultaneous LCD/CRT Display (use an optional 64Kx4 VRAM as a frame buffer)
- Lowest power consumption: use two 256Kx4 VRAMs plus 64Kx4 VRAM frame buffer / accelerator
- Higher Performance:

  2 VRAMs (separate serial and parallel data ports increase performance over 2 DRAMs)

  4 DRAMs (16-bit display memory data path increases performance relative to the 8-bit display memory data path of 2 DRAM implementations)

  4 VRAMs (achieves both of the above advantages: separate 16-bit serial and 16-bit parallel display memory data paths results in the highest performance in the industry)

- 512 KBytes of Video Memory

  (implemented via four 256Kx4 DRAMs, four 256Kx4 VRAMs, or two 512Kx8 DRAMs) Supports high-resolution flat panels (e.g., 1024x768)

  Supports high-resolution 256-color modes (640x480 on panels or CRTs and interlaced 1024x768 on CRTs only)

The use of one VGA subsystem speeds product development and facilitates manufacturing, since only one design needs to be laid out and debugged, only one VGA BIOS needs to be customized, and only a minimum number of components need to be qualified and stocked.

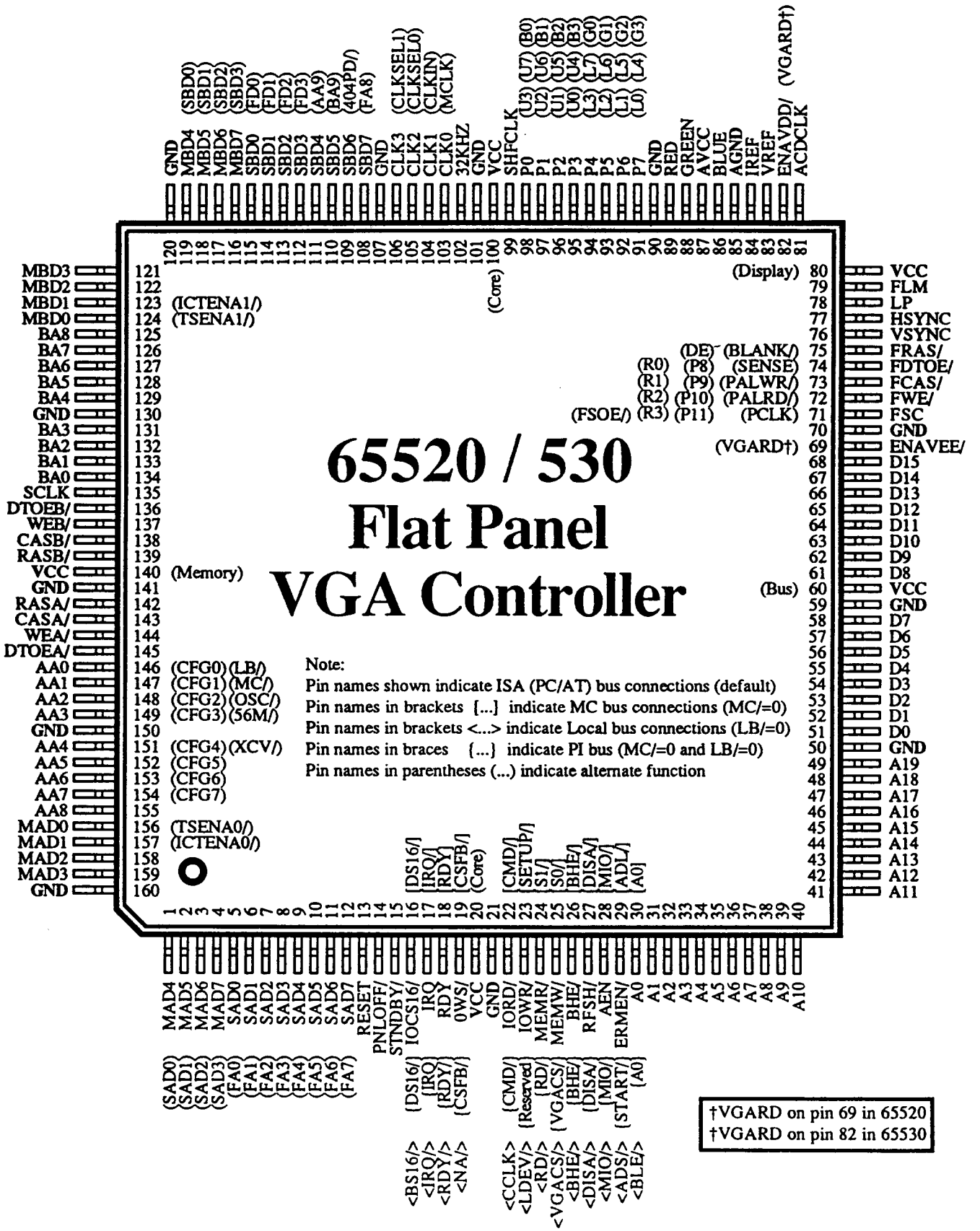
PACKAGE

The 65520 and 65530 are available in pin-compatible 160-pin plastic flat packs (PFPs).

APPLICATION SCHEMATIC EXAMPLES

Included in this document are application schematic examples of the following:

1. Bus Interface - 16-bit EISA/ISA Bus
   Bus Interface - 16-bit EISA/ISA Bus w/ Xcvrs
   Bus Interface - 8-bit PC/Chip (F8680)
   Bus Interface - 16-bit 386 SL PI Bus
   Bus Interface - 16-bit MC Bus
   Bus Interface - 16-bit 386 SX/DX Local Bus
2. Memory Interface - 2 / 4 256Kx4 DRAMs
   Memory Interface - 2 256Kx4 VRAMs
   Memory Interface - 4 256Kx4 VRAMs
   Memory Interface - 2 256Kx8 VRAMs
   Memory Interface - 2 128Kx8 PSRAMs
   Memory Interface - 2 512Kx8 DRAMs
3. Video Interface - 8/9/12/16-bit Panel Data
4. Clock Interface - 82C404 Clock Chip


65520 / 530
Flat Panel
VGA Controller
Note:
Pin names shown indicate ISA (PC/AT) bus connections (default)
Pin names in brackets [...] indicate MC bus connections (MC/=0)
Pin names in brackets <...> indicate Local bus connections (LB/=0)
Pin names in braces {...} indicate PI bus (MC/=0 and LB/=0)
Pin names in parentheses (...) indicate alternate function
(Core)
(Display)
(Memory)
(Bus)
†VGARD on pin 69 in 65520
†VGARD on pin 82 in 65530

Pin Name			Pin #	Dir	Drive
0WS/	[CSFB/]	{CSFB/}	19	Out	8mA
32KHZ			102	In	--
A0	<BLE/>		30	In	--
A1			31	In	--
A2			32	In	--
A3			33	In	--
A4			34	In	--
A5			35	In	--
A6			36	In	--
A7			37	In	--
A8			38	In	--
A9			39	In	--
A10			40	In	--
A11			41	In	--
A12			42	In	--
A13			43	In	--
A14			44	In	--
A15			45	In	--
A16			46	In	--
A17			47	In	--
A18			48	In	--
A19			49	In	--
AA0	(CFG0)	(LB/)	146	I/O	2mA
AA1	(CFG1)	(MC/)	147	I/O	2mA
AA2	(CFG2)	(OSC/)	148	I/O	2mA
AA3	(CFG3)	(56M/)	149	I/O	2mA
AA4	(CFG4)	(XCV/)	151	I/O	2mA
AA5	(CFG5)		152	I/O	2mA
AA6	(CFG6)		153	I/O	2mA
AA7	(CFG7)		154	I/O	2mA
AA8			155	I/O	2mA
ACDCLK			81	Out	2mA
AEN	[MIO/]	{MIO/}	28	In	--
AGND			85	--	--
AVCC			87	--	--
BLUE			86	Out	--
BA0			134	I/O	2mA
BA1			133	I/O	2mA
BA2			132	I/O	2mA
BA3			131	I/O	2mA
BA4			129	I/O	2mA
BA5			128	I/O	2mA
BA6			127	I/O	2mA
BA7			126	I/O	2mA
BA8			125	I/O	2mA
BHE/	[BHE/]	{BHE/}	26	In	--
CASA/			143	Out	4mA
CASB/			138	Out	4mA
CLK0	(MCLK)		103	In	--
CLK1	(CLKIN)		104	In	--
CLK2	(CLKSEL0)		105	I/O	2mA
CLK3	(CLKSEL1)		106	I/O	2mA
D0			51	I/O	4mA
D1			52	I/O	4mA
D2			53	I/O	4mA
D3			54	I/O	4mA
D4			55	I/O	4mA
D5			56	I/O	4mA
D6			57	I/O	4mA
D7			58	I/O	4mA
D8			61	I/O	4mA
D9			62	I/O	4mA
D10			63	I/O	4mA
D11			64	I/O	4mA
D12			65	I/O	4mA
D13			66	I/O	4mA
D14			67	I/O	4mA
D15			68	I/O	4mA
DTOEA/			145	Out	2mA

Pin Name			Pin #	Dir	Drive
DTOEB/			136	Out	2mA
ENAVDD/ (VGARD) (530)			82	Out	2mA
ENAVEE/ (VGARD) (520)			69	Out	2mA
ERMEN/	[ADL/]	{START/}	29	In	--
FCAS/	(P9)(R1)	(PALWR/)	73	Out	2mA
FDTOE/	(P8)(R0)	(SENSE)	74	I/O	2mA
FLM			79	Out	2mA
FRAS/	(DE)	(BLANK/)	75	Out	2mA
FSOE/-FSC(P11)(R3)(PCLK)			71	Out	4mA
FWE/	(P10)(R2)	(PALRD/)	72	Out	2mA
GREEN			88	Out	--
GND			21	--	--
GND			50	--	--
GND			59	--	--
GND			70	--	--
GND			90	--	--
GND			101	--	--
GND			107	--	--
GND			120	--	--
GND			130	--	--
GND			141	--	--
GND			150	--	--
GND			160	--	--
HSYNC			77	Out	8mA
IOCS16/	[DS16/]	{DS16/}	16	Out	8mA
IORD/	[CMD/]	{CMD/}	22	In	--
IOWR/	[SETUP/]		23	In	--
IREF			84	In	--
IRQ	[IRQ/]	{IRQ}	17	Out	8mA
LP			78	Out	2mA
MAD0	(TSENA0/)		156	I/O	2mA
MAD1	(ICTENA0/)		157	I/O	2mA
MAD2			158	I/O	2mA
MAD3			159	I/O	2mA
MAD4	(SAD0)		1	I/O	2mA
MAD5	(SAD1)		2	I/O	2mA
MAD6	(SAD2)		3	I/O	2mA
MAD7	(SAD3)		4	I/O	2mA
MBD0	(TSENA1/)		124	I/O	2mA
MBD1	(ICTENA1/)		123	I/O	2mA
MBD2			122	I/O	2mA
MBD3			121	I/O	2mA
MBD4	(SBD0)		119	I/O	2mA
MBD5	(SBD1)		118	I/O	2mA
MBD6	(SBD2)		117	I/O	2mA
MBD7	(SBD3)		116	I/O	2mA
MEMR/	[S1/]	{RD/}	24	In	--
MEMW/	[S0/]		25	In	--
P0	(U3) (U7)	(B0)	98	Out	4mA
P1	(U2) (U6)	(B1)	97	Out	4mA
P2	(U1) (U5)	(B2)	96	Out	4mA
P3	(U0) (U4)	(B3)	95	Out	4mA
P4	(L3) (L7)	(G0)	94	Out	4mA
P5	(L2) (L6)	(G1)	93	Out	4mA
P6	(L1) (L5)	(G2)	92	Out	4mA
P7	(L0) (L4)	(G3)	91	Out	4mA
PNLOFF/			14	In	--
RED			89	Out	--
RASA/			142	Out	4mA
RASB/			139	Out	4mA
RDY	[RDY]	{RDY/}	18	Out	8mA
RESET			13	In	--
RFSH/	[DISA/]	{DISA/}	27	In	--
SAD0	(FA0)		5	I/O	2mA
SAD1	(FA1)		6	I/O	2mA
SAD2	(FA2)		7	I/O	2mA
SAD3	(FA3)		8	I/O	2mA
SAD4	(FA4)		9	I/O	2mA
SAD5	(FA5)		10	I/O	2mA

Pin Name			Pin #	Dir	Drive
SAD6	(FA6)		11	I/O	2mA
SAD7	(FA7)		12	I/O	2mA
SBD0	(FD0)		115	I/O	2mA
SBD1	(FD1)		114	I/O	2mA
SBD2	(FD2)		113	I/O	2mA
SBD3	(FD3)		112	I/O	2mA
SBD4	(AA9)		111	I/O	2mA
SBD5	(BA9)		110	I/O	2mA
SBD6	(404PD/)		109	I/O	2mA
SBD7	(FA8)		108	I/O	2mA
SCLK			135	Out	2mA
SHFCLK			99	Out	4mA
STNDBY/			15	In	--
VCC			20	--	--
VCC			60	--	--
VCC			80	--	--
VCC			100	--	--
VCC			140	--	--
VREF			83	In	--
VSYNC			76	Out	8mA
WEA/			144	Out	2mA
WEB/			137	Out	2mA

(404PD/)	See SBD6
(56M/)	See AA3
(AA9)	See SBD4
(B0-3)	See P0-3
(BA9)	See SBD5
(BLANK/)	See FRAS/
(CFG0-7)	See AA0-7
(CLKIN)	See CLK1
(CLKSEL0)	See CLK2
(CLKSEL1)	See CLK3
(DE)	See FRAS/
(FA0-7)	See SAD0-7
(FA8)	See SBD7
(FD0-3)	See SBD0-3
(G0-3)	See P4-7
(ICTENA0/)	See MAD1
(ICTENA1/)	See MBD1
(L0-7)	See P7-4
(LB/)	See AA0
(MCLK)	See CLK0
(MC/)	See AA1
(OSC/)	See AA2
(P8)	See FDTOE/
(P9)	See FCAS/
(P10)	See FWE/
(P11)	See FSOE/-FSC
(PALRD/)	See FWE/
(PALWR/)	See FCAS/
(PCLK)	See FSOE/-FSC
(R0-3)	See (P8-11)
(SAD0-3)	See MAD4-7
(SBD0-3)	See MBD4-7
(SENSE)	See FDTOE/
(TSENA0/)	See MAD0
(TSENA1/)	See MBD0
(U0-7)	See P3-0
(VGARD)	See ENAVxx/
(XCV/)	See AA4
[ADL/] {START/} <ADS/>	See ERMEN/
[BHE/] {BHE/} <BHE/>	See BHE/
[CMD/] {CMD/} <CCLK>	See IORD/
[CSFB/] {CSFB/} <NA/>	See 0WS/
[DISA/] {DISA/} <DISA/>	See RFSH/
[DS16/] {DS16/} <DISA/>	See IOCS16/
[IRQ/] {IRQ} <IRQ/>	See IRQ
[MIO/] {MIO/} <MIO/>	See AEN
[RDY] {RDY/} <RDY/>	See RDY
[S0/] {VGACS/} <VGACS/>	See MEMW/
[S1/] {RD/} <RD/>	See MEMR/
[SETUP/] <LDEV/>	See IOWR/

PIN DESCRIPTIONS

System Bus Interface

Pin #	Pin Name		Type	Active	Description
51	D0		I/O	High	System Data Bus
52	D1		I/O	High	
53	D2		I/O	High	
54	D3		I/O	High	
55	D4		I/O	High	
56	D5		I/O	High	
57	D6		I/O	High	
58	D7		I/O	High	
61	D8		I/O	High	
62	D9		I/O	High	
63	D10		I/O	High	
64	D11		I/O	High	
65	D12		I/O	High	
66	D13		I/O	High	
67	D14		I/O	High	
68	D15		I/O	High	
30	A0	<BLE/>	In	High	System Address Bus
31	A1		In	High	
32	A2		In	High	A0 is connected to BLE/ (Byte Low Enable) in 386 SX
33	A3		In	High	local bus interfaces or to BE0/ in 386 DX local bus
34	A4		In	High	interfaces.
35	A5		In	High	
36	A6		In	High	
37	A7		In	High	
38	A8		In	High	
39	A9		In	High	
40	A10		In	High	
41	A11		In	High	
42	A12		In	High	
43	A13		In	High	
44	A14		In	High	
45	A15		In	High	
46	A16		In	High	
47	A17		In	High	
48	A18		In	High	
49	A19		In	High	

Note: Pin names in parentheses (...) indicate alternate functions
Pin names in brackets [...] indicate MC bus functionality if different from EISA/ISA (PC/AT) bus
Pin names in brackets <...> indicate Local Bus functionality if different from EISA/ISA (PC/AT) bus
Pin names in braces {...} indicate PI bus functionality if different from EISA/ISA (PC/AT) bus

PIN DESCRIPTIONS

System Bus Interface (continued)

Pin #	Pin Name	Type	Active	Description
13	RESET	In	High	Reset. Connect directly to the bus reset signal. For local bus, this input is used to synchronize the clock.
27	RFSH/ [DISA/] {DISA/} <DISA/>	In In In	Low Low Low	This pin is an active low signal indicating a Refresh cycle for the EISA/ISA bus. In MC, PI, and local bus systems, it is connected to the disable signal from system port 102h (or tied high). When this pin is low, display memory is not accessible.
26	BHE/ [BHE/] {BHE/} <BHE/ or BE1/>	In In In	Low Low Low	Byte High Enable. BHE/ low indicates the high order byte at the current word address is being accessed. Connected to BE1/ in 386 DX local bus interfaces.
28	AEN [MIO/] {MIO/} <MIO/>	In In In	Both Both Both	In EISA/ISA interface, defines valid I/O address: 0 = valid I/O address, 1 = Invalid I/O address (latched internally). In MC, PI, and local bus interfaces, indicates memory or I/O cycle: 1 = memory, 0 = I/O.
29	ERMEN/ [ADL/] {START/} <ADS/>	Out In In In	Low Low Low Low	Start input (PI bus), Address Latch input (MC Bus), Address Strobe input (local bus), or Early Memory R/W Indicator output (EISA/ISA Bus). Indicates the start of a bus cycle in MC, PI, and local bus interfaces. In ISA/EISA bus interfaces, when the CPU executes a memory read or write cycle in text mode, this pin is an output which goes low two MCLK cycles prior to the fall of display memory RAS/ and stays active until RAS/ is asserted. It is driven high in graphics mode and during all display refresh accesses.
24	MEMR/ [S1/] {RD/} <RD/>	In In In	Low Low Low	In the EISA/ISA bus, indicates a Memory Read cycle. In MC interface, indicates Status 1. In the PI and local bus, indicates read (low) or write (high) bus cycle.
25	MEMW/ [S0/] {VGACS/} <VGACS/>	In In In	Low Low Low	In the EISA/ISA bus, indicates a Memory Write cycle. In the MC bus, indicates Status 0. In PI and local bus it's used to select the VGA memory space. This input should be grounded in 65520 PI bus designs for compatibility with the 65530 (the 65520 always decodes the A0000-BFFFFh VGA address space on chip; the 65530 has a linear addressing feature which optionally allows this input to select display memory at other addresses).

S1/	S0/	Operation
0	0	Undefined
0	1	Read
1	0	Write
1	1	Undefined

Note: Pin names in parentheses (...) indicate alternate functions
Pin names in brackets [...] indicate MC bus functionality if different from EISA/ISA (PC/AT) bus
Pin names in brackets <...> indicate Local Bus functionality if different from EISA/ISA (PC/AT) bus
Pin names in braces {...} indicate PI bus functionality if different from EISA/ISA (PC/AT) bus

PIN DESCRIPTIONS

System Bus Interface (continued)

Pin #	Pin Name	Type	Active	Description
22	IORD/ [CMD/] {CMD/} <CCLK>	In In In	Low Low High	In EISA/ISA bus interfaces, indicates an I/O Read Cycle. In MC and PI bus interfaces, indicates the beginning of a command part of a bus cycle (driven off CMD/ on the MC bus, VGACMD/ on CHIPS/250). In local bus interfaces, connects to the 2X CPU clock (the local bus interface is synchronous to rising edges).
23	IOWR/ [SETUP/] {Reserved} <LDEV/>	In In Out	Low Low Low	In EISA/ISA bus interfaces, this pin is an input used to initiate an I/O Write Cycle. In MC bus systems, it is an input used to disable all on-chip memory and I/O functions. In PI bus systems, this pin is an input which should be tied high. In local bus interfaces, this pin is an open drain output which, when active, indicates the decode of a local bus display memory address.
18	RDY [RDY] {RDY/} <RDY/>	Out Out Out	High Low Low	Ready. Driven low during EISA/ISA and MC bus cycles to indicate that the current cycle should be extended with wait states. Driven low during PI bus and local bus cycles to indicate the current cycle should be completed. This signal is driven high at the end of the cycle, then tristated.
19	0WS/ [CSFB/] {CSFB/} <NA/>	Out Out Out	Low Low Low	Zero Wait State (EISA/ISA bus) or Card Select Feedback (MC, PI, and local bus). In PI bus systems, this pin is typically not required and may be left open. In local bus systems, this pin is used to drive the CPU NA/ input to allow pipeline mode.
16	IOCS16/ [DS16/] {DS16/} <BS16/>	Out Out Out	Low Low Low	I/O Select 16 (EISA/ISA bus) or Device Select 16 (MC and PI bus) or Bus Size 16 (Local Bus). In PI bus and 386SX local bus interfaces, this pin may not be required and, if not, may be left open.
17	IRQ [IRQ/] {IRQ} <IRQ/>	Out Out Out Out	High Low High Low	Frame Interrupt Output. Interrupt polarity is programmable. Set when interrupt on VSYNC is enabled. Cleared by reprogramming register 11h in the CRT Controller. (EISA/ISA and PI bus interrupts are active high, MC and local bus interrupts are active low). See also XR14 bit–7.

Note: Pin names in parentheses (...) indicate alternate functions
Pin names in brackets [...] indicate MC bus functionality if different from EISA/ISA (PC/AT) bus
Pin names in brackets <...> indicate Local Bus functionality if different from EISA/ISA (PC/AT) bus
Pin names in braces {...} indicate PI bus functionality if different from EISA/ISA (PC/AT) bus

PIN DESCRIPTIONS

Display Memory Interface

Pin #	Pin Name			Type	Active	Description
146	AA0	(LB/)	(CFG0)	Out	High	DRAM address bus for planes 0-1
147	AA1	(MC/)	(CFG1)	Out	High	
148	AA2	(OSC/)	(CFG2)	Out	High	
149	AA3	(56M/)	(CFG3)	Out	High	
151	AA4	(XCV/)	(CFG4)	Out	High	
152	AA5		(CFG5)	Out	High	
153	AA6		(CFG6)	Out	High	
154	AA7		(CFG7)	Out	High	
155	AA8			Out	High	
134	BA0			Out	High	DRAM address bus for planes 2-3
133	BA1			Out	High	
132	BA2			Out	High	
131	BA3			Out	High	
129	BA4			Out	High	
128	BA5			Out	High	
127	BA6			Out	High	
126	BA7			Out	High	
125	BA8			Out	High	
142	RASA/			Out	Low	Row address strobe for memory planes 0-1
139	RASB/			Out	Low	Row address strobe for memory planes 2-3
143	CASA/			Out	Low	Column address strobe for planes 0-1
138	CASB/			Out	Low	Column address strobe for planes 2-3
144	WEA/			Out	Low	Write enable for memory planes 0-1
137	WEB/			Out	Low	Write enable for memory planes 2-3
135	SCLK			Out	High	VRAM shift clock
145	DTOEA/			Out	Low	VRAM data transfer output enable for planes 0-1
136	DTOEB/			Out	Low	VRAM data transfer output enable for planes 2-3

Note: Pin names in parentheses (...) indicate alternate functions

PIN DESCRIPTIONS

Display Memory Interface (continued)

Pin #	Pin Name		Type	Active	Description
156	MAD0	(TSENA0/)	I/O	High	Display memory data bus for planes 0 and 1
157	MAD1	(ICTENA0/)	I/O	High	
158	MAD2		I/O	High	All modes: 0-3 = parallel data
159	MAD3		I/O	High	2-DRAM mode: 4-7 = not connected
1	MAD4	(SAD0)	I/O	High	2-VRAM mode: 4-7 = serial data
2	MAD5	(SAD1)	I/O	High	4-RAM mode: 4-7 = parallel data
3	MAD6	(SAD2)	I/O	High	
4	MAD7	(SAD3)	I/O	High	
5	SAD0	(FA0)	I/O	High	4-VRAM mode: Serial data for planes 0-1
6	SAD1	(FA1)	I/O	High	All other modes: Frame buffer address
7	SAD2	(FA2)	I/O	High	
8	SAD3	(FA3)	I/O	High	
9	SAD4	(FA4)	I/O	High	
10	SAD5	(FA5)	I/O	High	
11	SAD6	(FA6)	I/O	High	
12	SAD7	(FA7)	I/O	High	
124	MBD0	(TSENA1/)	I/O	High	Display memory data bus for planes 2 and 3
123	MBD1	(ICTENA1/)	I/O	High	
122	MBD2		I/O	High	All modes: 0-3 = parallel data
121	MBD3		I/O	High	2-DRAM mode: 4-7 = not connected
119	MBD4	(SBD0)	I/O	High	2-VRAM mode: 4-7 = serial data
118	MBD5	(SBD1)	I/O	High	4-RAM mode: 4-7 = parallel data
117	MBD6	(SBD2)	I/O	High	
116	MBD7	(SBD3)	I/O	High	
115	SBD0	(FD0)	I/O	High	4-VRAM mode: Serial data for planes 2-3
114	SBD1	(FD1)	I/O	High	All other modes: Frame buffer address
113	SBD2	(FD2)	I/O	High	
112	SBD3	(FD3)	I/O	High	
111	SBD4	(AA9)	I/O	High	
110	SBD5	(BA9)	I/O	High	
109	SBD6	(404PD/) (530)	I/O	High	404PD/ is the powerdown input to the 82C404, to be
108	SBD7	(FA8)	I/O	High	connected to the 82C404 PWRDN/ pin (65530 only)

If ICTENA0/ and ICTENA1/ are low with RESET high, a rising edge on CLK0 will put the chip into 'In Circuit Test' mode. In ICT mode, all digital signal pins become inputs which are part of a long path starting at FLM (pin 72) and proceeding to lower pin numbers around the chip to pin 1 then to pin 160 and ending at VSYNC (pin 73). If all pins in the path are high, the VSYNC output will be high. If any pin is low, the VSYNC output will be low. Thus the chip can be checked in circuit to determine if all pins are connected properly by toggling all pins one at a time (CLK0 last) and observing the effect on VSYNC. CLK0 must be toggled last because rising edges on CLK0 with ICTENA0/ or 1/ high or RESET low will exit ICT mode. As a side effect, ICT mode effectively 3-states all pins except VSYNC.

If TSENA0/ and TSENA1/ are low with RESET high, a rising edge on CLK0 will 3-state all pins. A CLK0 rising edge without the enabling conditions exits 3-state.

Note: Pin names in parentheses (...) indicate alternate functions

PIN DESCRIPTIONS

Frame Buffer and CRT Video Interface

Pin #	Pin Name			Type	Active	Description
71	FSC (FSOE/)	(P11)	(PCLK)	Out	High	Frame Buffer Shift Clock / Serial Output Enable (connected to both SC and SOE/ pins of the VRAM). When the frame buffer is disabled, this pin becomes a Pixel Clock for synchronizing CRT video data on P0-7. May also be programmed as P11 for color panels.
75	FRAS/	(DE)	(BLANK/)	Out	Both	Frame Buffer Row Address Strobe. When the frame buffer is disabled, this pin becomes a blanking signal for an external color palette chip (polarity is programmable: see XR28 bit-0). With the frame buffer disabled, this pin may also be redefined as a Display Enable signal (see XR28 bit-1).
73	FCAS/	(P9)	(PALWR/)	Out	Low	Frame Buffer Column Address Strobe. When the frame buffer is disabled, this pin becomes an I/O write strobe for an external color palette chip (82C411, IMSG176, BT471, or compatible). In this mode, it is asserted when the chip is enabled and an I/O Write occurs to addresses 3C6-3C9h. May also be programmed as P9 for color panels.
72	FWE/	(P10)	(PALRD/)	Out	Low	Frame Buffer Write Enable. When the frame buffer is disabled, this pin becomes an I/O read strobe for an external color palette chip (82C411, IMSG176, BT471, or compatible). In this mode, it is asserted when an I/O Read occurs from addresses 3C6h, 3C8h, or 3C9h. The chip responds directly for reads from 3C7h. May also be programmed as P10 for color panels.
74	FDTOE/	(P8)	(SENSE)	I/O	High	Frame Buffer Data Transfer / Output Enable (output). When the frame buffer is disabled, this pin becomes an input for reading monitor sense. Normally connected to the outputs of an LM339 comparator on the external color palette chip analog RGB outputs (or directly to the color palette chip if this function is built in such as in the BT475 or 82C411). With the frame buffer disabled, the state of this pin may read as bit-4 of Input Status Register 0 (port 3C2h). See also extension register XR1F (Virtual Switch Register). May also be programmed as P8 for color panels.
77	HSYNC			Out	Both	CRT Horizontal Sync (polarity is programmable)
76	VSYNC			Out	Both	CRT Vertical Sync (polarity is programmable)
89	RED			Out	High	CRT Analog Video Outputs from the internal color palette DAC.
88	GREEN			Out	High	
86	BLUE			Out	High	
84	IREF			In	n/a	Current and Voltage Reference pins for the internal color palette DAC.
83	VREF			In	n/a	

Note: Pin names in parentheses (...) indicate alternate functions

PIN DESCRIPTIONS

Flat Panel Interface

Pin #	Pin Name			Type	Active	Description
91	P7	(L0)	(L4)	Out	High	8-bit flat panel data output. Alternately, can be programmed to output CRT video data to bypass the internal RAMDAC (simultaneous display on CRT and flat panels is not possible in this configuration). (see also SENSE for P8 for 8-level VAM color panels) (see also SENSE, PALWR/, PALRD/, and PCLK for P8-11 for 16-level VAM color panels)
92	P6	(L1)	(L5)	Out	High	
93	P5	(L2)	(L6)	Out	High	
94	P4	(L3)	(L7)	Out	High	
95	P3	(U0)	(U4)	Out	High	
96	P2	(U1)	(U5)	Out	High	
97	P1	(U2)	(U6)	Out	High	
98	P0	(U3)	(U7)	Out	High	
79	FLM			Out	High	First Line Marker. Flat Panel equivalent of VSYNC.
78	LP			Out	High	Latch Pulse. Flat Panel equivalent of HSYNC.
99	SHFCLK			Out	High	Shift Clock. Pixel clock for flat panel data. In 16bit/pixel mode, the rising edge may be used externally to latch the 'upper' data byte and the following falling edge used to transfer the 'lower' byte (for panels with 16-bit data interface).
81	ACDCLK			Out	High	ACD Clock for flat panels (control signal for AC drive)
14	PNLOFF/			In	Low	Panel Off. Can be programmed (via XR52) to perform various power-down functions.
15	STNDBY/			In	Low	Standby. Power saving control to place the chip into power-saving mode.
82	ENAVDD/		(VGARD)	Out	Low	Power sequencing control for the panel driver electronics voltage V_{DD} (see note below)
69	ENAVEE/		(VGARD)	Out	High	Power sequencing control for the panel LCD bias voltage V_{EE} (see note below) Note: May also be configured (by connecting a 4.7K pulldown resistor to configuration bit-4, XCV/) to be a data transceiver direction control. If configured as VGARD (on pin 69 for the 65520 and pin 82 for the 65530), this pin is driven low during RESET (a low level output indicates data is being written to the chip, high indicates data is being read from the chip). The low bus data transceiver is enabled by A0 and the high bus transceiver is enabled by BHE/. In a typical laptop / notebook computer, the 65520 / 530 data bus drive is sufficient to drive the bus directly. Therefore, a transceiver direction control is typically not needed and this pin may be used for panel power sequencing control (or left unconnected).

Note: Pin names in parentheses (...) indicate alternate functions

PIN DESCRIPTIONS

Clock, Power, and Ground

Pin #	Pin Name		Type	Active	Description
103	CLK0	(MCLK)	In	High	If internal clock selection is enabled (default), CLK0, CLK1, CLK2, and CLK3 are inputs. One of the four is selected as the input dotclock per Misc Output Register (3C2h) bits 2 and 3. Memory clock may be selected from either CLK0 or CLK1 (see pin AD3 and configuration register XR01); if CLK0 is selected as MCLK, 50.35 MHz is used (CLK1 is 28.322); if CLK1 is selected as MCLK, 56.644 MHz is used (CLK0 is 25.175). If external clock selection is enabled (see pin AA2 and configuration register XR01), CLKIN becomes the input dotclock for all pixel clock frequencies and CLK2-3 become clock select outputs driven by Misc Output Register (3C2h) bits 2 and 3. In this mode, the CLK0 pin is always used for memory timing (MCLK).
104	CLK1	(MCLK/CLKIN)	In	High	
105	CLK2	(CLKSEL0)	I/O	High	
106	CLK3	(CLKSEL1)	I/O	High	
102	32KHZ		In	High	32.768 KHz. Used to perform CAS-Before-RAS (CBR) refresh cycles during power-down mode (see XR52 bit-6). Alternately, the chip can be programmed to perform refresh at various frequencies derived from MCLK (in this mode, the 32KHZ input is ignored).
20	VCC		VCC	--	Power (Internal Logic)
60	VCC		VCC	--	Power (Bus Interface)
80	VCC		VCC	--	Power (Display Interface)
100	VCC		VCC	--	Power (Internal Logic)
140	VCC		VCC	--	Power (Memory Interface)
21	GND		GND	--	Ground
50	GND		GND	--	
59	GND		GND	--	
70	GND		GND	--	
90	GND		GND	--	
101	GND		GND	--	
107	GND		GND	--	
120	GND		GND	--	
130	GND		GND	--	
141	GND		GND	--	
150	GND		GND	--	
160	GND		GND	--	
87	AVCC		VCC	--	Analog power and ground pins for noise isolation for internal RAMDAC.
85	AGND		GND	--	

VCC is specified as 5V or 3.3V

Note: Pin names in parentheses (...) indicate alternate functions

I/O Map

Port Address	Read	Write
102	Global Enable (ISA/MC)	Global Enable (ISA/MC)
3B0	Reserved for MDA/Hercules	Reserved for MDA/Hercules
3B1	Reserved for MDA/Hercules	Reserved for MDA/Hercules
3B2	Reserved for MDA/Hercules	Reserved for MDA/Hercules
3B3	Reserved for MDA/Hercules	Reserved for MDA/Hercules
3B4	CRTC Index	CRTC Index
3B5	CRTC Data	CRTC Data
3B6	Reserved for MDA/Hercules	Reserved for MDA/Hercules
3B7	Reserved for MDA/Hercules	Reserved for MDA/Hercules
3B8	Hercules Mode Register (MODE)	Hercules Mode Register (MODE)
3B9	--	Set Light Pen FF (ignored)
3BA	Status Register (STAT)	Feature Control Register (FCR)
3BB	--	Clear Light Pen FF (ignored)
3BC		
3BD	Reserved for system parallel port	
3BE		
3BF	Hercules Configuration Register (HCFG)	Hercules Configuration Register (HCFG)
3C0	Attribute Controller Index / Data	Attribute Controller Index / Data
3C1	Attribute Controller Index / Data	Attribute Controller Index / Data
3C2	Feature Read Register (FCR)	Miscellaneous Output Register (MSR)
3C3	Video Subsystem Enable (VSE)(MC/PI/LB)	Video Subsystem Enable (VSE)(MC/PI/LB)
3C4	Sequencer Index	Sequencer Index
3C5	Sequencer Data	Sequencer Data
3C6, 83C6	Color Palette Mask	Color Palette Mask
3C7, 83C7	Color Palette State	Color Palette Read Mode Index
3C8, 83C8	Color Palette Write Mode Index	Color Palette Write Mode Index
3C9, 83C9	Color Palette Data	Color Palette Data
3CA	Feature Read Register (FEAT)	--
3CB	--	--
3CC	Miscellaneous Output Register (MSR)	--
3CD	--	--
3CE	Graphics Controller Index	Graphics Controller Index
3CF	Graphics Controller Data	Graphics Controller Data
3D0	--	--
3D1	--	--
3D2	--	--
3D3	--	--
3D4	CRTC Index	CRTC Index
3D5	CRTC Data	CRTC Data
3D6	CHIPS™ Extensions Index	CHIPS™ Extensions Index
3D7	CHIPS™ Extensions Data	CHIPS™ Extensions Data
3D8	CGA Mode Register (MODE)	CGA Mode Register (MODE)
3D9	CGA Color Register (COLOR)	CGA Color Register (COLOR)
3DA	Status Register (STAT)	Feature Control Register (FCR)
3DB	--	Clear Light Pen FF (ignored)
3DC	--	Set Light Pen FF (ignored)
46E8	--	Setup Control (ISA bus only)

Mono Mode

Color Mode

REGISTER SUMMARY - CGA, MDA, AND HERCULES MODEs

Register	Register Name	Bits	Access	I/O Port - MDA/Herc	I/O Port - CGA	Comment
ST00 (STAT)	Display Status	7	R	3BA	3DA	
CLPEN	Clear Light Pen Flip Flop	0	W(n/a)	3BB (ignored)	3DB (ignored)	ref only: no light pen
SLPEN	Set Light Pen Flip Flop	0	W(n/a)	3B9 (ignored)	3DC (ignored)	ref only: no light pen
MODE	CGA/MDA/Hercules Mode Control	7	RW	3B8	3D8	
COLOR	CGA Color Select	6	RW	n/a	3D9	
HCFG	Hercules Configuration	2	W	3BF	n/a	
			R	3D6-3D7 index 14	n/a	XR14
RX, R0-11	'6845' Registers	0-8	RW	3B4-3B5	3D4-3D5	
XRX, XR0-7F	Extension Registers	0-8	RW	3D6-3D7	3D6-3D7	

REGISTER SUMMARY - EGA MODE

Register	Register Name	Bits	Access	I/O Port - Mono	I/O Port - Color	Comment
MSR	Miscellaneous Output	7	W	3C2	3C2	
FCR	Feature Control	3	W	3BA	3DA	
ST00 (FEAT)	Feature Read (Input Status 0)	4	R	3C2	3C2	
ST01 (STAT)	Display Status (Input Status 1)	7	R	3BA	3DA	
CLPEN	Clear Light Pen Flip Flop	0	W(n/a)	3BB (ignored)	3DB (ignored)	ref only: no light pen
SLPEN	Set Light Pen Flip Flop	0	W(n/a)	3B9 (ignored)	3DC (ignored)	ref only: no light pen
SRX, SR0-7	Sequencer	0-8	RW	3C4-3C5	3C4-3C5	
CRX, CR0-3F	CRT Controller	0-8	RW	3B4-3B5	3D4-3D5	
GRX, GR0-8	Graphics Controller	0-8	RW	3CE-3CF	3CE-3CF	
ARX, AR0-14	Attributes Controller	0-8	RW	3C0-3C1	3C0-3C1	
XRX, XR0-7F	Extension Registers	0-8	RW	3D6-3D7	3D6-3D7	

REGISTER SUMMARY - VGA MODE

Register	Register Name	Bits	Access	I/O Port - Mono	I/O Port - Color	Comment
VSE	Video Subsystem Enable	1	RW	3C3 if MC/PI/LB	3C3 if MC/PI/LB	Disabled by XR70 bit-6
SETUP	Setup Control	2	W	46E8 if ISA	46E8 if ISA	Disabled by XR70 bit-7
ENABLE	Global Enable	1	RW	102 if ISA/MC	102 if ISA/MC	Setup Only
MSR	Miscellaneous Output	7	W	3C2	3C2	
			R	3CC	3CC	
FCR	Feature Control	3	W	3BA	3DA	
			R	3CA	3CA	
ST00 (FEAT)	Feature Read (Input Status 0)	4	R	3C2	3C2	
ST01 (STAT)	Display Status (Input Status 1)	6	R	3BA	3DA	
CLPEN	Clear Light Pen Flip Flop	0	W(n/a)	3BB (ignored)	3DB (ignored)	ref only: no light pen
SLPEN	Set Light Pen Flip Flop	0	W(n/a)	3B9 (ignored)	3DC (ignored)	ref only: no light pen
DACMASK	Color Palette Pixel Mask	8	RW	3C6, 83C6	3C6, 83C6	
DACSTATE	Color Palette State	2	R	3C7, 83C7	3C7, 83C7	
DACRX	Color Palette Read-Mode Index	8	W	3C7, 83C7	3C7, 83C7	
DACWX	Color Palette Write-Mode Index	8	RW	3C8, 83C8	3C8, 83C8	
DACDATA	Color Palette Data 0-FF	3x6 or 3x8	RW	3C9, 83C9	3C9, 83C9	
SRX, SR0-7	Sequencer	0-8	RW	3C4-3C5	3C4-3C5	
CRX, CR0-3F	CRT Controller	0-8	RW	3B4-3B5	3D4-3D5	
GRX, GR0-8	Graphics Controller	0-8	RW	3CE-3CF	3CE-3CF	
ARX, AR0-14	Attributes Controller	0-8	RW	3C0-3C1	3C0-3C1	
XRX, XR0-7F	Extension Registers	0-8	RW	3D6-3D7	3D6-3D7	

REGISTER SUMMARY - INDEXED REGISTERS (VGA)

Register	Register Name	Bits	Register Type	Access (VGA)	Access (EGA)	I/O Port
SRX	Sequencer Index	3	VGA/EGA	RW	RW	3C4
SR0	Reset	2	VGA/EGA	RW	RW	3C5
SR1	Clocking Mode	6	VGA/EGA	RW	RW	3C5
SR2	Plane Mask	4	VGA/EGA	RW	RW	3C5
SR3	Character Map Select	6	VGA/EGA	RW	RW	3C5
SR4	Memory Mode	3	VGA/EGA	RW	RW	3C5
SR7	Reset Horizontal Character Counter	0	VGA	W	n/a	3C5
CRX	CRTC Index	6	VGA/EGA	RW	RW	3B4 Mono, 3D4 Color
CR0	Horizontal Total	8	VGA/EGA	RW	RW	3B5 Mono, 3D5 Color
CR1	Horizontal Display End	8	VGA/EGA	RW	RW	3B5 Mono, 3D5 Color
CR2	Horizontal Blanking Start	8	VGA/EGA	RW	RW	3B5 Mono, 3D5 Color
CR3	Horizontal Blanking End	5+2+1	VGA/EGA	RW	RW	3B5 Mono, 3D5 Color
CR4	Horizontal Retrace Start	8	VGA/EGA	RW	RW	3B5 Mono, 3D5 Color
CR5	Horizontal Retrace End	5+2+1	VGA/EGA	RW	RW	3B5 Mono, 3D5 Color
CR6	Vertical Total	8	VGA/EGA	RW	RW	3B5 Mono, 3D5 Color
CR7	Overflow	5	VGA/EGA	RW	RW	3B5 Mono, 3D5 Color
CR8	Preset Row Scan	5+2	VGA/EGA	RW	RW	3B5 Mono, 3D5 Color
CR9	Character Cell Height	5+3	VGA/EGA	RW	RW	3B5 Mono, 3D5 Color
CRA	Cursor Start	5+1	VGA/EGA	RW	RW	3B5 Mono, 3D5 Color
CRB	Cursor End	5+2	VGA/EGA	RW	RW	3B5 Mono, 3D5 Color
CRC	Start Address High	8	VGA/EGA	RW	RW	3B5 Mono, 3D5 Color
CRD	Start Address Low	8	VGA/EGA	RW	RW	3B5 Mono, 3D5 Color
CRE	Cursor Location High	8	VGA/EGA	RW	RW	3B5 Mono, 3D5 Color
CRF	Cursor Location Low	8	VGA/EGA	RW	RW	3B5 Mono, 3D5 Color
LPENH	Light Pen High	8	VGA/EGA	R	R	3B5 Mono, 3D5 Color
LPENL	Light Pen Low	8	VGA/EGA	R	R	3B5 Mono, 3D5 Color
CR10	Vertical Retrace Start	8	VGA/EGA	RW	W	3B5 Mono, 3D5 Color
CR11	Vertical Retrace End	4+4	VGA/EGA	RW	W	3B5 Mono, 3D5 Color
CR12	Vertical Display End	8	VGA/EGA	RW	RW	3B5 Mono, 3D5 Color
CR13	Offset	8	VGA/EGA	RW	RW	3B5 Mono, 3D5 Color
CR14	Underline Row Scan	5+2	VGA/EGA	RW	RW	3B5 Mono, 3D5 Color
CR15	Vertical Blanking Start	8	VGA/EGA	RW	RW	3B5 Mono, 3D5 Color
CR16	Vertical Blanking End	8	VGA/EGA	RW	RW	3B5 Mono, 3D5 Color
CR17	CRT Mode Control	7	VGA/EGA	RW	RW	3B5 Mono, 3D5 Color
CR18	Line Compare	8	VGA/EGA	RW	RW	3B5 Mono, 3D5 Color
CR22	Graphics Controller Data Latches	8	VGA	R	n/a	3B5 Mono, 3D5 Color
CR24	Attribute Controller Index/Data Latch	1	VGA	R	n/a	3B5 Mono, 3D5 Color
CR3x	Clear Vertical Display Enable FF	0	VGA	W	n/a	3B5 Mono, 3D5 Color
GRX	Graphics Controller Index	4	VGA/EGA	RW	RW	3CE
GR0	Set/Reset	4	VGA/EGA	RW	RW	3CF
GR1	Enable Set/Reset	4	VGA/EGA	RW	RW	3CF
GR2	Color Compare	4	VGA/EGA	RW	RW	3CF
GR3	Data Rotate	5	VGA/EGA	RW	RW	3CF
GR4	Read Map Select	2	VGA/EGA	RW	RW	3CF
GR5	Mode	6	VGA/EGA	RW	RW	3CF
GR6	Miscellaneous	4	VGA/EGA	RW	RW	3CF
GR7	Color Don't Care	4	VGA/EGA	RW	RW	3CF
GR8	Bit Mask	8	VGA/EGA	RW	RW	3CF
ARX	Attribute Controller Index	6	VGA/EGA	RW	RW	3C0 (3C1)
AR0-F	Internal Palette Regs 0-15	6	VGA/EGA	RW	RW	3C0 (3C1)
AR10	Mode Control	7	VGA/EGA	RW	RW	3C0 (3C1)
AR11	Overscan Color	6	VGA/EGA	RW	RW	3C0 (3C1)
AR12	Color Plane Enable	6	VGA/EGA	RW	RW	3C0 (3C1)
AR13	Horizontal Pixel Panning	4	VGA/EGA	RW	RW	3C0 (3C1)
AR14	Color Select	4	VGA	RW	n/a	3C0 (3C1)

EXTENSION REGISTER SUMMARY: 00-2F

Reg	Register Name	Bits	Access	Port	Reset	Chips' VGA Product Family								
						450	451	452	453	455	456	457	65520	65530
XRX	Extension Index Register	7	R/W	3B6/3D6	-xxxxxxx	✓	✓	✓	✓	✓	✓	✓	✓	✓
XR00	Chip Version (520: v=7, 530: v=8)	8	R/O	3B7/3D7	vvvvrrrr	✓	✓	✓	✓	✓	✓	✓	✓	✓
XR01	Configuration	8	R/O	3B7/3D7	dddddddd	✓	✓	✓	✓	✓	✓	✓	✓	✓
XR02	CPU Interface Control	8	R/W	3B7/3D7	00000000	✓	✓	✓	✓	✓	✓	✓	✓	✓
XR03	-reserved- *(ROM Interface)*	–	–	3B7/3D7		.	✓	✓	✓	.	.	✓	.	.
XR04	Memory Control	8	R/W	3B7/3D7	00000000	✓	✓	✓	.	✓	✓	✓	✓	✓
XR05	-reserved- *(Clock Control)*	–	–	3B7/3D7		.	.	✓	✓	.	.	✓	.	.
XR06	Color Palette Control *(DRAM Intfc)*	8	R/W	3B7/3D7	00000000	.	.	✓	.	.	.	.	✓	✓
XR07	-reserved-	–	–	3B7/3D7		.	.	.	.	.	.	.	.	.
XR08	-reserved- *(Gen Purp Output Select B)*	–	–	3B7/3D7		.	✓	✓	.	✓	✓	✓	.	.
XR09	-reserved- *(Gen Purp Output Select A)*	–	–	3B7/3D7		.	✓	✓	.	✓	✓	✓	.	.
XR0A	-reserved- *(Cursor Address Top)*	–	–	3B7/3D7		.	.	✓	.	.	.	.	.	.
XR0B	CPU Paging	5	R/W	3B7/3D7	---00000	✓	.	✓	✓	✓	✓	✓	✓	✓
XR0C	Start Address Top	2	R/W	3B7/3D7	------00	✓	.	✓	✓	.	.	.	✓	✓
XR0D	Auxiliary Offset	2	R/W	3B7/3D7	------00	✓	✓	✓	✓	✓	✓	✓	✓	✓
XR0E	Text Mode Control	2	R/W	3B7/3D7	----00--	✓	.	✓	.	.	.	.	✓	✓
XR0F	Software Flags 2	8	R/W	3B7/3D7	xxxxxxxx	.	.	.	.	.	.	.	✓	✓
XR10	Single/Low Map Register	8	R/W	3B7/3D7	xxxxxxxx	✓	.	✓	✓	.	.	.	✓	✓
XR11	High Map Register	8	R/W	3B7/3D7	xxxxxxxx	✓	.	✓	✓	.	.	.	✓	✓
XR12	-reserved-	–	–	3B7/3D7		.	.	.	.	.	.	.	.	.
XR13	-reserved-	–	–	3B7/3D7		.	.	.	.	.	.	.	.	.
XR14	Emulation Mode	8	R/W	3B7/3D7	0000hh00	✓	✓	✓	✓	✓	✓	✓	✓	✓
XR15	Write Protect	8	R/W	3B7/3D7	00000000	✓	✓	✓	✓	✓	✓	✓	✓	✓
XR16	-reserved- *(Trap Enable)*	–	–	3B7/3D7		.	✓	✓	✓	✓	✓	✓	.	.
XR17	-reserved- *(Trap Status)*	–	–	3B7/3D7		.	✓	✓	✓	✓	✓	✓	.	.
XR18	Alternate H Disp End	8	R/W	3B7/3D7	xxxxxxxx	✓	✓	✓	✓	✓	✓	✓	✓	✓
XR19	Alternate H Sync Start / Half-line	8	R/W	3B7/3D7	xxxxxxxx	✓	✓	✓	✓	✓	✓	✓	✓	✓
XR1A	Alternate H Sync End	8	R/W	3B7/3D7	xxxxxxxx	✓	✓	✓	✓	✓	✓	✓	✓	✓
XR1B	Alternate H Total	8	R/W	3B7/3D7	xxxxxxxx	✓	✓	✓	✓	✓	✓	✓	✓	✓
XR1C	Alternate H Blank Start / H Panel Size	8	R/W	3B7/3D7	xxxxxxxx	✓	✓	✓	✓	✓	✓	✓	✓	✓
XR1D	Alternate H Blank End	8	R/W	3B7/3D7	0xxxxxxx	✓	✓	✓	✓	✓	✓	✓	✓	✓
XR1E	Alternate Offset	8	R/W	3B7/3D7	xxxxxxxx	✓	✓	✓	✓	✓	✓	✓	✓	✓
XR1F	Virtual EGA Switch Register	5	R/W	3B7/3D7	0---xxxx	✓	.	.	.	.	.	.	✓	✓
XR20	-reserved- *(453 Interface II)/(SUD)*	–	–	3B7/3D7		.	.	✓	✓	.	.	.	.	.
XR21	-reserved- *(Sliding Hold A)*	–	–	3B7/3D7		.	.	✓	.	.	.	.	.	.
XR22	-reserved- *(Sliding Hold B)*	–	–	3B7/3D7		.	.	✓	.	.	.	.	.	.
XR23	-reserved- *(SHC)/(WBM Ctrl)*	–	–	3B7/3D7		.	.	✓	✓	.	.	.	.	.
XR24	FP AltMaxScanline *(SHD)/(WBM Patt)*	5	R/W	3B7/3D7	---xxxxx	.	.	✓	✓	.	.	.	✓	✓
XR25	FP AltGrHVirtPanel Size *(453PinDefn)*	8	R/W	3B7/3D7	xxxxxxxx	.	.	.	✓	.	.	.	✓	✓
XR26	-reserved- *(453 Config)*	–	–	3B7/3D7		.	.	.	✓	.	.	.	.	.
XR27	-reserved-	–	–	3B7/3D7		.	.	.	.	.	.	.	.	.
XR28	Video Interface	8	R/W	3B7/3D7	00000000	✓	✓	✓	✓	✓	✓	✓	✓	✓
XR29	-reserved- *(Function Control)*	–	–	3B7/3D7		.	.	✓	.	.	.	.	.	.
XR2A	-reserved- *(Frame Intrpt Count)*	–	–	3B7/3D7		.	.	✓	.	.	.	.	.	.
XR2B	Default Video	8	R/W	3B7/3D7	00000000	✓	✓	✓	.	✓	✓	✓	✓	✓
XR2C	FP Vsync (FLM) Delay *(Force H High)*	8	R/W	3B7/3D7	xxxxxxxx	.	.	✓	.	.	.	.	✓	✓
XR2D	FP Hsync (LP) Delay *(Force H Low)*	8	R/W	3B7/3D7	xxxxxxxx	.	.	✓	.	.	.	.	✓	✓
XR2E	FP Hsync (LP) Delay *(Force V High)*	8	R/W	3B7/3D7	xxxxxxxx	.	.	✓	.	.	.	.	✓	✓
XR2F	FP Hsync (LP) Width *(Force V Low)*	8	R/W	3B7/3D7	xxxxxxxx	.	.	✓	.	.	.	.	✓	✓

Reset Codes: x = Not changed by RESET (indeterminate on power-up)
d = Set from the corresponding data bus pin on falling edge of RESET
h = Read-only Hercules Configuration Register Readback bits
– = Not implemented (always reads 0)
r = Chip revision # (starting from 0000)
0/1 = Reset to 0/1 by falling edge of RESET

Note: Check marks in the table above indicate the register listed to the left is implemented in the chip named at the top of the column
Note: 450–453 VGAs drive CRTs only, 455–457 & 655x0 VGAs drive both CRT and Flat Panel displays (Plasma, EL, and LCD)

EXTENSION REGISTER SUMMARY: 30-5F

Reg	Register Name	Bits	Access	Port	Reset	Chips' VGA Product Family								
						450	451	452	453	455	456	457	65520	65530
XR30	*(Graphics Cursor Start Address High)*	–	–	3B7/3D7		.	.	✓	.	.	.	.	.	.
XR31	*(Graphics Cursor Start Address Low)*	–	–	3B7/3D7		.	.	✓	.	.	.	.	.	.
XR32	*(Graphics Cursor End Address)*	–	–	3B7/3D7		.	.	✓	.	.	.	.	.	.
XR33	*(Graphics Cursor X Position High)*	–	–	3B7/3D7		.	.	✓	.	.	.	.	.	.
XR34	*(Graphics Cursor X Position Low)*	–	–	3B7/3D7		.	.	✓	.	.	.	.	.	.
XR35	*(Graphics Cursor Y Position High)*	–	–	3B7/3D7		.	.	✓	.	.	.	.	.	.
XR36	*(Graphics Cursor Y Position Low)*	–	–	3B7/3D7		.	.	✓	.	.	.	.	.	.
XR37	*(Graphics Cursor Mode)*	–	–	3B7/3D7		.	.	✓	.	.	.	.	.	.
XR38	*(Graphics Cursor Mask)*	–	–	3B7/3D7		.	.	✓	.	.	.	.	.	.
XR39	*(Graphics Cursor Color 0)*	–	–	3B7/3D7		.	.	✓	.	.	.	.	.	.
XR3A	*(Graphics Cursor Color 1)*	–	–	3B7/3D7		.	.	✓	.	.	.	.	.	.
XR3B	-reserved-	–	–	3B7/3D7		.	.	.	.	.	.	.	.	.
XR3C	-reserved-	–	–	3B7/3D7		.	.	.	.	.	.	.	.	.
XR3D	-reserved-	–	–	3B7/3D7		.	.	.	.	.	.	.	.	.
XR3E	-reserved-	–	–	3B7/3D7		.	.	.	.	.	.	.	.	.
XR3F	-reserved-	–	–	3B7/3D7		.	.	.	.	.	.	.	.	.
XR40	-reserved-	–	–	3B7/3D7		.	.	.	.	.	.	.	.	.
XR41	-reserved- *(Virtual EGA Switch Reg)*	–	–	3B7/3D7		.	.	.	✓	.	.	.	.	.
XR42	-reserved-	–	–	3B7/3D7		.	.	.	.	.	.	.	.	.
XR43	-reserved-	–	–	3B7/3D7		.	.	.	.	.	.	.	.	.
XR44	**Software Flag Register**	8	R/W	3B7/3D7	xxxxxxxx	.	.	.	✓	.	.	.	✓	✓
XR45	-reserved- *(S/W Flag 2 / FG Color)*	–	–	3B7/3D7		.	.	.	✓	.	.	.	.	.
XR46	-reserved-	–	–	3B7/3D7		.	.	.	.	.	.	.	.	.
XR47	-reserved-	–	–	3B7/3D7		.	.	.	.	.	.	.	.	.
XR48	-reserved-	–	–	3B7/3D7		.	.	.	.	.	.	.	.	.
XR49	-reserved-	–	–	3B7/3D7		.	.	.	.	.	.	.	.	.
XR4A	-reserved-	–	–	3B7/3D7		.	.	.	.	.	.	.	.	.
XR4B	-reserved-	–	–	3B7/3D7		.	.	.	.	.	.	.	.	.
XR4C	-reserved-	–	–	3B7/3D7		.	.	.	.	.	.	.	.	.
XR4D	-reserved-	–	–	3B7/3D7		.	.	.	.	.	.	.	.	.
XR4E	-reserved-	–	–	3B7/3D7		.	.	.	.	.	.	.	.	.
XR4F	-reserved-	–	–	3B7/3D7		.	.	.	.	.	.	.	.	.
XR50	**Panel Format**	8	R/W	3B7/3D7	xxxxxxxx	.	.	.	.	✓	✓	✓	✓	✓
XR51	**Display Type**	8	R/W	3B7/3D7	xxxxx0xx	.	.	.	.	✓	✓	✓	✓	✓
XR52	**Power Down Control** *(Panel Size)*	8	R/W	3B7/3D7	00000000	.	.	.	.	✓	✓	✓	✓	✓
XR53	**Line Graphics Override**	7	R/W	3B7/3D7	x-xxxxx0	.	.	.	.	✓	✓	✓	✓	✓
XR54	**FP Interface** *(Alternate Misc Output)*	8	R/W	3B7/3D7	xxxxxxxx	.	.	.	.	✓	✓	✓	✓	✓
XR55	**H Compensation** *(Text 350_A Comp)*	6	R/W	3B7/3D7	xxxx--xx	.	.	.	.	✓	✓	✓	✓	✓
XR56	**H Centering** *(Text 350_B Comp)*	8	R/W	3B7/3D7	xxxxxxxx	.	.	.	.	✓	✓	✓	✓	✓
XR57	**V Compensation** *(Text 400 Comp)*	7	R/W	3B7/3D7	-xxxxxxx	.	.	.	.	✓	✓	✓	✓	✓
XR58	**V Centering** *(Graphics 350 Comp)*	8	R/W	3B7/3D7	xxxxxxxx	.	.	.	.	✓	✓	✓	✓	✓
XR59	**V Line Insertion** *(Graphics 400 Comp)*	6	R/W	3B7/3D7	-xx-xxxx	.	.	.	.	✓	✓	✓	✓	✓
XR5A	**V Line Replication** *(FP VDisp St 400)*	4	R/W	3B7/3D7	----xxxx	.	.	.	.	✓	✓	✓	✓	✓
XR5B	**Power Sequencing Delay** *(VD End 400)*	8	R/W	3B7/3D7	01110001	.	.	.	.	✓	✓	✓	.	✓
XR5C	-reserved- *(Weight Control Clock A)*	–	–	3B7/3D7		.	.	.	.	✓	✓	.	.	.
XR5D	-reserved- *(Weight Control Clock B)*	–	–	3B7/3D7		.	.	.	.	✓	✓	.	.	.
XR5E	**ACDCLK Control**	8	R/W	3B7/3D7	xxxxxxxx	.	.	.	.	✓	✓	✓	✓	✓
XR5F	**Power Down Mode Refresh**	8	R/W	3B7/3D7	xxxxxxxx	.	.	.	.	✓	✓	✓	✓	✓

Reset Codes: x = Not changed by RESET (indeterminate on power-up); – = Not implemented (always reads 0)
d = Set from the corresponding data bus pin on falling edge of RESET; r = Chip revision # (starting from 0000)
h = Read-only Hercules Configuration Register Readback bits; 0/1 = Reset to 0/1 by falling edge of RESET

Note: Check marks in the table above indicate the register listed to the left is implemented in the chip named at the top of the column
Note: 450–453 VGAs drive CRTs only, 455–457 & 655x0 VGAs drive both CRT and Flat Panel displays (Plasma, EL, and LCD)

EXTENSION REGISTER SUMMARY: 60-7F

Reg	Register Name	Bits	Access	Port	Reset	Chips' VGA Product Family								
						450	451	452	453	455	456	457	65520	65530
XR60	**Blink Rate Control**	8	R/W	3B7/3D7	10000011	.	.	.	.	✓	✓	✓	✓	✓
XR61	**SmartMap™ Control**	8	R/W	3B7/3D7	xxxxxxxx	.	.	.	.	✓	✓	.	✓	✓
XR62	**SmartMap™ Shift Parameter**	8	R/W	3B7/3D7	xxxxxxxx	.	.	.	.	✓	✓	.	✓	✓
XR63	**SmartMap™ Color Mapping Control**	7	R/W	3B7/3D7	x-xxxxxx	.	.	.	.	✓	✓	.	✓	✓
XR64	**FP Alternate Vertical Total**	8	R/W	3B7/3D7	xxxxxxxx	.	.	.	.	✓	✓	✓	✓	✓
XR65	**FP Alternate Overflow**	6	R/W	3B7/3D7	xxx--xxx	.	.	.	.	✓	✓	✓	✓	✓
XR66	**FP Alternate Vertical Sync Start**	8	R/W	3B7/3D7	xxxxxxxx	.	.	.	.	✓	✓	✓	✓	✓
XR67	**FP Alternate Vertical Sync End**	4	R/W	3B7/3D7	----xxxx	.	.	.	.	✓	✓	✓	✓	✓
XR68	**FP V Panel Size** *(FP Alt V DE End)*	8	R/W	3B7/3D7	xxxxxxxx	.	.	.	.	✓	✓	✓	✓	✓
XR69	-reserved- *(FP V Display Start 350)*	–	–	3B7/3D7		.	.	.	.	✓	✓	✓	.	.
XR6A	-reserved- *(FP V Display End 350)*	–	–	3B7/3D7		.	.	.	.	✓	✓	✓	.	.
XR6B	-reserved- *(FP V Overflow 2)*	–	–	3B7/3D7		.	.	.	.	✓	✓	✓	.	.
XR6C	**Programmable Output Drive** *(Wclk C)*	8	R/W	3B7/3D7	00000000	.	.	.	.	✓	✓	.	.	✓
XR6D	-reserved- *(FRC Control)*	–	–	3B7/3D7		.	.	.	.	.	✓	✓	.	.
XR6E	**Polynomial FRC Control**	8	R/W	3B7/3D7	10111101	.	.	.	.	.	.	✓	✓	✓
XR6F	**Frame Buffer Control**	6	R/W	3B7/3D7	--xxx000	.	.	.	.	.	.	.	✓	✓
XR70	**Setup / Disable Control**	1	R/W	3B7/3D7	0-------	✓	.	.	.	.	.	.	✓	✓
XR71	-reserved-	–	–	3B7/3D7		.	.	.	.	.	.	.	.	.
XR72	-reserved-	–	–	3B7/3D7		.	.	.	.	.	.	.	.	.
XR73	-reserved-	–	–	3B7/3D7		.	.	.	.	.	.	.	.	.
XR74	-reserved-	–	–	3B7/3D7		.	.	.	.	.	.	.	.	.
XR75	-reserved-	–	–	3B7/3D7		.	.	.	.	.	.	.	.	.
XR76	-reserved-	–	–	3B7/3D7		.	.	.	.	.	.	.	.	.
XR77	-reserved-	–	–	3B7/3D7		.	.	.	.	.	.	.	.	.
XR78	-reserved-	–	–	3B7/3D7		.	.	.	.	.	.	.	.	.
XR79	-reserved-	–	–	3B7/3D7		.	.	.	.	.	.	.	.	.
XR7A	-reserved-	–	–	3B7/3D7		.	.	.	.	.	.	.	.	.
XR7B	-reserved-	–	–	3B7/3D7		.	.	.	.	.	.	.	.	.
XR7C	-reserved-	–	–	3B7/3D7		.	.	.	.	.	.	.		
XR7D	**FP Compensation Diagnostic**	0	R/O	3B7/3D7	--------	.	.	.	.	.	.	.	✓	✓
XR7E	**CGA/Hercules Color Select**	6	R/W	3B7/3D7	--xxxxxx	✓	✓	✓	✓	✓	✓	✓	✓	✓
XR7F	**Diagnostic**	8	R/W	3B7/3D7	00xxxx00	✓	✓	✓	.	✓	✓	✓	✓	✓

Reset Codes: x = Not changed by RESET (indeterminate on power-up)
d = Set from the corresponding data bus pin on falling edge of RESET
h = Read-only Hercules Configuration Register Readback bits
– = Not implemented (always reads 0)
r = Chip revision # (starting from 0000)
0/1 = Reset to 0/1 by falling edge of RESET

Note: Check marks in the table above indicate the register listed to the left is implemented in the chip named at the top of the column
Note: 450–453 VGAs drive CRTs only, 455–457 & 655x0 VGAs drive both CRT and Flat Panel displays (Plasma, EL, and LCD)

Registers

GLOBAL CONTROL (SETUP) REGISTERS

The Setup Control Register and Video Subsystem Enable registers are used to enable or disable the VGA. The Setup Control register is also used to place the VGA in normal or setup mode (the Global Enable Register is accessible only during Setup mode). The Setup Control register is used only in ISA bus interfaces; the Video Subsystem Enable register is used only in MC, PI, and Local Bus configurations. In MC and PI Bus interfaces, disable and setup functions may also be performed by the DISA/ and SETUP/ pins respectively. The DISA/ pin and the various internal 'disable' bits 'OR' together to provide multiple ways of disabling the chip; all 'disable' bits must be off to enable access to the chip. When the chip is 'disabled' in this fashion, only bus access is disabled; other functions remain operational (memory refresh, display refresh, etc).

Note: In setup mode in the IBM VGA, the Global Setup Register (defined as port address 102) actually occupies the *entire I/O space*. Only the lower 3 bits are used to decode and select this register. To avoid bus conflicts with other peripherals, reads should only be performed at the 10xh port addresses while in setup mode. To eliminate potential compatibility problems in widely varying PC systems, the 65520 and 65530 decode the Global Setup register at I/O port 102h only.

GENERAL CONTROL REGISTERS

Two Input Status Registers read the SENSE pin (or Virtual Switch Register or internal comparator output instead), pending CRT interrupt, display enable / horizontal sync output, and vertical retrace / video output. The Feature Control Register selects the vertical sync function while the Miscellaneous Output Register controls I/O address select, clock selection, access to video RAM, memory page, and horizontal and vertical sync polarity.

CGA / HERCULES REGISTERS

CGA Mode and Color Select registers are provided on-chip for emulation of CGA modes. Hercules Mode and Configuration registers are provided on-chip for emulation of Hercules mode.

SEQUENCER REGISTERS

The Sequencer Index Register contains a 3-bit index to the Sequencer Data Registers. The Reset Register forces an asynchronous or synchronous reset of the sequencer. The Sequencer Clocking Mode Register controls master clocking functions, video enable/disable and selects either an 8 or 9 dot character clock. A Plane/Map Mask Register enables the color plane and write protect. The Character Font Select Register handles video intensity and character generation and controls the display memory plane through the character generator select. The Sequencer Memory Mode Register handles all memory, giving access by the CPU to 4 / 16 / 32 KBytes, Odd / Even addresses (planes) and writing of data to display memory.

CRT CONTROLLER REGISTERS

The CRT Controller Index Register contains a 6-bit index to the CRT Controller Registers. Twenty eight registers perform all display functions for modes: horizontal and vertical blanking and sync, panning and scrolling, cursor size and location, light pen, and underline.

GRAPHICS CONTROLLER REGISTERS

The Graphics Controller Index Register contains a 4-bit index to the Graphics Controller Registers. The Set/Reset Register controls the format of the CPU data to display memory. It also works with the Enable Set/Reset Register. Reducing 32 bits of display data to 8 bits of CPU data is accomplished by the Color Compare Register. Data Rotate Registers specify the CPU data bits to be rotated and subjected to logical operations. The Read Map Select Register reduces memory data for the CPU in the four plane (16 color) graphics mode. The Graphics Mode Register controls the write, read, and shift register modes. The Miscellaneous Register handles graphics/text, chaining of odd/even planes, and display memory mapping. Additional registers include Color Don't Care and Bit Mask.

ATTRIBUTE CONTROLLER AND COLOR PALETTE REGISTERS

The Attribute Controller Index Register contains a 5-bit index to the Attribute Controller Registers. A 6th

bit is used to enable the video. The Attribute Controller Registers handle internal color lookup table mapping, text/graphics mode, overscan color, and color plane enable. The horizontal Pixel Panning and Pixel Padding Registers control pixel attributes on screen.

Color palette registers handle CPU reads and writes to I/O address range 3C6h-3C9h. Inmos IMSG176 (Brooktree BT471/476) compatible registers are documented in this manual.

EXTENSION REGISTERS

The 65520 / 530 defines a set of extension registers which are addressed with the 7-bit Extension Register Index. The I/O port address is fixed at 3D6-3D7h and read/write access is always enabled to improve software performance.

The extension registers handle a variety of interfacing, compatibility, and display functions as discussed below. They are grouped into the following logical groups for discussion purposes:

1. Miscellaneous Registers include the Version number, Dip Switch, CPU interface, paging control, memory mode control, and diagnostic functions.
2. General Purpose Registers handle video blanking and the video default color.
3. Backwards Compatibility Registers control Hercules, MDA, and CGA emulation modes. Write Protect functions are provided to increase flexibility in providing backwards compatibility.
4. Alternate Horizontal and Vertical Registers handle all horizontal and vertical timing, including sync, blank and offset. These are used for backwards compatibility.
5. Flat Panel Registers handle all internal logic specific to driving of flat panel displays.

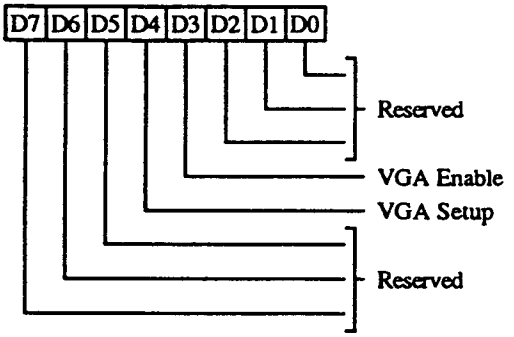
Note: The state of most of the Standard VGA Registers is undefined at reset. All registers specific to the 65520 / 530 (Extension Registers) are summarized in the Extension Register Table.

Global Control (Setup) Registers

Register Mnemonic	Register Name	Index	Access	I/O Address	Protect Group	Page
SETUP	Setup Control	–	W	46E8h (ISA bus only)	–	37
VSE	Video Subsystem Enable	–	W	3C3h (MC/PI/LB bus only)	–	37
ENAB	Global Enable	–	RW	102h (Setup mode only)	–	38

SETUP CONTROL REGISTER (SETUP)

Write only at I/O Address 46E8h



This register is accessable in ISA (PC) bus configurations only. It is ignored completely in MC, PI, and Local Bus configurations. It is also ignored if XR70 bit-7 is set to 1 (the default is 0). In MC and PI bus configurations, Setup mode and VGA Disable are controlled through the SETUP/ and DISA/ pins, respectively and by register 3C3.

This register is cleared by RESET.

2-0 **Reserved (0)**

3 **VGA Enable**

0 VGA is disabled
1 VGA is enabled

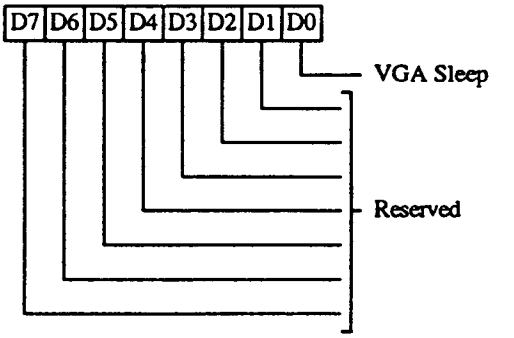
4 **Setup Mode**

0 VGA is in Normal Mode
1 VGA is in Setup Mode

7-5 **Reserved (0)**

VIDEO SUBSYSTEM ENABLE REGISTER (VSE)

Write Only at I/O Address 3C3h



This register is accessable in MC, PI, and Local Bus configurations only. It is ignored in ISA (PC) bus configurations (register 46E8 is used in ISA bus configurations). Access to this register may be disabled by setting XR70 bit-7 to 1 (the default is 0).

This register is cleared by RESET.

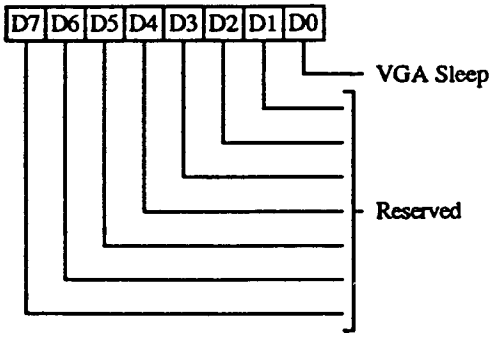
0 **VGA Sleep**

0 VGA is disabled
1 VGA is enabled

7-1 **Reserved (0)**

GLOBAL ENABLE REGISTER (ENAB)

Read/Write at I/O Address 102h



This register is only accessible in Setup Mode (enabled by register 46E8 in ISA bus configurations or by the SETUP/ pin in MC bus configurations).

Bit-0 of this register is cleared by RESET in ISA and MC bus configurations and set by RESET in PI and Local Bus configurations.

0 VGA Sleep

0 VGA is disabled
1 VGA is enabled

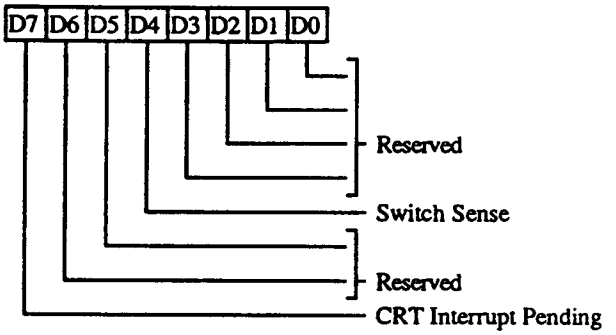
7-1 Reserved (0)

General Control & Status Registers

Register Mnemonic	Register Name	Index	Access	I/O Address	Protect Group	Page
ST00	Input Status 0	–	R	3C2h	–	39
ST01	Input Status 1	–	R	3BAh/3DAh	–	39
FCR	Feature Control	–	W	3BAh/3DAh	5	40
			R	3CAh		
MSR	Miscellaneous Output	–	W	3C2h	5	40
			R	3CCh		

INPUT STATUS REGISTER 0 (ST00)

Read only at I/O Address at 3C2h



3-0 Reserved (0)

4 Switch Sense

This bit returns the Status of the SENSE pin or the Virtual Switch Register (XR1F) output if enabled by XR1F bit-7 or the output of the internal comparator if enabled by XR06 bit-4 (Sense Source). XR1F bit-7 takes priority over the other settings if set.

6-5 Reserved

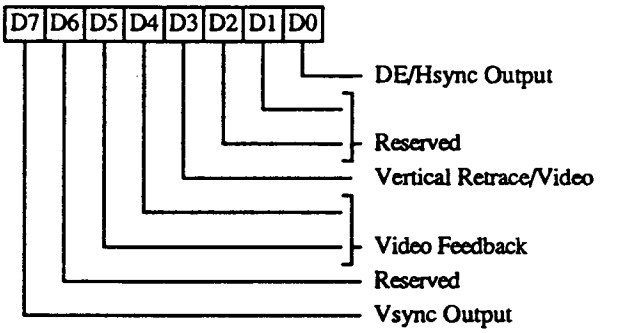
These bits read back 00 in PC and PI bus configurations and 11 in MC configuration.

7 CRT Interrupt Pending

0 Indicates no CRT interrupt is pending
1 Indicates a CRT interrupt is waiting to be serviced

INPUT STATUS REGISTER 1 (ST01)

Read only at I/O Address 3BAh/3DAh



0 Display Enable/HSYNC Output

The functionality of this bit is controlled by the Emulation Mode register (XR14 bit-4).

0 Indicates DE or HSYNC inactive
1 Indicates DE or HSYNC active

2-1 Reserved (0)

3 Vertical Retrace/Video

The functionality of this bit is controlled by the Emulation Mode register (XR14 bit-5).

0 Indicates VSYNC or video inactive
1 Indicates VSYNC or video active

5-4 Video Feedback 1, 0

These are diagnostic video bits which are selected via the Color Plane Enable Register.

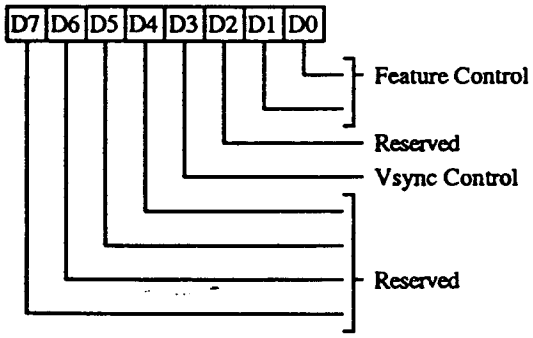
6 Reserved (0)

7 Vsync Output

The functionality of this bit is controlled by the Emulation Mode register (XR14 bit-6). It reflects the active status of the VSYNC output: 0=inactive, 1=active.

FEATURE CONTROL REGISTER (FCR)

Write at I/O Address 3BAh/3DAh
Read at I/O Address 3CAh
Group 5 Protection



1-0 Feature Control

These bits are used internal to the chip in conjunction with the Configuration Register (XR01). When enabled by XR01 bits 2-3 and Misc Output Register bits 3-2 = 10, these bits determine the pixel clock frequency typically as follows:

FCR1:0 = 00 = 40.000 MHz
FCR1:0 = 01 = 50.350 MHz
FCR1:0 = 10 = User defined
FCR1:0 = 11 = 44.900 MHz

This preserves compatibility with drivers developed for earlier generation Chips and Technologies VGA controllers.

2 Reserved (0)

3 Vsync Control

This bit is cleared by RESET.

0 VSync output on the VSYNC pin
1 Logical 'OR' of VSync and Display Enable output on the VSYNC pin

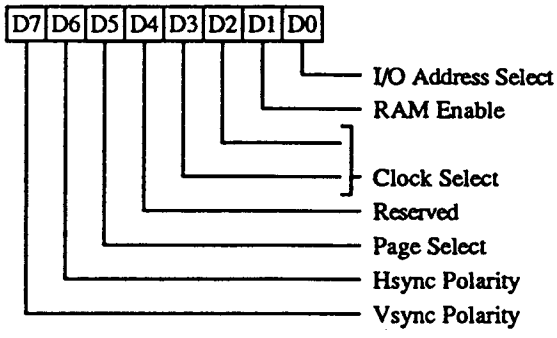
This capability is not typically very useful, but is provided for IBM compatibility.

7-4 Reserved (0)

CRT Display Sync Polarities				
V	H	Display	H Freq	V Freq
P	P	>480 Line	Variable	Variable
P	P	200 Line	15.7 KHz	60 Hz
N	P	350 Line	21.8 KHz	60 Hz
P	N	400 Line	31.5 KHz	70 Hz
N	N	480 Line	31.5 KHz	60 Hz

MISCELLANEOUS OUTPUT REGISTER (MSR)

Write at I/O Address 3C2h
Read at I/O Address 3CCh
Group 5 Protection



This register is cleared by RESET.

0 I/O Address Select. This bit selects 3Bxh or 3Dxh as the I/O address for the CRT Controller registers, the Feature Control Register (FCR), and Input Status Register 1 (ST01).

0 Select 3Bxh I/O address
1 Select 3Dxh I/O address

1 RAM Enable

0 Prevent CPU access to display memory
1 Allow CPU access to display memory

3-2 Clock Select. These bits usually select the dot clock source for the CRT interface:

MSR3:2 = 00 = Select CLK0
MSR3:2 = 01 = Select CLK1
MSR3:2 = 10 = Select CLK2
MSR3:2 = 11 = Select CLK3

See extension register XR01 bits 2-3 (Configuration) and FCR bits 0-1 for variations of the above clock selection mapping. See also XR1F (Virtual Switch Register) for additional functionality potentially controlled by these bits.

4 Reserved (0)

5 Page Select. In Odd/Even Memory Map Mode 1 (GR6), this bit selects the upper or lower 64 KByte page in display memory for CPU access: 0=select upper page; 1=select lower page.

6 CRT Hsync Polarity. 0=pos, 1=neg

7 CRT Vsync Polarity. 0=pos, 1=neg

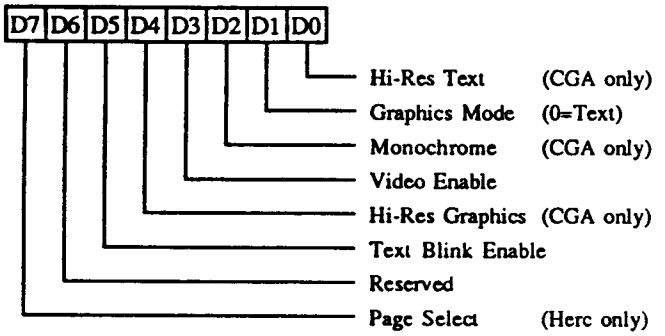
(Blank pin polarity can be controlled via the Video Interface Register, XR28). XR55 bits 6-7 are used to control H/V sync polarity instead of these bits if XR51 bit-2 = 1 (display type = flat panel).

CGA / Hercules Registers

Register Mnemonic	Register Name	Index	Access	I/O Address	Protect Group	Page
MODE	CGA/Hercules Mode	–	RW	3D8h	–	41
COLOR	CGA Color Select	–	RW	3D9h	–	42
HCFG	Hercules Configuration	–	RW	3BFh	–	43

CGA / HERCULES MODE CONTROL REGISTER (MODE)

Read/Write at I/O Address 3B8h/3D8h



This register is effective only in CGA and Hercules modes. It is accessible if CGA or Hercules emulation mode is selected or the extension registers are enabled. If the extension registers are enabled, the address is determined by the address select in the Miscellaneous Outputs register. Otherwise the address is determined by the emulation mode. It is cleared by RESET.

0 CGA 80/40 Column Text Mode
- 0 Select 40 column CGA text mode
- 1 Select 80 column CGA text mode

1 CGA/Hercules Graphics/Text Mode
- 0 Select text mode
- 1 Select graphics mode

2 CGA Mono/Color Mode
- 0 Select CGA color mode
- 1 Select CGA monochrome mode

3 CGA/Hercules Video Enable
- 0 Blank the screen
- 1 Enable video output

4 CGA High Resolution Mode
- 0 Select 320x200 graphics mode
- 1 Select 640x200 graphics mode

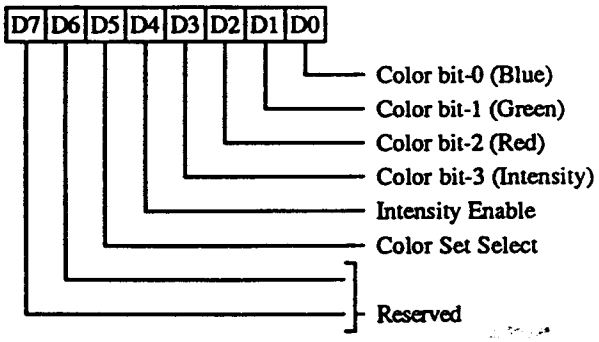
5 CGA/Hercules Text Blink Enable
- 0 Disable character blink attribute (blink attribute bit-7 used to control background intensity)
- 1 Enable character blink attribute

6 Reserved (0)

7 Hercules Page Select
- 0 Select the lower part of memory (starting address B0000h) in Hercules Graphics Mode
- 1 Select the upper part of the memory (starting address B8000h) in Hercules Graphics Mode

CGA COLOR SELECT REGISTER (COLOR)

Read/Write at I/O Address 3D9h



This register is effective only in CGA modes. It is accessible if CGA emulation mode is selected or the extension registers are enabled. This register may also be read or written as an Extension Register (XR7E). It is cleared by RESET.

3-0 Color

320x200 4-color: Background Color (color when the pixel value is 0)

The foreground colors (colors when the pixel value is 1-3) are determined by bit-5 of this register.

640x200 2-color: Foreground Color (color when the pixel value is 1)

The background color (color when the pixel value is 0) is black.

4 Intensity Enable

Text Mode: Enables intensified background colors

320x200 4-color: Enables intensified colors 0-3

640x200 2-color: Don't care

5 Color Set Select

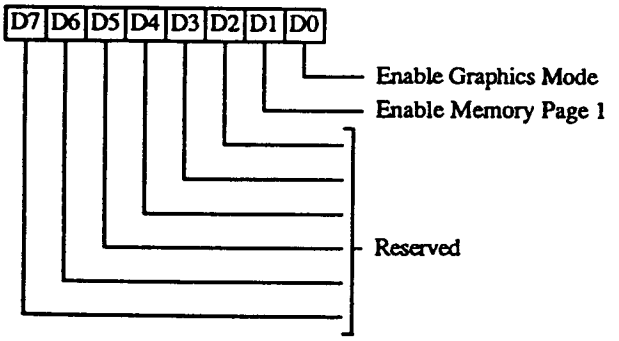
This bit selects one of two available CGA color palettes to be used in 320x200 graphics mode (it is ignored in all other modes) according to the following table:

Pixel Value	Color Set 0	Color Set 1
0 0	Color per bits 0-3	Color per bits 0-3
0 1	Green	Cyan
1 0	Red	Magenta
1 1	Brown	White

7-6 Reserved (0)

HERCULES CONFIGURATION REGISTER (HCFG)

Write only at I/O Address 3BFh



This register is effective only in Hercules mode. It is accessible in Hercules emulation mode or if the extension registers are enabled. It may be read back through XR14 bits 2 & 3. It is cleared by RESET.

0 Enable Graphics Mode

- 0 Lock the chip in Hercules text mode. In this mode, the CPU has access only to memory address range B0000h-B7FFFh (in text mode the same area of display memory wraps around 8 times within this range such that B0000 accesses the same display memory location as B1000, B2000, etc.).
- 1 Permit entry to Hercules Graphics mode

1 Enable Memory Page 1

- 0 Prevent setting of the Page Select bit (bit 7 of the Hercules Mode Control Register). This function also restricts memory usage to addresses B0000h-B7FFFh.
- 1 The Page Select bit can be set and the upper part of display memory (addresses B8000h - BFFFFh) is available.

7-2 Reserved (0)

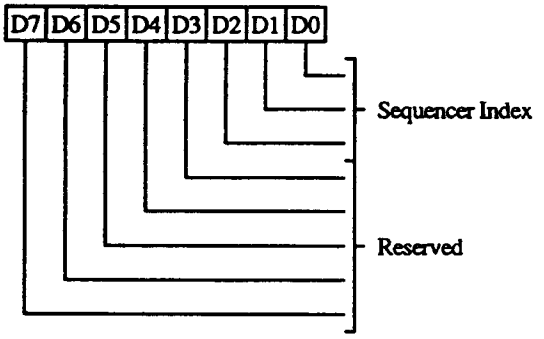
This Page Intentionally Left Blank

Sequencer Registers

Register Mnemonic	Register Name	Index	Access	I/O Address	Protect Group	Page
SRX	Sequencer Index	–	RW	3C4h	1	45
SR00	Reset	00h	RW	3C5h	1	45
SR01	Clocking Mode	01h	RW	3C5h	1	46
SR02	Plane/Map Mask	02h	RW	3C5h	1	46
SR03	Character Font	03h	RW	3C5h	1	47
SR04	Memory Mode	04h	RW	3C5h	1	48
SR07	Horizontal Character Counter Reset	07h	W	3C5h	–	48

SEQUENCER INDEX REGISTER (SRX)

Read/Write at I/O Address 3C4h



This register is cleared by reset.

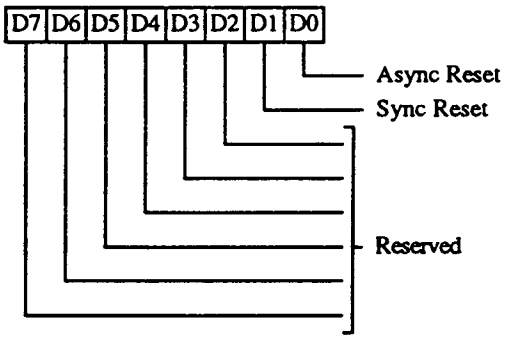
2-0 Sequencer Index

These bits contain a 3-bit Sequencer Index value used to access sequencer data registers at indices 0 through 7.

7-3 Reserved (0)

SEQUENCER RESET REGISTER (SR00)

Read/Write at I/O Address 3C5h
Index 00h
Group 1 Protection



0 Asynchronous Reset

0 Force asynchronous reset
1 Normal operation

Display memory data will be corrupted if this bit is set to zero.

1 Synchronous Reset

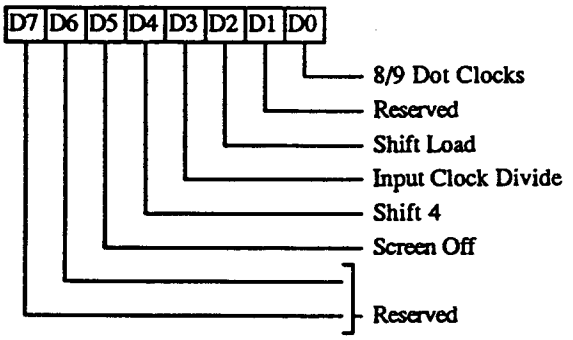
0 Force synchronous reset
1 Normal operation

Display memory data is not corrupted if this bit is set to zero for a short period of time (a few tens of microseconds).

7-2 Reserved (0)

SEQUENCER CLOCKING MODE REGISTER (SR01)

Read/Write at I/O Address 3C5h
Index 01h
Group 1 Protection



0 8/9 Dot Clocks

This bit determines whether a character clock is 8 or 9 dot clocks long.

0 Select 9 dots/character clock
1 Select 8 dots/character clock

1 Reserved (0)

2 Shift Load

0 Load video data shift registers every character clock
1 Load video data shift registers every other character clock

Bit-4 of this register must be 0 for this bit to be effective.

3 Input Clock Divide

0 Sequencer master clock output on the PCLK pin (used for 640 (720) pixel modes)
1 Master clock divided by 2 output on the PCLK pin (used for 320 (360) pixel modes)

4 Shift 4

0 Load video shift registers every 1 or 2 character clocks (depending on bit-2 of this register)
1 Load shift registers every 4th character clock.

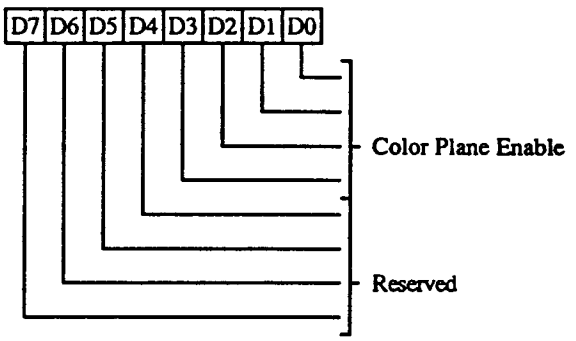
5 Screen Off

0 Normal Operation
1 Disable video output and assign all display memory bandwidth for CPU accesses

7-6 Reserved (0)

SEQUENCER PLANE/MAP MASK REGISTER (SR02)

Read/Write at I/O Address 3C5h
Index 02h
Group 1 Protection



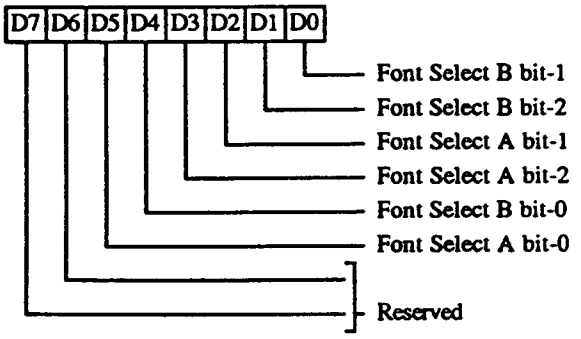
3-0 Color Plane Enable

0 Write protect corresponding color plane
1 Allow write to corresponding color plane.

In Odd/Even and Quad modes, these bits still control access to the corresponding color plane.

7-4 Reserved (0)

CHARACTER FONT SELECT REGISTER (SR03)
Read/Write at I/O Address 3C5h
Index 03h
Group 1 Protection



In text modes, bit-3 of the video data's attribute byte normally controls the foreground intensity. This bit may be redefined to control switching between character sets. This latter function is enabled whenever there is a difference in the values of the Character Font Select A and the Character Font Select B bits. If the two values are the same, the character select function is disabled and attribute bit-3 controls the foreground intensity.

SR04 bit-1 must be 1 for the character font select function to be active. Otherwise, only character fonts 0 and 4 are available.

1-0 **High order bits of Character Generator Select B**

3-2 **High order bits of Character Generator Select A**

4 **Low order bit of Character Generator Select B**

5 **Low order bit of Character Generator Select A**

7-6 **Reserved (0)**

The following table shows the display memory plane selected by the Character Generator Select A and B bits.

Code	Character Generator Table Location
0	First 8K of Plane 2
1	Second 8K of Plane 2
2	Third 8K of Plane 2
3	Fourth 8K of Plane 2
4	Fifth 8K of Plane 2
5	Sixth 8K of Plane 2
6	Seventh 8K of Plane 2
7	Eighth 8K of Plane 2

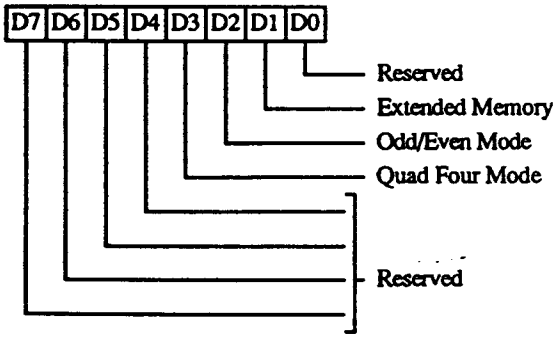
where 'code' is:

Character Generator Select A (bits 3, 2, 5) when bit-3 of the the attribute byte is one.

Character Generator Select B (bits 1, 0, 4) when bit-3 of the attribute byte is zero.

SEQUENCER MEMORY MODE REGISTER (SR04)

Read/Write at I/O Address 3C5h
Index 04h
Group 1 Protection



0 **Reserved (0)**

1 **Extended Memory**

0 Restrict CPU access to 4/16/32 Kbytes
1 Allow complete access to memory

This bit should normally be 1.

2 **Odd/Even Mode**

0 CPU accesses to Odd/Even addresses are directed to corresponding odd/even planes
1 All planes are accessed simultaneously (IRGB color)

Bit-3 of this register must be 0 for this bit to be effective. This bit affects only CPU write accesses to display memory.

3 **Quad Four Mode**

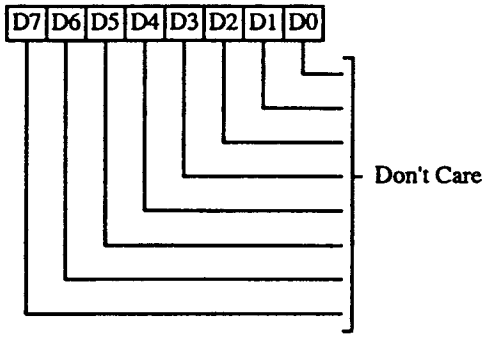
0 CPU addresses are mapped to display memory as defined by bit-2 of this register
1 CPU addresses are mapped to display memory modulo 4. The two low order CPU address bits select the display memory plane.

This bit affects both CPU reads and writes to display memory.

7-4 **Reserved (0)**

SEQUENCER HORIZONTAL CHARACTER COUNTER RESET (SR07)

Read/Write at I/O Address 3C5h
Index 07h



Writing to SR07 with any data will cause the horizontal character counter to be held reset (character counter output = 0) until a write to any other sequencer register with any data value. The write to any index in the range 0-6 clears the latch that is holding the reset condition on the character counter.

The vertical line counter is clocked by a signal derived from horizontal display enable (which does not occur if the horizontal counter is held reset). Therefore, if the write to SR07 occurs during vertical retrace, the horizontal and vertical counters will both be set to zero. A write to any other sequencer register may then be used to start both counters with reasonable synchronization to an external event via software control.

This is a standard VGA register which was not documented by IBM.

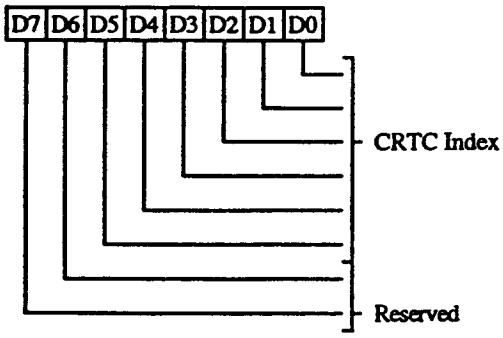
CRT Controller Registers

Register Mnemonic	Register Name	Index	Access	I/O Address	Protect Group	Page
CRX	CRTC Index	–	RW	3B4h/3D4h	–	50
CR00	Horizontal Total	00h	RW	3B5h/3D5h	0	50
CR01	Horizontal Display Enable End	01h	RW	3B5h/3D5h	0	50
CR02	Horizontal Blank Start	02h	RW	3B5h/3D5h	0	51
CR03	Horizontal Blank End	03h	RW	3B5h/3D5h	0	51
CR04	Horizontal Sync Start	04h	RW	3B5h/3D5h	0	52
CR05	Horizontal Sync End	05h	RW	3B5h/3D5h	0	52
CR06	Vertical Total	06h	RW	3B5h/3D5h	0	53
CR07	Overflow	07h	RW	3B5h/3D5h	0/3	53
CR08	Preset Row Scan	08h	RW	3B5h/3D5h	3	54
CR09	Maximum Scan Line	09h	RW	3B5h/3D5h	2/4	54
CR0A	Cursor Start Scan Line	0Ah	RW	3B5h/3D5h	2	55
CR0B	Cursor End Scan Line	0Bh	RW	3B5h/3D5h	2	55
CR0C	Start Address High	0Ch	RW	3B5h/3D5h	–	56
CR0D	Start Address Low	0Dh	RW	3B5h/3D5h	–	56
CR0E	Cursor Location High	0Eh	RW	3B5h/3D5h	–	56
CR0F	Cursor Location Low	0Fh	RW	3B5h/3D5h	–	56
CR10	Vertical Sync Start (See Note 2)	10h	W or RW	3B5h/3D5h	4	57
CR11	Vertical Sync End (See Note 2)	11h	W or RW	3B5h/3D5h	3/4	57
CR10	Lightpen High (See Note 2)	10h	R	3B5h/3D5h	–	57
CR11	Lightpen Low (See Note 2)	11h	R	3B5h/3D5h	–	57
CR12	Vertical Display Enable End	12h	RW	3B5h/3D5h	4	58
CR13	Offset	13h	RW	3B5h/3D5h	3	58
CR14	Underline Row	14h	RW	3B5h/3D5h	3	58
CR15	Vertical Blank Start	15h	RW	3B5h/3D5h	4	59
CR16	Vertical Blank End	16h	RW	3B5h/3D5h	4	59
CR17	CRT Mode Control	17h	RW	3B5h/3D5h	3/4	60
CR18	Line Compare	18h	RW	3B5h/3D5h	3	61
CR22	Memory Data Latches	22h	R	3B5h/3D5h	–	62
CR24	Attribute Controller Toggle	24h	R	3B5h/3D5h	–	62
CR3x	Clear Vertical Display Enable	3xh	W	3B5h/3D5h	–	62

Note 1: When MDA or Hercules emulation is enabled, the CRTC I/O address should be set to 3B0h-3B7h by setting the I/O address select bit in the Miscellaneous Output register (3C2h/3CCh bit-0) to zero. When CGA emulation is enabled, the CRTC I/O address should be set to 3D0h-3D7h by setting Misc Output Register bit-0 to 1.

Note 2: In the EGA, all CRTC registers except the cursor (CR0C-CR0F) and light pen (CR10 and CR11) registers are write-only (i.e., no read back). In both the EGA and VGA, the light pen registers are at index locations conflicting with the vertical sync registers. This would normally prevent reads and writes from occurring at the same index. Since the light pen registers are not normally useful, the VGA provides software control (CR03 bit-7) of whether the vertical sync or light pen registers are readable at indices 10-11.

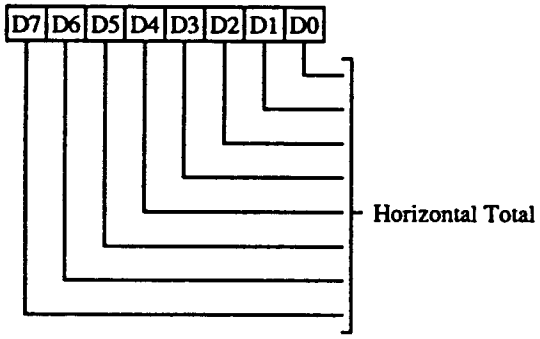
CRTC INDEX REGISTER (CRX)
Read/Write at I/O Address 3B4h/3D4h



5-0 CRTC data register index

7-6 Reserved (0)

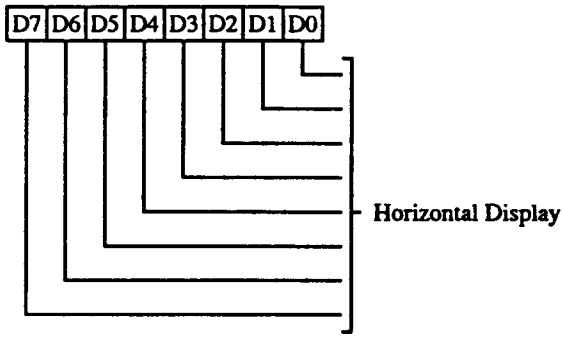
HORIZONTAL TOTAL REGISTER (CR00)
Read/Write at I/O Address 3B5h/3D5h
Index 00h
Group 0 Protection



This register is used for all VGA and EGA modes. It is also used for 640 column CGA modes and MDA/Hercules text mode. In all 320 column CGA modes and Hercules graphics mode, the alternate register is used.

7-0 Horizontal Total. Total number of character clocks per line = contents of this register + 5. This register determines the horizontal sweep rate.

HORIZONTAL DISPLAY ENABLE END REGISTER (CR01)
Read/Write at I/O Address 3B5h/3D5h
Index 01h
Group 0 Protection

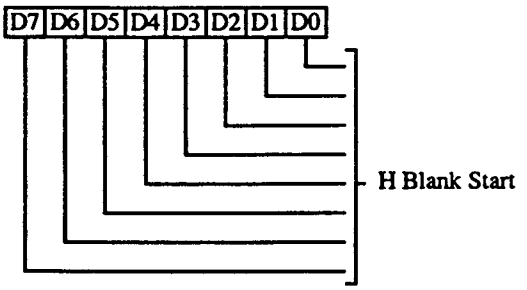


This register is used for all VGA and EGA modes on CRTs. It is also used for 640 column CGA modes and MDA/Hercules text mode. In all 320 column CGA modes and Hercules graphics mode, the alternate register is used.

7-0 Number of Characters displayed per scan line - 1.

HORIZONTAL BLANK START REGISTER (CR02)

Read/Write at I/O Address 3B5h/3D5h
Index 02h
Group 0 Protection



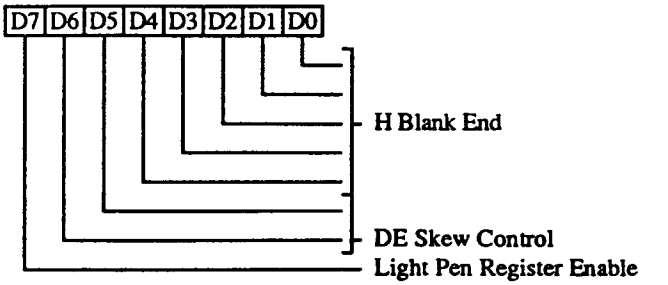
This register is used for all VGA and EGA modes. It is also used for 640 column CGA modes and MDA/Hercules text mode. In all 320 column CGA modes and Hercules graphics mode, the alternate register is used.

7-0 Horizontal Blank Start

These bits specify the beginning of horizontal blank in terms of character clocks from the beginning of the display scan. The period between Horizontal Display Enable End and Horizontal Blank Start is the right side border on screen.

HORIZONTAL BLANK END REGISTER (CR03)

Read/Write at I/O Address 3B5h/3D5h
Index 03h
Group 0 Protection



This register is used for all VGA and EGA modes. It is also used for 640 column CGA modes and MDA/Hercules text mode. In all 320 column CGA modes and Hercules graphics mode, the alternate register is used.

4-0 Horizontal Blank End

These are the lower 5 bits of the character clock count used to define the end of horizontal blank. The interval between the end of horizontal blank and the beginning of the display (a count of 0) is the left side border on the screen. If the horizontal blank width desired is W clocks, the 5-bit value programmed in this register = [contents of CR02 + W] and 1Fh. The most significant bit is programmed in CR05 bit-7. This bit = [(CR02 + W) and 20h]/20h.

6-5 Display Enable Skew Control

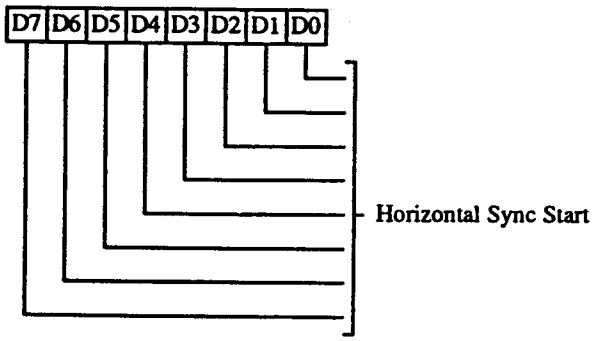
Defines the number of character clocks that the Display Enable signal is delayed to compensate for internal pipeline delays.

7 Light Pen Register Enable

This bit must be 1 for normal operation; when this bit is 0, CRTC registers CR10 and CR11 function as lightpen readback registers.

HORIZONTAL SYNC START REGISTER (CR04)

Read/Write at I/O Address 3B5h/3D5h
Index 04h
Group 0 Protection



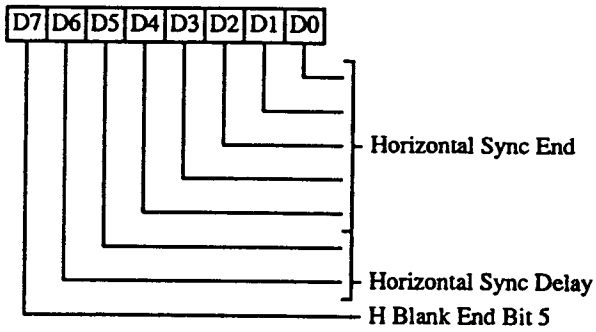
This register is used for all VGA and EGA modes. It is also used for 640 column CGA modes and MDA/Hercules text mode. In all 320 column CGA modes and Hercules graphics mode, the alternate register is used.

7-0 Horizontal Sync Start

These bits specify the beginning of Hsync in terms of Character clocks from the beginning of the display scan. These bits also determine display centering on the screen.

HORIZONTAL SYNC END REGISTER (CR05)

Read/Write at I/O Address 3B5h/3D5h
Index 05h
Group 0 Protection



This register is used for all VGA and EGA modes. It is also used for 640 column CGA modes and MDA/Hercules text mode. In all 320 column CGA modes and Hercules graphics mode, the alternate register is used.

4-0 Horizontal Sync End

Lower 5 bits of the character clock count which specifies the end of Horizontal Sync. If the horizontal sync width desired is N clocks, then these bits = (N + contents of CR04) and 1Fh.

6-5 Horizontal Sync Delay

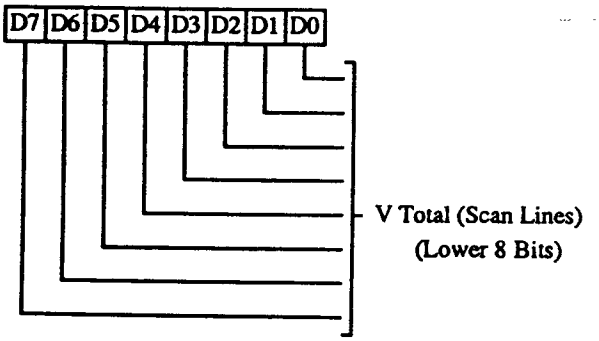
These bits specify the number of character clocks that the Horizontal Sync is delayed to compensate for internal pipeline delays.

7 Horizontal Blank End Bit 5

This bit is the sixth bit of the Horizontal Blank End Register (CR03).

VERTICAL TOTAL REGISTER (CR06)

Read/Write at I/O Address 3B5h/3D5h
Index 06h
Group 0 Protection



This register is used in all modes.

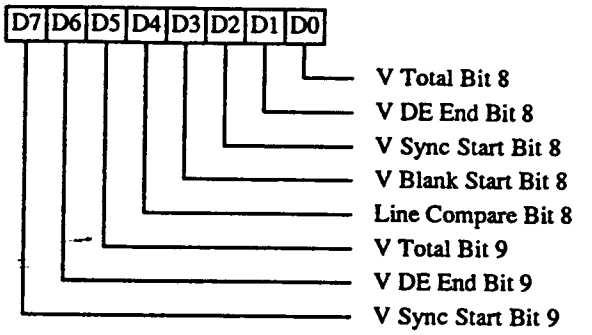
7-0 Vertical Total

These are the 8 low order bits of a 10-bit register. The 9th and 10th bits are located in the CRT Controller Overflow Register. The Vertical Total value specifies the total number of scan lines (horizontal retrace periods) per frame.

Programmed Count = Actual Count – 2

OVERFLOW REGISTER (CR07)

Read/Write at I/O Address 3B5h/3D5h
Index 07h
Group 0 Protection on bits 0-3 and bits 5-7
Group 3 Protection on bit 4



This register is used in all modes.

0 Vertical Total Bit 8

1 Vertical Display Enable End Bit 8

2 Vertical Sync Start Bit 8

3 Vertical Blank Start Bit 8

4 Line Compare Bit 8

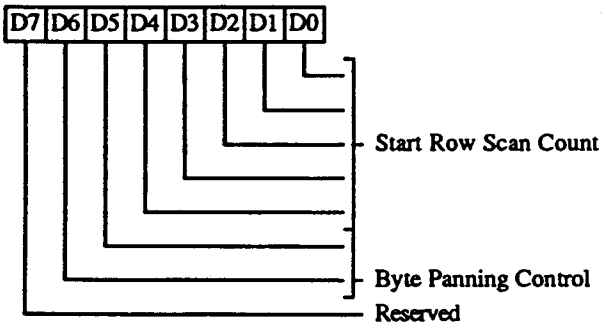
5 Vertical Total Bit 9

6 Vertical Display Enable End Bit 9

7 Vertical Sync Start Bit 9

PRESET ROW SCAN REGISTER (CR08)

Read/Write at I/O Address 3B5h/3D5h
Index 08h
Group 3 Protection



4-0 Start Row Scan Count

These bits specify the starting row scan count after each vertical retrace. Every horizontal retrace increments the character row scan line counter. The horizontal row scan counter is cleared at maximum row scan count during active display. This register is used for soft scrolling in text modes.

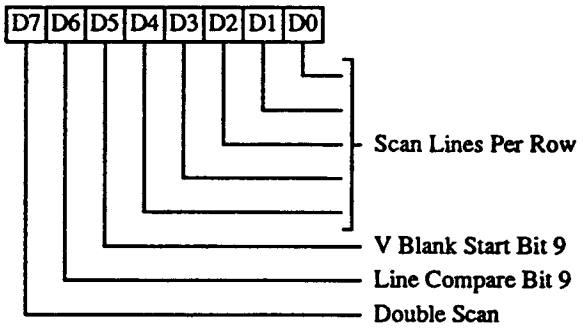
6-5 Byte Panning Control

These bits specify the lower order bits for the display start address. They are used for horizontal panning in Odd/Even and Quad modes.

7 Reserved (0)

MAXIMUM SCAN LINE REGISTER (CR09)

Read/Write at I/O Address 3B5h/3D5h
Index 09h
Group 2 Protection on bits 0-4
Group 4 Protection on bits 5-7



4-0 Scan Lines Per Row

These bits specify the number of scan lines in a row:

Programmed Value = Actual Value + 1

5 Vertical Blank Start Register Bit 9

6 Line Compare Register Bit 9

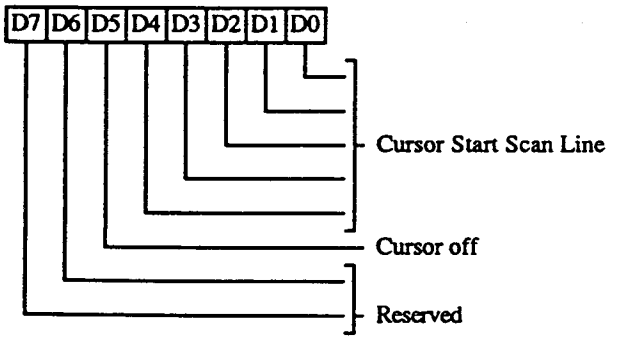
7 Double Scan

0 Normal Operation
1 Enable scan line doubling

The vertical parameters in the CRT Controller (even for a split screen) are not affected, only the CRTC row scan counter (bits 0-4 of this register) and display memory addressing screen refresh are affected.

CURSOR START SCAN LINE REGISTER (CR0A)

Read/Write at I/O Address 3B5h/3D5h
Index 0Ah
Group 2 Protection



4-0 Cursor Start Scan Line

These bits specify the scan line of the character row where the cursor display begins.

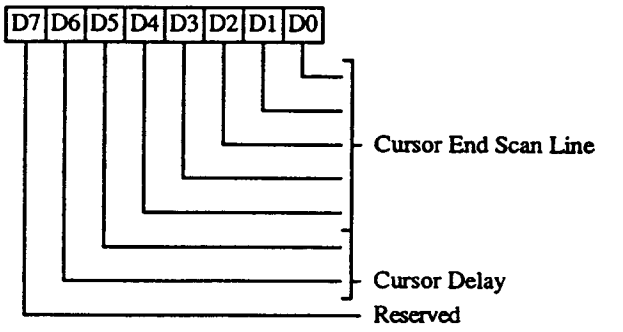
5 Cursor Off

0 Text Cursor On
1 Text Cursor Off

7-6 Reserved (0)

CURSOR END SCAN LINE REGISTER (CR0B)

Read/Write at I/O Address 3B5h/3D5h
Index 0Bh
Group 2 Protection



4-0 Cursor End Scan Line

These bits specify the scan line of a character row where the cursor display ends (i.e., last scan line for the block cursor):

Programmed Value = Actual Value + 1

6-5 Cursor Delay

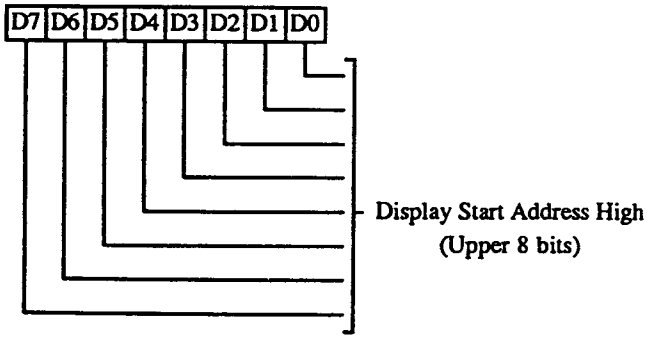
These bits define the number of character clocks that the cursor is delayed to compensate for internal pipeline delay.

7 Reserved (0)

Note: If the Cursor Start Line is greater than the Cursor End Line, then no cursor is generated.

START ADDRESS HIGH REGISTER (CR0C)

Read/Write at I/O Address 3B5h/3D5h
Index 0Ch

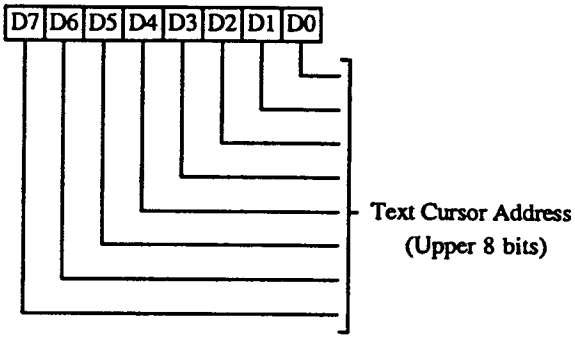


7-0 Display Start Address High

This register contains the upper 8 bits of the display start address. In CGA / MDA / Hercules modes, this register wraps around at the 16K, 32K, and 64Kbyte boundaries respectively.

CURSOR LOCATION HIGH REGISTER (CR0E)

Read/Write at I/O Address 3B5h/3D5h
Index 0Eh

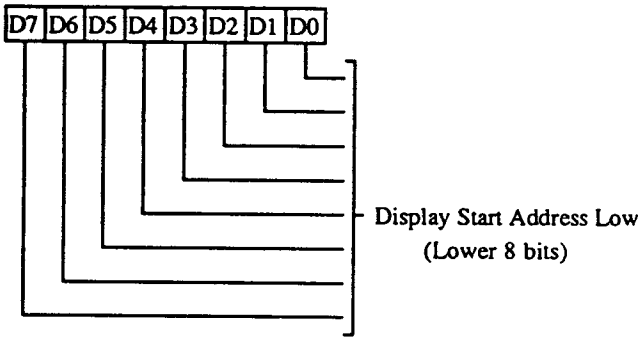


7-0 Cursor Location High

This register contains the upper 8 bits of the memory address where the text cursor is active. In CGA / MDA / Hercules modes, this register wraps around at 16K, 32K, and 64Kbyte boundaries respectively.

START ADDRESS LOW REGISTER (CR0D)

Read/Write at I/O Address 3B5h/3D5h
Index 0Dh

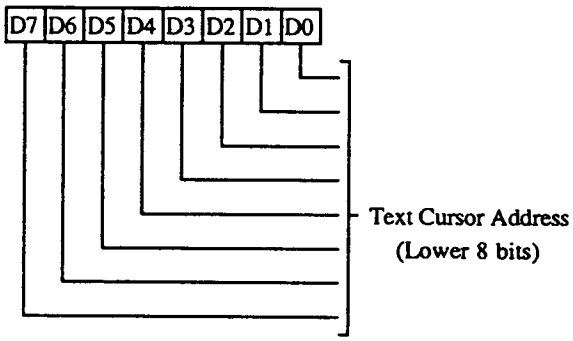


7-0 Display Start Address Low

This register contains the lower 8 bits of the display start address. The display start address points to the memory address corresponding to the top left corner of the screen.

CURSOR LOCATION LOW REGISTER (CR0F)

Read/Write at I/O Address 3B5h/3D5h
Index 0Fh



7-0 Cursor Location Low

This register contains the lower 8 bits of the memory address where the text cursor is active. In CGA / MDA / Hercules modes, this register wraps around at 16K, 32K, and 64Kbyte boundaries respectively.

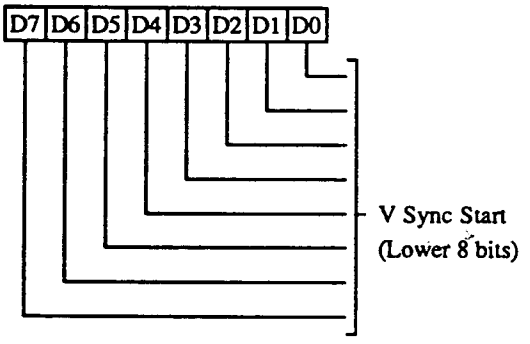
LIGHTPEN HIGH REGISTER (CR10)
Read only at I/O Address 3B5h/3D5h
Index 10h

Read-only Register loaded at line compare (the light pen flip-flop is not implemented). Effective only in MDA and Hercules modes or when CR03 bit-7 = 0.

LIGHTPEN LOW REGISTER (CR11)
Read only at I/O Address 3B5h/3D5h
Index 11h

Read-only Register loaded at line compare (the light pen flip-flop is not implemented). Effective only in MDA and Hercules modes or when CR03 bit-7 = 0.

VERTICAL SYNC START REGISTER (CR10)
Read/Write at I/O Address 3B5h/3D5h
Index 10h
Group 4 Protection

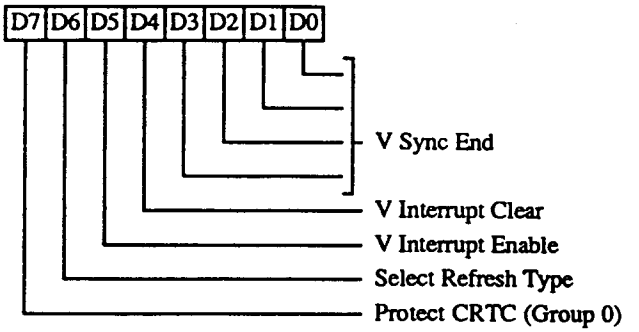


This register is used in all modes. This register is not readable in (Line Compare bit-9) MDA/Hercules emulation or when CR03 bit-7=1.

7-0 Vertical Sync Start

The eight low order bits of a 10-bit register. The 9th and 10th bits are located in the CRTC Overflow Register. They define the scan line position at which Vertical Sync becomes active.

VERTICAL SYNC END REGISTER (CR11)
Read/Write at I/O Address 3B5h/3D5h
Index 11h
Group 3 Protection for bits 4 and 5
Group 4 Protection for bits 0-3, 6, and 7



This register is used in all modes. This register is not readable in MDA/Hercules emulation or when CR03 bit-7=1.

3-0 Vertical Sync End

The lower 4 bits of the scan line count that defines the end of vertical sync. If the vertical sync width desired is N lines, then bits 3-0 of this register = (CR10 + N) AND 0Fh.

4 Vertical Interrupt Clear

0=Clear vertical interrupt generated on the IRQ output; 1=Normal operation. This bit is cleared by RESET.

5 Vertical Interrupt Enable

0 Enable vertical interrupt (default)
1 Disable vertical interrupt

This bit is cleared by RESET.

6 Select Refresh Type

0 3 refresh cycles per scan line
1 5 refresh cycles per scan line

7 Group Protect 0

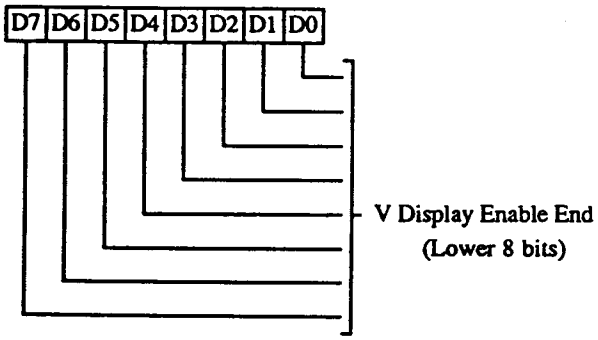
This bit is logically ORed with XR15 bit-6 to determine the protection for group 0 registers. This bit is cleared by RESET.

0 Enable writes to CR00-CR07
1 Disable writes to CR00-CR07

CR07 bit-4 (Line Compare bit-9) is not affected by this bit.

VERTICAL DISPLAY ENABLE END REGISTER (CR12)

Read/Write at I/O Address 3B5h/3D5h
Index 12h
Group 4 Protection

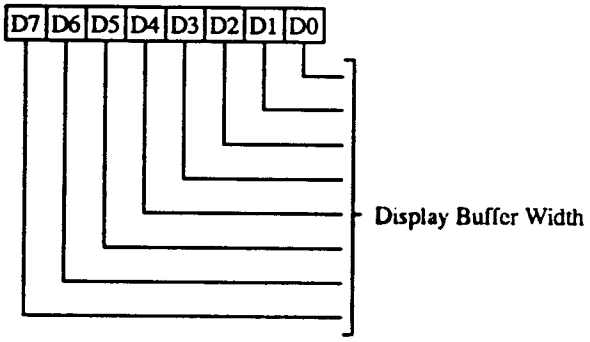


7-0 Vertical Display Enable End

These are the eight low order bits of a 10-bit register. The 9th and 10th bits are located in the CRT Controller Overflow register. The actual count = Contents of this register + 1.

OFFSET REGISTER (CR13)

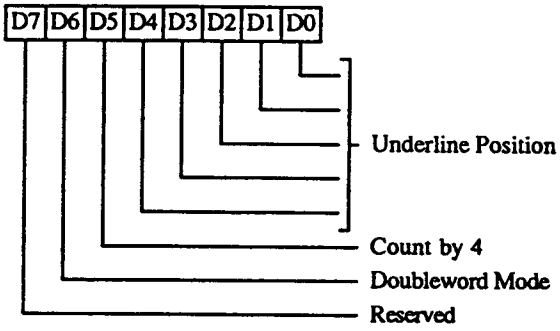
Read/Write at I/O Address 3B5h/3D5h
Index 13h
Group 3 Protection



7-0 Display Buffer Width. The byte starting address of the next display row = Byte Start Address for current row + K* (CR13 + Z/2), where Z = bit defined in XR0D, K = 2 in byte mode, and K = 4 in word mode. Byte, word and double word mode is selected by bit-6 of CR17 and bit-6 of CR14. A less significant bit than bit-0 of this register is defined in the Auxiliary Offset register (XR0D). This allows finer resolution of the bit map width. Byte, word and doubleword mode affects the translation of the 'logical' display memory address to the 'physical' display memory address.

UNDERLINE LOCATION REGISTER (CR14)

Read/Write at I/O Address 3B5h/3D5h
Index 14h
Group 3 Protection



4-0 Underline Position

These bits specify the underline's scan line position within a character row.

Programmed Value = Actual scan line number – 1

5 Count by 4 for Doubleword Mode

0 Frame Buffer Address is incremented by 1 or 2
1 Frame Buffer Address is incremented by 4 or 2

See CR17 bit-3 for further details.

6 Doubleword Mode

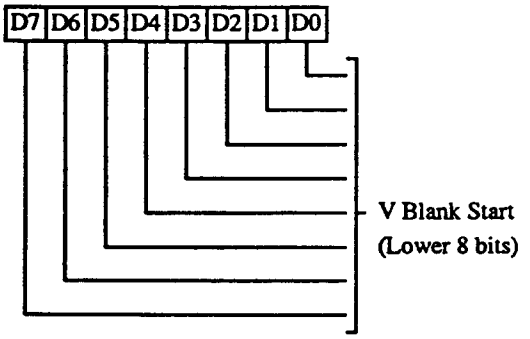
0 Frame Buffer Address is byte or word address
1 Frame Buffer Address is doubleword address

This bit is used in conjunction with CR17 bit-6 to select the display memory addressing mode.

7 Reserved (0)

VERTICAL BLANK START REGISTER (CR15)

Read/Write at I/O Address 3B5h/3D5h
Index 15h
Group 4 Protection



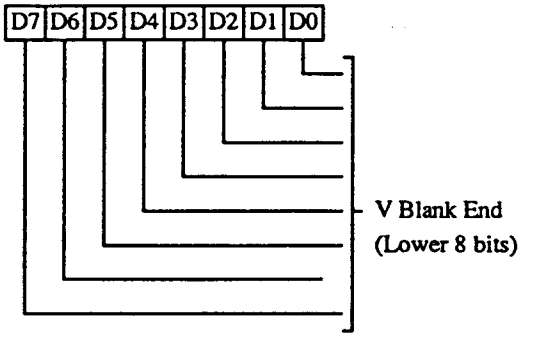
This register is used in all modes.

7-0 Vertical Blank Start

These are the 8 low order bits of a 10-bit register. The 9th and 10th bits are located in the CRT Controller Overflow and Maximum Scan Line Registers respectively. Together these 10 bits define the scan line position where vertical blank begins. The interval between the end of the vertical display and the beginning of vertical blank is the bottom border on the screen.

VERTICAL BLANK END REGISTER (CR16)

Read/Write at I/O Address 3B5h/3D5h
Index 16h
Group 4 Protection



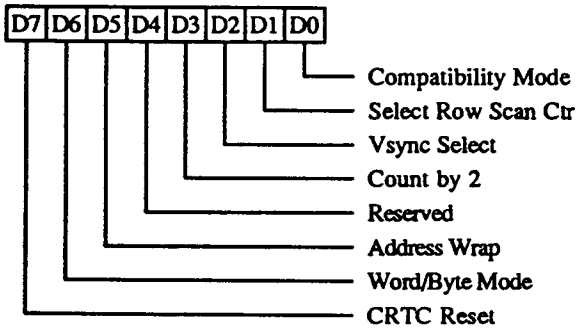
This register is used in all modes.

7-0 Vertical Blank End

These are the 8 low order bits of the scan line count which specifies the end of Vertical Blank. If the vertical blank width desired is Z lines these bits = (Vertical Blank Start + Z) and 0FFh.

CRT MODE CONTROL REGISTER (CR17)

Read/Write at I/O Address 3B5h/3D5h
Index 17h
Group 3 Protection for bits 0, 1, and 3-7
Group 4 Protection for bit 2



0 Compatibility Mode Support

This bit allows compatibility with the IBM CGA two-bank graphics mode.

0 Character row scan line counter bit 0 is substituted for memory address bit 13 during active display time
1 Normal operation, no substitution takes place

1 Select Row Scan Counter

This bit allows compatibility with Hercules graphics and with any other 4-bank graphics system.

0 Character row scan line counter bit 1 is substituted for memory address bit 14 during active display time
1 Normal operation, no substitution takes place

2 Vertical Sync Select

This bit controls the vertical resolution of the CRT Controller by permitting selection of the clock rate input to the vertical counters. When set to 1, the vertical counters are clocked by the horizontal retrace clock divided by 2.

3 Count By Two

0 Memory address counter is incremented every character clock
1 Memory address counter is incremented every two character clocks, used in conjunction with bit 5 of 0Fh.

Note: This bit is used in conjunction with CR14 bit-5. The net effect is as follows:

CR14 Bit-5	CR17 Bit-3	Increment Addressing Every
0	0	1 CCLK
0	1	2 CCLK
1	0	4 CCLK
1	1	2 CCLK

Note: In Hercules graphics and Hi-res CGA modes, address inrements every two clocks.

4 Reserved (0)

5 Address Wrap (effective only in word mode)

0 Wrap display memory address at 16 Kbytes. Used in IBM CGA mode.
1 Normal operation (extended mode).

6 Word Mode or Byte Mode

0 Select Word Mode. In this mode the display memory address counter bits are shifted down by one, causing the most-significant bit of the counter to appear on the least-significant bit of the display memory address output
1 Select byte mode

Note: This bit is used in conjunction with CR14 bit-6 to select byte, word, or double word memory addressing as follows:

CR14 Bit-6	CR17 Bit-6	Addressing Mode
0	0	Word Mode
0	1	Byte Mode
1	0	Double Word Mode
1	1	Double Word Mode

Display memory addresses are affected as shown in the table on the following page.

7 Hardware Reset

0 Force HSYNC and VSYNC inactive. No other registers or outputs affected.
1 Normal Operation

This bit is cleared by RESET.

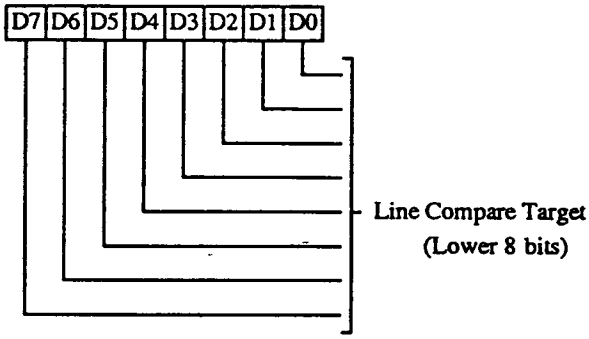
Display memory addresses are affected by CR17 bit 6 as shown in the table below:

Logical Memory Address	Physical Memory Address Byte Mode	Word Mode	Double Word Mode
MA00	A00	Note 1	Note 2
MA01	A01	A00	Note 3
MA02	A02	A01	A00
MA03	A03	A02	A01
MA04	A04	A03	A02
MA05	A05	A04	A03
MA06	A06	A05	A04
MA07	A07	A06	A05
MA08	A08	A07	A06
MA09	A09	A08	A07
MA10	A10	A09	A08
MA11	A11	A10	A09
MA12	A12	A11	A10
MA13	A13	A12	A11
MA14	A14	A13	A12
MA15	A15	A14	A13

Note 1 = A13 * NOT CR17 bit 5
+ A15 * CR17 bit 5
Note 2 = A12 xor (A14 * XR04 bit 2)
Note 3 = A13 xor (A15 * XR04 bit 2)

LINE COMPARE REGISTER (CR18)

Read/Write at I/O Address 3B5h/3D5h
Index 18h
Group 3 Protection

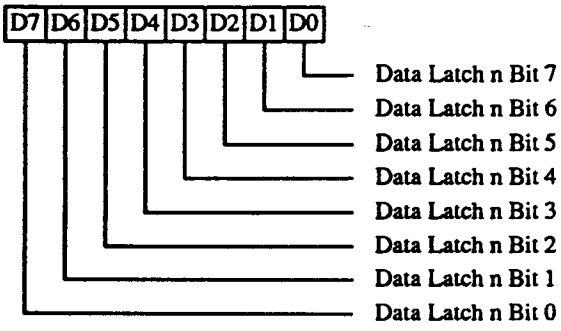


7-0 Line Compare Target

These are the low order 8 bits of a 10-bit register. The 9th and 10th bits are located in the CRT Controller Overflow and Maximum Scan Line Registers, respectively. This register is used to implement a split screen function. When the scan line counter value is equal to the contents of this register, the memory address counter is cleared to 0. The display memory address counter then sequentially addresses the display memory starting at address 0. Each subsequent row address is generated by the addition of the Offset Register contents. This register is not affected by the double scanning bit (CR09 bit 7).

MEMORY DATA LATCH REGISTER (CR22)

Read only at I/O Address 3B5h/3D5h
Index 22h



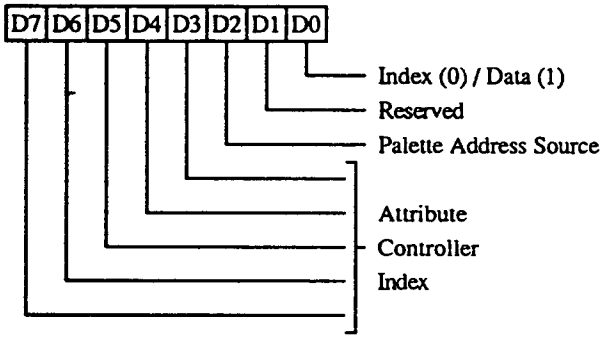
This register may be used to read the state of Graphics Controller Memory Data Latch 'n', where 'n' is controlled by the Graphics Controller Read Map Select Register (GR04 bits 0–1) and is in the range 0–3.

Writes to this register are not decoded and will be ignored.

This is a standard VGA register which was not documented by IBM.

ATTRIBUTE CONTROLLER TOGGLE REGISTER (CR24)

Read only at I/O Address 3B5h/3D5h
Index 24h



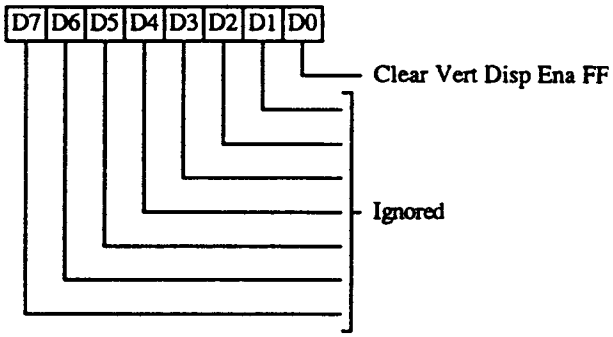
This register may be used to read back the state of the attribute controller index/data latch.

Writes to this register are not decoded and will be ignored.

This is a standard VGA register which was not documented by IBM.

CLEAR VERTICAL DISPLAY ENABLE FFh (CR3X)

Write only at I/O Address 3B5h/3D5h
Index 3xh



Writing odd data values to CRTC index 30-3Fh causes the vertical display enable flip-flop to be cleared. The flip-flop is automatically set by reaching vertical total. The effect of this is to force a longer vertical retrace period. There are two side effects of terminating vertical display enable early: first, the screen blanks early for one frame causing a minor visual disturbance and second, the sequencer gives more display memory cycles to the CPU because vertical display is not enabled.

Reads from this register are not decoded and will return indeterminate data.

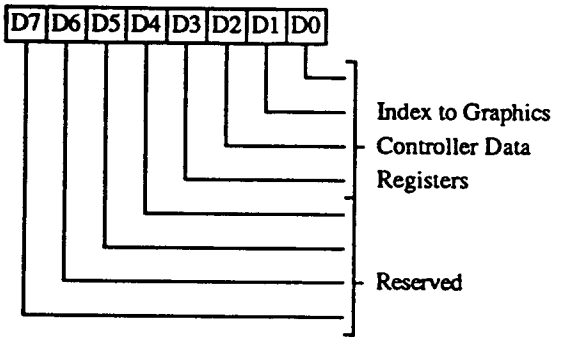
This is a standard VGA register which was not documented by IBM.

Graphics Controller Registers

Register Mnemonic	Register Name	Index	Access	I/O Address	Protect Group	Page
GRX	Graphics Index	–	RW	3CEh	1	63
GR00	Set/Reset	00h	RW	3CFh	1	63
GR01	Enable Set/Reset	01h	RW	3CFh	1	64
GR02	Color Compare	02h	RW	3CFh	1	64
GR03	Data Rotate	03h	RW	3CFh	1	64
GR04	Read Map Select	04h	RW	3CFh	1	65
GR05	Graphics mode	05h	RW	3CFh	1	66
GR06	Miscellaneous	06h	RW	3CFh	1	67
GR07	Color Don't Care	07h	RW	3CFh	1	68
GR08	Bit Mask	08h	RW	3CFh	1	69

GRAPHICS CONTROLLER INDEX REGISTER (GRX)

Write only at I/O Address 3CEh
Group 1 Protection

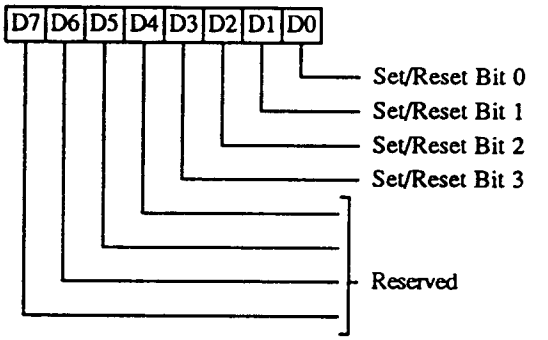


3-0 **4-bit Index to Graphics Controller Registers**

7-4 **Reserved (0)**

SET/RESET REGISTER (GR00)

Read/Write at I/O Address 3CFh
Index 00h
Group 1 Protection



The SET/RESET and ENABLE SET/RESET registers are used to 'expand' 8 bits of CPU data to 32 bits of display memory.

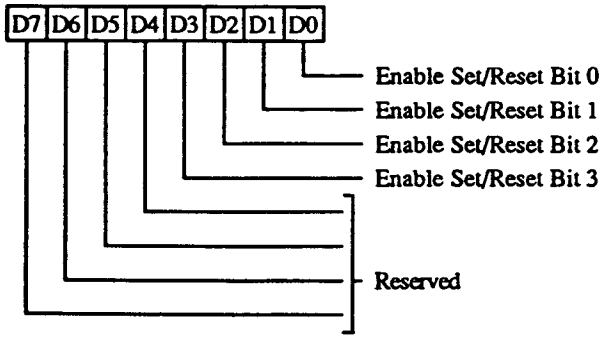
3-0 **Set / Reset Planes 3-0**

When the Graphics Mode register selects Write Mode 0, all 8 bits of each display memory plane are set as specified in the corresponding bit in this register. The Enable Set/Reset register (GR01) allows selection of some of the source of data to be written to individual planes. In Write Mode 3 (see GR05), these bits determine the color value.

7-4 **Reserved (0)**

ENABLE SET/RESET REGISTER (GR01)

Read/Write at I/O Address 3CFh
Index 01h
Group 1 Protection



3-0 Enable Set / Reset Planes 3-0

This register works in conjunction with the Set/Reset register (GR00). The Graphics Mode register must be programmed to Write Mode 0 in order for this register to have any effect.

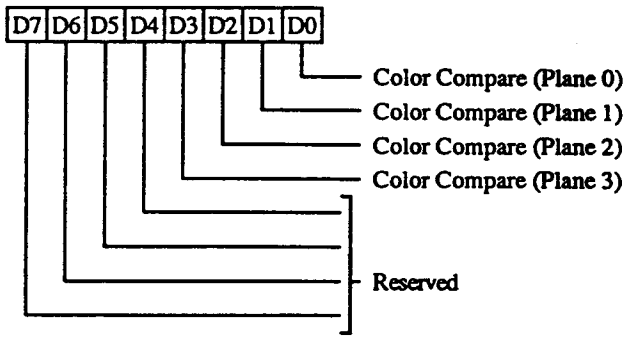
0 The corresponding plane is written with the data from the CPU data bus

1 The corresponding plane is set to 0 or 1 as specified in the Set/Reset Register

7-4 Reserved (0)

COLOR COMPARE REGISTER (GR02)

Read/Write at I/O Address 3CFh
Index 02h
Group 1 Protection



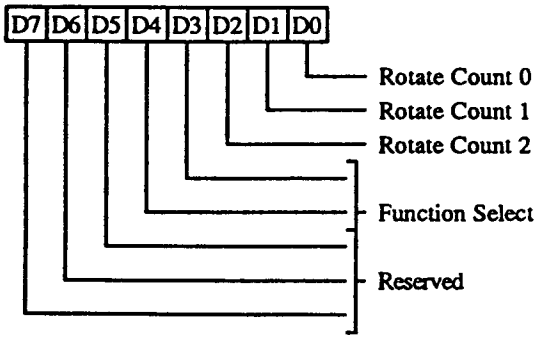
3-0 Color Compare Planes 3-0

This register is used to 'reduce' 32 bits of memory data to 8 bits for the CPU in 4-plane graphics mode. These bits provide a reference color value to compare to data read from display memory planes 0-3. The Color Don't Care register (GR07) is used to affect the result. This register is active only if the Graphics Mode register (GR05) is set to Read Mode 1. A match between the memory data and the Color Compare register (GR02) (for the bits specified in the Color Don't Care register) causes a logical 1 to be placed on the CPU data bus for the corresponding data bit; a mis-match returns a logical 0.

7-4 Reserved (0)

DATA ROTATE REGISTER (GR03)

Read/Write at I/O Address 3CFh
Index 03h
Group 1 Protection



2-0 Data Rotate Count

These bits specify the number of bits to rotate to the right the data being written by the CPU. The CPU data bits are first rotated, then subjected to the logical operation as specified in the Function Select bit field. The rotate function is active only if the Graphics Mode register is programmed for Write Mode 0.

4-3 Function Select

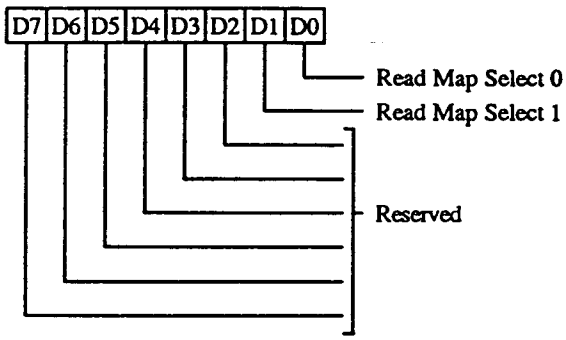
These Function Select bits specify the logical function performed on the contents of the processor latches (loaded on a previous CPU read cycle) before the data is written to display memory. These bits operate as follows:

Bit 4	Bit 3	Result
0	0	No change to the Data, Latches are updated
0	1	Logical 'AND' between Data and latched data
1	0	Logical 'OR' between Data and latched data
1	1	Logical 'XOR' between Data and latched data

7-5 Reserved (0)

READ MAP SELECT REGISTER (GR04)

Read/Write at I/O Address 3CFh
Index 04h
Group 1 Protection



1-0 Read Map Select

This register is also used to 'reduce' 32 bits of memory data to 8 bits for the CPU in the 4-plane graphics mode. These bits select the memory plane from which the CPU reads data in Read Mode 0. In Odd/Even mode, bit-0 is ignored. In Quad mode, bits 0 and 1 are both ignored.

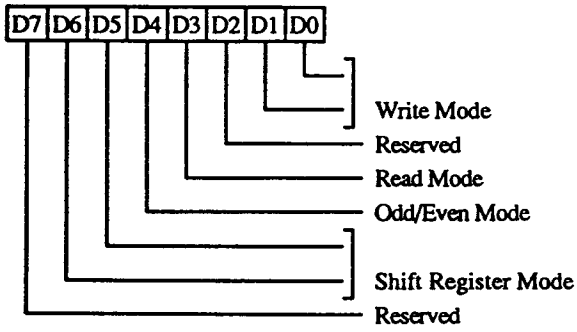
The four memory maps are selected as follows:

Bit 1	Bit 0	Map Selected
0	0	Plane 0
0	1	Plane 1
1	0	Plane 2
1	1	Plane 3

7-2 Reserved (0)

GRAPHICS MODE REGISTER (GR05)

Read/Write at I/O Address 3CFh
Index 05h
Group 1 Protection



1-0 Write Mode

For 16-bit writes, the operation is repeated on the lower and upper bytes of CPU data.

1	0	Write Mode
0	0	**Write mode 0.** Each of the four display memory planes is written with the CPU data rotated by the number of counts in the Rotate Register, except when the Set/Reset Register is enabled for any of the four planes. When the Set/Reset Register is enabled, the corresponding plane is written with the data stored in the Set/Reset Register.
0	1	**Write mode 1.** Each of the four display memory planes is written with the data previously loaded in the processor latches. These latches are loaded during all read operations.
1	0	**Write mode 2.** The CPU data bus data is treated as the color value for the addressed byte in planes 0-3. All eight pixels in the addressed byte are modified unless protected by the Bit Mask register setting. A logical 1 in the Bit Mask register sets the corresponding pixel in the addressed byte to the color specified on the data bus. A 0 in the Bit Mask register sets the corresponding pixel in the addressed byte to the corresponding pixel in the processor latches. The Set/Reset and Enable Set/Reset registers are ignored. The Function Select bits in the Data Rotate register are used.
1	1	**Write mode 3.** The CPU data is rotated then logically ANDed with the contents of the Bit Mask register (GR08) and then treated as the addressed data's bit mask, while the contents of the Set/Reset register is treated as the color value. A '0' on the data bus (mask) causes the corresponding pixel in the addressed byte to be set to the corresponding pixel in the processor latches. A '1' on the data bus (mask) causes the corresponding pixel in the addressed byte to be set to the color value specified in the Set/Reset register. The Enable Set/Reset register is ignored. The Data Rotate is used. This write mode can be used to fill an area with a single color and pattern.

2 Reserved (0)

3 Read Mode

0 The CPU reads data from one of the planes as selected in the Read Map Select register.

1 The CPU reads the 8-bit result of the logical comparison between all eight pixels in the four display planes and the contents of the Color Compare and Color Don't Care registers. The CPU reads a logical 1 if a match occurs for each pixel and logical 0 if a mis-match occurs. In 16-bit read cycles, this operation is repeated on the lower and upper bytes.

(Continued on following page)

4 Odd/Even Mode

0 All CPU addresses sequentially access all planes

1 Even CPU addresses access planes 0 and 2, while odd CPU addresses access planes 1 and 3. This option is useful for compatibility with the IBM CGA memory organization.

6-5 Shift Register Mode

These two bits select the data shift pattern used when passing data from the four memory planes through the four video shift registers. If data bits 0-7 in memory planes 0-3 are represented as M0D0-M0D7, M1D0-M1D7, M2D0-M2D7, and M3D0-M3D7 respectively, then the data in the serial shift registers is shifted out as follows:

65	Last Bit Shifted Out			Shift Direction →				1st Bit Shifted Out	Output to:
00:	M0D0	M0D1	M0D2	M0D3	M0D4	M0D5	M0D6	M0D7	Bit 0
	M1D0	M1D1	M1D2	M1D3	M1D4	M1D5	M1D6	M1D7	Bit 1
	M2D0	M2D1	M2D2	M2D3	M2D4	M2D5	M2D6	M2D7	Bit 2
	M3D0	M3D1	M3D2	M3D3	M3D4	M3D5	M3D6	M3D7	Bit 3
01:	M1D0	M1D2	M1D4	M1D6	M0D0	M0D2	M0D4	M0D6	Bit 0
	M1D1	M1D3	M1D5	M1D7	M0D1	M0D3	M0D5	M0D7	Bit 1
	M3D0	M3D2	M3D4	M3D6	M2D0	M2D2	M2D4	M2D6	Bit 2
	M3D1	M3D3	M3D5	M3D7	M2D1	M2D3	M2D5	M2D7	Bit 3
1x:	M3D0	M3D4	M2D0	M2D4	M1D0	M1D4	M0D0	M0D4	Bit 0
	M3D1	M3D5	M2D1	M2D5	M1D1	M1D5	M0D1	M0D5	Bit 1
	M3D2	M2D6	M3D2	M2D6	M1D2	M1D6	M0D2	M0D6	Bit 2
	M3D3	M3D7	M2D3	M2D7	M1D3	M1D7	M0D3	M0D7	Bit 3

Note: If the Shift Register is not loaded every character clock (see SR01 bits 2&4) then the four 8-bit shift registers are effectively 'chained' with the output of shift register 1 becoming the input to shift register 0 and so on. This allows one to have a large monochrome (or 4 color) bit map and display one portion thereof.

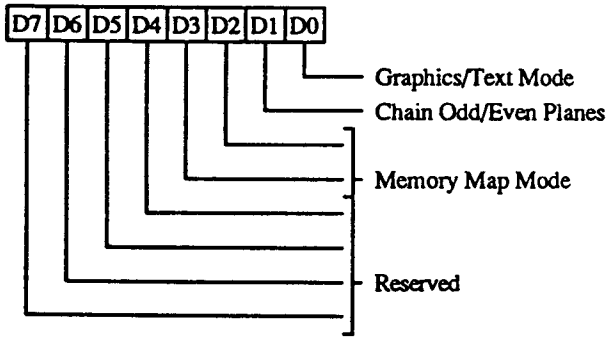
Note: If XR28 bit-4 is set (8-bit video path), GR05 bit-6 must be set to 0:

0x and XR28 bit-4=1:					
	M3D0	M2D0	M1D0	M0D0	Bit 0
	M3D1	M2D1	M1D1	M0D1	Bit 1
	M3D2	M2D2	M1D2	M0D2	Bit 2
	M3D3	M2D3	M1D3	M0D3	Bit 3
	M3D4	M2D4	M1D4	M0D4	Bit 4
	M3D5	M2D5	M1D5	M0D5	Bit 5
	M3D6	M2D6	M1D6	M0D6	Bit 6
	M3D7	M2D7	M1D7	M0D7	Bit 7

7 Reserved (0)

MISCELLANEOUS REGISTER (GR06)

Read/Write at I/O Address 3CFh
Index 06h
Group 1 Protection



0 Graphics/Text Mode

0 Text Mode
1 Graphics mode

1 Chain Odd/Even Planes

This mode can be used to double the address space into display memory.

1 CPU address bit A0 is replaced by a higher order address bit. The state of A0 determines which memory plane is to be selected:

A0 = 0: select planes 0 and 2
A0 = 1: select planes 1 and 3

0 A0 not replaced

3-2 Memory Map Mode

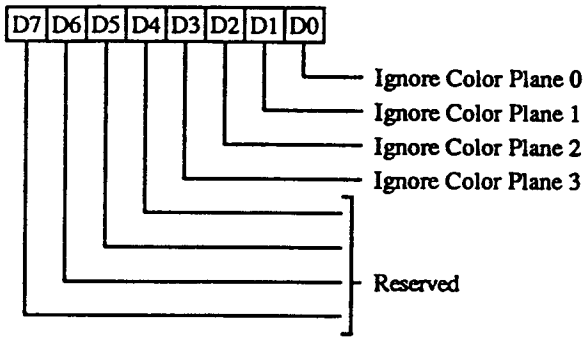
These bits control the mapping of the display memory into the CPU address space as follows (also used in extended modes):

Bit 3	Bit 2	CPU Address
0	0	A0000h-BFFFFh
0	1	A0000h-AFFFFh
1	0	B0000h-B7FFFh
1	1	B8000h-BFFFFh

7-4 Reserved (0)

COLOR DON'T CARE REGISTER (GR07)

Read/Write at I/O Address 3CFh
Index 07h
Group 1 Protection



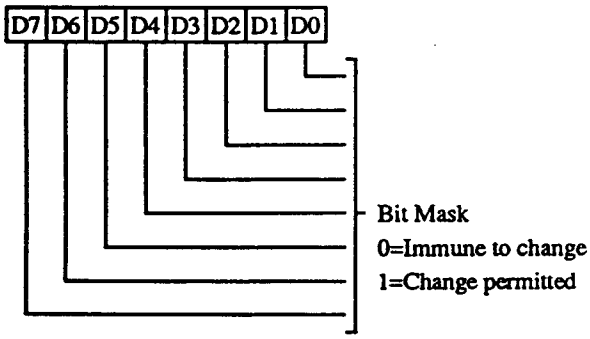
3-0 Ignore Color Plane (3-0)

0 This causes the corresponding bit of the Color Compare register to be a don't care during a comparison.

1 The corresponding bit of the Color Compare register is enabled for color comparison. This register is active in Read Mode 1 only.

7-4 Reserved (0)

BIT MASK REGISTER (GR08)
Read/Write at I/O Address 3CFh
Index 08h
Group 1 Protection



7-0 Bit Mask

This bit mask is applicable to any data written by the CPU, including that subject to a rotate, logical function (AND, OR, XOR), Set/Reset, and No Change. In order to execute a proper read-modify-write cycle into displayed memory, each byte must first be read (and latched by the VGA), the Bit Mask register set, and the new data then written. The bit mask applies to all four planes simultaneously.

0 The corresponding bit in each of the four memory planes is written from the corresponding bit in the latches

1 Unrestricted manipulation of the corresponding data bit in each of the four memory planes is permitted

—This Page Intentionally Left Blank—

Attribute Controller and VGA Color Palette Registers

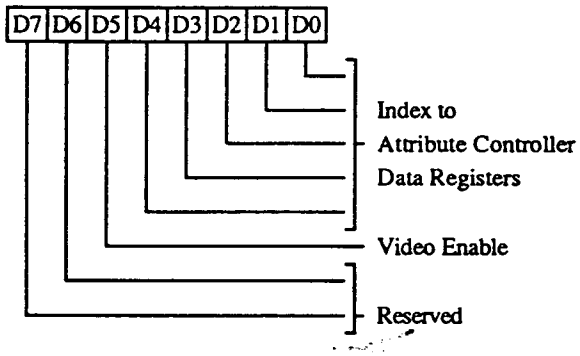
Register Mnemonic	Register Name	Index	Access	I/O Address	Protect Group	Page
ARX	Attribute Index (for 3C0/3C1h)	–	RW	3C0h	1	71
AR00-AR0F	Attribute Controller Color Data	00-0Fh	RW	3C0h/3C1h	1	72
AR10	Mode Control	10h	RW	3C0h/3C1h	1	72
AR11	Overscan Color	11h	RW	3C0h/3C1h	1	73
AR12	Color Plane Enable	12h	RW	3C0h/3C1h	1	73
AR13	Horizontal Pixel Panning	13h	RW	3C0h/3C1h	1	74
AR14	Pixel Pad	14h	RW	3C0h/3C1h	1	74
DACMASK	Color Palette Pixel Mask	–	RW	3C6h	6	75
DACSTATE	Color Palette State	–	R	3C7h	–	75
DACRX	Color Palette Read-Mode Index	–	W	3C7h	6	76
DACX	Color Palette Index (for 3C9h)	–	RW	3C8h	6	76
DACDATA	Color Palette Data	00-FFh	RW	3C9h	6	76

In regular VGA mode, all Attribute Controller registers are located at the same byte address (3C0h) in the CPU I/O space. An internal flip-flop controls the selection of either the Attribute Index or Data Registers. To select the Index Register, an I/O Read is executed to address 3BAh/3DAh to clear this flip-flop. After the Index Register has been loaded by an I/O Write to address 3C0h, this flip-flop toggles, and the Data Register is ready to be accessed. Every I/O Write to address 3C0h toggles this flip-flop. The flip-flop does not have any effect on the reading of the Attribute Controller registers. The Attribute Controller index register is always read back at address 3C0h, the data register is always read back at address 3C1h.

In one of the extended modes (See "CPU Interface Register"), the Attribute Controller Index register is located at address 3C0h and the Attribute Controller Data register is located at address 3C1h (to allow word I/O accesses). In another extended mode, the Attribute Controller can be both read and written at either 3C0h or 3C1h (EGA compatible mode).

The VGA color palette logic is used to further modify the video color output following the attribute controller color registers. The color palette logic is contained on-chip, however an external color palette chip may still be used by disabling the internal color palette (see XR06). DAC logic is provided on-chip (or in the external 'RAMDAC' chip if used) to convert the final video output of the color palette to analog RGB outputs for use in driving a CRT display.

ATTRIBUTE INDEX REGISTER (ARX)
Read/Write at I/O Address 3C0h
Group 1 Protection



4-0 Attribute Controller Index

These bits point to one of the internal registers of the Attribute Controller.

5 Enable Video

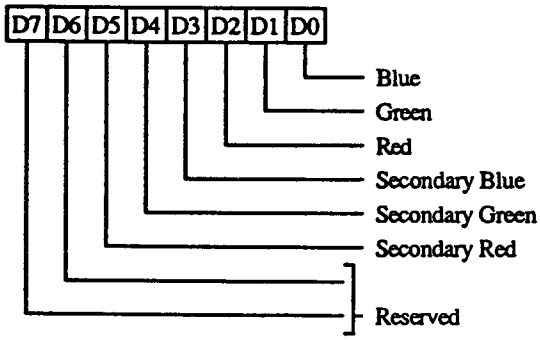
0 Disable video, allowing the Attribute Controller Color registers to be accessed by the CPU

1 Enable video, causing the Attribute Controller Color registers (AR00-AR0F) to be inaccessible to the CPU

7-6 Reserved (0)

ATTRIBUTE CONTROLLER COLOR REGISTERS (AR00-AR0F)

Read at I/O Address 3C1h
Write at I/O Address 3C0/1h
Index 00-0Fh
Group 1 Protection or XR63 bit-6



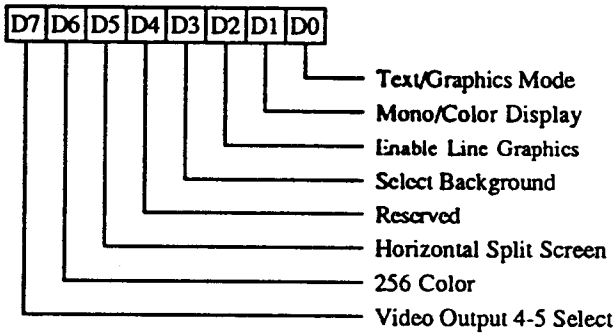
5-0 Color Value

These bits are the color value in the respective attribute controller color register as pointed to by the attribute index register.

7-6 Reserved (0)

ATTRIBUTE CONTROLLER MODE CONTROL REGISTER (AR10)

Read at I/O Address 3C1h
Write at I/O Address 3C0/1h
Index 10h
Group 1 Protection



0 Text/Graphics Mode

- 0 Select text mode
- 1 Select graphics mode

1 Monochrome/Color Display

- 0 Select color display attributes
- 1 Select mono display attributes

2 Enable Line Graphics Character Codes

This bit is dependent on bit 0 of the Override register.

- 0 Make the ninth pixel appear the same as the background
- 1 For special line graphics character codes (0C0h-0DFh), make the ninth pixel identical to the eighth pixel of the character. For other characters, the ninth pixel is the same as the background.

3 Enable Blink/Select Background Intensity

The blinking counter is clocked by the VSYNC signal. The Blink frequency is defined in the Blink Rate Control Register (XR60).

- 0 Disable Blinking and enable text mode background intensity
- 1 Enable the blink attribute in text and graphics modes.

4 Reserved (0)

5 Split Screen Horizontal Panning Mode

- 0 Scroll both screens horizontally as specified in the Pixel Panning register
- 1 Scroll horizontally only the top screen as specified in the Pixel panning register

6 256 Color Output Assembler

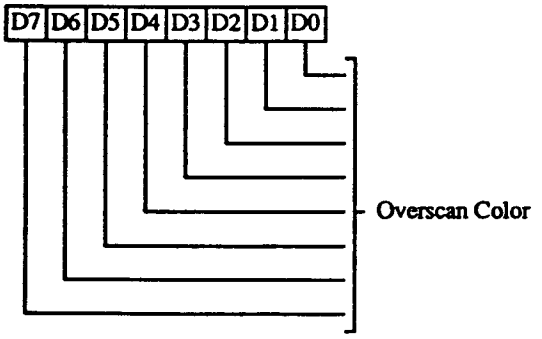
- 0 6-bits of video (translated from 4-bits by the internal color palette) are output every dot clock
- 1 Two 4-bit sets of video data are assembled to generate 8-bit video data at half the frequency of the internal dot clock (256 color mode).

7 Video Output 5-4 Select

- 0 Video bits 4 and 5 are generated by the internal Attribute Controller color palette registers
- 1 Video bits 4 and 5 are the same as bits 0 and 1 in the Pixel Pad register (AR14)

OVERSCAN COLOR REGISTER (AR11)

Read at I/O Address 3C1h
Write at I/O Address 3C0/1h
Index 11H
Group 1 Protection



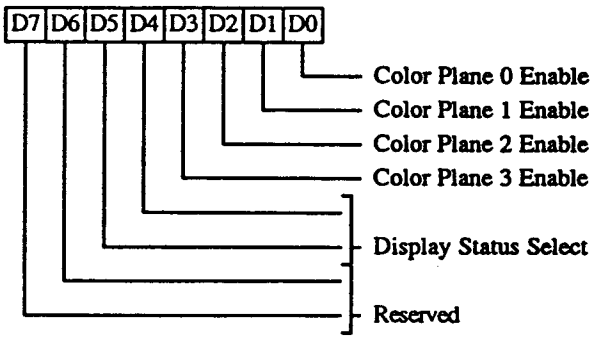
7-0 Overscan Color

These 8 bits define the overscan (border) color value. For monochrome displays, these bits should be zero.

The border color is displayed in the interval after Display Enable End and before Blank Start (end of display area; i.e. right side and bottom of screen) and between Blank End and Display Enable Start (beginning of display area; i.e. left side and top of screen).

COLOR PLANE ENABLE REGISTER (AR12)

Read at I/O Address 3C1h
Write at I/O Address 3C0/1h
Index 12h
Group 1 Protection



3-0 Color Plane (3-0) Enable

0 Force the corresponding color plane pixel bit to 0 before it addresses the color palette

1 Enable the plane data bit of the corresponding color plane to pass

5-4 Display Status Select

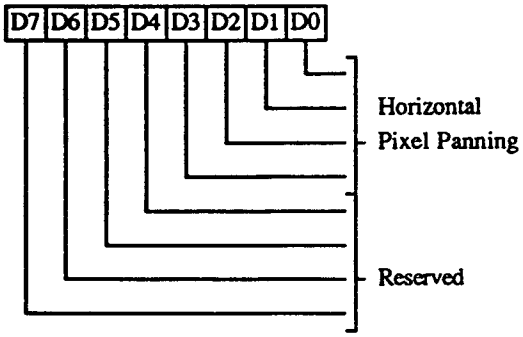
These bits select two of the eight color outputs to be read back in the Input Status Register 1 (port 3BAh or 3DAh). The output color combinations available on the status bits are as follows:

		Status Register 1	
Bit 5	Bit 4	Bit 5	Bit 4
0	0	P2	P0
0	1	P5	P4
1	0	P3	P1
1	1	P7	P6

7-6 Reserved (0)

ATTRIBUTE CONTROLLER HORIZONTAL PIXEL PANNING REGISTER (AR13)

Read at I/O Address 3C1h
Write At I/O Address 3C0/1h
Index 13h
Group 1 Protection



3-0 Horizontal Pixel Panning

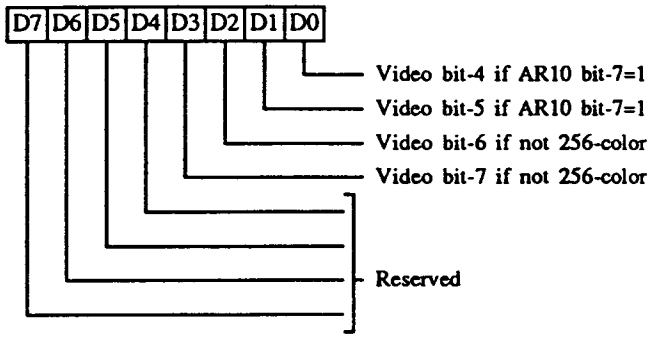
These bits select the number of pixels to shift the display horizontally to the left. Pixel panning is available in both text and graphics modes. In 9 pixel/character text mode, the output can be shifted a maximum of 9 pixels. In 8 pixel/character text mode and all graphics modes a maximum shift of 8 pixels is possible. In 256-color mode (output assembler AR10 bit-6 = 1), bit 0 of this register must be 0 which results in only 4 panning positions per display byte. In Shift Load 2 and Shift Load 4 modes, register CR08 provides single pixel resolution for panning. Panning is controlled as follows:

	Number of Pixels Shifted		
AR13	9-dot mode	8-dot mode	256-color mode
0	1	0	0
1	2	1	--
2	3	2	1
3	4	3	--
4	5	4	2
5	6	5	--
6	7	6	3
7	8	7	--
8	0	--	--

7-4 Reserved (0)

ATTRIBUTE CONTROLLER PIXEL PAD REGISTER (AR14)

Read at I/O Address 3C1h
Write At I/O Address 3C0/1h
Index 14h
Group 1 Protection



1-0 Video Bits 5-4

These bits are output as video bits 5 and 4 when AR10 bit-7 = 1. They are disabled in the 256 color mode.

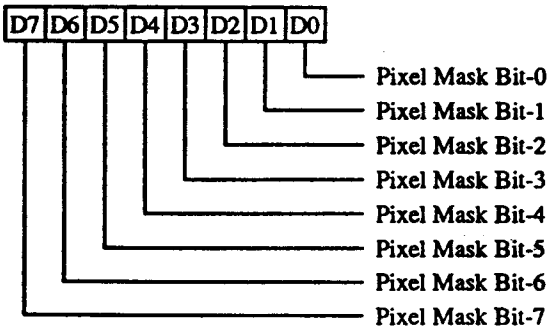
3-2 Video Bits 7-6

These bits are output as video bits 7 and 6 in all modes except 256-color mode.

7-4 Reserved (0)

COLOR PALETTE PIXEL MASK REGISTER (DACMASK)

Read/Write at I/O Address 3C6h
Group 6 Protection

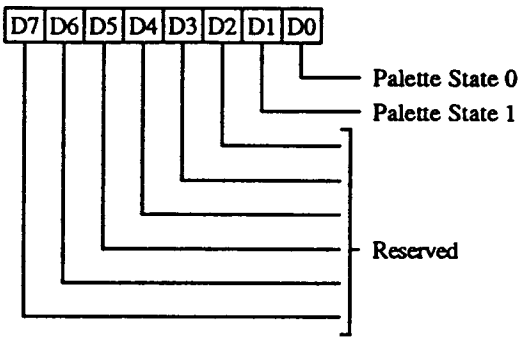


The contents of this register are logically ANDed with the 8 bits of video data coming into the color palette. Zero bits in this register therefore cause the corresponding address input to the color palette to be zero. For example, if this register is programmed with 7, only color palette registers 0-7 would be accessible; video output bits 3-7 would be ignored and all color values would map into the lower 8 locations in the color palette.

This register is physically located on-chip (the chip will respond directly if the internal color palette is enabled). This register is also implemented in external color palette chips (RAMDACs) and the external copy will be used if an external RAMDAC is used instead (the on-chip mask register will be ignored if the internal color palette is disabled). Reads from this I/O location cause the PALRD/ pin to be asserted if the internal color palette is disabled. Writes to this I/O location cause the PALWR/ pin to be asserted if the internal color palette is disabled. If the internal color palette is disabled, the functionality of this port is therefore determined by the external palette chip.

COLOR PALETTE STATE REGISTER (DACSTATE)

Read only at I/O Address 3C7h



1-0 Palette State 1-0

Status bits indicate the I/O address of the last CPU write to the Color Palette:

00 The last write was to 3C8h (write mode)

11 The last write was to 3C7h (read mode)

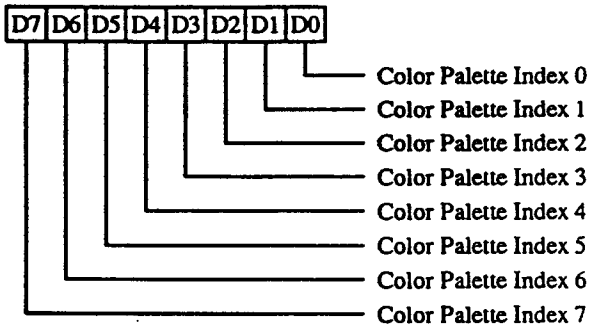
7-2 Reserved (0)

To allow saving and restoring the state of the video subsystem, this register is required since the color palette index register is automatically incremented differently depending on whether the index is written at 3C7h or 3C8h.

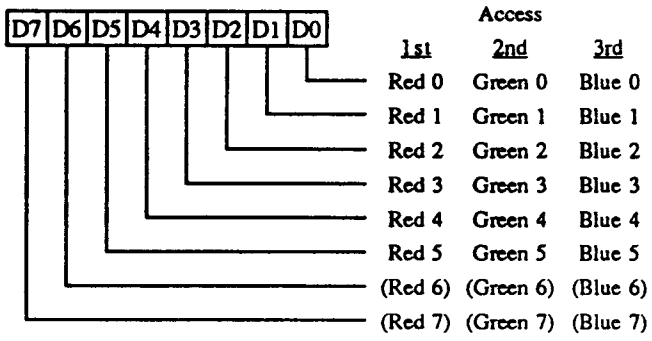
This register is physically located on-chip (PALRD/ is *not* asserted for reads from this I/O address independent of whether the internal palette is enabled or disabled).

COLOR PALETTE
READ-MODE INDEX REGISTER (DACRX)
Write only at I/O Address 3C7h
Group 6 Protection

COLOR PALETTE
INDEX REGISTER (DACX)
Read/Write at I/O Address 3C8h
Group 6 Protection



COLOR PALETTE
DATA REGISTERS (DACDATA 00-FF)
Read/Write at I/O Address 3C9h
Index 00h-FFh
Group 6 Protection



The color palette index and data registers are physically located on-chip and in the external color palette chip if one is used. Which set of registers is used depends on whether the on-chip color palette is enabled. If the on-chip palette is enabled, PALRD/ and PALWR/ are never active. If the on-chip color palette is disabled, PALRD/ and PALWR/ are active on I/O reads and writes respectively to enable the external palette chip.

In either case, the index register is used to point to one of 256 data registers. Each data register is either 18 or 24 bits in length depending on the type of palette chip used (6 or 8 bits each for red, green, and blue), so the data values must be read as a sequence of 3 bytes. After writing the index register (3C7h or 3C8h), data values may be read from or written to the color palette data register port (3C9h) in sequence: first red, then green, then blue, then repeat for the next location if desired (the index is incremented automatically by the palette logic).

The index may be written at 3C7h and may be read or written at 3C8h. When the index value is written to either port, it is written to both the index register and a 'save' register. The save register (not the index register) is used by the palette logic to point at the current data register. When the index value is written to 3C7h (**read mode**), it is written to both the index register and the save register, then the index register is automatically incremented. When the index value is written to 3C8h (**write mode**), the automatic incrementing of the index register does not occur.

After the third of the three sequential data reads from (or writes to) 3C9h is completed, the save and index registers are both automatically incremented by the palette logic. This allows the entire palette (or any subset) to be read (written) by writing the index of the first color in the set, then sequentially reading (writing) the values for each color, without having to reload the index every three bytes.

The state of the RGB sequence is not saved; the user must access each three bytes in an uninterruptable sequence (or be assured that interrupt service routines will not access the palette index or data registers). When the index register is written (at either port), the RGB sequence is restarted. Data value reads and writes may be intermixed; either reads or writes increment the palette logic's RGB sequence counter.

The palette's save register always contains a value one less than the readable index value if the last index write was to the 'read mode' port. The state is saved for which port (3C7h or 3C8h) was last written and that information is returned on reads from 3C7h (PALRD/ is only asserted on reads from 3C8h and not on reads from 3C7h if the internal palette is disabled). Writes to 3C7h or 3C8h cause the PALWR/ pin to be asserted if the on-chip palette is disabled.

If the on-chip color palette is disabled, the functionality of the index and data ports is determined by the external palette chip.

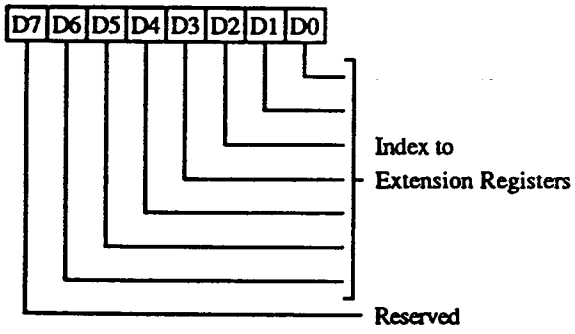
Extension Registers

Register Mnemonic	Register Group	Extension Register Name	Index	I/O Access	Address	State After Reset	Page
XRX	–	Extension Index	–	RW	3D6h	-xxxxxxx	78
XR00	Misc	Chip Version (65520: v=7, 65530: v=8)	00h	RO	3D7h	vvvvrrrr	78
XR01	Misc	Configuration	01h	RO	3D7h	dddddddd	79
XR02	Misc	CPU Interface	02h	RW	3D7h	00000000	80
XR04	Misc	Memory Control	04h	RW	3D7h	00000000	80
XR06	Misc	Color Palette Control	06h	RW	3D7h	00000000	81
XR0D	Misc	Auxiliary Offset	0Dh	RW	3D7h	------00	83
XR0E	Misc	Text Mode Control	0Eh	RW	3D7h	----00--	83
XR0F	Misc	Software Flags 2	0Fh	R/W	3D7h	xxxxxxxx	83
XR28	Misc	Video Interface	28h	RW	3D7h	00000000	92
XR2B	Misc	Default Video	2Bh	RW	3D7h	00000000	93
XR44	Misc	Software Flags	44h	RW	3D7h	xxxxxxxx	95
XR70	Misc	Setup / Disable Control	70h	RW	3D7h	0-------	113
XR7F	Misc	Diagnostic	7Fh	RW	3D7h	00xxxx00	113
XR0B	Mapping	CPU Paging	0Bh	RW	3D7h	---00000	82
XR0C	Mapping	Start Address Top	0Ch	RW	3D7h	------00	82
XR10	Mapping	Single/Low Map	10h	RW	3D7h	xxxxxxxx	84
XR11	Mapping	High Map	11h	RW	3D7h	xxxxxxxx	84
XR14	Compatibility	Emulation Mode	14h	RW	3D7h	0000hh00	85
XR15	Compatibility	Write Protect	15h	RW	3D7h	00000000	86
XR1F	Compatibility	Virtual EGA Switch	1Fh	RW	3D7h	0---xxxx	40
XR7E	Compatibility	CGA/Hercules Color Select	7Eh	RW	3D7h	--xxxxxx	114
XR18	Alternate	Alternate Horizontal Display End	18h	RW	3D7h	xxxxxxxx	87
XR19	Alternate	Alt H Sync Start / Half Line Compare	19h	RW	3D7h	xxxxxxxx	87
XR1A	Alternate	Alternate Horizontal Sync End	1Ah	RW	3D7h	xxxxxxxx	88
XR1B	Alternate	Alternate Horizontal Total	1Bh	RW	3D7h	xxxxxxxx	88
XR1C	Alternate	Alternate H Blank Start / H Panel Size	1Ch	RW	3D7h	xxxxxxxx	89
XR1D	Alternate	Alternate Horizontal Blank End	1Dh	RW	3D7h	0xxxxxxx	89
XR1E	Alternate	Alternate Offset	1Eh	RW	3D7h	xxxxxxxx	90
XR24	Flat Panel	Alternate Maximum Scan Line	24h	RW	3D7h	---xxxxx	91
XR25	Flat Panel	Alternate Text Mode H Virtual Panel Size	25h	RW	3D7h	xxxxxxxx	91
XR2C	Flat Panel	Vertical Sync (FLM) Delay	2Ch	RW	3D7h	xxxxxxxx	93
XR2D	Flat Panel	Horizontal Sync (LP) Delay	2Dh	RW	3D7h	xxxxxxxx	94
XR2E	Flat Panel	Horizontal Sync (LP) Delay	2Eh	RW	3D7h	xxxxxxxx	94
XR2F	Flat Panel	Horizontal Sync (LP) Width	2Fh	RW	3D7h	xxxxxxxx	95
XR50	Flat Panel	Panel Format	50h	RW	3D7h	xxxxxxxx	96
XR51	Flat Panel	Display Type	51h	RW	3D7h	xxxxx0xx	97
XR52	Flat Panel	Power Down Control	52h	RW	3D7h	00000000	98
XR53	Flat Panel	Line Graphics Override	53h	RW	3D7h	x-xxxxx0	99
XR54	Flat Panel	Panel Interface	54h	RW	3D7h	xxxxxxxx	100
XR55	Flat Panel	Horizontal Compensation	55h	RW	3D7h	xxxx--xx	101
XR56	Flat Panel	Horizontal Centering	56h	RW	3D7h	xxxxxxxx	102
XR57	Flat Panel	Vertical Compensation	57h	RW	3D7h	-xxxxxxx	103
XR58	Flat Panel	Vertical Centering	58h	RW	3D7h	xxxxxxxx	104
XR59	Flat Panel	Vertical Line Insertion	59h	RW	3D7h	-xx-xxxx	104
XR5A	Flat Panel	Vertical Line Replication	5Ah	RW	3D7h	----xxxx	105
XR5B	Flat Panel	Panel Power Sequencing Delay (65530)	5Bh	RW	3D7h	01110001	105
XR5E	Flat Panel	ACDCLK Control	5Eh	RW	3D7h	xxxxxxxx	105
XR5F	Flat Panel	Power Down Mode Refresh	5Fh	RW	3D7h	xxxxxxxx	106
XR60	Flat Panel	Blink Rate Control	60h	RW	3D7h	10000011	106
XR61	Flat Panel	SmartMap™ Control	61h	RW	3D7h	xxxxxxxx	107
XR62	Flat Panel	SmartMap™ Shift Parameter	62h	RW	3D7h	xxxxxxxx	108
XR63	Flat Panel	SmartMap™ Color Mapping Control	63h	RW	3D7h	x-xxxxxx	108
XR64	Flat Panel	Alternate Vertical Total	64h	RW	3D7h	xxxxxxxx	109
XR65	Flat Panel	Alternate Overflow	65h	RW	3D7h	xxx--xxx	109
XR66	Flat Panel	Alternate Vertical Sync Start	66h	RW	3D7h	xxxxxxxx	110
XR67	Flat Panel	Alternate Vertical Sync End	67h	RW	3D7h	----xxxx	110
XR68	Flat Panel	Vertical Panel Size	68h	RW	3D7h	xxxxxxxx	111
XR6C	Flat Panel	Programmable Output Drive (65530)	6Ch	RW	3D7h	00000000	111
XR6E	Flat Panel	Polynomial FRC Control	6Eh	RW	3D7h	10111101	111
XR6F	Flat Panel	Frame Buffer Control	6Fh	RW	3D7h	--xxx000	112
XR7D	Flat Panel	Compensation Diagnostic	7Dh	RO	3D7h	--------	113

Reset Codes: x = Not changed by RESET (indeterminate on power-up)
d = Set from the corresponding data bus pin on falling edge of RESET
h = Read-only Hercules Configuration Register Readback bits
– = Not implemented (always reads 0)
r = Chip revision # (starting from 0000)
0/1 = Reset to 0 or 1 by falling edge of RESET

EXTENSION INDEX REGISTER (XRX)

Read/Write at I/O Address 3B6h/3D6h

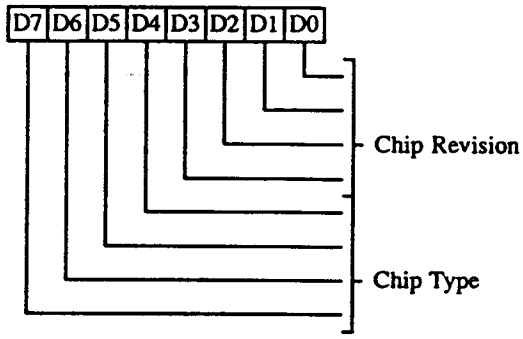


6-0 Index value used to access the extension registers

7 Reserved (0)

CHIPS VERSION REGISTER (XR00)

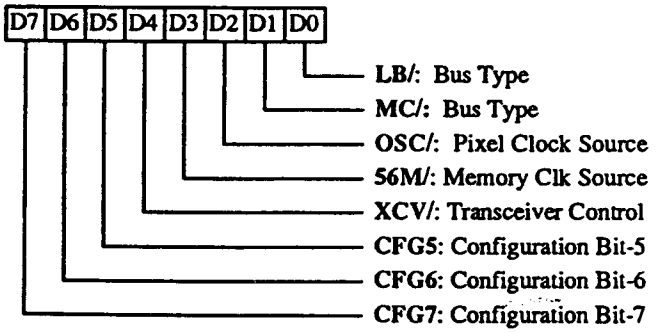
Read only at I/O Address 3B7h/3D7h
Index 00h



7-0 **Chip Version** - Chip Versions start at 70h in the 65520 and 80h in the 65530 and are incremented for every silicon step.

CONFIGURATION REGISTER (XR01)

Read only at I/O Address 3B7h/3D7h
Index 01h



These bits latch the state of memory address bus A (AA bus) bits 0-7 on the falling edge of RESET. The state of bits 0-4 after RESET effect chip internal logic as indicated below; bits 5-7 have no hardware effect on the chip. AA0-4 have on-chip high-value pullups, but AA5-7 do not; therefore, the state of bits 5-7 after RESET will be indeterminate if no external pullup or pulldown resistors are present.

This register is not related to the Virtual EGA Switch register (XR1F).

1-0 CPU Bus Type

00 PI bus
01 MC bus
10 Local Bus (65530 only)
11 ISA bus

2 Pixel Clock Source (OSC/)

0 Oscillator Configuration:
CLK0-CLK3 are pixel clock inputs
CLK0 or CLK1 pin is MCLK input

1 Clock Chip Configuration:
CLK0 pin is MCLK input
CLK1 pin is pixel clock input
CLK2 pin is CLKSEL0 output
CLK3 pin is CLKSEL1 output

Note: Actual pixel clock frequencies generated (and how the CLKSEL1-0 outputs are driven) is determined by Miscellaneous Output register bits 3-2 and by Feature Control Register bits 1-0 in CRT mode and by Flat Panel Interface Register (XR54) bits 5-2 in flat panel mode.

3 Memory Clock Source (56M/)

0 MCLK = 56.644 MHz (80ns RAMs)
If bit-2=0 (oscillators):
CLK0=50.350 MHz
CLK1=56.644 MHz (MCLK src)
CLK2=40.000 MHz
CLK3=44.900 MHz
If bit-2=1 (clock chip):
MCLK (CLK0)=56.644 MHz
Clock Select 0=40.000 MHz
Clock Select 1=50.350 MHz
Clock Select 2=User-defined
Clock Select 3=44.900MHz

1 MCLK = 50.350 MHz (100ns RAMs)
If bit-2=0 (oscillators):
CLK0=50.350 MHz (MCLK src)
CLK1=28.322 MHz
CLK2=40.000 MHz
CLK3=44.900 MHz
If bit-2=1 (clock chip):
MCLK (CLK0)=50.350 MHz
Clock Select 0=40.000 MHz
Clock Select 1=28.322 MHz
Clock Select 2=User-defined
Clock Select 3=44.900 MHz

4 Transceiver Control

0 External transceivers
(pin 69 is VGARD output)
1 No external transceivers
(pin 69 is ENAVEE/ output)

7-5 Configuration bits 7-5 (CFG7-5)

Latched from AA7-5 on the falling edge (end) of RESET and readable, but otherwise have no hardware effect. State after RESET will be unknown unless external pullup or pulldown resisters are used.

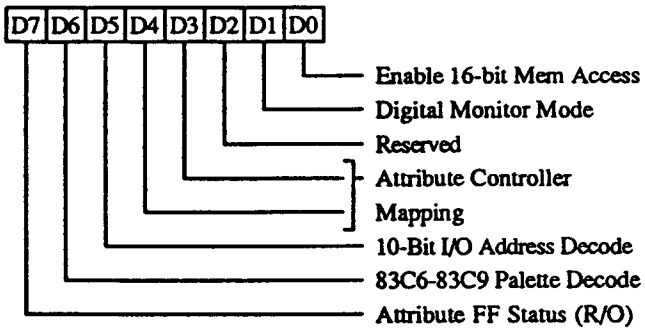
Pixel Clock Frequency Generation

XR02 Bit-1	XR54 3:2 or MSR 3:2	XR54 5:4 or FCR 1:0	OSC/ = 0 (Oscillators) 56M/ = 0 (Mclk=56.644) Pclk Freq (Clk Selected)	OSC/ = 0 (Oscillators) 56M/ = 1 (Mclk=50.350) Pclk Freq (Clk Selected)	OSC/ = 1 (Clock Chip)† 56M/=0 (Mclk=CLK0=56.644) Pclk Freq (Clkin=CLK1)	OSC/ = 1 (Clock Chip)† 56M/=1 (Mclk=CLK0=50.350) Pclk Freq (Clkin=CLK1)
0	00	xx	25.175 MHz (CLK0+2)	25.175 MHz (CLK0+2)	25.175 MHz (Clkin+2,Sel=01)	25.175 MHz (MCLK+2)
0	01	xx	28.322 MHz (CLK1+2)	28.322 MHz (CLK1)	28.322 MHz (MCLK+2)	28.322 MHz (Clkin,Sel=01)
x	1x	00	40.000 MHz (CLK2)	40.000 MHz (CLK2)	40.000 MHz (Clkin,Sel=00)	40.000 MHz (Clkin,Sel=00)
x	1x	01	50.350 MHz (CLK1)	28.322 MHz (CLK1)	50.350 MHz (Clkin,Sel=01)	28.322 MHz (Clkin,Sel=01)
x	1x	10	56.644 MHz (CLK0)†††	50.350 MHz (CLK0)†††	User-defined (Clkin,Sel=10)††	User-defined (Clkin,Sel=10)††
x	1x	11	44.900 MHz (CLK3)	44.900 MHz (CLK3)	44.900 MHz (Clkin,Sel=11)	44.900 MHz (Clkin,Sel=11)
1	00	xx	14.161 MHz (CLK1+4)	14.161 MHz (CLK1+2)	14.161 MHz (MCLK+4)	14.161 MHz (Clkin+2,Sel=01)
1	01	xx	16.783 MHz (CLK0+3)	16.783 MHz (CLK0+3)	16.783 MHz (Clkin+3,Sel=01)	16.783 MHz (MCLK+3)

† Alternatively, an external clock multiplexer may be used to select between multiple discrete oscillators of the frequencies listed
†† One additional user-defined frequency is available by using the clock chip option (more using the 82C404 programmable clock).
††† Pixel clock frequencies ≥ MCLK are generally not useful (no memory bandwidth is available for CPU accesses to display memory).

CPU INTERFACE REGISTER (XR02)

Read/Write at I/O Address 3B7h/3D7h
Index 02h



0 8/16-bit CPU Memory Access
- 0 8-bit CPU memory access (default)
- 1 16-bit CPU memory access

1 Digital Monitor Clock Mode
- 0 Normal (clk 0-1=25,28 MHz) (default)
- 1 Digital Monitor (clk 0-1=14,16MHz) 14MHz = 56MHz ÷ 4 or 28MHz ÷ 2 16MHz = 50MHz ÷ 3

2 Reserved

4-3 Attribute Controller Mapping
- 00 Write Index and Data at 3C0h. (8-bit access only) (default - VGA mapping)
- 01 Write Index at 3C0h and Data at 3C1h (8-bit or 16-bit access). Attribute flip-flop (bit-7) is always reset in this mode (16-bit mapping)
- 10 Write Index and Data at 3C0h/3C1h (8-bit access only) (EGA mapping)
- 11 Reserved

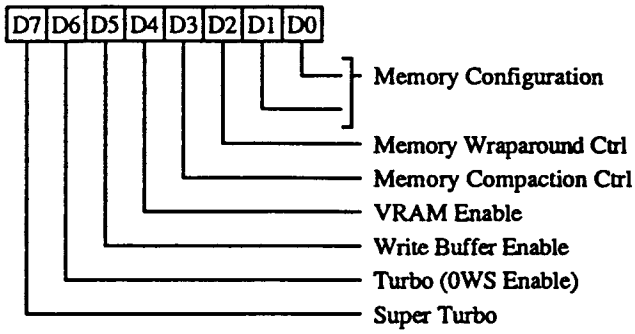
5 I/O Address Decoding
- 0 Decode all 16 bits of I/O address (default)
- 1 Decode only lower 10 bits of I/O address. This affects the following addresses: 3B4h, 3B5h, 3B8h, 3BAh, 3BFh, 3C0h, 3C1h, 3C2h, 3C4h, 3C5h, 3CEh, 3CFh, 3D4h, 3D5h, 3D8h, 3D9h, and 3DAh.

6 Palette Address Decoding
- 0 External palette registers can be accessed only at 3C6h-3C9h (default)
- 1 External palette registers can be accessed at both 3C6h-3C9h and 83C6h-83C9h (for Brooktree-type palette chips)

7 Attribute Flip-flop Status (read only)
0 = Index, 1 = Data

MEMORY CONTROL REGISTER (XR04)

Read/Write at I/O Address 3B7h/3D7h
Index 04h



1-0 Memory Configuration

	Data Path	# of Chips	Config	RAM Type	Total Memory
00	8-bit	2	256Kx4	D/V	0.25MB
01	16-bit	4	256Kx4	D/V	0.50MB
10	Reserved for future use				
11	16-bit	2	512Kx8	D	1MB

2 Memory Wraparound Control

This bit enables bit-17 of the CRT Controller address counter (default = 0 on reset).
- 0 Disable CRTC address counter bit-17
- 1 Enable CRTC address counter bit-17

3 Memory Compaction Control (VRAM only)
- 0 VGA-Compatible Memory Mapping
- 1 Compact memory maps in 256-color and text modes

4 Enable VRAM Interface
- 0 Use DRAM interface (default)
- 1 Use VRAM interface

5 CPU Memory Write Buffer
- 0 Disable CPU memory write buffer (default)
- 1 Enable CPU memory write buffer

6 Turbo (0WS Enable)

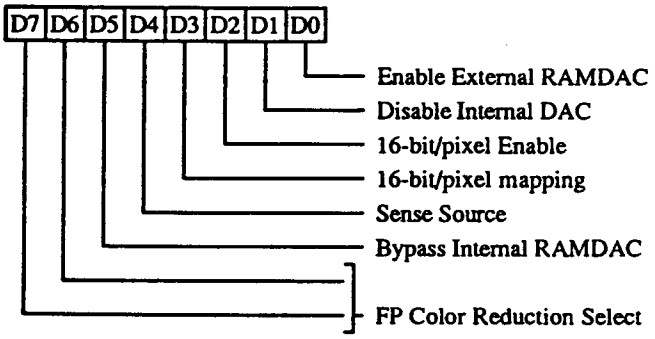
This bit may be set to enable 0WS capability

7 Super-Turbo (Faster 0WS Cycle Enable)

This bit may be set to allow faster 0WS cycle timing. This may not work on all systems.

PALETTE CONTROL REGISTER (XR06)

Read/Write at I/O Address 3B7h/3D7h
Index 06h



0 Enable External RAMDAC

This bit affects CPU I/O addresses 3C6h-3C9h (and I/O addresses 83C6h-83C9h if XR02 bit-6 = 1).

Note: CPU writes to these addresses will always go to internal RAMDAC.

0 Enable internal RAMDAC (default on Reset). PALRD/ and PALWR/ will not be generated.
1 Enable CPU read/write to external RAMDAC if XR6F bit-0 = 0 (external Frame Buffer disabled). If XR6F bit-0 = 1, this bit will be ignored.

1 Disable Internal DAC

This bit affects the DAC analog outputs.

0 Enable internal DAC (default on Reset). DAC analog outputs (R, G, B) will be active. Default on reset.
1 Disable internal DAC. The DAC analog outputs (R, G, B) will be 3-stated. Setting this bit forces power down of the internal DAC.

2 16-Bit Color Mapping Enable

0 Video output is 8-bit/pixel using the RAMDAC color palette (default on Reset)
1 Video output is 16-bit/pixel (bypass color palette portion of RAMDAC)

This bit is effective for both internal and external RAMDAC modes (but the implementation is different). When using an external palette, setting this bit causes the PCLK output to be Sierra RAMDAC compatible by effectively dividing the PCLK output by two. This is used to output one 16-bit pixel per PCLK cycle by outputting 8 bits on the rising edge and the other 8 bits on the falling edge.

3 16-Bit Color Mapping

0 Map 16-bit/pixel modes as 5-5-5 for Sierra RAMDAC compatibility (default on reset)
1 Map 16-bit/pixel modes as 5-6-5 for XGA compatibility

This bit has no effect if the external RAMDAC is selected.

4 Sense Source

0 The sense status bit (3C2 bit-4) is driven by the internal sense circuit (default on Reset)
1 The sense status bit (3C2 bit-4) is driven by the SENSE pin from external logic. (Setting this bit powers off the internal sense circuit).

5 Bypass Internal RAMDAC (Test Mode only)

This is a test bit and should not be set. This feature is necessary for testing the FRC logic.

0 Use internal RAMDAC. RAMDAC palette output consists of 6 bits/pixel. Default on reset.
1 Bypass internal RAMDAC. The input to the FRC logic consists of the least significant 6 bits of the 8-bit CRT video data.

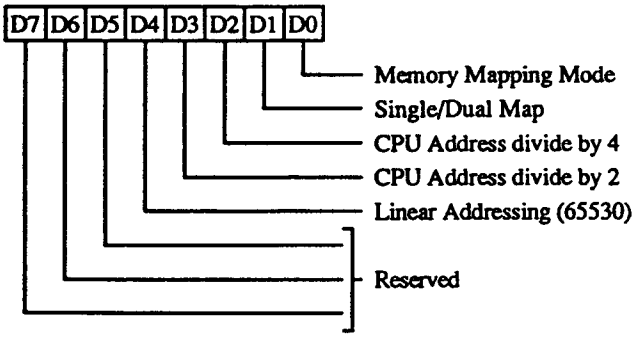
7-6 Color Reduction Select

These bits are effective in flat panel mode. These bits select the algorithm used to reduce 18-bit palette color data to 6-bit color data for monochrome panels.

00 NTSC weighting algorithm (default)
01 Equivalent weighting algorithm
10 Green only
11 Color

CPU PAGING REGISTER (XR0B)

Read/Write at I/O Address 3B7h/3D7h
Index 0Bh



0 Memory Mapping Mode

- 0 Normal Mode (VGA compatible) (default on Reset)
- 1 Extended Mode (mapping for > 256 KByte memory configurations)

1 CPU Single/Dual Mapping

- 0 CPU uses only a single map to access the extended video memory space (default on Reset)
- 1 CPU uses two maps to access the extended video memory space. The base addresses for the two maps are defined in the Low Map Register (XR10) and High Map Register (XR11).

2 CPU address Divide by 4

- 0 Disable divide by 4 for CPU addresses (default on Reset)
- 1 Enable divide by 4 for CPU addresses. This allows the video memory to be accessed sequentially in mode 13. In addition, all video memory is available in mode 13 by setting this bit.

3 CPU Address Divide by 2

- 0 Disable divide by 2 for CPU address (default on Reset)
- 1 Enable divide by 2 for CPU addresses

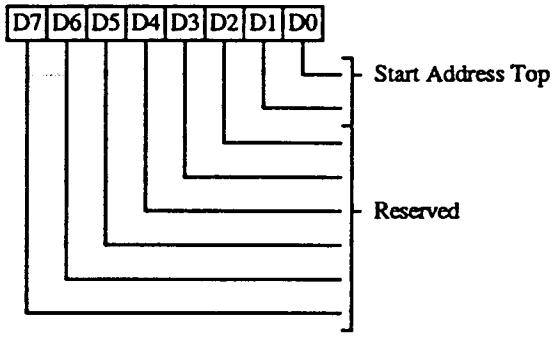
4 Linear Addressing (65530 only)

- 0 Standard VGA (A0000 - BFFFF) memory space decoded on-chip using A17-19 (default on Reset)
- 1 Linear Addressing (1MB using A0-19)

7-5 Reserved (0)

START ADDRESS TOP REGISTER (XR0C)

Read/Write at I/O Address 3B7h/3D7h
Index 0Ch



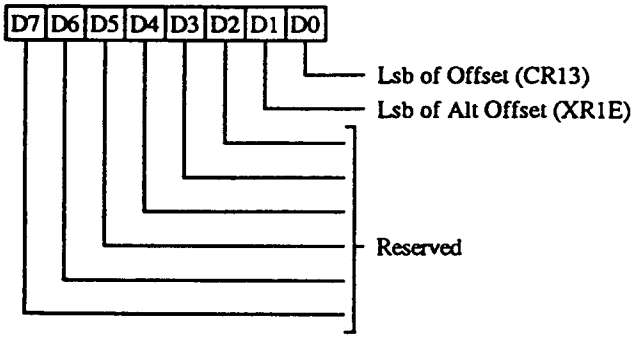
0-1 Start Address Top

These bits defines the high order bits for the Display Start Address when 512 KBytes or more of memory is used (see XR04 bits 1–0).

7-2 Reserved (0)

AUXILIARY OFFSET REGISTER (XR0D)

Read/Write at I/O Address 3B7h/3D7h
Index 0Dh



0 Offset Register LSB

This bit provides finer granularity to the display memory address offset when word and doubleword modes are used. This bit is used with the regular Offset register (CR13).

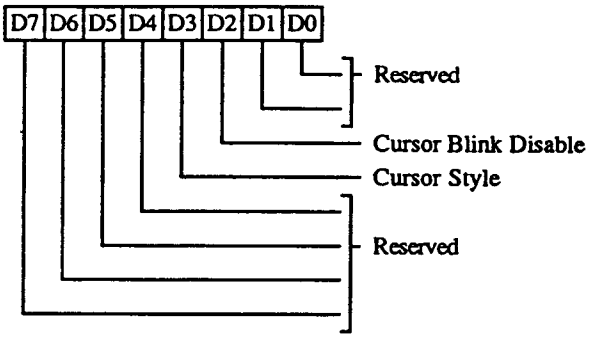
1 Alternate Offset Register LSB

This bit provides finer granularity to the display memory address offset when word and doubleword modes are used. This bit is used with the Alternate Offset register (XR1E).

7-2 Reserved (0)

TEXT MODE CONTROL REGISTER (XR0E)

Read/Write at I/O Address 3B7h/3D7h
Index 0Eh



This register is effective for both CRT and flat panel text modes.

1-0 Reserved (0)

2 Cursor Mode

0 Blinking (default on Reset).
1 Non-blinking

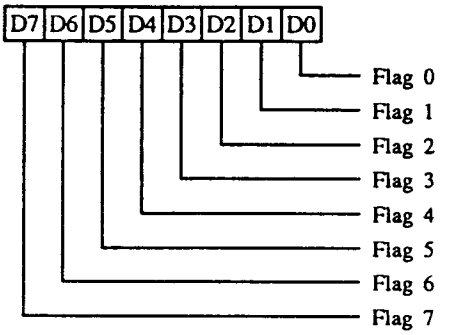
3 Cursor Style

0 Replace (default on Reset)
1 Exclusive-Or

7-4 Reserved (0)

SOFTWARE FLAGS REGISTER #2 (XR0F)

Read/Write at I/O Address 3B7h/3D7h
Index 0Fh



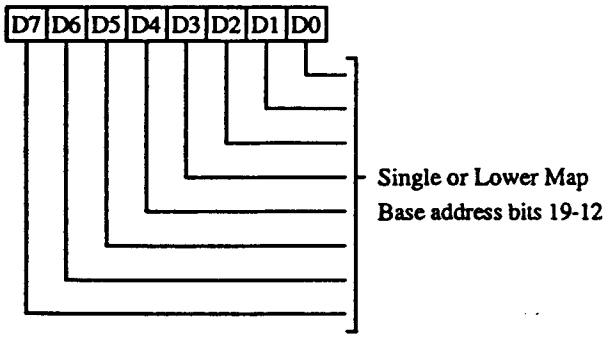
This register contains eight read-write bits which have no internal hardware function. All bits are reserved for use by BIOS and driver software.

7-0 Flags

(See also XR44)

SINGLE/LOW MAP REGISTER (XR10)

Read/Write at I/O Address 3B7h/3D7h
Index 10h



This register effects CPU memory address mapping.

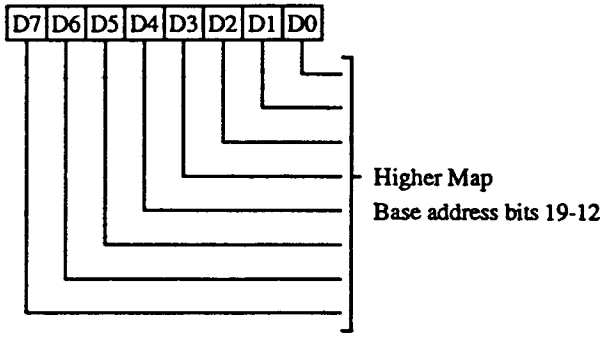
7-0 Single / Low Map Base Address Bits 17-10

These bits define the base address in single map mode (XR0B bit-1 = 0), or the lower map base address in dual map mode (XR0B bit-1 = 1). The memory map starts on a 1K boundary in planar modes and on a 4K boundary in packed pixel modes. In case of dual mapping, this register controls the CPU window into display memory based on the contents of GR06 bits 3-2 as follows:

GR06 Bits 3-2	Low Map	
00	A0000-AFFFF	
01	A0000-A7FFF	
10	B0000-B7FFF	Single mapping only
11	B8000-BFFFF	Single mapping only

HIGH MAP REGISTER (XR11)

Read/Write at I/O Address 3B7h/3D7h
Index 11h



This register effects CPU memory address mapping.

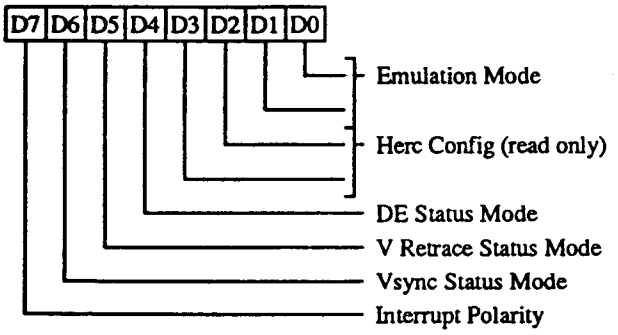
7-0 High Map Base Address Bits 17-10

These bits define the Higher Map base address in dual map modes (XR0B bit-1=1). The memory map starts on a 1K boundary in planar modes and on a 4K boundary in packed pixel modes. This register controls the CPU window into display memory based on the contents of GR06 bits 3-2 as follows:

GR06 bits 3-2	High Map
00	B0000-BFFFF
01	A8000-AFFFF
10	Don't care
11	Don't care

EMULATION MODE REGISTER (XR14)

Read/Write at I/O Address 3B7h/3D7h
Index 14h



1-0 Emulation Mode

00 VGA mode (default on Reset)
01 CGA mode
10 MDA/Hercules mode
11 EGA mode

3-2 Hercules Configuration Register (3BFh) readback (read only)

4 Display Enable Status Mode

0 Select Display Enable status to appear at bit 0 of Input Status register 1 (I/O Address 3BAh/3DAh) (default on reset). Normally used for CGA, EGA, and VGA modes.

1 Select Hsync status to appear at bit 0 of Input Status register 1 (I/O Address 3BAh/3DAh). Normally used for MDA / Hercules mode.

5 Vertical Retrace Status Mode

0 Select Vertical Retrace status to appear at bit 3 of Input Status register 1 (I/O Address 3BAh/3DAh) (default on Reset). Normally used for CGA, EGA, and VGA modes.
1 Select Video to appear at bit 3 of Input Status register 1 (I/O Address 3BAh/3DAh). Normally used for MDA / Hercules mode.

6 VSync Status Mode

0 Prevent Vsync status from appearing at bit 7 of Input Status Register 1 (I/O Address 3BAh/3DAh). Normally used for CGA, EGA, and VGA modes.
1 Enable Vsync status to appear as bit-7 of Input Status Register 1 (I/O Address 3BAh/3DAh). Normally used for MDA/Hercules mode.

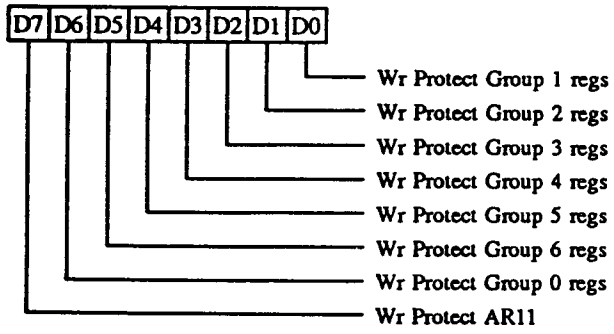
7 Interrupt Output Function

This bit controls the function of the interrupt output pin (IRQ):

Interrupt State	bit-7=0 PC Bus	bit-7=0 MC Bus	bit-7=1 Either Bus
Disabled	3-state	3-state	3-state
Enabled, Inactive	3-state	3-state	Low
Enabled, Active	3-state	Low	High

WRITE PROTECT REGISTER (XR15)

Read/Write at I/O Address 3B7h/3D7h
Index 15h



This register controls write protection for various groups of registers as shown. 0 = unprotected (default on Reset), 1= protected.

0 Write Protect Group 1 Registers

This bit affects the Sequencer registers (SR00-04), Graphics Controller registers (GR00-08), and Attribute Controller registers (AR00-14).

Note that AR11 is also protected by bit-7 which is ORed with this bit.

1 Write Protect Group 2 Registers

This bit affects CR09 bits 0-4, CR0A, and CR0B.

2 Write Protect Group 3 Registers

This bit affects CR07 bit-4, CR08, CR11 bits 5-4, CR13, CR14, CR17 bits 0-1 and bits 3-7, and CR18.

3 Write Protect Group 4 Registers

This bit affects CR09 bits 5-7, CR10, CR11 bits 0-3 and bits 6-7, CR12, CR15, CR16, and CR17 bit-2.

4 Write Protect Group 5 Registers

This bit affects the Miscellaneous Output register (3C2h) and the Feature Control register (3BAh/3DAh).

5 Write Protect Group 6 Registers

This bit affects the RAMDAC registers (3C6h-3C9h). If this bit is set, PALRD/ and PALWR/ are disabled and all internal DAC registers are also write protected.

6 Write Protect Group 0 Registers

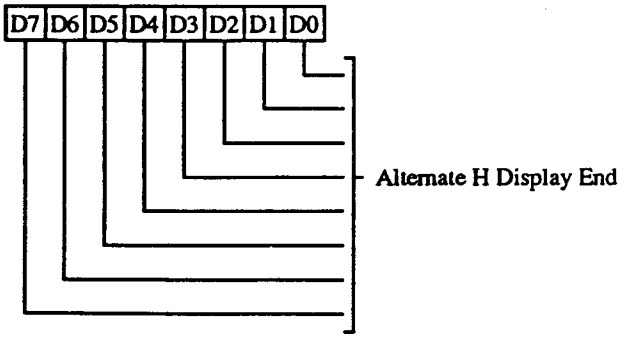
This bit affects CR0-7 (except CR07 bit-4). This bit is logically ORed with CR11 bit-7.

7 Write Protect AR11

This bit is ORed with bit-0, therefore writing to AR11 is possible only if both bit-0 and bit-7 are 0.

ALTERNATE HORIZONTAL DISPLAY END REGISTER (XR18)

Read/Write at I/O Address 3B7h/3D7h
Index 18h



This register is used in flat panel and CRT CGA text and graphics modes, and Hercules graphics mode.

7-0 Alternate Horizontal Display End

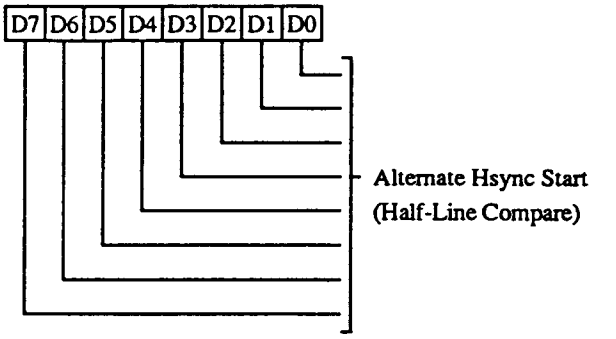
This register specifies the number of characters displayed per scan line, similar to CR01.

Programmed Value = Actual Value – 1

Note: This register is used in emulation modes only. It is not used in CRT or flat panel VGA modes.

ALTERNATE HORIZONTAL SYNC START / HALF LINE COMPARE REGISTER (XR19)

Read/Write at I/O Address 3B7h/3D7h
Index 19h



This register is used in all flat panel modes with horizontal compression disabled, to set the horizontal sync start. This register is also used in CRT CGA text and graphics modes, and Hercules graphics mode.

Alternately, in the Interlaced mode of CRT operation, this register is used to generate the Half Line Compare Signal.

7-0 FP Alternate Horizontal Sync Start

These bits specifiy the begining of the Hsync in terms of character clocks from the begining of the display scan. Similar to CR04.

Programmed Value = Actual Value – 1

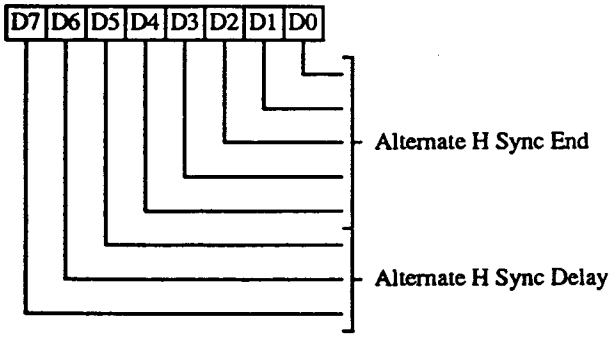
or

7-0 CRT Half-line Value

In CRT interlaced video mode this value is used to generate the 'half-line compare' signal that controls the positioning of the VSync for odd frames.

ALTERNATE HORIZONTAL SYNC END REGISTER (XR1A)

Read/Write at I/O Address 3B7h/3D7h
Index 1Ah



This register is used in all flat panel modes with horizontal compression disabled, CRT CGA text and graphics modes, and Hercules graphics mode.

4-0 Alternate Horizontal Sync End

Lower 5 bits of the character clock count which specifies the end of horizontal sync. Similar to CR05. If the horizontal sync width desired is N clocks, then programmed value is:

(N + Contents of XR19) ANDed with 01F Hex

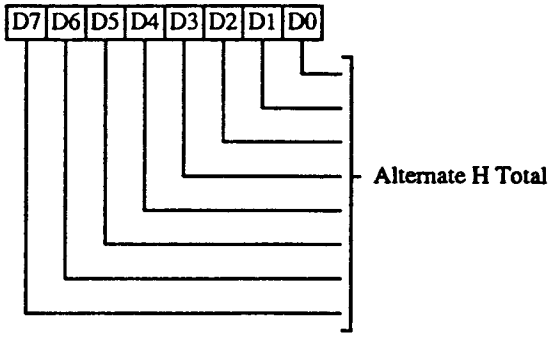
7-5 CRT Alternate Horizontal Sync Delay

See CR05 for description

FP Reserved

ALTERNATE HORIZONTAL TOTAL REGISTER (XR1B)

Read/Write at I/O Address 3B7h/3D7h
Index 1Bh



This register is used in all flat panel modes with horizontal compression disabled, CRT CGA text and graphics modes, and Hercules graphics mode.

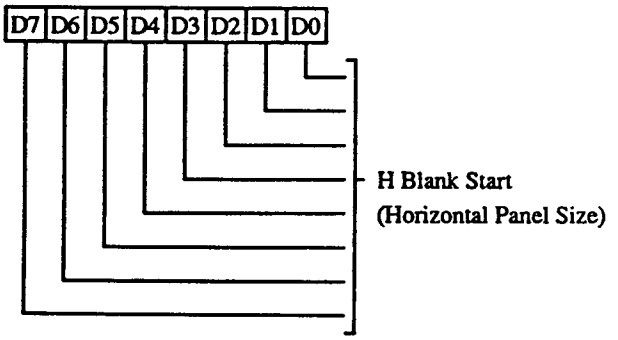
7-0 Alternate Horizontal Total

This register contents are the total number of character clocks per line. Similar to CR00.

Programmed Value = Actual Value – 5

ALTERNATE HORIZONTAL BLANK START / HORIZONTAL PANEL SIZE REGISTER (XR1C)

Read/Write at I/O Address 3B7h/3D7h
Index 1Ch



The value in this register is the Horizontal Panel Size in all Flat Panel Modes. In CRT mode, it is used for CGA text and graphics and Hercules graphics modes.

7-0 FP Horizontal Panel Size

Horizontal panel size is programmed in terms of number of 8-bit (graphics/text) or 9-bit (text) characters. For double drive flat panels the actual horizontal panel size must be a multiple of two character clocks.

Programmed Value = Actual Value – 1

or

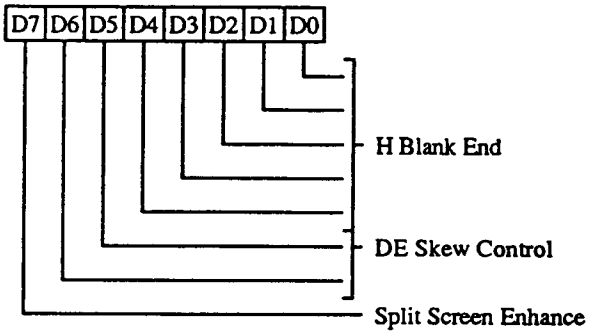
7-0 CRT Alternate Horizontal Blank Start

See CR02 for description

Programmed Value = Actual Value – 1

ALTERNATE HORIZONTAL BLANK END REGISTER (XR1D)

Read/Write at I/O Address 3B7h/3D7h
Index 1Dh



Bits 0-6 of this register are used in CRT CGA text and graphics modes and CRT Hercules graphics mode. Bit 7 of this register is used for all CRT and flat panel modes.

4-0 CRT Alternate Horizontal Blank Start

See CR03 for description

6-5 CRT Alternate Display Enable Skew Control

See CR03 for description

7 Line Compare Fix

This bit affects all CRT and FP text modes. This bit is 0 on reset.

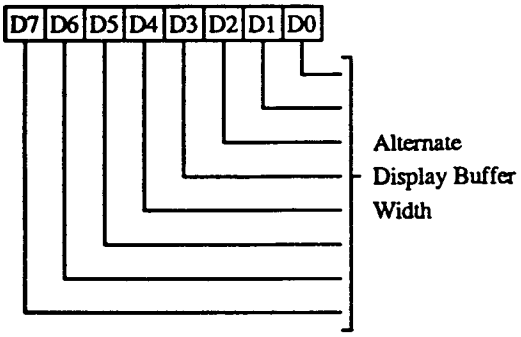
0 Internal Line Compare (split screen) flag is not delayed so that the Vertical Row Counter is reset too early which in text mode causes the first scanline of the first character row following split screen to be skipped (not displayed). This is IBM VGA compatible.

1 Internal Line Compare (split screen) flag is delayed so that the Vertical Row Counter is reset properly which in text mode causes the first scanline of the first character row following split screen to be displayed.

Note: This register is used in emulation modes only. It is not used in CRT or flat panel VGA modes.

ALTERNATE OFFSET REGISTER (XR1E)

Read/Write at I/O Address 3B7h/3D7h
Index 1Eh



This register is used in all flat panel modes, CRT CGA text and graphics modes and Hercules graphics mode.

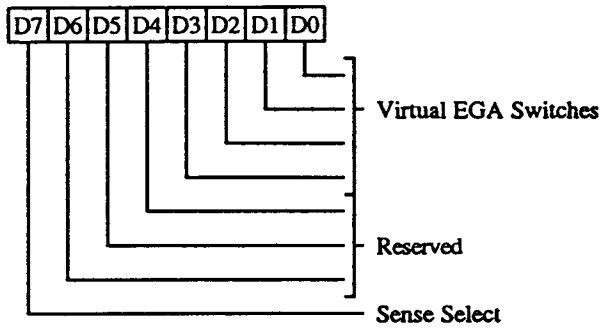
7-0 Alternate Offset

See CR13 for description

Programmed Value = Actual Value – 1

VIRTUAL EGA SWITCH REGISTER (XR1F)

Read/Write at I/O Address 3B7h/3D7h
Index 1Fh



3-0 Virtual Switch Register

If bit-7 is '1', then one of these four bits is read back in Input Status Register 0 (3C2h) bit 4. The selected bit is determined by Miscellaneous Output Register (3C2h) bits 3-2 as follows:

Misc 3-2	XR1F Bit Selected
00	bit-3
01	bit-2
10	bit-1
11	bit-0

6-4 Reserved (0)

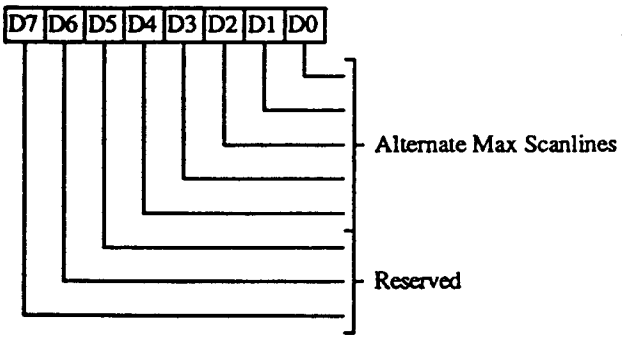
7 Sense Select

0 Select the SENSE pin for readback in Input Status Register 0 bit-4 (default on Reset).

1 Select one of bits 3-0 for readback in Input Status Register 0 bit-4.

ALTERNATE MAXIMUM SCANLINE REGISTER (XR24)

Read/Write at I/O Address 3B7h/3D7h
Index 24h



This register is used in flat panel text mode when TallFont is enabled during vertical compensation.

4-0 Alternate Maximum Scanlines (AMS)

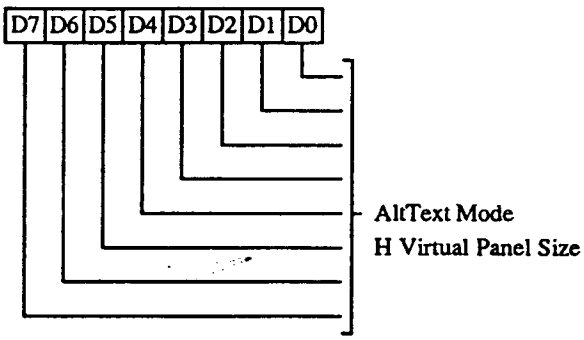
Programmed Value = number of scanlines minus one per character row of TallFont

Double scanned lines, inserted lines, and replicated lines are not counted.

7-5 Reserved (0)

FP ALTERNATE TEXT MODE HORIZONTAL VIRTUAL PANEL SIZE REGISTER (XR25)

Read/Write at I/O Address 3B7h/3D7h
Index 25h



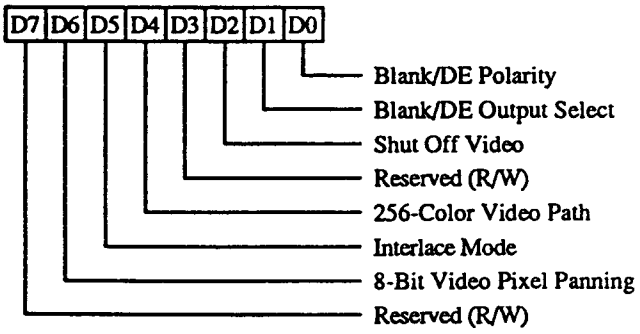
This register is used in flat panel 9-dot text modes.

7-0 FP Alternate Text Mode Horizontal Virtual Panel Size

Programmed Value = 9/8 [XR1C + 1] – 1

VIDEO INTERFACE REGISTER (XR28)

Read/Write at I/O Address 3B7h/3D7h
Index 28h



0 Blank / Display Enable Polarity

This bit is effective in CRT mode only. In flat panel mode, XR54 bit-0 controls the polarity of the BLANK/ pin.

0 Negative polarity (default on Reset)
1 Positive polarity

1 Blank / Display Enable Select

This bit is effective in CRT mode only. In flat panel mode, XR54 bit-1 controls BLANK/ pin functionality.

0 BLANK/ pin outputs BLANK/ (default on reset)
1 BLANK/ pin outputs Display Enable

Note: The signal polarity selected by bit-0 is applicable for either selection.

2 Shut Off Video

This bit is effective in CRT and flat panel modes during horizontal / vertical blank time. This bit should be set properly when using CRT/FP displays which look at video signals during blank time. It has no effect on displays that ignore video signals during blank time. This bit is also ignored when the screen is blanked (see XR2B for conditions when the screen is blanked).

0 When the screen is not blanked, video is forced to the border / overscan color (AR11) during blank time (default on Reset)
1 When the screen is not blanked, video is forced to default video (XR2B) during blank time.

Note: In flat panel mode, video is forced to the border / overscan color (AR11) or to default video (XR2B) before the internal RAMDAC palette and before the FRC logic.

3 Reserved

This bit is implemented as a read/write bit but has no internal hardware function.

4 256-Color Video Path

This bit is effective for both CRT and flat panel when AR10 bit-6 = 1 (256-color mode).

0 4-bit video data path (default on reset)
1 8-bit video data path (horizontal pixel panning is controlled by bit-6)

Note: GR05 bit-5 must be 0 if this bit is set

5 Interlace Video

This bit is effective only for CRT graphics mode. This bit should be programmed to 0 for flat panel. In interlace mode XR19 holds the half-line positioning of VSync for odd frames.

0 Non-interlaced video (default on reset)
1 Interlaced video

6 8-Bit Video Pixel Panning

This bit is effective for both CRT and flat panel when the 8-bit video data path is selected (bit-4 = 1 and AR10 bit-6 = 1).

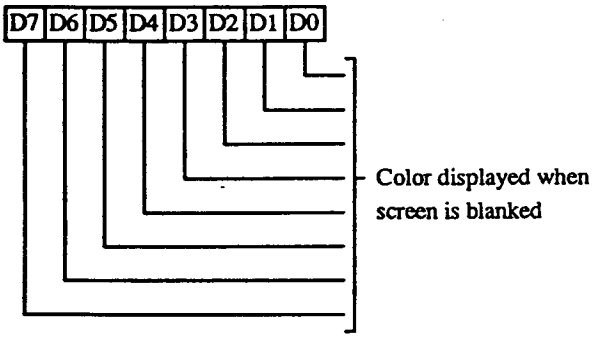
0 AR13 bits 2-1 are used to control pixel panning (default on Reset)
1 AR13 bits 2-0 are used to control pixel panning

7 Reserved

This bit is implemented as a read/write bit but has no internal hardware function.

DEFAULT VIDEO REGISTER (XR2B)

Read/Write at I/O Address 3B7h/3D7h
Index 2Bh



This register affects both CRT and flat panel modes when the screen is not blanked and XR28 bit-2 = 1. This register effects both CRT and flat panel when the screen is blanked independent of XR28 bit-2. Screen blank occurs when SR01 bit-5 is set in any emulation mode, or when bit-3 of the CGA / Hercules Mode Control Register (3B8h/3D8h) is reset in CGA / Hercules mode.

Note: For flat panel, video data output during screen blank is different than video data output during Panel Off power-saving mode. In Panel Off power-saving mode, video data is forced low or high or 3-stated (see XR52, XR61 bit-7, and XR63 bit-7). In Standby power saving mode, video data is 3-stated.

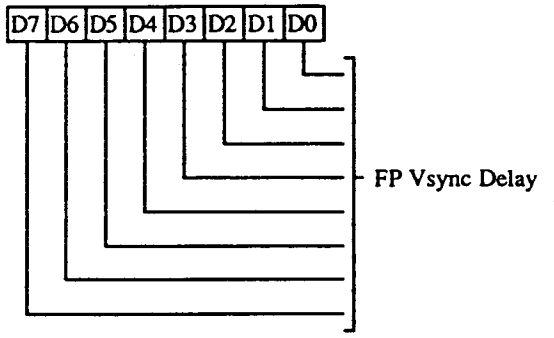
7-0 Default Video

When the screen is not blanked, these bits specify the color to be displayed during CRT/FP blank time when XR28 bit-2 = 1. When the screen is blanked, these bits specify the color to be displayed for both CRT and flat panel.

Note: In flat panel mode, video data is forced to default video before the internal RAMDAC palette and before the FRC logic.

FP VSYNC (FLM) DELAY REGISTER (XR2C)

Read/Write at I/O Address 3B7h/3D7h
Index 2Ch



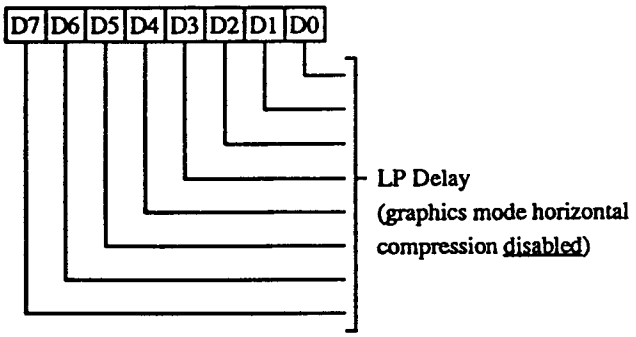
This register is used only in flat panel mode when XR2F bit-7=0. The First Line Marker (FLM) signal is generated from an internal FP Vsync active edge with a delay specified by this register. The FLM pulse width is always one line for SS panels and two lines for DS/DD panels.

7-0 FP VSync Delay (VDelay)

These bits define the number of Hsyncs between the internal Vsync and the rising edge of FLM.

FP HSYNC (LP) DELAY REGISTER (XR2D)

Read/Write at I/O Address 3B7h/3D7h
Index 2Dh



This register is used only in flat panel mode when XR2F bit-6 = 0 and graphics mode horizontal compression is disabled. The LP output is generated from the FP Blank inactive edge with a delay specified by XR2F bit-5 and the value in this register. The LP pulse width is specified in register XR2F.

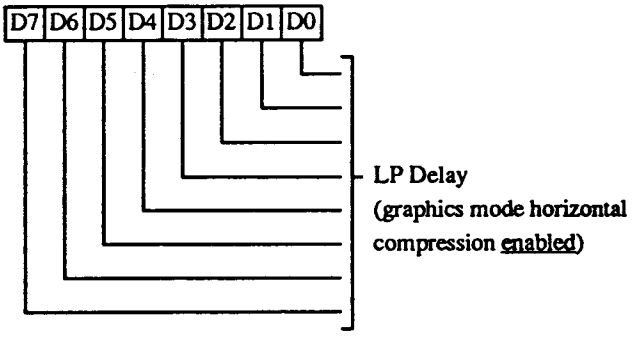
7-0 FP HSync (LP) Delay (HDelay)

These bits define the number of character clocks between the FP Blank inactive edge and the rising edge of the LP output in flat panel mode with graphics mode horizontal compression disabled. The msb (bit 8) of this parameter is XR2F bit-5.

Programmed Value = Actual Value – 1

FP HSYNC (LP) DELAY REGISTER (XR2E)

Read/Write at I/O Address 3B7h/3D7h
Index 2Eh



This register is used only in flat panel mode when XR2F bit-6 = 0 and 9-dot text mode is used. The LP output is generated from the FP Blank inactive edge with a delay specified by XR2F bit-4 and the value in this register. The LP pulse width is specified in register XR2F.

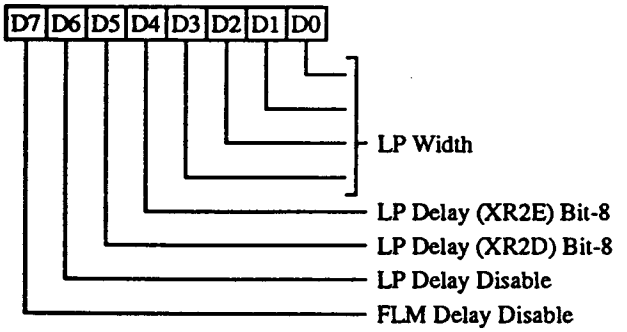
7-0 FP HSync (LP) Delay (HDelay)

These bits define the number of character clocks between the FP Blank inactive edge and the rising edge of the LP output in flat panel 9-dot text modes. The msb (bit 8) of this parameter is XR2F bit-4.

Programmed Value = Actual Value – 1

FP HSYNC (LP) WIDTH REGISTER (XR2F)

Read/Write at I/O Address 3B7h/3D7h
Index 2Fh



This register is used only in flat panel mode. This register together with XR2D or XR2E defines the LP output pulse in flat panel mode.

3-0 FP HSync (LP) Width (HWidth)

These bits define the width of LP output pulse in terms of number of character (8-dot only) clocks in flat panel mode.

Programmed Value = Actual Value – 1

4 FP HSync (LP) Delay (XR2E) Bit 8

This bit is the msb of the FP HSync (LP) Delay parameter for 9-dot text modes.

5 FP HSync (LP) Delay (XR2D) Bit 8

This bit is the msb of the FP HSync (LP) Delay parameter for graphics mode horizontal compression disabled.

6 FP HSync (LP) Delay Disable

0 FP HSync (LP) Delay Enable: XR2D and XR2F bit-5 (or XR2E and XR2F bit-4) are used to delay the FP HSync (LP) active edge with respect to the FP Blank inactive edge.

1 FP HSync (LP) Delay Disable: FP HSync (LP) active edge will coincide with the FP Blank inactive edge.

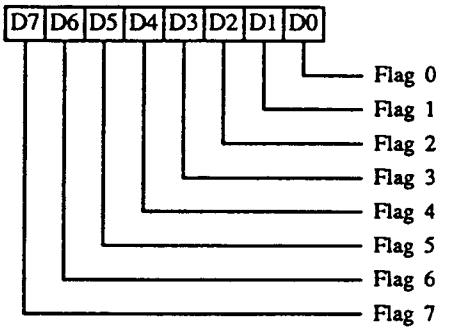
7 FP VSync (FLM) Delay Disable

0 FP VSync (FLM) Delay Enable: XR2C is used to delay the external FP VSync (FLM) active edge with respect to the internal FP VSync active edge.

1 FP VSync (FLM) Delay Disable: the external FP VSync (FLM) active edge will coincide with the internal FP VSync (FLM) active edge.

SOFTWARE FLAGS REGISTER (XR44)

Read/Write at I/O Address 3B7h/3D7h
Index 44h

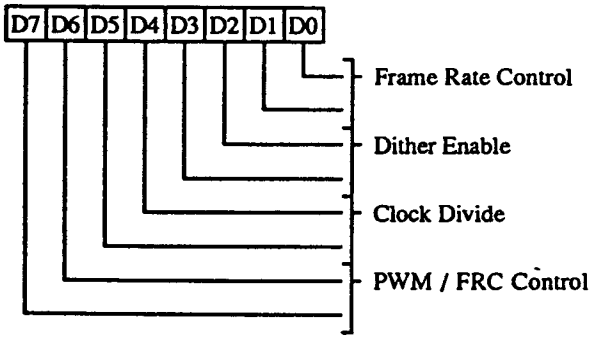


This register contains eight read-write bits which have no internal hardware function. All bits are reserved for use by BIOS and driver software.

7-0 Flags

(See also XR0F)

PANEL FORMAT REGISTER (XR50)
Read/Write at I/O Address 3B7h/3D7h
Index 50h



This register is used only in flat panel mode.

1-0 Frame Rate Control (FRC)

If bit-6 of this register is 0, these bits specify grayscale simulation on a frame by frame basis on monochrome flat panels that do not support gray levels internally.

00 8-frame FRC: 9-level grayscale simulation without dithering or 32-level grayscale simulation with dithering.
01 16-frame FRC: 16-level grayscale simulation with or without dithering.
10 4-frame FRC: 5-level grayscale simulation without dithering or 16-level grayscale simulation with dithering.
11 See description for bits 7-6.

3-2 Dither Enable

00 Disable dithering
01 Enable dithering only for 256-color mode (AR10 bit-6 = 1)
10 Enable dithering for all modes
11 Reserved

5-4 Clock Divide (CD)

These bits specify the frequency ratio between the dot clock and the flat panel shift clock (SHFCLK) signal.

00 Shift Clock Freq = Dot Clock Freq

This setting is used to output 1 pixel per shift clock with a maximum of 6 bpp (bits/pixel) for single drive monochrome panels and 4 bpp for single drive color panels. This setting cannot be used for double drive (DD) panels. FRC and Dithering can be enabled.

01 Shift Clk Freq = 1/2 Dot Clock Freq

This setting is used to output 2 pixels per shift clock with a maximum of 4 bpp (bits/pixel) for single drive monochrome panels and 2 bpp for single drive color panels. This setting can be used for color double drive (DD) panels in the 65530 (only) if the frame accelerator is not used (XR6F bit-1 = 0). FRC and dithering can be enabled.

10 Shift Clk Freq = 1/4 Dot Clock Freq

This setting is used to output 4 pixels per shift clock with a maximum of 2 bpp for single drive mono panels and is used to output 8 pixels per shift clock with 1 bpp for mono double drive (DD) panels if a frame accelerator is used (XR6F bit-1=1). FRC and dithering can be enabled.

11 Shift Clk Freq = 1/8 Dot Clock Freq

This setting is used to output 8 pixels per shift clock with a maximum of 1 bpp for single drive mono panels and is used to output 8 pixels per shift clock with 1 bpp for mono double drive (DD) panels if a frame accelerator is not used (XR6F bit-1=0). FRC and dithering can be enabled.

7-6 VAM / FRC Control

00 CD=00: 6 bpp VAM (dither bits 1,0)
CD=01: 4 bpp VAM (dither bits 1,0)
CD=10: 2 bpp VAM (dither bits 3,2)
CD=11: 1 bpp VAM (dither bits 5,4)

01 3 Bits/Pixel VAM (dither bits 2,1)
use only CD=00 & 01 for mono panels
use only CD=00 for color panels

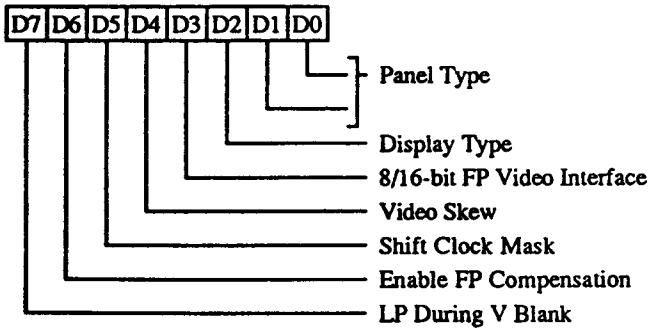
10 2-Frame FRC (65530 only)
3-level gray scale simulation without dithering or 9-level grayscale simulation with dithering (dither bits 3, 2)

11 3 Bits/Pixel VAM + 2-Frame FRC
15-level gray scale simulation without dithering and 56-level grayscale simulation with dithering (dither bits 1, 0). (65530 only)

Note: bit-7 of this register (and therefore selections 10 and 11 above) is not implemented in the 65520 (it is only implemented in the 65530). To use settings 10 and 11 above, the Polynomial FRC Control Register should be programmed to 0.

To use settings 01, 10, or 11 above, bits 1-0 of this register must be set to 11. In other words, if bits 1-0 are not 11 then bits 7-6 must be programmed to 00.

DISPLAY TYPE REGISTER (XR51)
Read/Write at I/O Address 3B7h/3D7h
Index 51h



1-0 Panel Type (PT)

These bits are effective for flat panel only.

00 Single Panel Single Drive (SS)
01 Reserved
10 Dual Panel Single Drive (DS)
11 Dual Panel Double Drive (DD)

2 Display Type (DT)

This bit is effective for CRT and flat panel. This bit also controls the BLANK/ pin.

0 CRT display (default on Reset) BLANK/ pin outputs CRT Blank
1 FP (Flat Panel) display BLANK/ pin outputs FP Blank

3 8/16-bit FP Video Interface

This bit is effective for flat panel only.

0 8-bit FP video interface
1 16-bit FP video interface

This feature provides support for panels with 16-bit interfaces with a minimum of additional external logic. In this mode, the Shift Clock is further divided by 2 and different video data is valid on the rising and falling edges of Shift Clock. The first 8 bits of video data can be latched into temporary external latches using the rising edge of Shift Clock; the content of this external latch and the second 8 bits of video data can then be latched into the panel using the falling edge of Shift Clock.

4 Video Skew

This bit affects both CRT and flat panel video.

0 No video data delay
1 Video data is delayed by 1 shift clock cycle

5 Shift Clock Mask (SM)

This bit is effective for flat panel only.

0 Allow shift clock output to toggle outside the display enable interval
1 Force the shift clock output low outside the display enable interval

6 Enable FP Compensation (EFCP)

This bit is effective for flat panel only. It enables flat panel horizontal and vertical compensation depending on panel size, current display mode, and contents of the compensation registers.

0 Disable FP compensation
1 Enable FP compensation

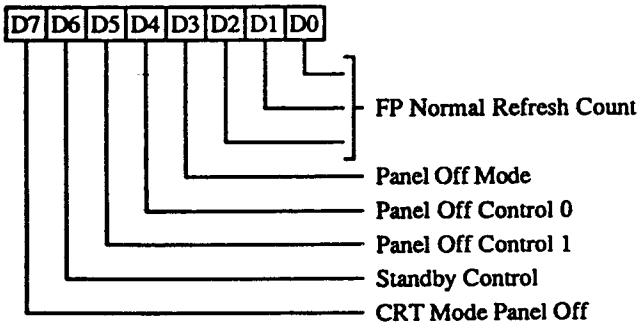
7 LP During Vertical Blank

This bit should be set only for SS panels which require FP Hsync (LP) to be active during vertical blank time when XR54 bit-1 = 0 (e.g., Plasma / EL panels). This bit should be reset when using non-SS panels or when XR54 bit-1 = 1.

0 FP Hsync (LP) is generated from internal FP Blank inactive edge
1 FP Hsync (LP) is generated from internal FP Horizontal Blank inactive edge

POWER DOWN CONTROL REGISTER (XR52)

Read/Write at I/O Address 3B7h/3D7h
Index 52h



2-0 FP Normal Refresh Count

These bits are effective for flat panel only. They specify the number of memory refresh cycles to be performed per scanline. A minimum value of 1 should be programmed in this register.

3 Panel Off Mode

This bit provides a software alternative to enter Panel Off mode. Note that Panel Off mode will be effective in both CRT and flat panel modes of operation.

0 Normal mode (default on reset)
1 Panel Off mode

In Panel Off mode, the CRT / FP display memory interface is inactive but CPU interface and display memory refresh are still active. The internal RAMDAC is also inactive.

4 Panel Off Control Bit 0

This bit is effective only in Panel Off mode (bit-3 = 1 or PNLOFF/ = 0).

0 Video data is forced inactive but CRT and flat panel timing signals (HSync, VSync, Blank / Display Enable, and PCLK/SHFCLK) are active (default on reset)
1 Video data and CRT and flat panel timing signals are forced inactive

Note: XR61 bit-7 controls the inactive level for video data in text mode; XR63 bit-7 controls the inactive level for video data in graphics mode: 0=low when inactive
1=high when inactive

5 Panel Off Control Bit 1

This bit is effective only in Panel Off mode (bit-3 = 1 or PNLOFF/ = 0).

0 Inactive video data and/or timing pins are driven (default on reset)
1 Inactive video data and/or timing pins are tri-stated

6 Standby Control

This bit is effective only in Standby mode (STNDBY/ pin low). Standby mode is effective for both CRT and flat panel modes. In Standby mode, CPU interface to display memory and internal registers is inactive. The CRT / FP display memory interface, video data and timing signals, and internal RAMDAC are inactive (all CRT and flat panel video control and data pins are 3-stated). Display memory refresh is controlled by this bit.

0 Self-Refresh DRAM support.
1 Display memory refresh frequency is derived from the 32KHZ input (divided per a 2-bit value in XR5F)

7 CRT Mode Panel Off

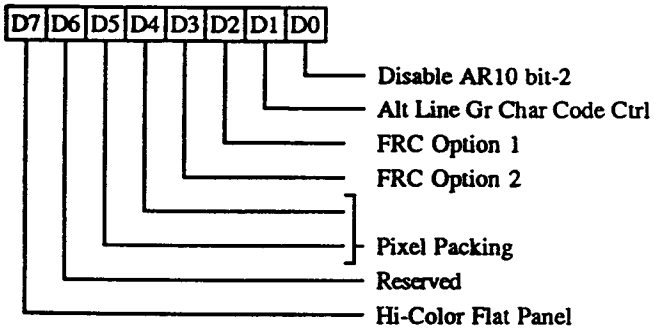
This bit is effective in CRT mode only (non-simultaneous CRT and flat panel) (XR51 bit-2 = 0).

0 Video data (P7-0) and flat panel timing signals (BLANK/, LP, FLM, SHFCLK, ACDCLK) are not 3-stated (default on reset)
1 Video data (P7-0) and flat panel timing signals (BLANK/, LP, FLM, SHFCLK, ACDCLK) are 3-stated

If XR06 bit-0 = 1 (external RAMDAC), P0-7 and BLANK/ are not tri-stated, even if the above bit is set to 1.

LINE GRAPHICS OVERRIDE REGISTER (XR53)

Read/Write at I/O Address 3B7h/3D7h
Index 53h



0 Disable AR10 Bit-2

- 0 Use AR10 bit-2 for Line Graphics control (default on Reset).
- 1 Use XR53 bit-1 instead of AR10 bit-2 for Line Graphics control

1 Alternate Line Graphics Character Control

This bit is effective only if bit-0 = 1.

- 0 Ninth pixel of line graphics character is set to the background color
- 1 Ninth pixel of line graphics character is identical to the eighth pixel

2 FRC Option 1

3 FRC Option 2

5-4 Pixel Packing (65530 only)

These bits should be programmed only when color STN panels are used. These bits should be programmed to 00 for monochrome panels or TFT color panels.

- 00 3-bit Pack. XR50 bits 5-4 can be 00, 01, or 10.
- 01 4-bit Pack. XR50 bits 5-4 can be 00 or 01. If a DD panel is used, XR50 bits 5-4 must be set to 01 without frame acceleration or 00 with frame acceleration (not available currently).
- 10 Reserved
- 11 Extended 4-bit Pack. XR50 bits 5-4 must be programmed to 01.

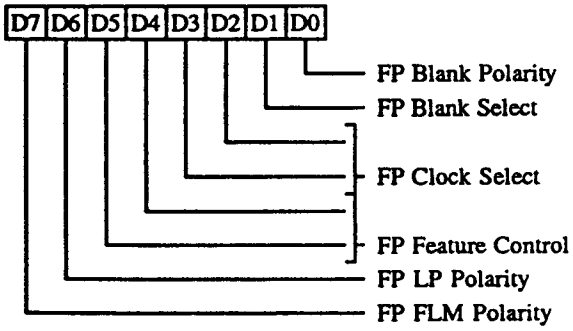
These bits are effective in the 65530 only for Color STN panels when FRC is enabled.

6 Reserved (0)

7 High Color Mode Flat Panel Operation (65530 only)

- 0 Hi Color operation in low-resolution modes on flat panel
- 1 Hi Color operation in hi-resolution modes on flat panel

FP INTERFACE REGISTER (XR54)
Read/Write at I/O Address 3B7h/3D7h
Index 54h



This register is used only in flat panel modes.

0 FP Blank Polarity

This bit controls the polarity of the BLANK/ pin in flat panel mode. In CRT mode, XR28 bit-0 controls polarity of the BLANK/ pin.

0 Positive polarity
1 Negative polarity

1 FP Blank Select

This bit controls the BLANK/ pin output in flat panel mode. In CRT mode, XR28 bit-1 controls the BLANK/ output. This bit also affects operation of the flat panel video logic, generation of the FP HSync (LP) pulse signals, and masking of the Shift Clock.

0 The BLANK/ pin outputs both FP Vertical and Horizontal Blank. In 480-line DD panels, this option will generate exactly 240 FP HSync (LP) pulses.
1 The BLANK/ pin outputs only FP Horizontal Blank. During FP Vertical Blank, the flat panel video logic will be active, the FP HSync (LP) pulse will be generated, and Shift Clock can not be masked. Note however that Shift Clock can still be masked during FP Horizontal Blank.

Note: The signal polarity selected by bit-0 is applicable for either selection.

3-2 FP Clock Select Bits 1-0

Select flat panel dot clock source. These bits are used instead of Miscellaneous Output Register (MSR) bits 3-2 in flat panel mode. See description of MSR bits 3-2.

5-4 FP Feature Control bits 1-0

Select flat panel dot clock source. These bits are used instead of Feature Control Register (FCR) bits 1-0 in flat panel mode. See description of FCR bits 1-0.

6 FP HSync (LP) Polarity

This bit controls the polarity of the flat panel HSync (LP) pin.

0 Positive polarity
1 Negative polarity

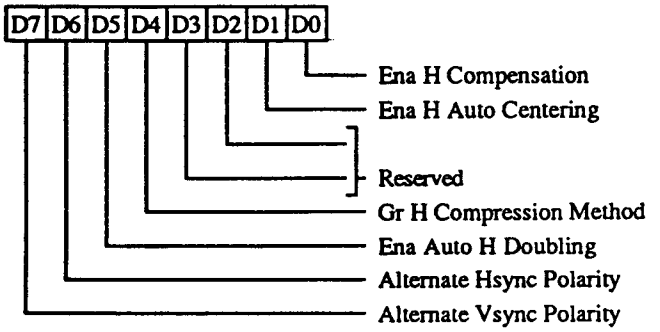
7 FP VSync (FLM) Polarity

This bit controls the polarity of the flat panel VSync (FLM) pin.

0 Positive polarity
1 Negative polarity

HORIZONTAL COMPENSATION REGISTER (XR55)

Read/Write at I/O Address 3B7h/3D7h
Index 55h



This register is used only in flat panel modes when flat panel compensation is enabled (XR51 bit-6 = 1).

0 Enable Horizontal Compensation (EHCP)

0 Disable horizontal compensation
1 Enable horizontal compensation

1 Enable Automatic Horizontal Centering (EAHC) (effective only if bit-0 is 1)

0 Enable non-automatic horizontal centering. The Horizontal Centering Register is used to specify the left border. If no centering is desired then the Horizontal Centering Register can be programmed to 0.
1 Enable automatic horizontal centering. Horizontal left and right borders will be computed automatically.

2 Enable Text Mode Horizontal Compression (ETHC) (this bit is effective only if bit-0 is 1 in flat panel text mode). Setting this bit will turn on text mode horizontal compression regardless of horizontal display width or horizontal panel size.

0 Text mode horizontal compression off
1 Text mode horizontal compression on. 8-dot text mode is forced when 9-dot text mode is specified (SR01 bit-0 = 0 or Hercules text).

Note: This bit affects the horizontal pixel panning logic. When text mode horizontal compression is active, programming 9-bit panning will result in 8-bit panning.

3 Reserved

4 Reserved

5 Enable Automatic Horizontal Doubling (EAHD) (this bit is effective if bit-0 is 1)

0 Disable Automatic Horizontal Doubling. Horizontal doubling will only be performed for flat panels when SR01 bit-3 = 1 in any emulation mode or when 3B8/3D8 bit-0 & 3B8/3D8 bit-4 = 0 in CGA emulation.
1 Enable Automatic Horizontal Doubling. Horizontal doubling will be performed for flat panels when SR01 bit-3 = 1 in any emulation mode or when 3B8/3D8 bit-0 & 3B8/3D8 bit-4 = 0 in CGA emulation or when the Horizontal Display width (CR01) is equal to or less than half of the Horizontal Panel Size (XR18).

6 Alternate CRT Hsync Polarity

0 Positive
1 Negative

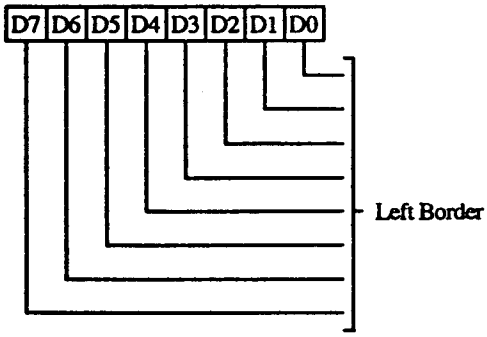
7 Alternate CRT Vsync Polarity

0 Positive
1 Negative

Note: bits 6 and 7 above are used in flat panel mode (XR51 bit-2 = 1) instead of MSR bits 6 and 7). This is primarily used for simultaneous CRT / Flat Panel display.

HORIZONTAL CENTERING REGISTER (XR56)

Read/Write at I/O Address 3B7h/3D7h
Index 56h



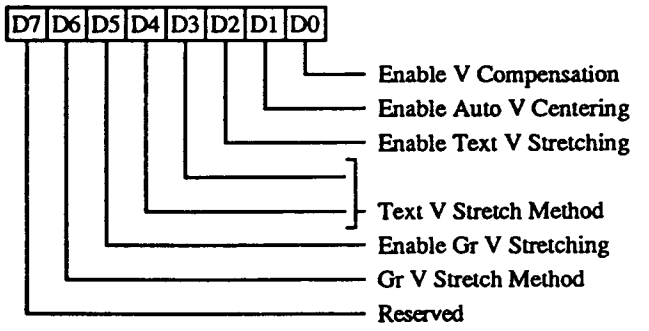
This register is used only in flat panel modes when non-automatic horizontal centering is enabled.

7-0 Horizontal Left Border (HLB)

Programmed Value (in character clocks)
= Width of Left Border – 1

VERTICAL COMPENSATION REGISTER (XR57)

Read/Write at I/O Address 3B7h/3D7h
Index 57h



This register is used only in flat panel modes when flat panel compensation is enabled.

0 Enable Vertical Compensation (EVCP)

0 Disable vertical compensation
1 Enable vertical compensation

1 Enable Automatic Vertical Centering (EAVC)

This bit is effective only if bit-0 is 1.

0 Enable non-automatic vertical centering. The Vertical Centering Register is used to specify the top border. If no centering is desired then the Vertical Centering Register can be programmed to 0.
1 Enable automatic vertical centering. Vertical top and bottom borders will be computed automatically.

2 Enable Text Mode Vertical Stretching (ETVS)

This bit is effective only if bit-0 is 1.

0 Disable text mode vertical stretching; graphics mode vertical stretching is used if enabled.
1 Enable text mode vertical stretching

4-3 Text Mode Vertical Stretching (TVS1-0)

These bits are effective if bits 2 and 0 are 1.

00 Double Scanning (DS) and Line Insertion (LI) with the following priority: DS+LI, DS, LI.
01 Double Scanning (DS) and Line Insertion (LI) with the following priority: DS+LI, LI, DS.
10 Double Scanning (DS) and TallFont (TF) with the following priority: DS+TF, DS, TF.
11 Double Scanning (DS) and TallFont (TF) with the following priority: DS+TF, TF, DS.

5 Enable Vertical Stretching (EVS)

This bit is effective only if bit-0 is 1.

0 Disable vertical stretching
1 Enable vertical stretching

6 Vertical Stretching (VS)

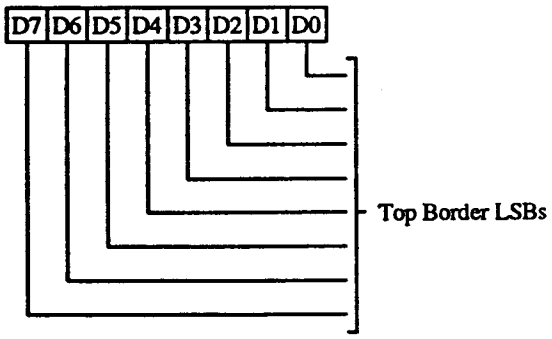
Vertical Stretching can be enabled in both text and graphics modes. This bit is effective only if bits 5 and 0 are 1.

0 Double Scanning (DS) and Line Replication (LR) with the following priority: DS+LR, DS, LR.
1 Double Scanning (DS) and Line Replication (LR) with the following priority: DS+LR, LR, DS.

7 Reserved (0)

VERTICAL CENTERING REGISTER (XR58)

Read/Write at I/O Address 3B7h/3D7h
Index 58h



This register is used only in flat panel modes when non-automatic vertical centering is enabled.

7-0 Vertical Top Border LSBs (VTB7-0)

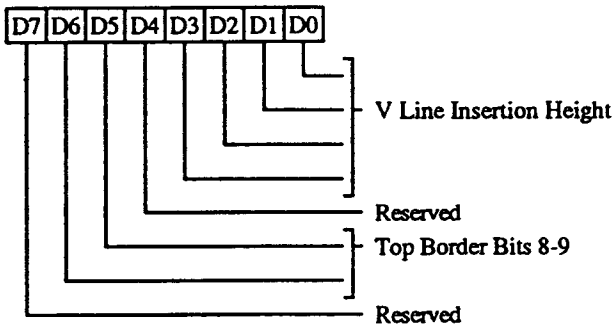
Programmed value:

Top Border Height (in scan lines) – 1

This register contains the eight least significant bits of the programmed value of the Vertical Top Border (VTB). The two most significant bits are in the Vertical Line Insertion Register (XR59).

VERTICAL LINE INSERTION REGISTER (XR59)

Read/Write at I/O Address 3B7h/3D7h
Index 59h



This register is used only in flat panel text mode when vertical line insertion is enabled.

3-0 Vertical Line Insertion Height (VLIH3-0)

Programmed Value:

Number of Insertion Lines – 1

The value promgrammed in this register - 1 is the number of lines to be inserted between the rows. Insertion lines are never double scanned even if double scanning is enabled. Insertion lines use the background color.

4 Reserved (0)

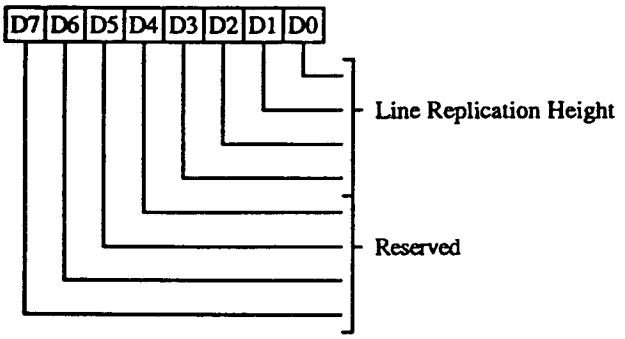
6-5 Vertical Top Border MSBs (VTB9-8)

This register contains the two most significant bits of the programmed value of the Vertical Top Border (VTB). The eight least significant bits are in the Vertical Centering Register (XR58).

7 Reserved (0)

VERTICAL LINE REPLICATION REGISTER (XR5A)

Read/Write at I/O Address 3B7h/3D7h
Index 5Ah



This register is used only in flat panel text or graphics modes when vertical line replication is enabled.

3-0 Vertical Line Replication Height (VLRH)

Programmed Value = Number of Lines Between Replicated Lines – 1

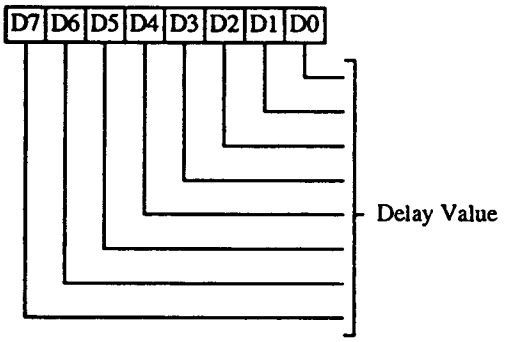
Double scanned lines are also counted.

In other words, if this field is programmed with '7', every 8th line will be replicated.

7-4 Reserved (0)

PANEL POWER SEQUENCING DELAY REGISTER (XR5B) (65530 Only)

Read/Write at I/O Address 3B7h/3D7h
Index 5Bh



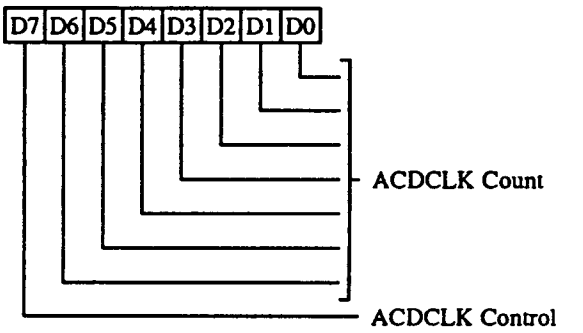
This register is used only when the Panel Power Sequencing feature is enabled. Defaults to 81h on RESET to be compatible with the 65520 which has a fixed delay of 32 mS.

7-4 Programmable value of panel power sequencing during power up. Can be programmed up to 60 milliseconds in increments of four milliseconds each. A value of 0 results in no delay.

3-0 Programmble value of panel power sequencing during power down. Can be programmed up to 480 milliseconds in increments of 32 milliseconds. A value of 0 results in no delay.

ACDCLK CONTROL REGISTER (XR5E)

Read/Write at I/O Address 3B7h/3D7h
Index 5Eh



This register is used only in flat panel mode.

6-0 ACDCLK Count (ACDCNT)

These bits define the number of Hsyncs between adjacent phase changes on the ACDCLK output. These bits are effective only when bit 7 = 0 and contents of this register are grater than 2.

Programmed Value = Actual Value – 2

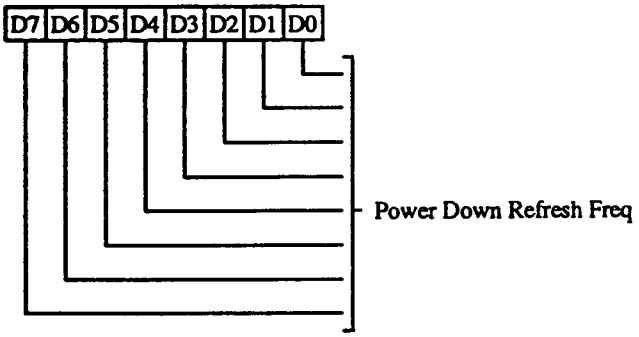
7 ACDCLK Control

0 The ACDCLK phase changes depending on bits 0-6 of this register

1 The ACDCLK phase changes every frame if frame accelerator is not used. If frame accelerator is used, the ACDCLK phase changes every other frame.

POWER DOWN REFRESH REGISTER (XR5F)

Read/Write at I/O Address 3B7h/3D7h
Index 5Fh



7-0 Power Down Refresh Frequency

These bits define the frequency of memory refresh cycles in power down (standby) mode (STNDBY/ pin low). CAS-Before-RAS (CBR) refresh cycles are performed.

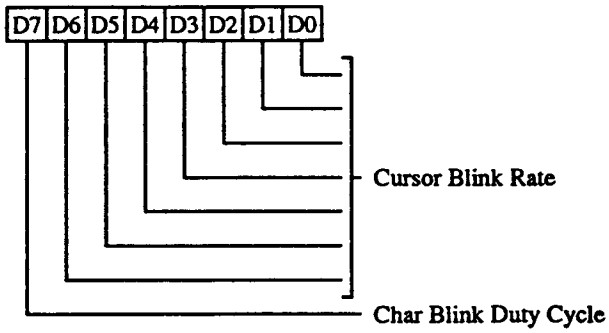
If XR52 bit-6 = 1, the interval between two refresh cycles is determined by bits 0-1 of this register per the table below. Bits 2-7 of this register are reserved for future use in this mode (and should be programmed to 0).

1	0	Approximate Refresh Interval
0	0	16 usec (32KHZ pin period ÷ 2)
0	1	32 usec (32KHZ pin period)
1	0	64 usec (32KHZ pin period * 2)
1	1	128 usec (32KHZ pin period * 4)

If XR52 bit-6 = 0, a value of 0 causes no refresh to be performed. Self-Refresh DRAMs should be used.

BLINK RATE CONTROL REGISTER (XR60)

Read/Write at I/O Address 3B7h/3D7h
Index 60h



This register is used in all modes.

5-0 Cursor Blink Rate

These bits specify the cursor blink period in terms of number of Vsyncs (50% duty cycle). In text mode, the character blink period and duty cycle is controlled by bits 7-6 of this register. These bits default to 000011 (decimal 3) on reset which corresponds to eight Vsyncs per cursor blink period per the following formula (four Vsyncs on and four Vsyncs off):

Programmed Value = (Actual Value) / 2 – 1

Note: In graphics mode, the pixel blink period is fixed at 32 Vsyncs per cursor blink period with 50% duty cycle (16 on and 16 off).

7-6 Character Blink Duty Cycle

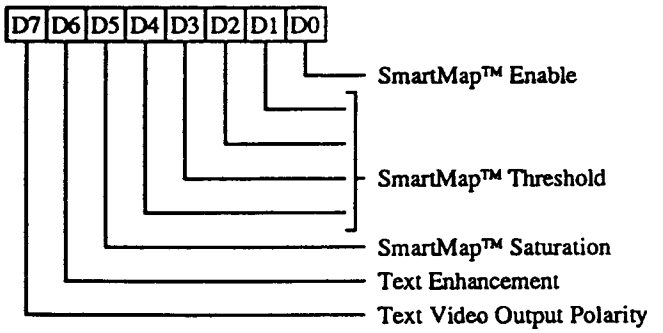
These bits specify the character blink (also called 'attribute blink') duty cycle in text mode.

7	6	Character Blink Duty Cycle	
0	0	50%	
0	1	25%	
1	0	50%	(default on Reset)
1	1	75%	

For setting 00, the character blink period is equal to the cursor blink period. For all other settings, the character blink period is twice the cursor blink period (character blink is twice as slow as cursor blink).

SMARTMAP™ CONTROL REGISTER (XR61)

Read/Write at I/O Address 3B7h/3D7h
Index 61h



This register is used in flat panel text mode only.

0 SmartMap Enable

0 Disable SmartMap, use color lookup table and use internal RAMDAC palette if enabled (XR06 bit-2 = 1).

1 Enable SmartMap, bypass both color lookup table and internal RAMDAC palette in flat panel text mode. Although color lookup table is bypassed, translation of 4 bits/pixel data to 6 bits/pixel data is still performed depending on AR10 bit-1 (monochrome / color display) as follows:

Output	AR10 bit-1 = 0	AR10 bit-1 = 1
Out0	In0	In0
Out1	In1	In1
Out2	In2	In2
Out3	In3	In0+In1+In2+In3
Out4	In3	In3
Out5	In3	In3

Note: This bit does not affect CRT text / graphics mode or flat panel graphics mode; i.e: the color lookup table is always used, and similarly the internal RAMDAC palette is used if enabled.

4-1 SmartMap Threshold

These bits are used only in flat panel text mode when SmartMap is enabled (bit-0 = 1). They define the minimum difference between the foreground and background colors. If the difference is less than this threshold, the colors are separated by adding and subtracting the shift values (XR62) to the foreground and background colors. However, if the foreground and background color values are the same, then the color values are not adjusted.

5 SmartMap Saturation

This bit is used only in flat panel text mode when SmartMap is enabled (bit-0 = 1). It selects the clamping level after the color addition/subtraction.

0 The color result is clamped to the maximum and minimum values (0Fh and 00h respectively)

1 The color result is computed modulo 16 (no clamping)

6 Text Enhancement

This bit is used only in flat panel text mode.

0 Normal text

1 Text attribute 07h and 0Fh are reversed to maximize the brightness of the normal DOS prompt

7 Text Video Output Polarity (TVP)

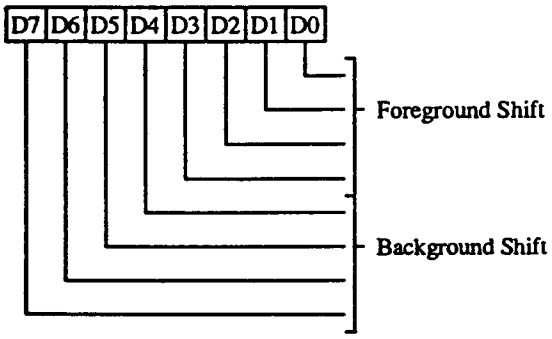
This bit is effective for flat panel text mode only.

0 Normal polarity
1 Inverted polarity

Note: Graphics video output polarity is controlled by XR63 bit-7 (GVP).

SMARTMAP™ SHIFT PARAMETER REGISTER (XR62)

Read/Write at I/O Address 3B7h/3D7h
Index 62h



This register is used in flat panel text mode when SmartMap is enabled (XR61 bit-0 = 1).

3-0 Foreground Shift

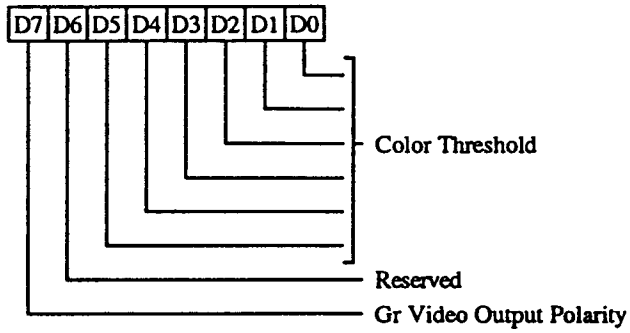
These bits define the number of levels that the foreground color is shifted when the foreground and background colors are closer than the SmartMap Threshold (XR61 bits 1-4). If the foreground color is "greater" than the background color, then this field is added to the foreground color. If the foreground color is "smaller" than the background color, then this field is subtracted from the foreground color.

7-4 Background Shift

These bits define the number of levels that the background color is shifted when the foreground and background colors are closer than the SmartMap Threshold (XR61 bits 1-4). If the background color is "greater" than the foreground color, then this field is added to the background color. If the background color is "smaller" than the foreground color, then this field is subtracted from the background color.

SMARTMAP™ COLOR MAPPING CONTROL REGISTER (XR63)

Read/Write at I/O Address 3B7h/3D7h
Index 63h



5-0 Color Threshold

These bits are effective for monochrome (XR51 bit-5 = 1) single/double drive flat panel with 1 bit/pixel (XR50 bits 4-5 = 11) without FRC (XR50 bits 0-1 = 11). They specify the color threshold used to reduce 6-bit video to 1-bit video color. Color values equal to or greater than the threshold are mapped to 1 and color values less than the threshold are mapped to 0.

6 Reserved

This bit must be set to 1 in rev 0 silicon (reset defaults this bit to 1 in rev 0)

7 Graphics Video Output Polarity (GVP)

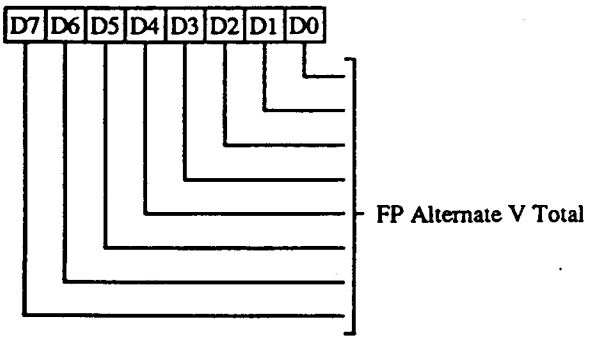
This bit is effective for CRT and flat panel graphics mode only.

0 Normal polarity
1 Inverted polarity

Note: Text video output polarity is controlled by XR61 bit-7 (TVP).

FP ALTERNATE VERTICAL TOTAL REGISTER (XR64)

Read/Write at I/O Address 3B7h/3D7h
Index 64h



This register is used in all flat panel modes.

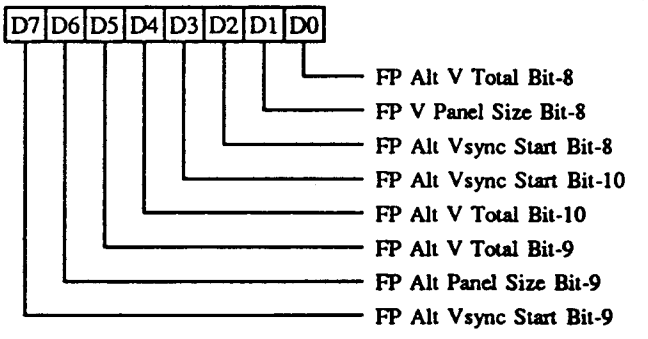
7-0 FP Alternate Vertical Total

The contents of this register are 8 low order bits of a 10-bit value. Bits 9 and 10 are defined in XR65. The vertical total value specifies the total number of scan lines per frame. Similar to CR06.

Programmed Value = Actual Value - 2

FP ALTERNATE OVERFLOW REGISTER (XR65)

Read/Write at I/O Address 3B7h/3D7h
Index 65h



This register is used in all flat panel modes.

0 FP Alternate Vertical Total Bit-8

1 FP Vertical Panel Size Bit-8

2 FP Alternate Vertical Sync Start Bit-8

3 FP Alternate Vertical Sync Start Bit-10

4 FP Alternate Vertical Total Bit-10

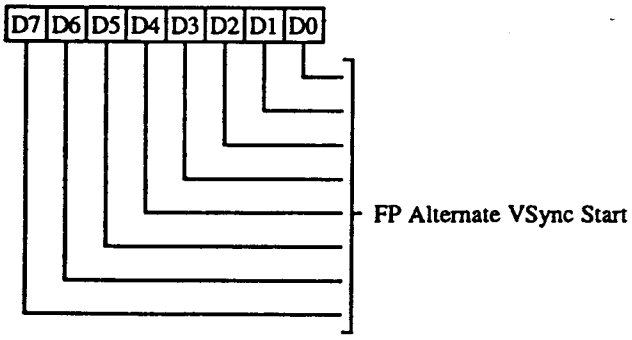
5 FP Alternate Vertical Total Bit-9

6 FP Vertical Panel Size Bit-9

7 FP Alternate Vertical Sync Start Bit-9

FP ALTERNATE VERTICAL SYNC START REGISTER (XR66)

Read/Write at I/O Address 3B7h/3D7h
Index 66h



This register is used in all flat panel modes.

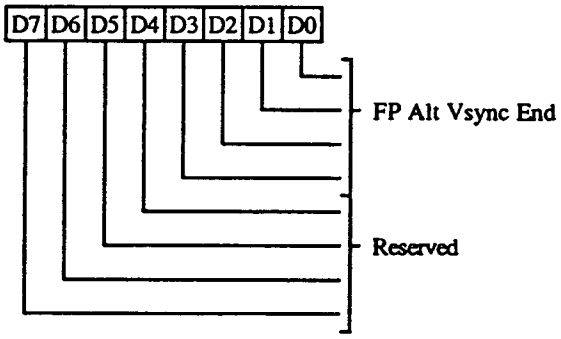
7-0 FP Alternate Vertical Sync Start

The contents of this register are the 8 low order bits of a 10-bit value. Bits 9 and 10 are defined in XR65. This value defines the scan line position at which vertical sync becomes active. Similar to CR10.

Programmed Value = Actual Value – 1

FP ALTERNATE VERTICAL SYNC END REGISTER (XR67)

Read/Write at I/O Address 3B7h/3D7h
Index 67h



This register is used in all flat panel modes.

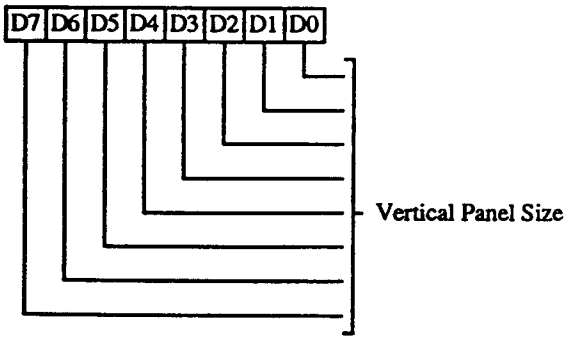
3-0 FP Alternate Vertical Sync End

The lower 4 bits of the scan line count that defines the end of vertical sync. Similar to CR11. If the vertical sync width desired is N lines, the programmed value is:

(contents of XR66 + N) ANDed with 0FH

7-4 Reserved (0)

VERTICAL PANEL SIZE REGISTER (XR68)
Read/Write at I/O Address 3B7h/3D7h
Index 68h



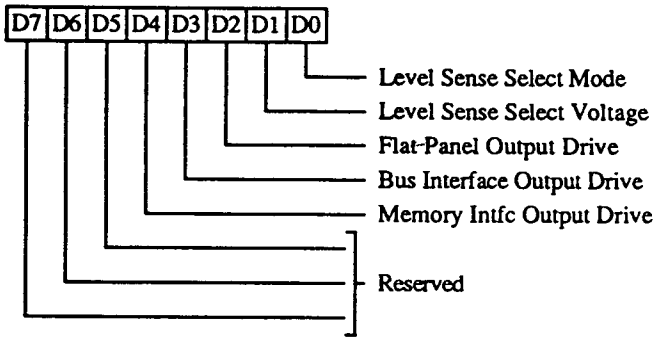
This register is used in all flat panel modes.

7-0 Vertical Panel Size

The contents of this register define the number of scan lines per frame.

Programmed Value = Actual Value – 1

PROGRAMMABLE OUTPUT DRIVE REGISTER (XR6C) (65530 Only)
Read/Write at I/O Address 3B7h/3D7h
Index 6Ch



This register is used to control the output drive of the bus, video, and memory interface pins.

0 Input Level Sense Selection Mode

0 Automatic level sense select (Default) (chip detects Vcc voltage internally)
1 Manual level sense selection (bit-1 used to determine input threshold)

1 Input Level Sense Selection Voltage

0 Vcc for internal logic is 5V (Default)
1 Vcc for internal logic is 3.3V

2 Flat Panel Interface Output Drive Select

0 Lower drive (Default)
1 Higher drive

3 Bus Interface Output Drive Select

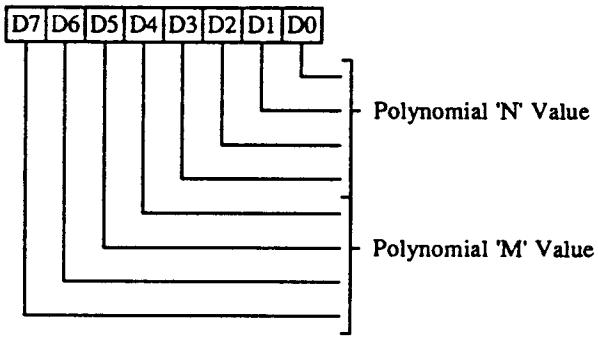
0 Lower drive (Default)
1 Higher drive

4 Memory Interface Output Drive Select

0 Lower drive (Default)
1 Higher drive

7-5 Reserved

POLYNOMIAL FRC CONTROL REGISTER (XR6E)
Read/Write at I/O Address 3B7h/3D7h
Index 6Eh



This register is effective in flat panel mode when polynomial FRC is enabled (see XR50 bits 0-1). It is used to control the FRC polynomial counters. The values in the counters determine the offset in rows and columns of the FRC count. These values are usually determined by trial and error.

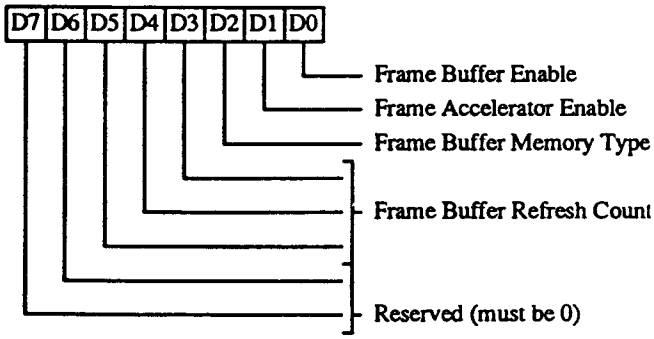
3-0 Polynomial 'N' value

7-4 Polynomial 'M' value

This register defaults to '10111101' on RESET.

FRAME BUFFER CONTROL REGISTER (XR6F)

Read/Write at I/O Address 3B7h/3D7h
Index 6Fh



This register is effective in flat panel mode only.

0 Frame Buffer Enable

This bit is used to enable the external frame buffer. Frame acceleration is available by setting bit-1 = 1. Frame buffering (with or without acceleration) is needed for simultaneous CRT and DD/DS panel operation. In case of simultaneous CRT and plasma or SS panels, the frame buffer is not used therefore this bit should be set to 0. In all cases of simultaneous CRT and flat panel display, XR51 bit-2 (Display Type) should be set to 1 (flat panel display) and XR06 bit-2 (Disable Internal DAC) must be programmed to 0 to enable the internal DAC. The frame buffer with acceleration may also be needed to drive high resolution DD panels.

0 Disable external frame buffer (default)
1 Enable external frame buffer

1 Enable Frame Accelerator

This bit should be used for DD flat panels only. This bit should be programmed to 0 when bit-0 = 0 or for non-DD panels. It enables frame acceleration using an external frame buffer consisting of a single 64Kx4 or 256Kx4 VRAM which can be used to support high resolution DD panels. The user must program XR51 bits 1-0 to 11 (DD panel), XR51 bits 5-4 to 10 (Clock Divide by 4) and bit-0 of this register to 1 (enable external frame buffer) when using the frame accelerator.

0 Disable frame accelerator (default)
1 Enable frame accelerator

2 Frame Buffer Memory Type

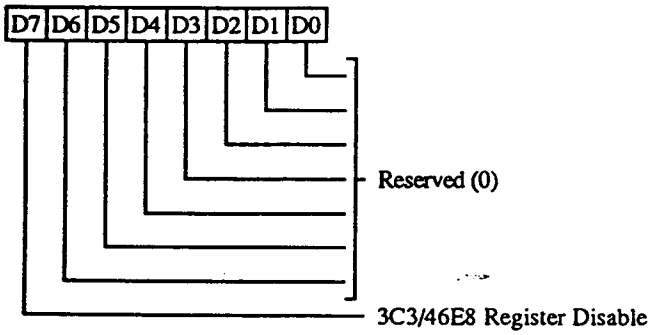
0 Frame buffer consists of a 64Kx4 VRAM. This buffer allows a maximum panel size of 1024x512 (subject to other restrictions) (default on reset).
1 Frame buffer consists of a 256Kx4 VRAM. This buffer allows a maximum panel size of 2048x1024. Note that if there is no frame acceleration, the maximum panel size is limited to 1280x1024 because the maximum capacity of the internal line buffer for DD panels is limited to 1280.

5-3 Frame Buffer Refresh Count

7-6 Reserved (must be programmed to 0)

SETUP / DISABLE CONTROL REGISTER (XR70)

Read/Write at I/O Address 3B7h/3D7h
Index 70h



6-0 Reserved (0)

7 3C3 / 46E8 Register Disable

0 In the MC and PI bus, port 3C3h works as defined to provide control of VGA disable (the DISA/ pin may also be used to disable the VGA). In the PC bus, port 46E8h works as defined to provide control of VGA disable and setup mode (DISA/ and SETUP/ functions are not provided on pins).

1 In the MC and PI bus, writes to I/O port 3C3 have no effect (the VGA can still be disabled via the DISA/ pin). In the PC bus, writes to I/O port 46E8h have no effect (the VGA remains enabled and will not go into setup mode).

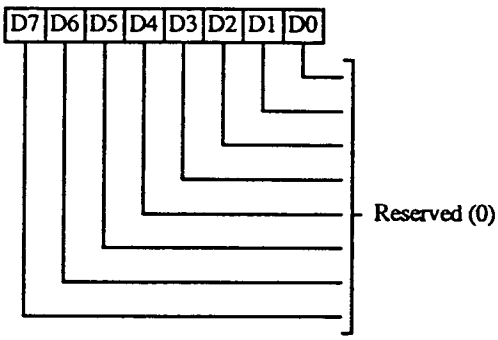
Note: Writes to register 46E8 are only effective in PC bus configurations (46E8 is ignored in MC and PI bus configurations independent of the state of this bit). Writes to 3C3 are only effective in MC and PI bus configurations (3C3 is ignored in PC bus configurations independent of the state of this bit).

Reads from ports 3C3 and 46E8h have no effect independent of the programming of this register (both 3C3 and 46E8h are write-only registers).

This register is cleared by RESET.

FP COMPENSATION DIAGNOSTIC REGISTER (XR7D)

Read/Only at I/O Address 3B7h/3D7h
Index 7Dh

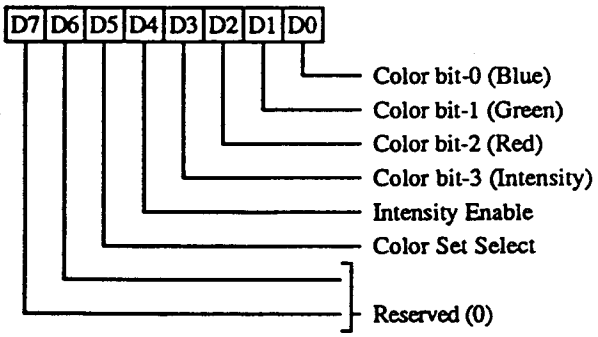


This register is effective in flat panel mode only.

These bits are reserved for future use and currently all read back zero.

CGA / HERCULES COLOR SELECT REGISTER (XR7E)

Read/Write at I/O Address 3B7h/3D7h
Index 7Eh



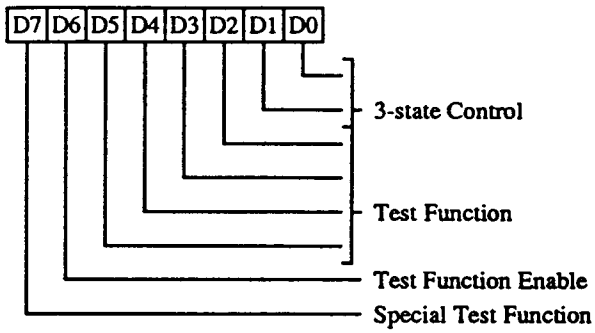
This I/O address is mapped to the same register as I/O address 3D9h. This alternate mapping effectively provides a color select register for Hercules mode. Writes to this register will change the copy at 3D9h. The copy at 3D9h is visible only in CGA emulation or when the extension registers are enabled. The copy at XR7E is visible when the extension registers are enabled.

5-0 See register 3D9

7-6 Reserved (0)

DIAGNOSTIC REGISTER (XR7F)

Read/Write at I/O Address 3B7h/3D7h
Index 7Fh



0 3-State Control Bit 0

- 0 Normal outputs (default on Reset)
- 1 3-state output pins: PALRD/, PALWR/, P7-0, PCLK, HSYNC, VSYNC, BLANK/, FLM, LP, ACDCLK, SHFCLK, RDY, 0WS/, IOCS16/, and IRQ.

1 3-State Control Bit 1

- 0 Normal outputs (default on Reset)
- 1 3-state output pins: RASA/, RASB/, CASA/, CASB/, WEA/, WEB/, DTOEA/, DTOEB/, SCLK, AA0-8 and BA0-8.

5-2 Test Function

These bits are used for internal testing of the chip when bit-6 = 1.

6 Test Function Enable

This bit enables bits 5-2 for internal testing.

- 0 Disable test function bits (default)
- 1 Enable test function bits

7 Special Test Function

This bit is used for internal testing and should be set to 0 (default to 0 on reset) for normal operation.

Programming and Parameters

GENERAL PROGRAMMING HINTS

The values presented in this section make certain assumptions about the operating environment. The flat panel clock is assumed to be input on CLKIN. The values programmed into the SmartMap™ control registers (XR61 and XR62) give a threshold of 3 with foreground and background shift of 3 but SmartMap™ is turned off. To enable it, set XR61 bit-0 = 1. The value programmed in the ACDCLK Register (XR5E) will produce minimal ghosting on most LCD panels. However, this value should be optimized for each panel model. Certain LCD Panels (Epson in particular) require the ACDCLK to be synchronized to vertical sync. For this panel XR5E should be programmed to 80h.

The horizontal parameter values presented here are the minimum required for each panel type. For high resolution panels, these parameters may be changed to suit the panel size. The horizontal values equal the number of characters clocks output per line. In dual drive panels this value includes both panels. Therefore, the horizontal values are double those expected.

Due to pipelining of the horizontal counters, certain sync or blank values may result in no display. Generally, the horizontal blank start must equal the display end and the blank end must equal the horizontal total. The horizontal sync start and end values have a wide range of acceptable values. The 65520 / 530 also has the versatility to program an LP delay to aid in interfacing to panels with a wide variety of timing requirements.

If a 400 or 350 Line Panel is used, vertical compensation should be enabled via register XR57. Generally, the vertical sync start should equal the vertical total and panel size. The panel size should be increased to include the blank times. For DD panels, this should be done in multiples of 2 to accommodate both the upper and lower panel. The 65520 / 530 also has the versatility to insert extra LPs for every extra line the panel requires.

In order to program the 65520 / 530 for simultaneous display, two FLM signals are required. The first shorter FLM will match the normal FLM frequency as the data is displayed on the first half of the CRT display data. The second FLM will be longer to allow for the CRT blank time. The FLM delay is programmed in XR2C and should be equal to the CRT blank time + 1.

For flat panel types and sizes not presented here, start with the parameters for a panel that most closely resembles the target panel. Adjust the flat panel configuration registers as needed and adjust the horizontal and vertical parameters as needed. Adaption to a non-standard panel is usually a trial and error process.

These parameters are recommended by Chips and Technologies for the 65520 / 65530. They have been tested on several different flat panel displays. Customers should feel free to test other register values to improve the screen appearance or to customize the 65520 / 530 for other flat panel displays.

EXTENSION REGISTER VALUES

The 65520/530 controller can be programmed for a wide variety of flat panels, compensation techniques and backwards compatibility. The following pages provide the following 65520/530 Extension Register Value tables:

Table	Extension Registers	Display Type Description
#1	Minimum	Analog CRT Monitor (VGA Mode)
#2	Additional	CRT, Flat Panel & Simultaneous Display Emulation Modes
#3	Additional	640x480 Monochrome LCD-DD Panels (Sharp LM64P80)
#4	Additional	Simultaneous 640x480 Monochrome LCD-DD & CRT Display
#5	Additional	640x480 16 Internal Gray Scale Plasma Panel (Matsushita S804)
#6	Additional	640x480 16 Internal Gray Scale EL Panel (Sharp LJ64ZU50)
#7	Additional	640x480 Color TFT LCD (Sharp LQ9D011/Hitachi TX26D02VC2AAA)
#8	Additional	Simultaneous 640x480 Color TFT LCD & CRT Display
#9	Additional	1024x768 Monochrome LCD-DD Panel (Sanyo LCM-5941-24NAK)
#10	Additional	1024x768 Monochrome LCD-DD Panel (Sharp LM10P10)
#11	Additional	1024x768 Monochrome LCD-DD Panel (Hitachi LMG9050ZZFC)
#12	Additional	1280x1024 Monochrome LCD-DD Panel (Hitachi LMG9100ZZFC)

Table #1 specifies the values for the minimum Extension Registers required for the 65520/530 to boot to an analog CRT monitor.

Table #2 specifies values for the additional Extension Registers required for emulation of EGA, CGA, MDA and Hercules backwards compatibility modes. Note that the registers in Table #2 should be used in conjuction with the registers specified in Table #1. For registers listed in both tables, use the values in Table #2 (shown in bold text).

Tables #3 - #12 specify values for the additional Extension Registers required to support various flat panels. Note that the registers in Tables #3 - #12 should be used in conjuction with the registers specified in Table #1 (and optionally Table #2). For registers listed in more than one table, use the values in Tables #3 - #12 (shown in bold text) for the particular flat panel.

Table #1 - Analog CRT Monitor Display Mode

Initial Boot-Up Extension Register Values

Register	Value (in Hex)	Register	Comments
XR02	01	CPU Interface	
XR04	20	Memory Mapping	Note 1
XR06	00	Palette Control	
XR0B	00	CPU Paging	
XR0C	00	Start Address Top	
XR0D	00	Auxilary Offset	
XR0E	00	Text Mode	
XR0F	00	Software Flag	Note 2
XR10	00	Single/Low Map	
XR11	00	High Map	
XR14	00	Emulation Mode	
XR15	00	Write Protect	
XR1E	00	Alternate Offset	
XR1F	00	Virtual EGA Switch	
XR24	12	Alternate Scanline	
XR25	59	Horizontal Virtual Panel Size	
XR28	00	Video Interface	
XR2B	00	Default Video	
XR51	67	Display Type	
XR52	41	Power Down Control	
XR53	0C	Override	
XR54	3A	Alternate Miscellenous Output	
XR55	05	Horizontal Compensation	
XR56	00	Horizontal Centering	
XR57	1B	Vertical Compensation	
XR58	00	Vertical Centering	
XR59	00	Vertical Line Insertion	
XR5A	00	Vertical Line Replication	
XR5E	80	ACDCLK Control	
XR5F	4E	Power Down Mode Refresh	
XR60	A0	Blink Rate Control	
XR61	6E	SMARTMAP Control	
XR62	07	SMARTMAP Control	
XR63	41	Color Mapping Control	
XR70	80	Setup Control	
XR7F	00	Diagnostic	

Note 1) Memory Mapping Register XR04 is automatically re-programmed with the video memory configuration by the video BIOS

Note 2) Software Flag Register XR0F's definition:

Bits 0-1 Set by the BIOS depending upon the video memory configuration
Bit 5 0 - All modes use the BMP selected dot clock
1 - All extended packed pixel modes use 40 MHz dot clock
All other modes use the BMP selected dot clock
Bit 6 0 - 1024x768 16 color Interlaced CRT monitor
1 - 1024x768 16 color Non-Interlaced CRT monitor
Bit 7 0 - TallFonts (8x19/8x30 font) disabled
1 - TallFonts (8x19/8x30 font) enabled

Table #2 - CRT, Flat Panel & Simultaneous Display Emulation Modes

Extension Register Values

Register	Value (in Hex)	Register	Comments
XR14	**00**	**Emulation Mode**	**EGA Emulation**
XR15	**18**	**Write Protect**	**EGA Emulation**

Register	Value (in Hex)	Register	Comments
XR14	**01**	**Emulation Mode**	**CGA Emulation**
XR15	**0D**	**Write Protect**	**CGA Emulation**
XR18	27	Alternate Horizontal Display Enable End	CGA Emulation
XR19	2B	Alternate Horizontal Retrace Start	CGA Emulation
XR1A	A0	Alternate Horizontal Retrace End	CGA Emulation
XR1B	2D	Alternate Horizontal Total	CGA Emulation
XR1C	28	Alternate Horizontal Blanking Start	CGA Emulation
XR1D	10	Alternate Horizontal Blanking End	CGA Emulation
XR1E	14	Alternate Offset	CGA Emulation
XR7E	30	Monochrome Color Select	CGA Emulation

Register	Value (in Hex)	Register	Comments
XR14	**52**	**Emulation Comments**	**MDA Emulation**
XR15	**0D**	**Write Protect**	**MDA Emulation**
XR7E	**0F**	**Monochrome Color Select**	**MDA Emulation**

Register	Value (in Hex)	Register	Comments
XR0D	**02**	**Auxiliary Offset**	**Hercules Emulation**
XR14	**52**	**Emulation Mode**	**Hercules Emulation**
XR15	**0D**	**Write Protect**	**Hercules Emulation**
XR18	59	Alternate Horizontal Display Enable End	Hercules Emulation
XR19	60	Alternate Horizontal Retrace Start	Hercules Emulation
XR1A	8F	Alternate Horizontal Retrace End	Hercules Emulation
XR1B	6E	Alternate Horizontal Total	Hercules Emulation
XR1C	5C	Alternate Horizontal Blanking Start	Hercules Emulation
XR1D	31	Alternate Horizontal Blanking End	Hercules Emulation
XR1E	**16**	**Alternate Offset**	**Hercules Emulation**
XR7E	**0F**	**Monochrome Color Select**	**Hercules Emulation**

Note: 1) **Bold** text indicates registers with values different from those shown in Table #1
2) Non-bold text indicates additional registers (not included in Table #1)

Table #3 - Monochrome 640x480 LCD-DD (e.g., Sharp LM64P80) Panel Mode

Extension Register Values (with a 64k x 4 VRAM frame accelerator)

Register	Value (in Hex)	Register	Comments
XR06	**02**	**Palette Control**	**Disable Internal DAC**
XR19	54	Alternate Horizontal Retrace Start	
XR1A	19	Alternate Horizontal Retrace End	
XR1B	59	Alternate Horizontal Total	
XR1C	4F	Alternate Horizontal Blanking Start	
XR2C	04	Flat Panel Vsync Delay	
XR2D	50	Flat Panel Hsync Delay (CP disabled)	
XR2E	50	Flat Panel Hsync Delay (CP enabled)	
XR2F	00	Flat Panel Hsync Width	
XR50	25	Panel Format	
XR52	**41**	**Power Down Control**	
XR53	**0C**	**Override**	
XR64	E4	Alternate Vertical Total	
XR65	07	Alternate Overflow	
XR66	E0	Alternate Vertical Sync Start	
XR67	01	Alternate Vertical Sync End	
XR68	DF	Alternate Vertical Display Enable End	
XR6E	BD	Polynomial FRC Control Register	Optimize For LCD
XR6F	1B	Frame Buffer Control	

Note: 1) **Bold** text indicates registers with values different from those shown in Table #1
2) Non-bold text indicates additional registers (not included in Table #1)

Table #4 - Simultaneous Monochrome 640x480 LCD-DD & CRT Display Mode

Extension Register Values (With A 64Kx4 or 256Kx4 VRAM Frame Buffer)

Register	Value (in Hex)	Register	Comments
XR19	5A	Alternate Horizontal Retrace Start	
XR1A	1F	Alternate Horizontal Retrace End	
XR1B	68	Alternate Horizontal Total	
XR2C	21	Flat Panel Vsync Delay	
XR2D	50	Flat Panel Hsync Delay (CP disabled)	
XR2E	50	Flat Panel Hsync Delay (CP enabled)	
XR2F	00	Flat Panel Hsync Width	
XR50	25	Panel Format	
XR52	**41**	**Power Down Control**	
XR53	**0C**	**Override**	
XR64	0B	Alternate Vertical	
XR65	26	Alternate Overflow	
XR66	EA	Alternate Vertical Sync	
XR67	0C	Alternate Vertical Sync	
XR68	DF	Alternate Vertical Display Enable	
XR6E	BD	Polynomial FRC Control Register	Optimize For LCD
XR6F	1B	Frame Buffer Control	

Note: 1) **Bold** text indicates registers with values different from those shown in Table #1
2) Non-bold text indicates additional registers (not included in Table #1)

Table #5 - 640x480 16 Internal Gray Scale Plasma Panel (Matsushita S804)

Extension Register Values (No Frame Buffer)

Register	Value (in Hex)	Register	Comments
XR19	60	Alternate Horizontal Retrace Start	
XR1A	00	Alternate Horizontal Retrace End	
XR1B	60	Alternate Horizontal Total	
XR1C	4F	Flat Panel Horizontal Panel Size	
XR2C	04	Flat Panel Vsync Delay	
XR2D	62	Flat Panel Hsync Delay (CP disabled)	
XR2E	6d	Flat Panel Hsync Delay (CP enabled)	
XR2F	08	Flat Panel Hsync Width	
XR50	17	Panel Format	
XR51	**C4**	**Display Type**	
XR52	**01**	**Power Down Control**	
XR53	**0C**	**Override**	
XR54	**39**	**Alternate Miscellenous Output**	
XR64	0D	Alternate Vertical	
XR65	26	Alternate Overflow	
XR66	E8	Alternate Vertical Sync	
XR67	0A	Alternate Vertical Sync	
XR68	DF	Alternate Vertical Display Enable	
XR6F	00	Frame Buffer Control	

Note: 1) **Bold** text indicates registers with values different from those shown in Table #1
2) Non-bold text indicates additional registers (not included in Table #1)

Table #6 - 640x480 16 Internal Gray Level EL Panel (Sharp LJ64ZU50)

Extension Register Values (No Frame Buffer)

Register	Value (in Hex)	Register	Comments
XR19	52	Alternate Horizontal Retrace Start	
XR1A	15	Alternate Horizontal Retrace End	
XR1B	54	Alternate Horizontal Total	
XR1C	4F	Flat Panel Horizontal Panel Size	
XR2C	0C	Flat Panel Vsync Delay	
XR2D	4F	Flat Panel Hsync Delay (CP disabled)	
XR2E	4E	Flat Panel Hsync Delay (CP enabled)	
XR2F	81	Flat Panel Hsync Width	
XR50	17	Panel Format	
XR51	**C4**	**Display Type**	
XR52	**41**	**Power Down Control**	
XR54	**F9**	**Alternate Miscellenous Output**	
XR64	F0	Alternate Vertical	
XR65	07	Alternate Overflow	
XR66	E5	Alternate Vertical Sync	
XR67	0E	Alternate Vertical Sync	
XR68	DF	Alternate Vertical Display Enable	
XR6F	00	Frame Buffer Control	

Note: 1) **Bold** text indicates registers with values different from those shown in Table #1
2) Non-bold text indicates additional registers (not included in Table #1)

Table #7 - 640x480 Color TFT LCD Flat Panel Mode (Sharp LQ9D011 or Hitachi TX26A02VC)

Extension Register Values (No Frame Buffer)

Register	Value (in Hex)	Register	Comments
XR06	**C2**	**Palette Control**	**Color Reduction**
XR19	56	Alternate Horizontal Retrace Start	
XR1A	13	Alternate Horizontal Retrace End	
XR1B	5F	Alternate Horizontal Total	
XR1C	4F	Flat Panel Horizontal Panel Size	
XR28	**02**	**Video Interface**	**Change Polarity**
XR2C	00	Flat Panel Vsync Delay	
XR2D	80	Flat Panel Hsync Delay (CP disabled)	
XR2E	02	Flat Panel Hsync Delay (CP enabled)	
XR2F	42	Flat Panel Hsync Width	
XR50	47	Panel Format	
XR51	**C4**	**Display Type**	
XR52	**41**	**Power Down Control**	
XR53	**0C**	**Override**	
XR54	**F9**	**Alternate Miscellenous Output**	
XR64	04	Alternate Vertical	
XR65	26	Alternate Overflow	
XR66	E2	Alternate Vertical Sync	
XR67	05	Alternate Vertical Sync	
XR68	E0	Alternate Vertical Display Enable	
XR6F	00	Frame Buffer Control	

Note: 1) **Bold** text indicates registers with values different from those shown in Table #1
2) Non-bold text indicates additional registers (not included in Table #1)

Table #8 - Simultaneous 640x480 Color TFT LCD & CRT Display Mode (Sharp LQ9D011 or Hitachi TX26A02VC)

Extension Register Values (No Frame Buffer)

Register	Value (in Hex)	Register	Comments
XR06	**C0**	**Palette Control**	**Color Reduction**
XR19	5A	Alternate Horizontal Retrace Start	
XR1A	1F	Alternate Horizontal Retrace End	
XR1B	68	Alternate Horizontal Total	
XR28	**02**	**Video Interface**	**Change Polarity**
XR2C	00	Flat Panel Vsync Delay	
XR2D	80	Flat Panel Hsync Delay (CP disabled)	
XR2E	02	Flat Panel Hsync Delay (CP enabled)	
XR2F	46	Flat Panel Hsync Width	
XR50	47	Panel Format	
XR51	**C4**	**Display Type**	
XR52	**41**	**Power Down Control**	
XR53	**0C**	**Override**	
XR54	**F9**	**Alternate Miscellenous Output**	
XR64	04	Alternate Vertical	
XR65	26	Alternate Overflow	
XR66	E2	Alternate Vertical Sync	
XR67	05	Alternate Vertical Sync	
XR68	E0	Alternate Vertical Display Enable	
XR6F	00	Frame Buffer Control	

Note: 1) **Bold** text indicates registers with values different from those shown in Table #1
2) Non-bold text indicates additional registers (not included in Table #1)

Table #9 - 1024x768 Monochrome LCD-DD (Sanyo LCM-5941-24NAK) Panel Mode

Extension Register Values (With A 256Kx4 VRAM Frame Buffer)

Register	Value (in Hex)	Register	Comments
XR06	**02**	**Palette Control**	
XR19	88	Alternate Horizontal Retrace Start	
XR1A	07	Alternate Horizontal Retrace End	
XR1B	8A	Alternate Horizontal Total	
XR1C	7F	Flat Panel Horizontal Panel Size	
XR2C	01	Flat Panel Vsync Delay	
XR2D	80	Flat Panel Hsync Delay (CP disabled)	
XR2E	80	Flat Panel Hsync Delay (CP enabled)	
XR2F	00	Flat Panel Hsync Width	
XR50	25	Panel Format	
XR51	**6F**	**Display Type**	
XR52	**41**	**Power Down Control**	
XR53	**0C**	**Override**	
XR64	01	Alternate Vertical	
XR65	E5	Alternate Overflow	
XR66	00	Alternate Vertical Sync	
XR67	01	Alternate Vertical Sync	
XR68	FF	Alternate Vertical Display Enable	
XR6E	33	Polynomial FRC Control Register	Optimize For LCD
XR6F	1F	Frame Buffer Control	

Note: 1) **Bold** text indicates registers with values different from those shown in Table #1
2) Non-bold text indicates additional registers (not included in Table #1)

Table #10 - 1024x768 Monochrome LCD-DD (Sharp LM10P10) Panel Mode

Extension Register Values (With A 256Kx4 VRAM Frame Buffer)

Register	Value (in Hex)	Register	Comments
XR06	**02**	**Palette Control**	
XR0F	**20**	**Software Flag**	
XR19	82	Alternate Horizontal Retrace Start	
XR1A	09	Alternate Horizontal Retrace End	
XR1B	8A	Alternate Horizontal Total	
XR1C	7F	Flat Panel Horizontal Panel Size	
XR2C	05	Flat Panel Vsync Delay	
XR2D	00	Flat Panel Hsync Delay (CP disabled)	
XR2E	00	Flat Panel Hsync Delay (CP enabled)	
XR2F	30	Flat Panel Hsync Width	
XR50	35	Panel Format	
XR51	**6F**	**Display Type**	
XR52	**41**	**Power Down Control**	
XR53	**0C**	**Override**	
XR64	06	Alternate Vertical	
XR65	E5	Alternate Overflow	
XR66	03	Alternate Vertical Sync	
XR67	03	Alternate Vertical Sync	
XR68	FF	Alternate Vertical Display Enable	
XR6E	33	Polynomial FRC Control Register	Optimize For LCD
XR6F	1D	Frame Buffer Control	

Note: 1) **Bold** text indicates registers with values different from those shown in Table #1
2) Non-bold text indicates additional registers (not included in Table #1)

Table #11 - 1024x768 Monochrome LCD-DD (Hitachi LMG9050ZZFC) Panel Mode

Extension Register Values (With A 256Kx4 VRAM Frame Buffer)

Register	Value (in Hex)	Register	Comments
XR06	**02**	**Palette Control**	
XR0F	**20**	**Software Flag**	
XR19	82	Alternate Horizontal Retrace Start	
XR1A	09	Alternate Horizontal Retrace End	
XR1B	8A	Alternate Horizontal Total	
XR1C	7F	Flat Panel Horizontal Panel Size	
XR2C	07	Flat Panel Vsync Delay	
XR2D	00	Flat Panel Hsync Delay (CP disabled)	
XR2E	00	Flat Panel Hsync Delay (CP enabled)	
XR2F	30	Flat Panel Hsync Width	
XR50	35	Panel Format	
XR51	**6F**	**Display Type**	
XR52	**41**	**Power Down Control**	
XR53	**0C**	**Override**	
XR64	06	Alternate Vertical	
XR65	E7	Alternate Overflow	
XR66	03	Alternate Vertical Sync	
XR67	03	Alternate Vertical Sync	
XR68	00	Alternate Vertical Display Enable	
XR6E	33	Polynomial FRC Control Register	Optimize For LCD
XR6F	1D	Frame Buffer Control	

Note: 1) **Bold** text indicates registers with values different from those shown in Table #1
2) Non-bold text indicates additional registers (not included in Table #1)

Table #12 - 1280x1024 Monochrome LCD-DD (Hitachi LMG9100ZZFC) Panel Mode

Extension Register Values (With A 256Kx4 VRAM Frame Buffer)

Register	Value (in Hex)	Register	Comments
XR06	02	Palette Control	
XR19	A6	Alternate Horizontal Retrace Start	
XR1A	1E	Alternate Horizontal Retrace End	
XR1B	AA	Alternate Horizontal Total	
XR1C	9F	Flat Panel Horizontal Panel Size	
XR2C	00	Flat Panel Vsync Delay	
XR2D	A0	Flat Panel Hsync Delay (CP disabled)	
XR2E	A0	Flat Panel Hsync Delay (CP enabled)	
XR2F	03	Flat Panel Hsync Width	
XR50	25	Panel Format	
XR51	**6F**	**Display Type**	
XR52	**41**	**Power Down Control**	
XR53	**0C**	**Override**	
XR57	**1F**	**Vertical Compensation**	
XR64	FF	Alternate Vertical	
XR65	E7	Alternate Overflow	
XR66	FF	Alternate Vertical Sync	
XR67	00	Alternate Vertical Sync	
XR68	FF	Alternate Vertical Display Enable	
XR6E	9D	Polynomial FRC Control Register	Optimize For LCD
XR6F	1F	Frame Buffer Control	

Note: 1) **Bold** text indicates registers with values different from those shown in Table #1
2) Non-bold text indicates additional registers (not included in Table #1)

Application Schematic Examples

This section includes schematic examples showing various 65520/530 interfaces. The schematics are broken down into four main groups for discussion:

1) **System Bus Interface**
   - PC/AT-Bus (ISA 16-Bit)
   - PC/Chip (F8680) Bus Interface (ISA 8-Bit)
   - MC-Bus
   - 386 SL PI-Bus
   - 386 SX or 386 DX Local Bus

2) **Display Memory Interface**
   - Two or Four 256Kx4 DRAMs with optional Frame Buffer
   - Two 256Kx4 VRAMs with optional Frame Buffer
   - Four 256Kx4 VRAMs
   - Two 256Kx8 VRAMs
   - Two 128Kx8 PSRAMs with optional Frame Buffer
   - Two 512Kx8 DRAMs with optional Frame Buffer

3) **CRT / Flat Panel Interface**

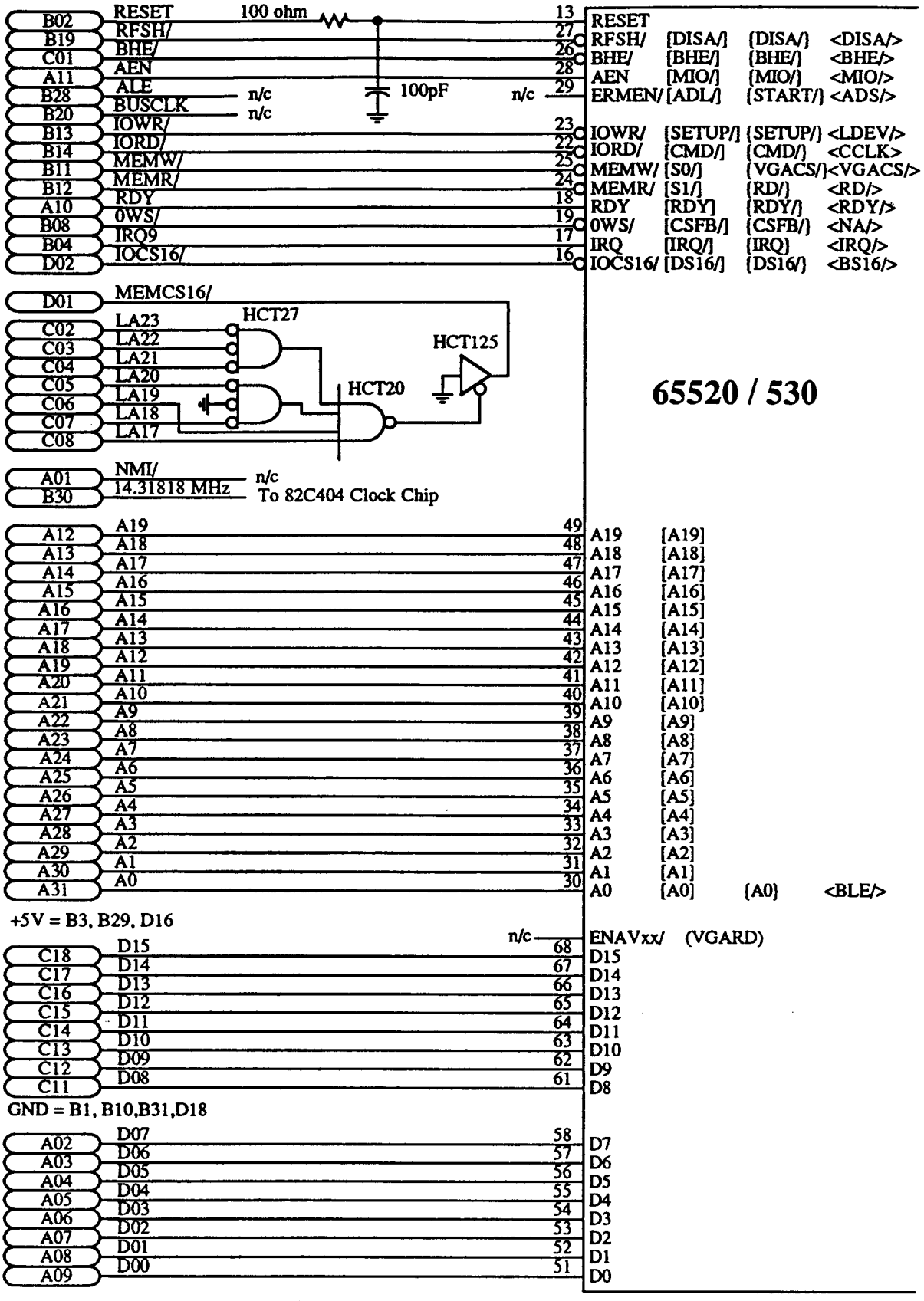
4) **Clock Interface (82C404 Clock Chip)**

To design a system around the 65520 or 65530, select one schematic page from each of the four groups above.

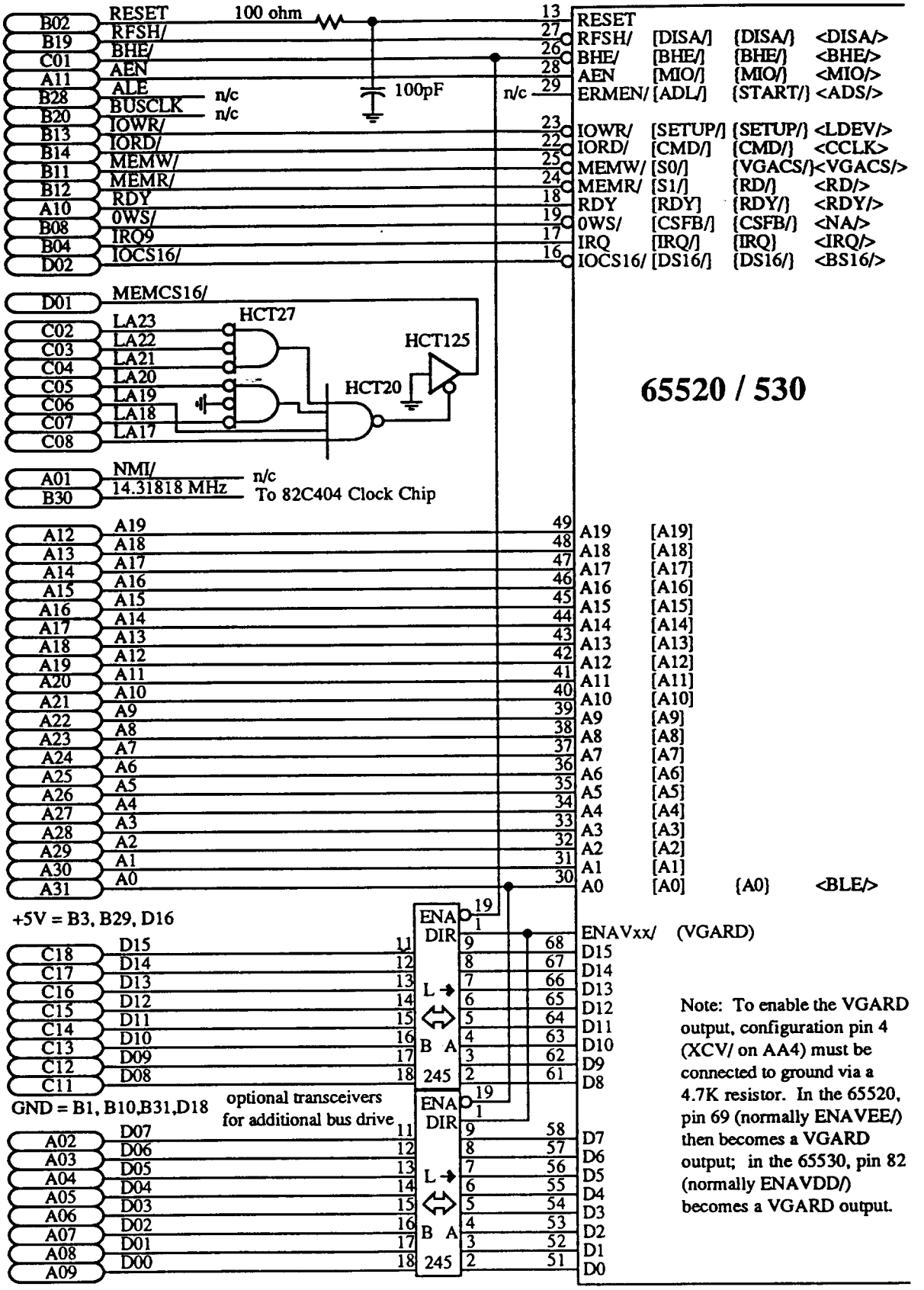
Selection of a bus interface for the VGA controller is generally dictated by the type of bus available in the system. If performance is a concern, however, and a 386 CPU is being used, a local bus interface should be used instead.

Selection of a memory interface involves several factors:

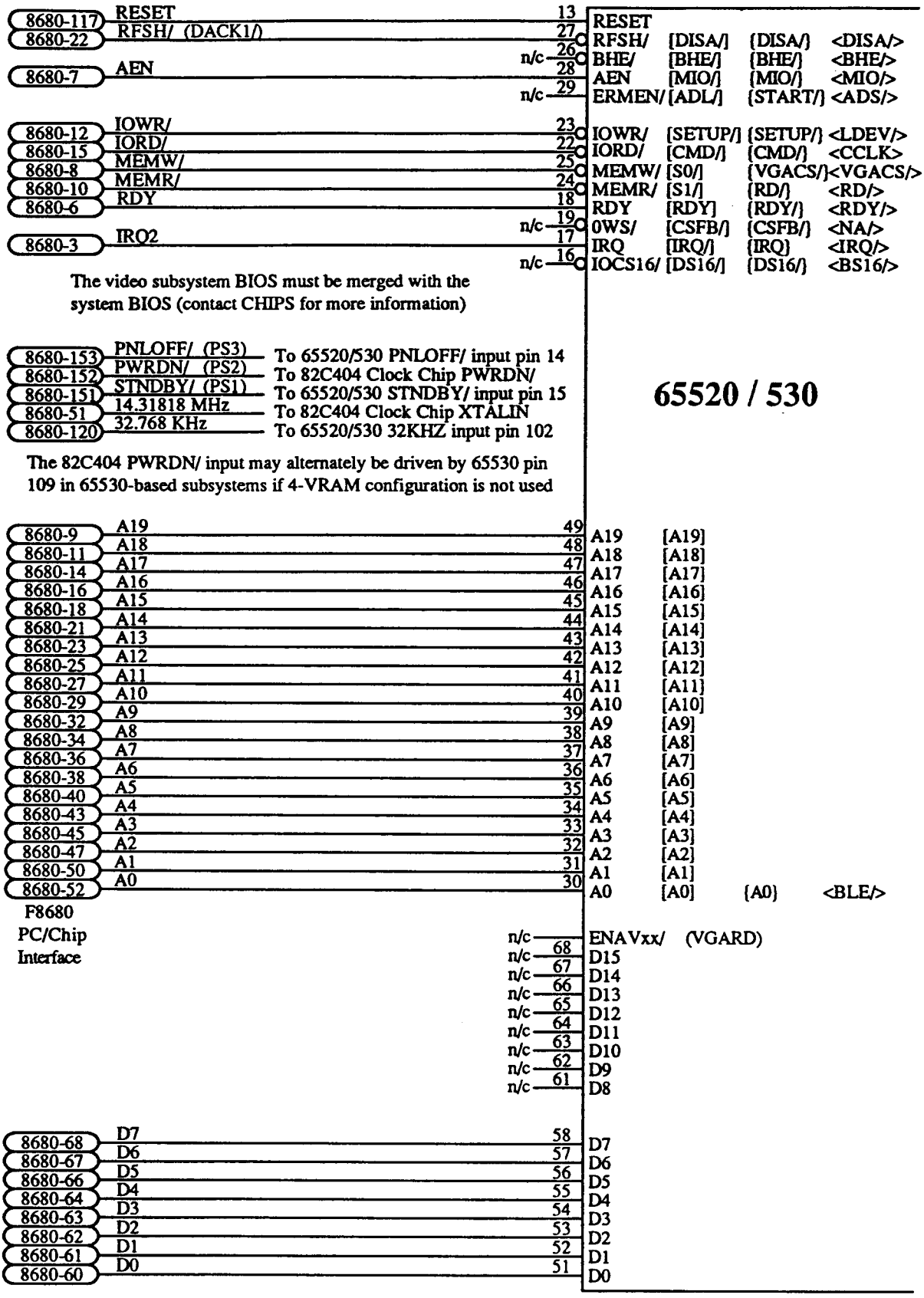
- Designing with four 256Kx4 DRAMs and a 64Kx4 VRAM frame buffer offers the most flexibility, allows interface to all panel types, and allows all 65520/530 features to be used. In this configuration, two of the DRAMs and the frame buffer can be left uninstalled on the PCB for the lowest cost subsystem (addition of the two extra DRAMs allows the use of Super-VGA modes of operation on CRTs; addition of the frame buffer allows the use of simultaneous display capability).
- Designing with VRAMs results in faster performance and lower power, but with a cost penalty (VRAMs are more expensive). An additional consideration is that some of the VRAM interface pins are used to support the frame buffer. As a result, the frame buffer can only be implemented in 256KB VRAM configurations (two 256Kx4 VRAMs) and cannot be implemented in 512KB display memory configurations (four 256Kx4 or two 256Kx8 VRAMs). As a result, 512KB VRAM memory configurations cannot be used if simultaneous display capability or interface to high-resolution flat panels (1024x768 monochrome) is required.
- Designing with two 512Kx8 DRAMs results in a total of 1MB of display memory with only two memory chips. This may result in less PCB space used by the graphics subsystem. However, the 256Kx4 DRAM configurations will generally be more cost effective, since generally only 512KB of display memory is required.
- Psuedo-Static RAMs may result in lower power, but require external data latches, since these pins do not have a standard DRAM row/column addressing scheme.
- Replacing the 64Kx4 VRAM frame buffer with a 256Kx4 VRAM allows interfacing to high resolution flat panel displays with frame acceleration.



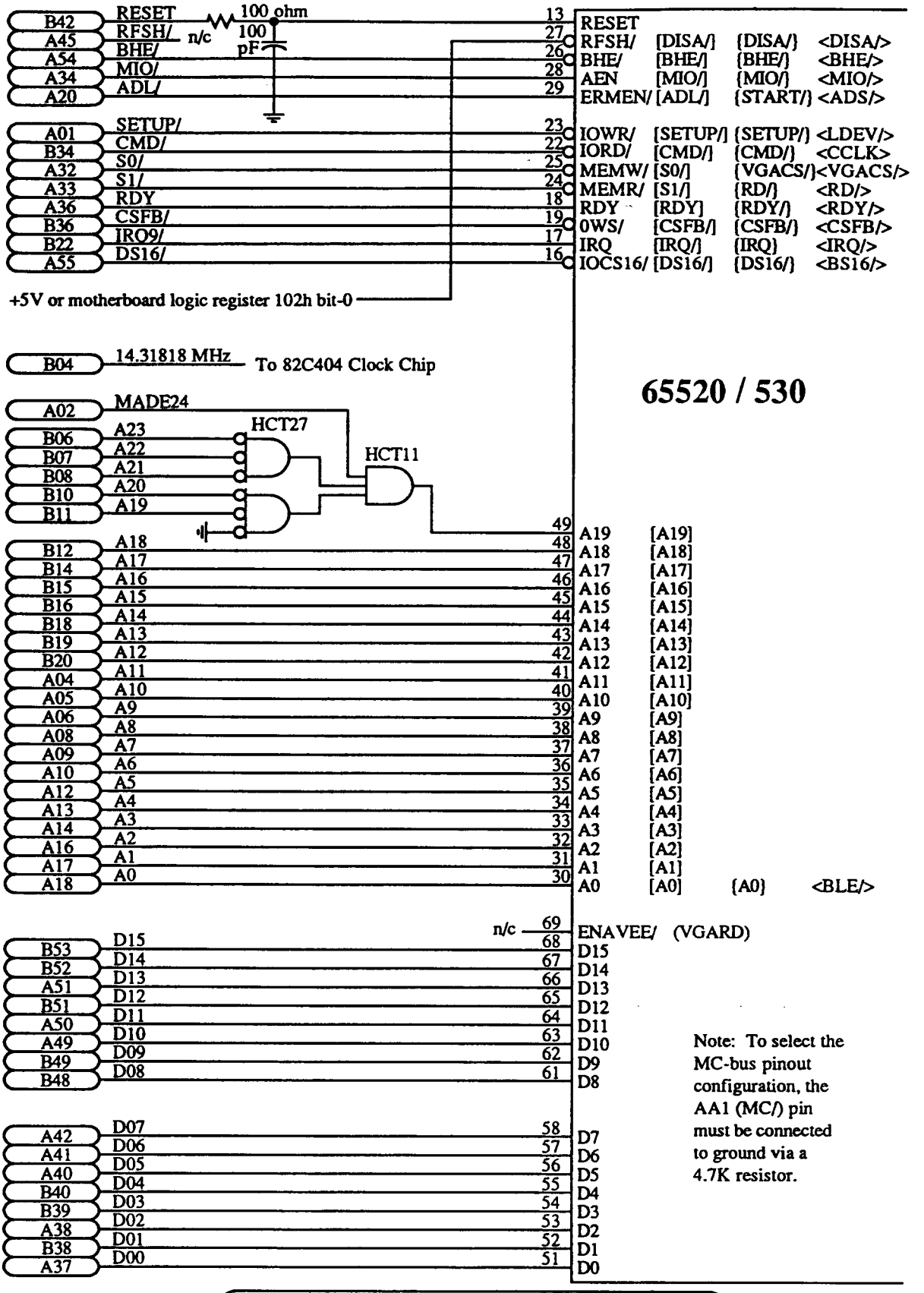
Circuit Example - 65520 / 530 Notebook ISA Bus



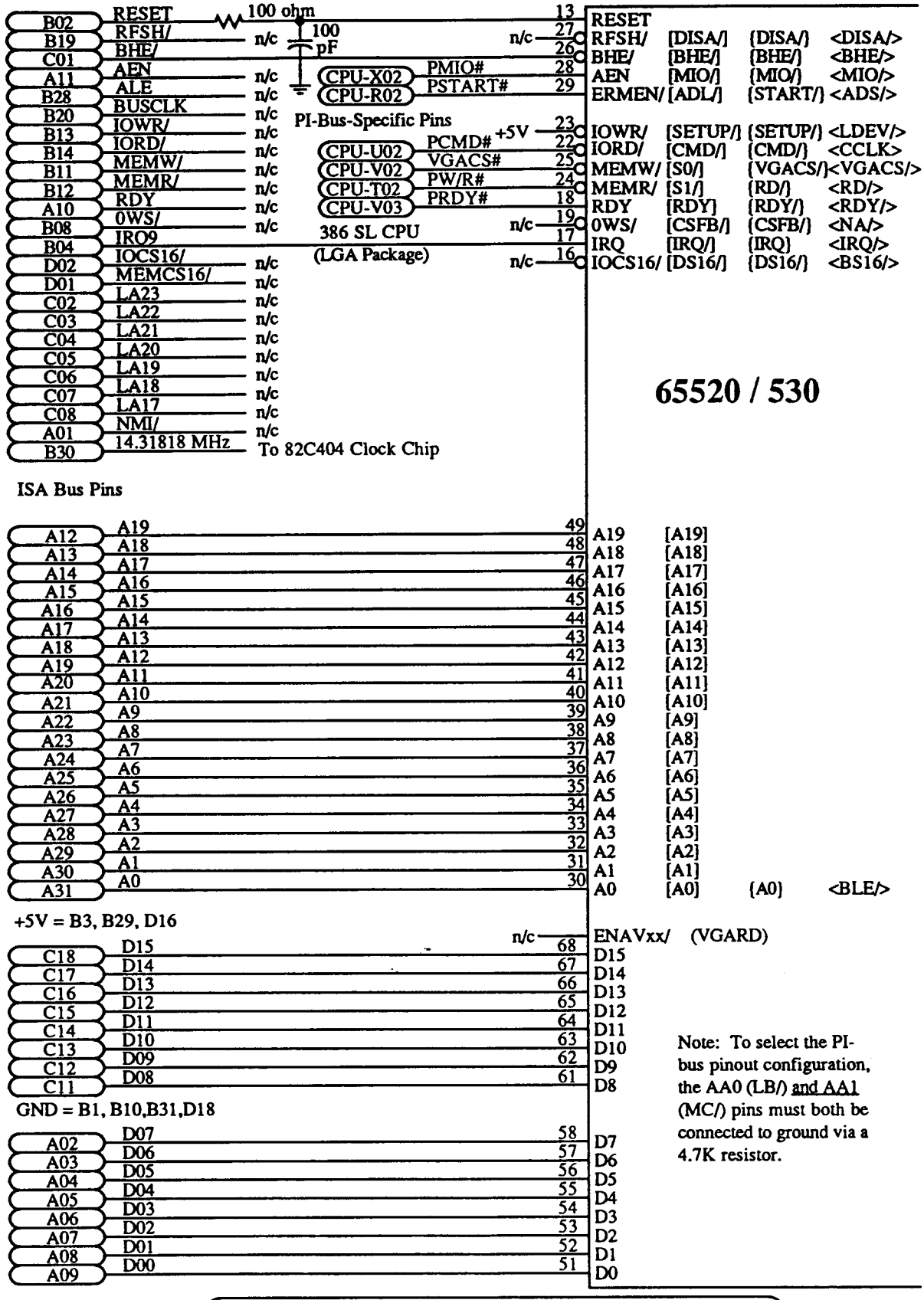
Circuit Example - 65520 / 530 Add-In Card ISA Bus (Extra Bus Drive Option)



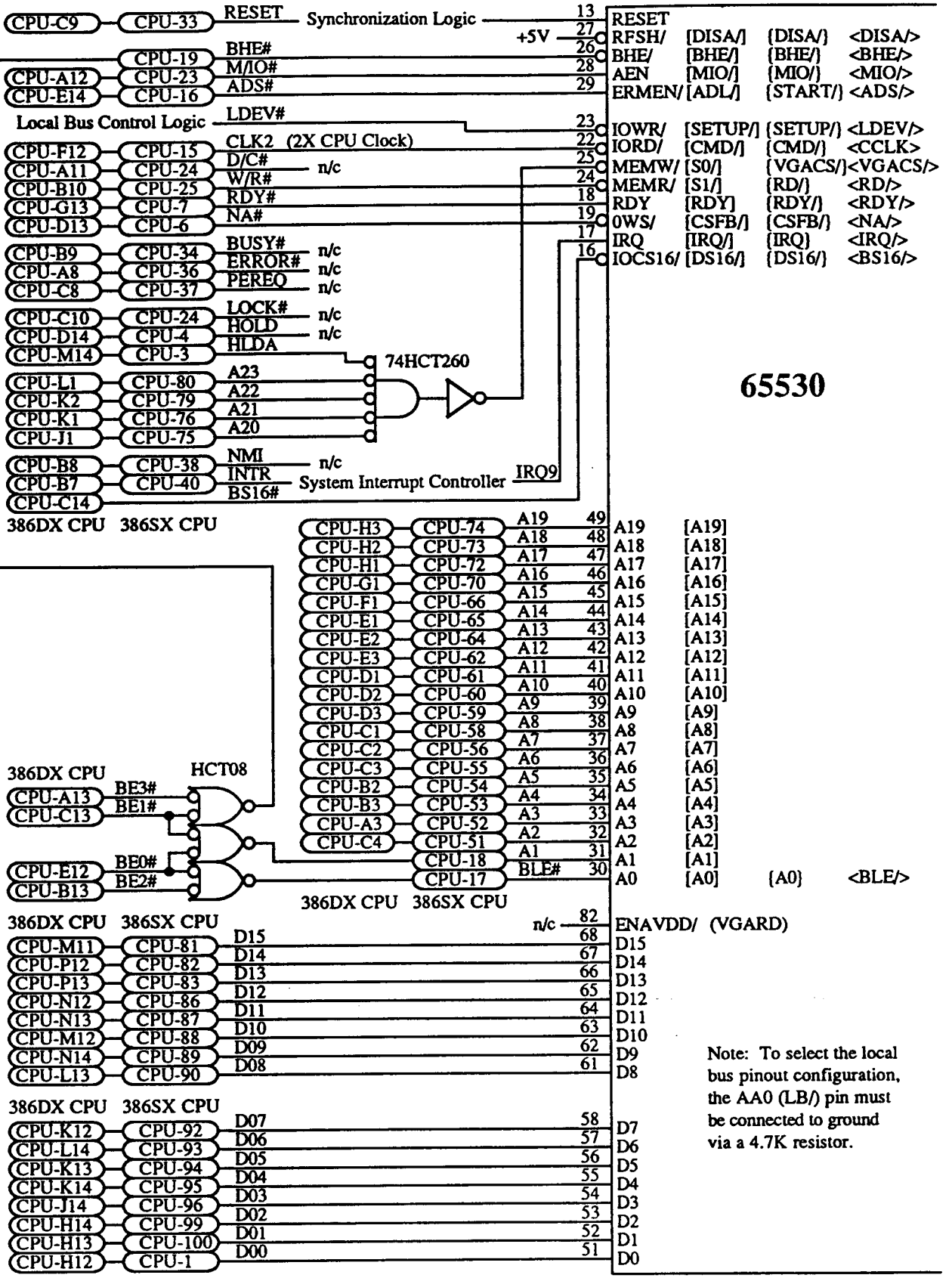
Circuit Example - 65520 / 530 Interface to PC/Chip (8-bit ISA Bus)



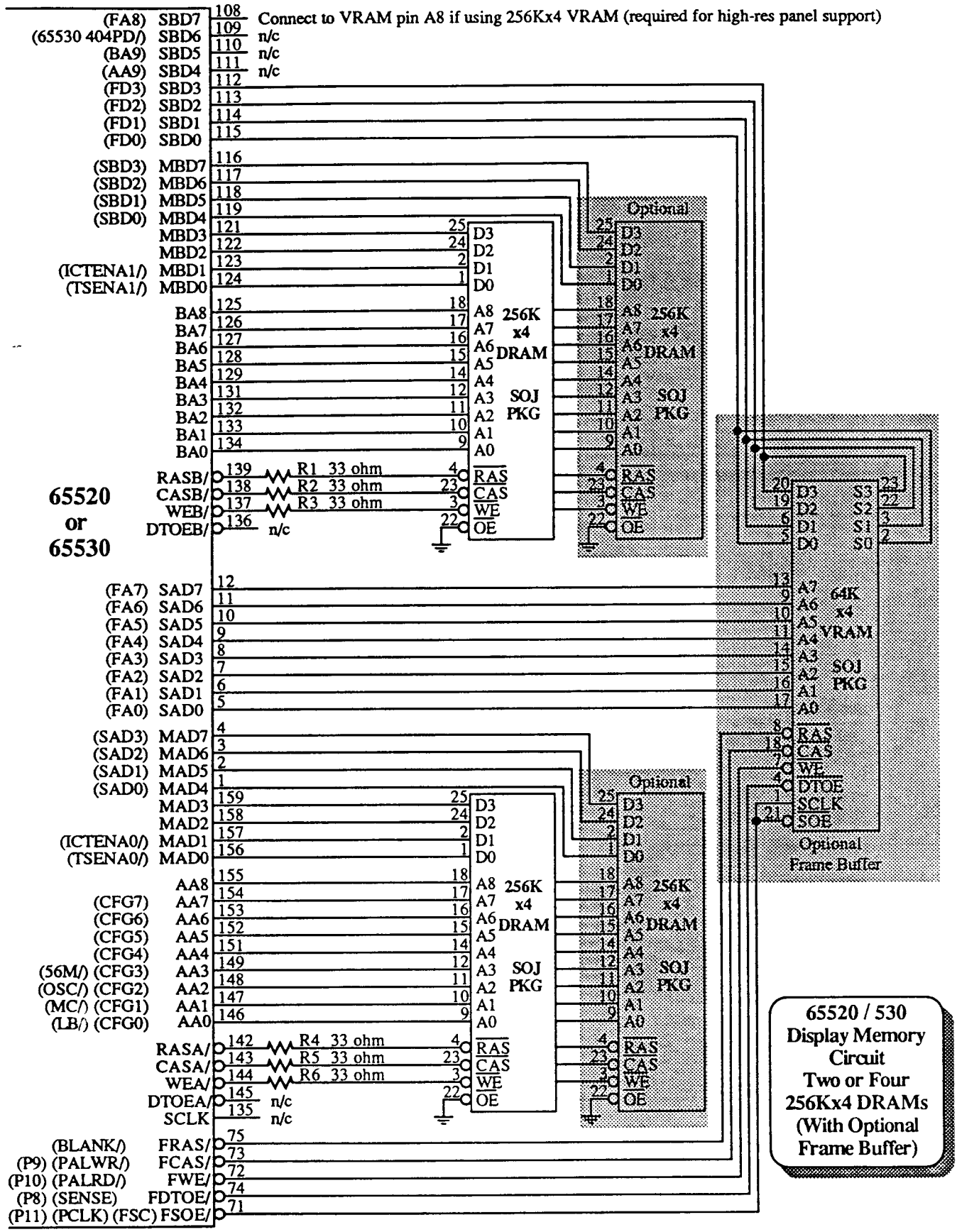
Circuit Example - 65520 / 530 Notebook MC Bus

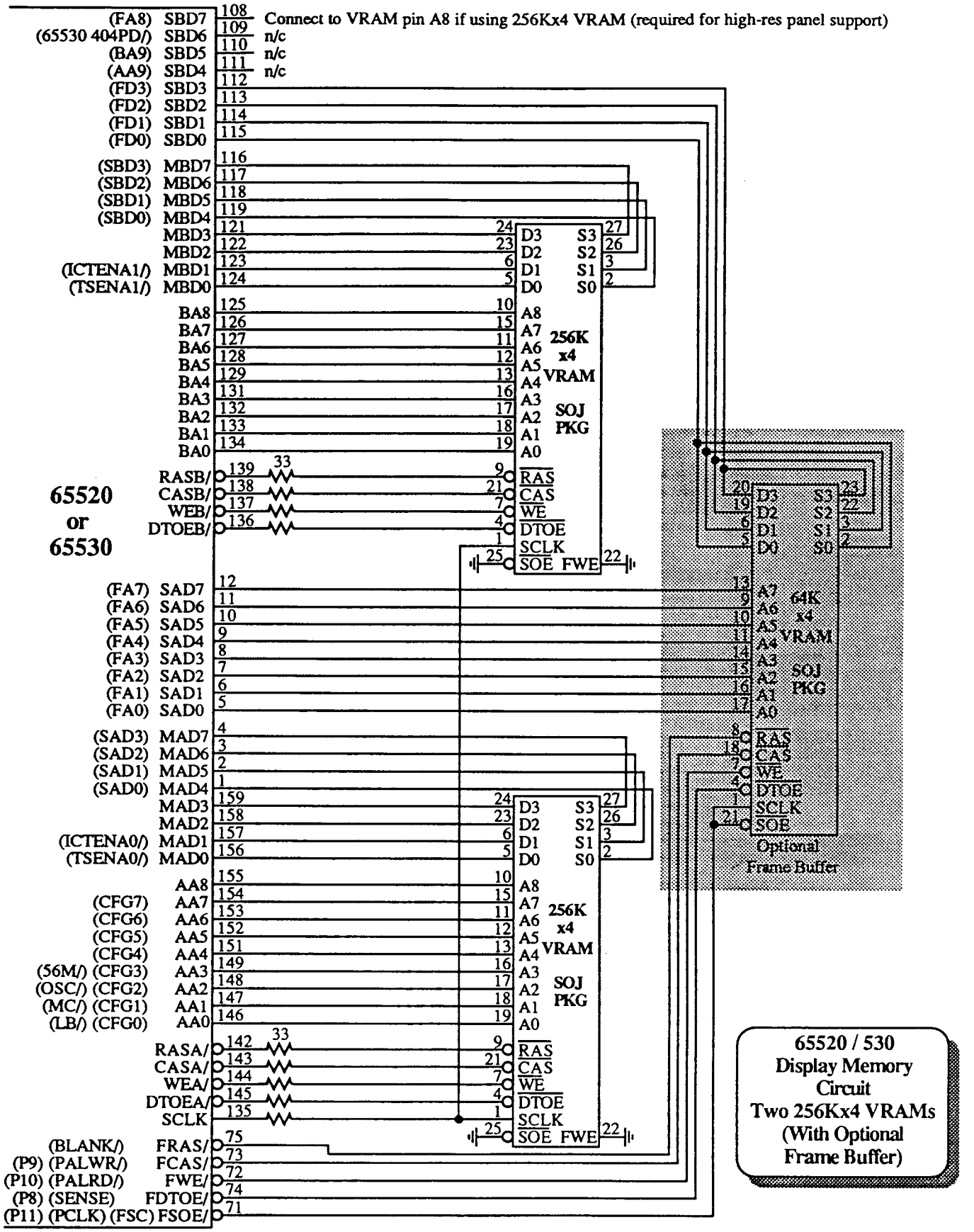


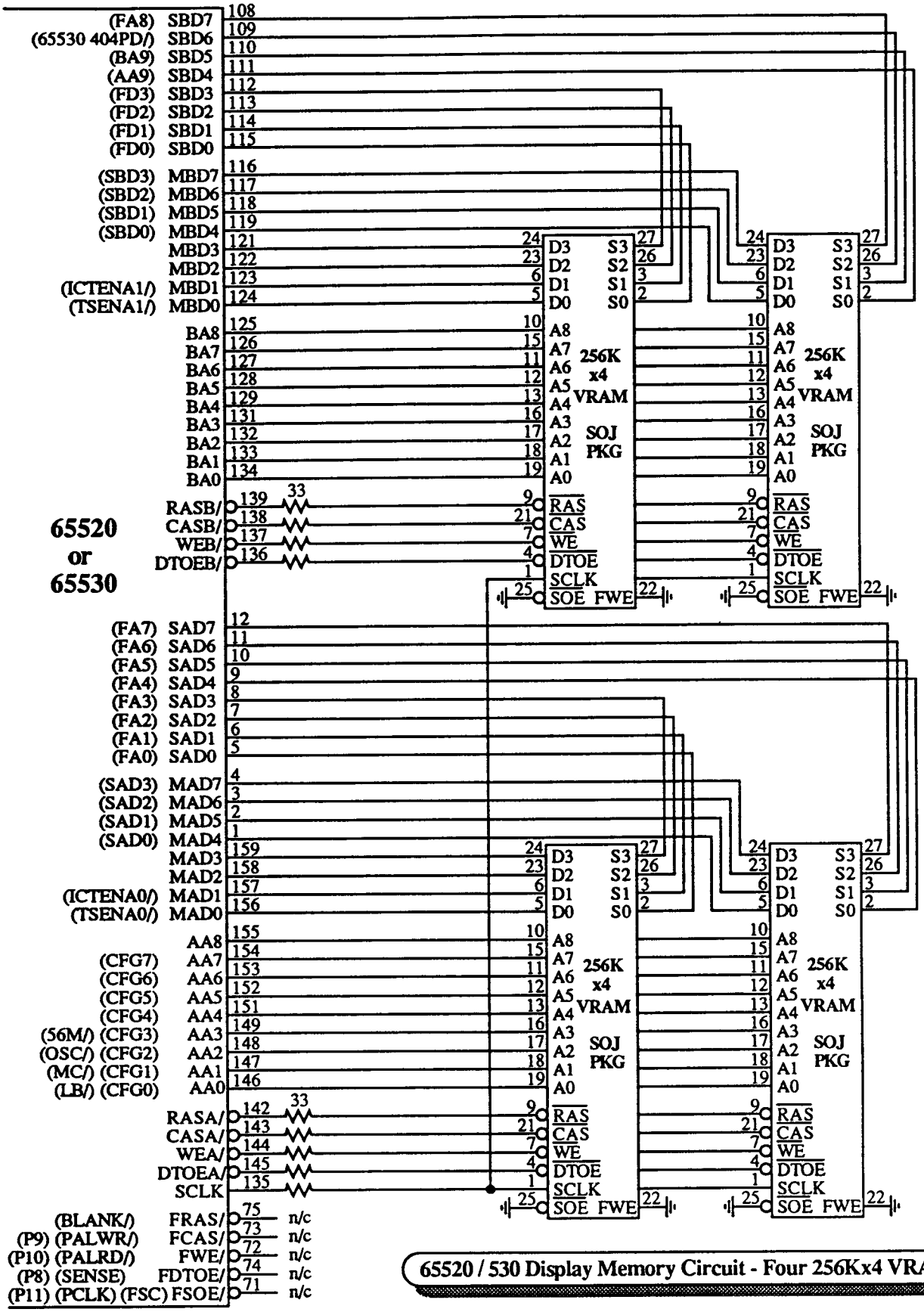
Circuit Example - 65520 / 530 Notebook PI Bus (386 SL)



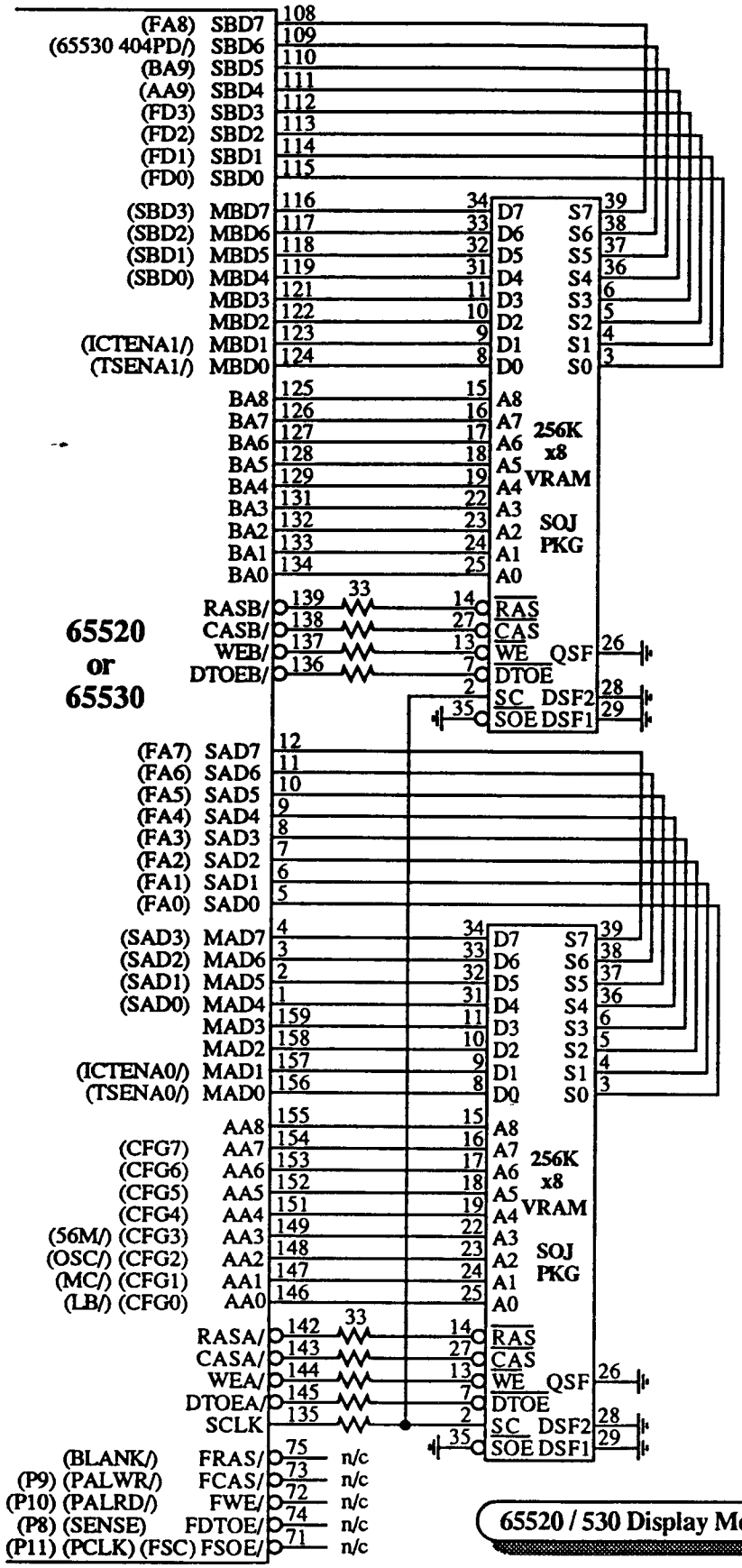
Circuit Example - 65530 Notebook 386SX/DX Local Bus


(FA8) SBD7 108
(65530 404PD/) SBD6 109
(BA9) SBD5 110
(AA9) SBD4 111
(FD3) SBD3 112
(FD2) SBD2 113
(FD1) SBD1 114
(FD0) SBD0 115
Connect to VRAM pin A8 if using 256Kx4 VRAM (required for high-res panel support)
n/c
n/c
n/c
(SBD3) MBD7 116
(SBD2) MBD6 117
(SBD1) MBD5 118
(SBD0) MBD4 119
MBD3 121
MBD2 122
(ICTENA1/) MBD1 123
(TSENA1/) MBD0 124
BA8 125
BA7 126
BA6 127
BA5 128
BA4 129
BA3 131
BA2 132
BA1 133
BA0 134
RASB/ 139 R1 33 ohm
CASB/ 138 R2 33 ohm
WEB/ 137 R3 33 ohm
DTOEB/ 136 n/c
65520 or 65530
D3 D2 D1 D0
A8 A7 A6 A5 A4 A3 A2 A1 A0
256K x4 DRAM SOJ PKG
RAS CAS WE OE
Optional
(FA7) SAD7 12
(FA6) SAD6 11
(FA5) SAD5 10
(FA4) SAD4 9
(FA3) SAD3 8
(FA2) SAD2 7
(FA1) SAD1 6
(FA0) SAD0 5
(SAD3) MAD7 4
(SAD2) MAD6 3
(SAD1) MAD5 2
(SAD0) MAD4 1
MAD3 159
MAD2 158
(ICTENA0/) MAD1 157
(TSENA0/) MAD0 156
AA8 155
(CFG7) AA7 154
(CFG6) AA6 153
(CFG5) AA5 152
(CFG4) AA4 151
(56M/) (CFG3) AA3 149
(OSC/) (CFG2) AA2 148
(MC/) (CFG1) AA1 147
(LB/) (CFG0) AA0 146
RASA/ 142 R4 33 ohm
CASA/ 143 R5 33 ohm
WEA/ 144 R6 33 ohm
DTOEA/ 145 n/c
SCLK 135 n/c
(BLANK/) FRAS/ 75
(P9) (PALWR/) FCAS/ 73
(P10) (PALRD/) FWE/ 72
(P8) (SENSE) FDTOE/ 74
(P11) (PCLK) (FSC) FSOE/ 71
D3 D2 D1 D0 S3 S2 S1 S0
A7 A6 A5 A4 A3 A2 A1 A0
64K x4 VRAM SOJ PKG
RAS CAS WE DTOE SCLK SOE
Optional Frame Buffer
65520 / 530 Display Memory Circuit Two or Four 256Kx4 DRAMs (With Optional Frame Buffer)

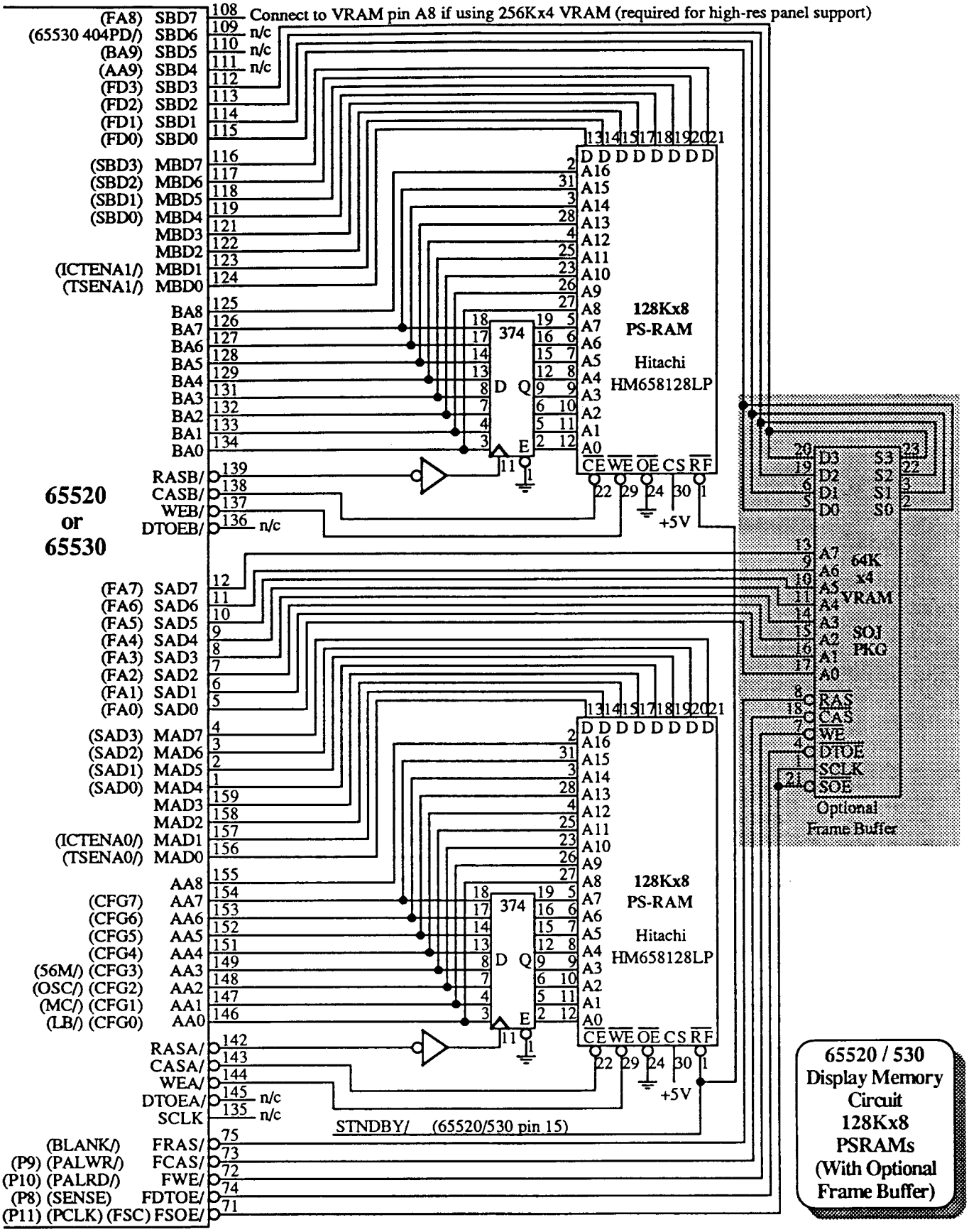

(FA8) SBD7
(65530 404PD/) SBD6
(BA9) SBD5
(AA9) SBD4
(FD3) SBD3
(FD2) SBD2
(FD1) SBD1
(FD0) SBD0
Connect to VRAM pin A8 if using 256Kx4 VRAM (required for high-res panel support)
n/c
n/c
n/c
(SBD3) MBD7
(SBD2) MBD6
(SBD1) MBD5
(SBD0) MBD4
MBD3
MBD2
(ICTENA1/) MBD1
(TSENA1/) MBD0
BA8
BA7
BA6
BA5
BA4
BA3
BA2
BA1
BA0
RASB/
CASB/
WEB/
DTOEB/
65520
or
65530
(FA7) SAD7
(FA6) SAD6
(FA5) SAD5
(FA4) SAD4
(FA3) SAD3
(FA2) SAD2
(FA1) SAD1
(FA0) SAD0
(SAD3) MAD7
(SAD2) MAD6
(SAD1) MAD5
(SAD0) MAD4
MAD3
MAD2
(ICTENA0/) MAD1
(TSENA0/) MAD0
AA8
(CFG7) AA7
(CFG6) AA6
(CFG5) AA5
(CFG4) AA4
(56M/) (CFG3) AA3
(OSC/) (CFG2) AA2
(MC/) (CFG1) AA1
(LB/) (CFG0) AA0
RASA/
CASA/
WEA/
DTOEA/
SCLK
(BLANK/) FRAS/
(P9) (PALWR/) FCAS/
(P10) (PALRD/) FWE/
(P8) (SENSE) FDTOE/
(P11) (PCLK) (FSC) FSOE/
256K x4 VRAM SOJ PKG
64K x4 VRAM SOJ PKG
Optional Frame Buffer
65520 / 530
Display Memory
Circuit
Two 256Kx4 VRAMs
(With Optional
Frame Buffer)



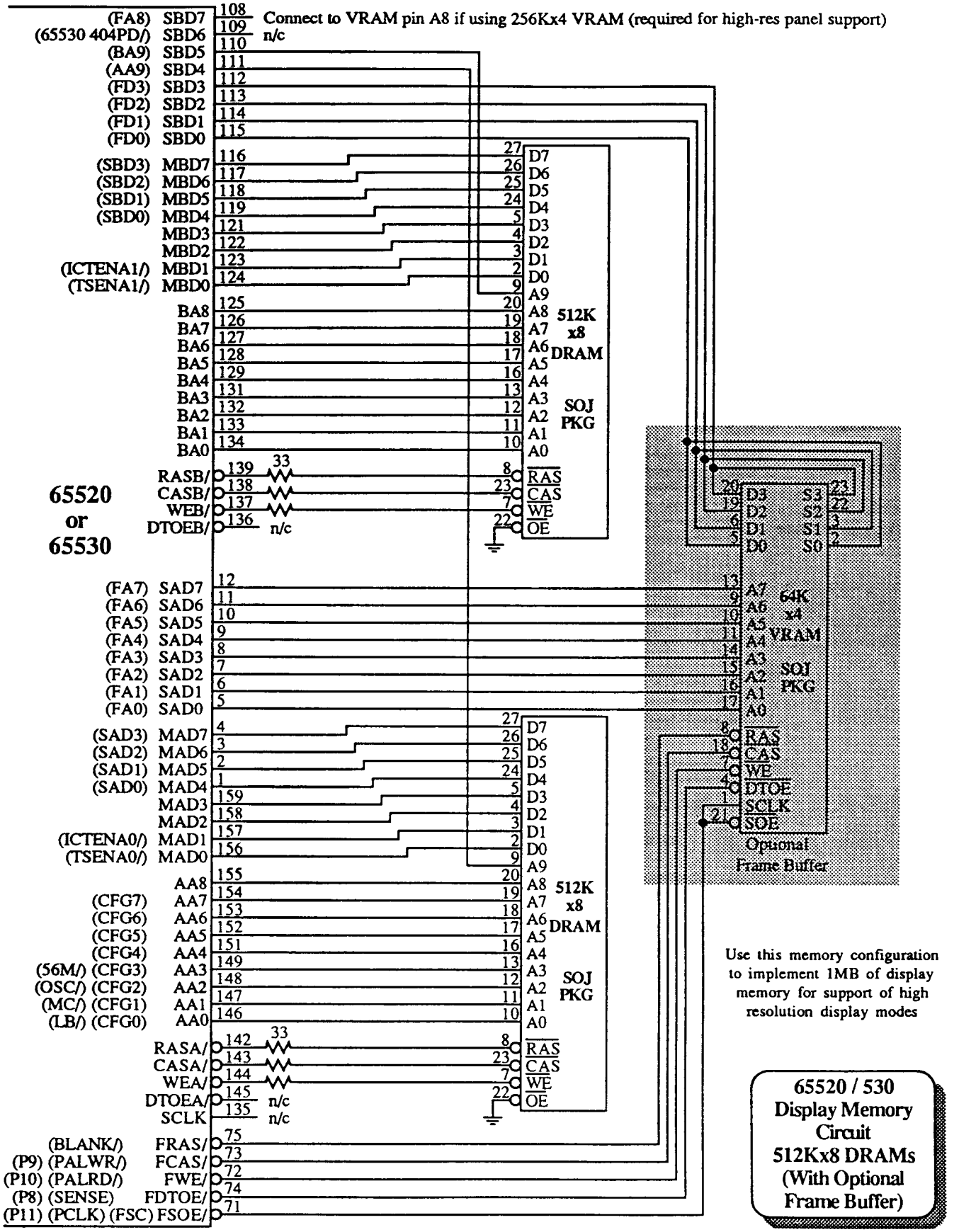
65520 / 530 Display Memory Circuit - Four 256Kx4 VRAMs



65520 / 530 Display Memory Circuit - Two 256Kx8 VRAMs

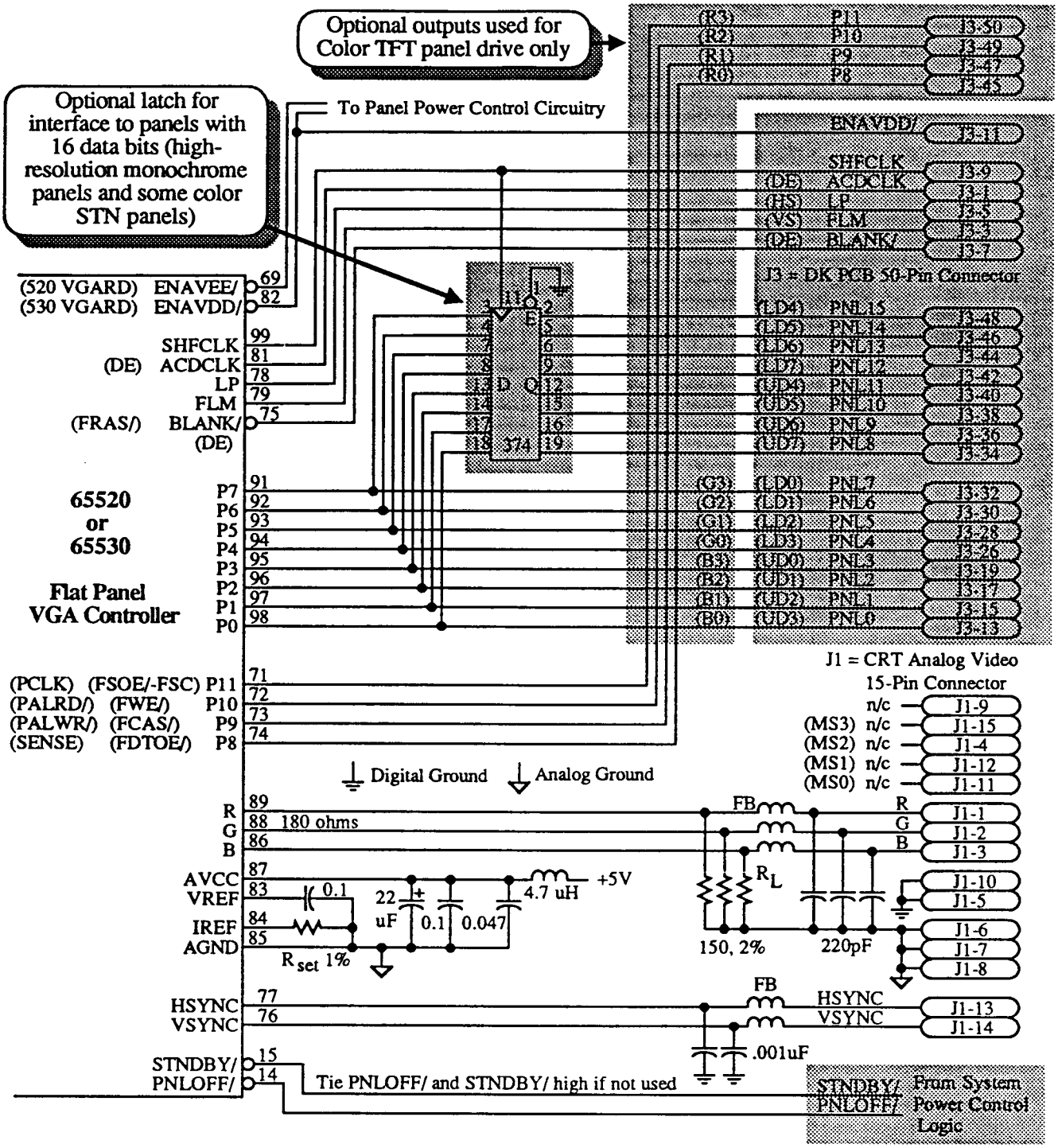


65520 / 530 Display Memory Circuit 128Kx8 PSRAMs (With Optional Frame Buffer)



Use this memory configuration to implement 1MB of display memory for support of high resolution display modes

65520 / 530 Display Memory Circuit 512Kx8 DRAMs (With Optional Frame Buffer)



65520 / 530 Rset Calculations

The following equations are used to determine the optimal Rset value for the 65520 or 65530:

$$Iref = \frac{VBGAP}{Rset}$$

$$Idac = Ratio \times Iref \quad \text{(where Ratio = 2.1)}$$

$$Idac = \frac{2.1 \times VBGAP}{Rset} \quad \text{(where VBGAP = 1.23V)}$$

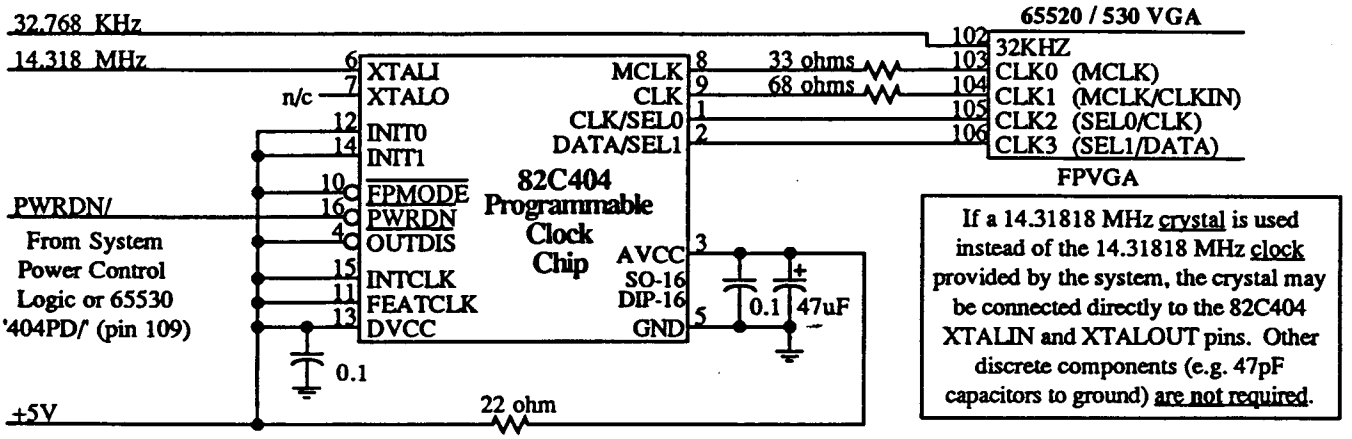
$$Rset = \frac{2.1 \times VBGAP}{Idac}$$

For doubly terminated outputs (RLOAD plus CRT monitor load of 75Ω), Rcolor = 50Ω for RL=150Ω and Rcolor = 37.5Ω for RL=75Ω. For 0.7V full scale output voltage, calculations are:

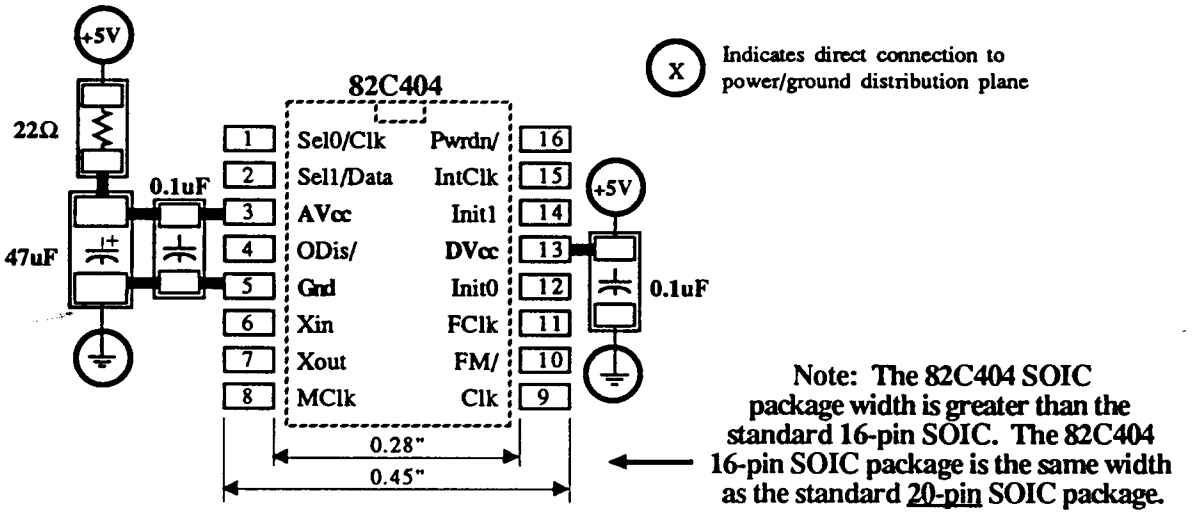
for RL=150Ω: Idac = 0.7 + 50.0 = 35.0 mA
for RL=75Ω: Idac = 0.7 + 37.5 = 18.6 mA

for RL=150Ω: Rset = (2.1 x 1.23 + 35.0) x 1000 = 74Ω
for RL=75Ω: Rset = (2.1 x 1.23 + 18.6) x 1000 = 138Ω

Circuit Example - 65520 / 530 CRT / FP Interface



Circuit Example - 65520 / 530 to 82C404 Clock Chip



82C404 Recommended PCB Layout

—This Page Intentionally Left Blank—

Flat Panel Interface Examples

This section includes schematic examples showing how to connect the 65520 / 530 to various flat panel displays.

Monochrome Panels

	Manufacturer	Part Number	Panel Resolution	Panel Technology	Panel Drive	Panel Interface	Panel Data Transfer	Panel Gray Levels
1)	Epson	EG-9005F-LS	640x480	LCD	DD	8-Bit	8 Pixels/Clk	2
2)	Citizen	G6481L-FF	640x480	LCD	DD	8-Bit	8 Pixels/Clk	2
3)	Sharp	LM64P80	640x480	LCD	DD	8-Bit	8 Pixels/Clk	2
4)	Sanyo	LCM-6494-24NAC	640x480	LCD	DD	8-Bit	8 Pixels/Clk	2
5)	Hitachi	LMG5162XUFC	640x480	LCD	DD	8-Bit	8 Pixels/Clk	2
6)	Matsushita	S804	640x480	Plasma	SS	8-Bit	2 Pixels/Clk	16
7)	Sharp	LJ64ZU50	640x480	EL	SS	8-Bit	2 Pixels/Clk	16

High Resolution Panels

	Manufacturer	Part Number	Panel Resolution	Panel Technology	Panel Drive	Panel Interface	Panel Data Transfer	Panel Gray Levels
8)	Hitachi	LMG9100ZZFC	1280x1024	LCD	DD	16-Bit	16 Pixels/Clk	2
9)	Hitachi	LMG9050ZZFC	1024x768	LCD	DD	16-Bit	16 Pixels/Clk	2
10)	Sharp	LM10P10	1024x768	LCD	DD	16-Bit	16 Pixels/Clk	2
11)	Sanyo	LCM-5491-24NAK	1024x768	LCD	DD	16-Bit	16 Pixels/Clk	2

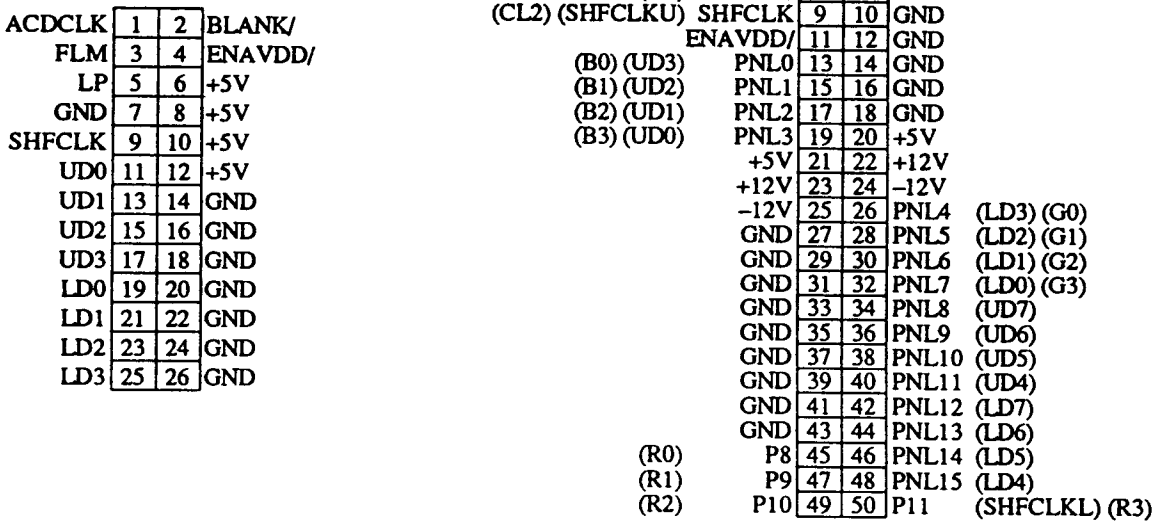
Color Panels

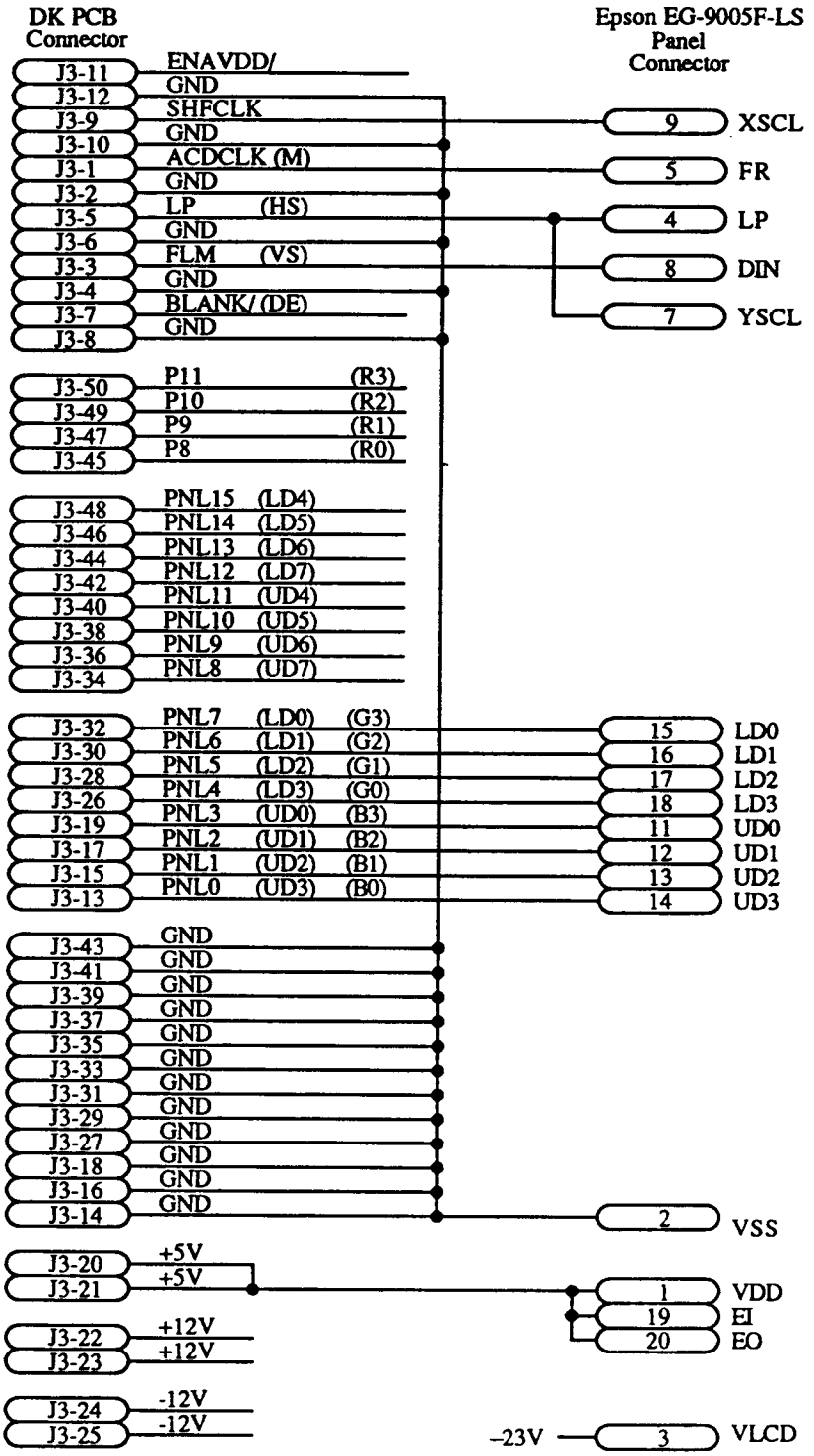
	Manufacturer	Part Number	Panel Resolution	Panel Technology	Panel Drive	Panel Interface	Panel Data Transfer	Panel Colors
12)	Hitachi	TM26D50VC2AA	640x480x3	TFT LCD	SS	9-Bit	1 Pixel/Clk	512
13)	Sharp	LQ9D011	640x480x3	TFT LCD	SS	9-Bit	1 Pixel/Clk	512
14)	Optrex †	DMF6121	640x480x3	STN LCD	SS	16-Bit	5-1/3 Pixels/Clk	8
15)	Sanyo †	LCM5313/5314-22NAK	640x480x3	STN LCD	SS	16-Bit	5-1/3 Pixels/Clk	8
16)	Sanyo †	LCM5327-24NAK	640x480x3	STN LCD	SS	16-Bit	5-1/3 Pixels/Clk	8
17)	Seiko †	X642G	640x480x3	STN LCD	SS	8-Bit	2-2/3 Pixels/Clk	8
18)	Sharp †	LM64C03P	640x480x3	STN LCD	SS	8-Bit	2-2/3 Pixels/Clk	8

† = Requires 65530 to support Color STN LCD Panels

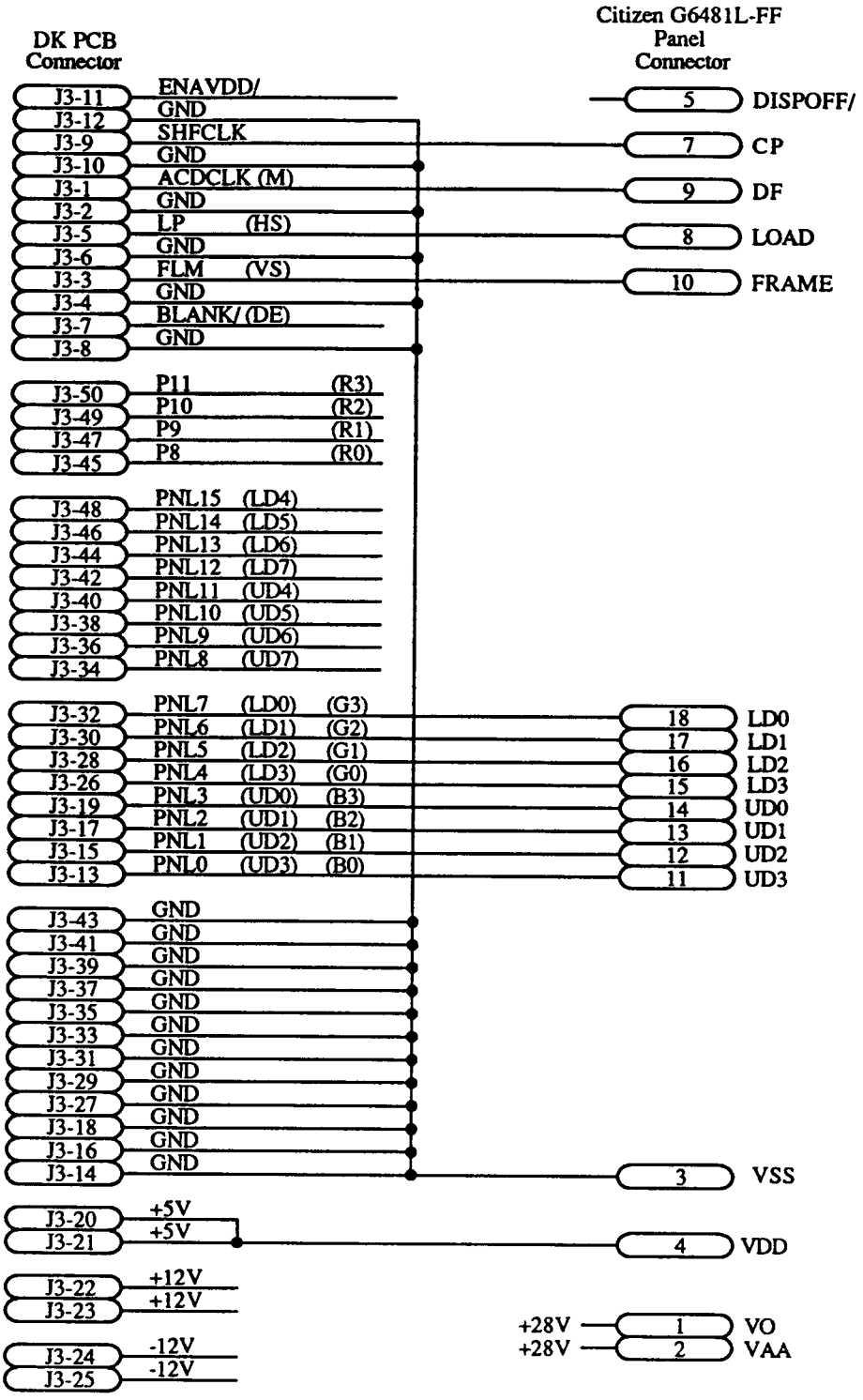
SS = Single Panel Single Scan
DD = Dual Panel Dual Scan
TFT = Thin Film Transistor
STN = Super Twist Nematic

65520 65530 Pin #	65520 65530 Pin Name	PCB Signal Name	DK Board 26-Pin Connector	DK Board 50-Pin Connector	Mono Single Panel	Mono Dual Panel	Color TFT Panel	Color STN 4-bit Pack	Color STN Extended 4-bit Pack
98	P0	PNL0	17	13	P0	UD3	B0	R0	R0-G0-G5-B5-B10-R11
97	P1	PNL1	15	15	P1	UD2	B1	G0	B0-R1-R6-G6-G11-B11
96	P2	PNL2	13	17	P2	UD1	B2	B0	G1-B1-B6-R7-R12-G12
95	P3	PNL3	11	19	P3	UD0	B3	R1	R2-G2-G7-B7-B12-R13
94	P4	PNL4	25	26	P4	LD3	G0	G1	B2-R3-R8-G8-G13-B13
93	P5	PNL5	23	28	P5	LD2	G1	B1	G3-B3-B8-R9-R14-G14
92	P6	PNL6	21	30	P6	LD1	G2	R2	R4-G4-G9-B9-B14-R15
91	P7	PNL7	19	32	P7	LD0	G3	G2	B4-R5-R10-G10-G15-B15
n/a	Latched P0	PNL8	–	34	–	UD7	–	B2	–
n/a	Latched P1	PNL9	–	36	–	UD6	–	R3	–
n/a	Latched P2	PNL10	–	38	–	UD5	–	G3	–
n/a	Latched P3	PNL11	–	40	–	UD4	–	B3	–
n/a	Latched P4	PNL12	–	42	–	LD7	–	R4	–
n/a	Latched P5	PNL13	–	44	–	LD6	–	G4	–
n/a	Latched P6	PNL14	–	46	–	LD5	–	B4	–
n/a	Latched P7	PNL15	–	48	–	LD4	–	R5	–
74	FDTOE/	P8	–	45	–	–	R0	–	–
73	FCAS/	P9	–	47	–	–	R1	–	–
72	FWE/	P10	–	49	–	–	R2	–	–
71	FSOE/	P11	–	50	–	–	R3	–	SHFCLKL
99	SHFCLK	SHFCLK	9	9	CL2	CL2	CL2	CL2	SHFCLKU
81	ACDCLK	ACDCLK	1	1	M	M	M	M	M
79	FLM	FLM	3	3	FLM	FLM	FLM	FLM	FLM
78	LP	LP	5	5	CL1	CL1	CL1	CL1	CL1
75	FRAS/	BLANK/ (DE)	2	7	–	–	–	–	–
82	ENAVDD/	ENAVDD/	4	11	–	–	–	–	–
–	–	VCC	6,8	20,21	–	–	–	–	–
–	–	VCC	10,12	–	–	–	–	–	–
–	–	GND	7,14	2,4,6,8,10	–	–	–	–	–
–	–	GND	16,18	12,14,16,18	–	–	–	–	–
–	–	GND	20,22	27,29,31,33	–	–	–	–	–
–	–	GND	24,26	37,39,41,43	–	–	–	–	–

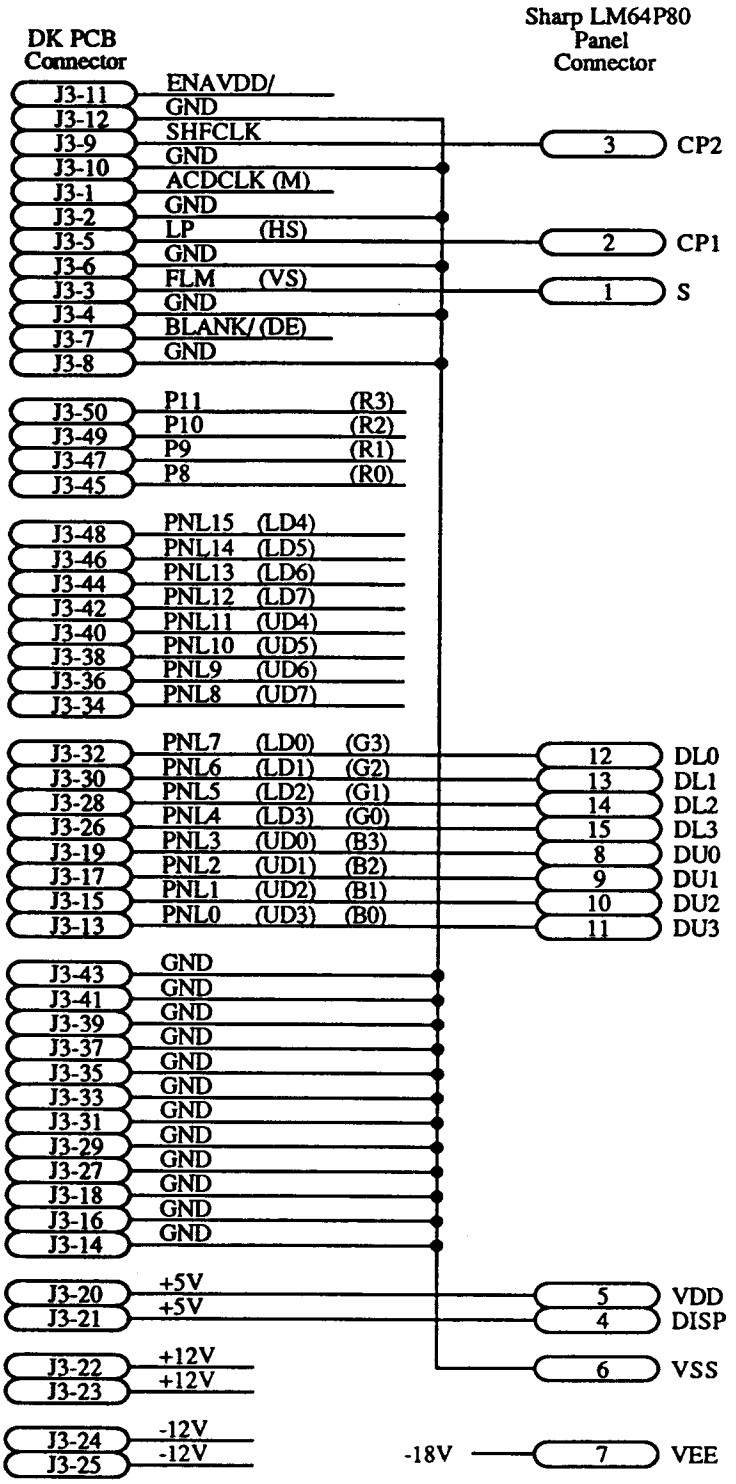




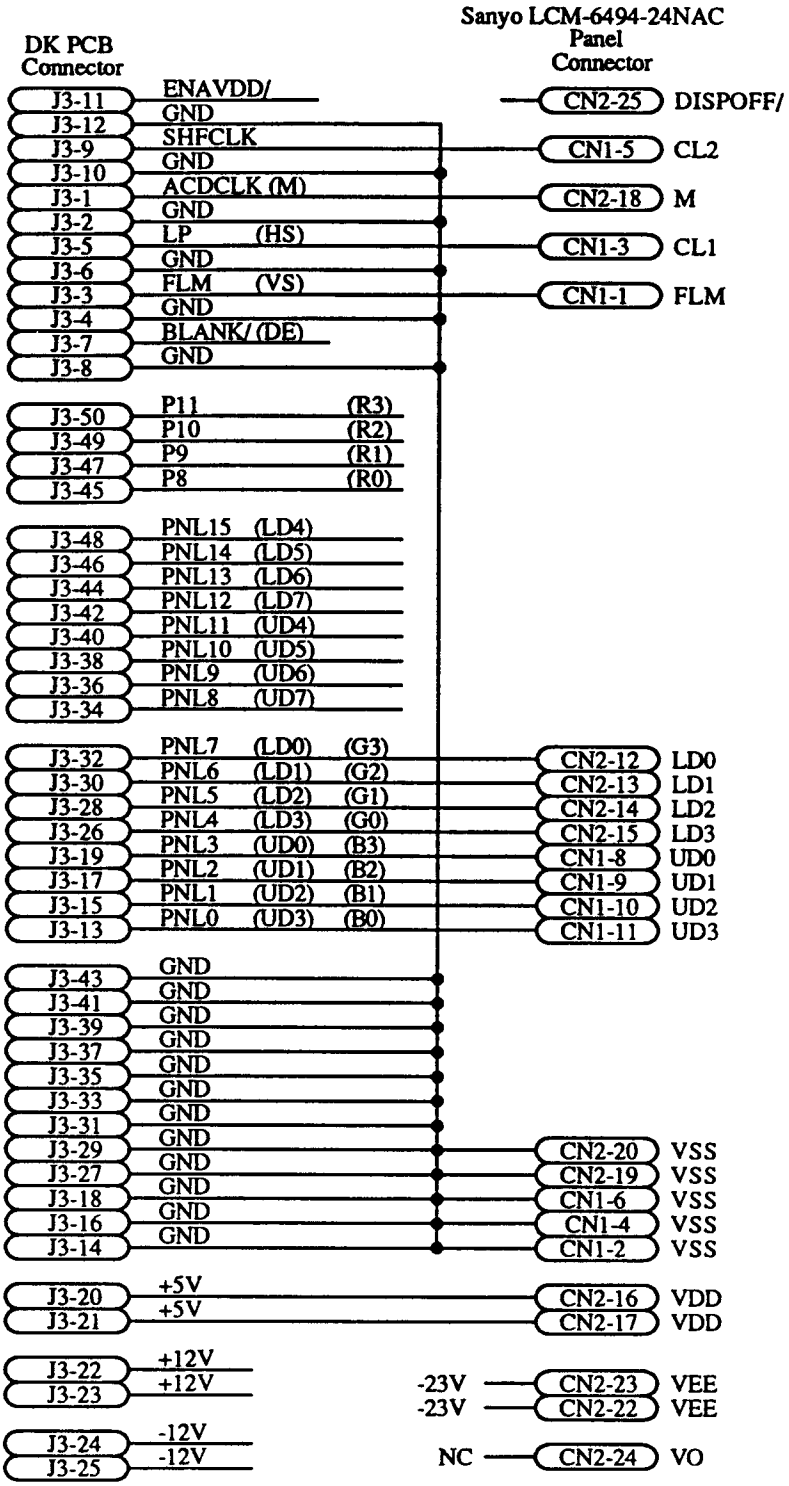
65520 / 530 Interface - Epson EG-9005F-LS (640x480 Monochrome LCD DD Panel)



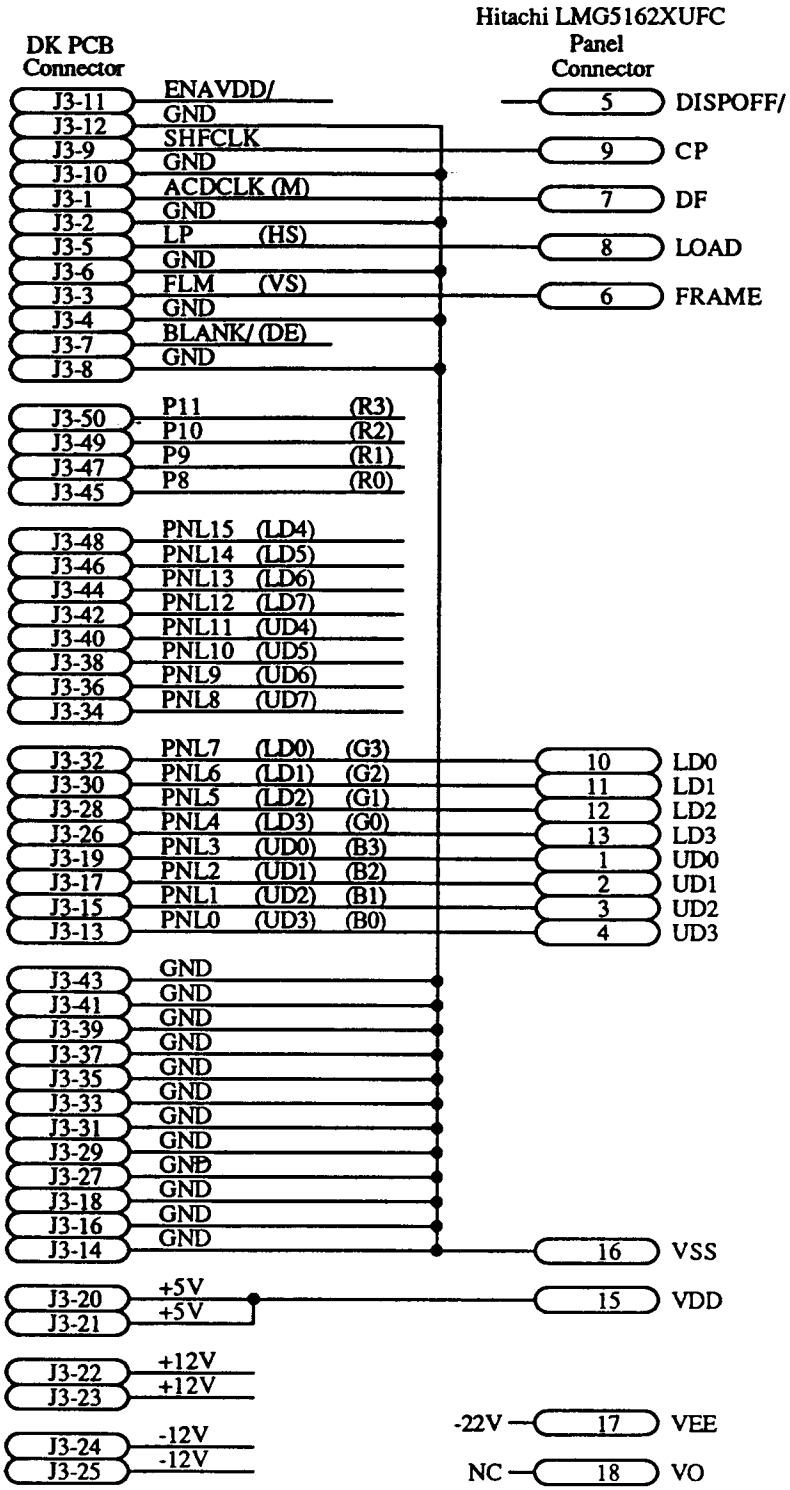
65520 / 530 Interface - Citizen G6481L-FF (640x480 Monochrome LCD DD Panel)



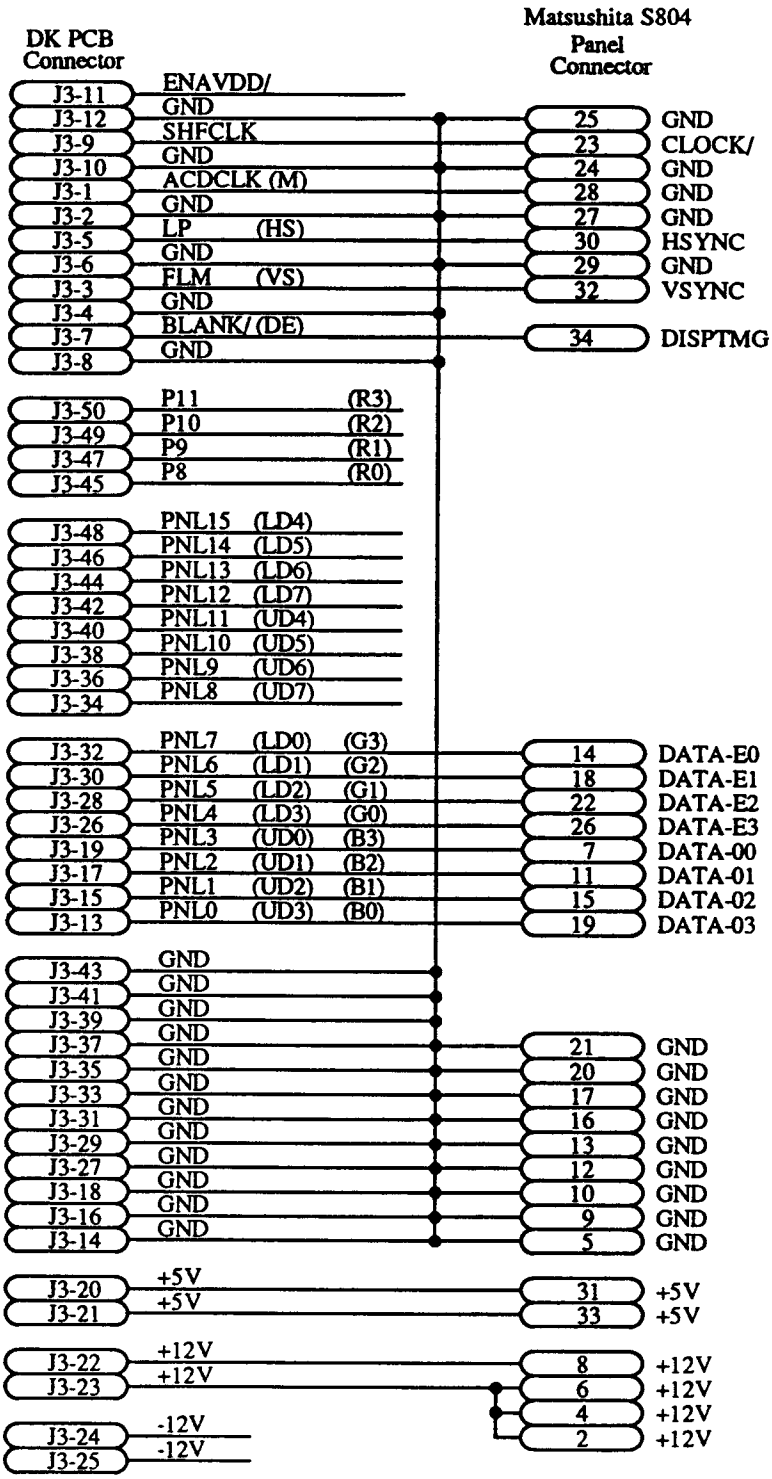
65520 / 530 Interface - Sharp LM64P80 (640x480 Monochrome LCD DD Panel)



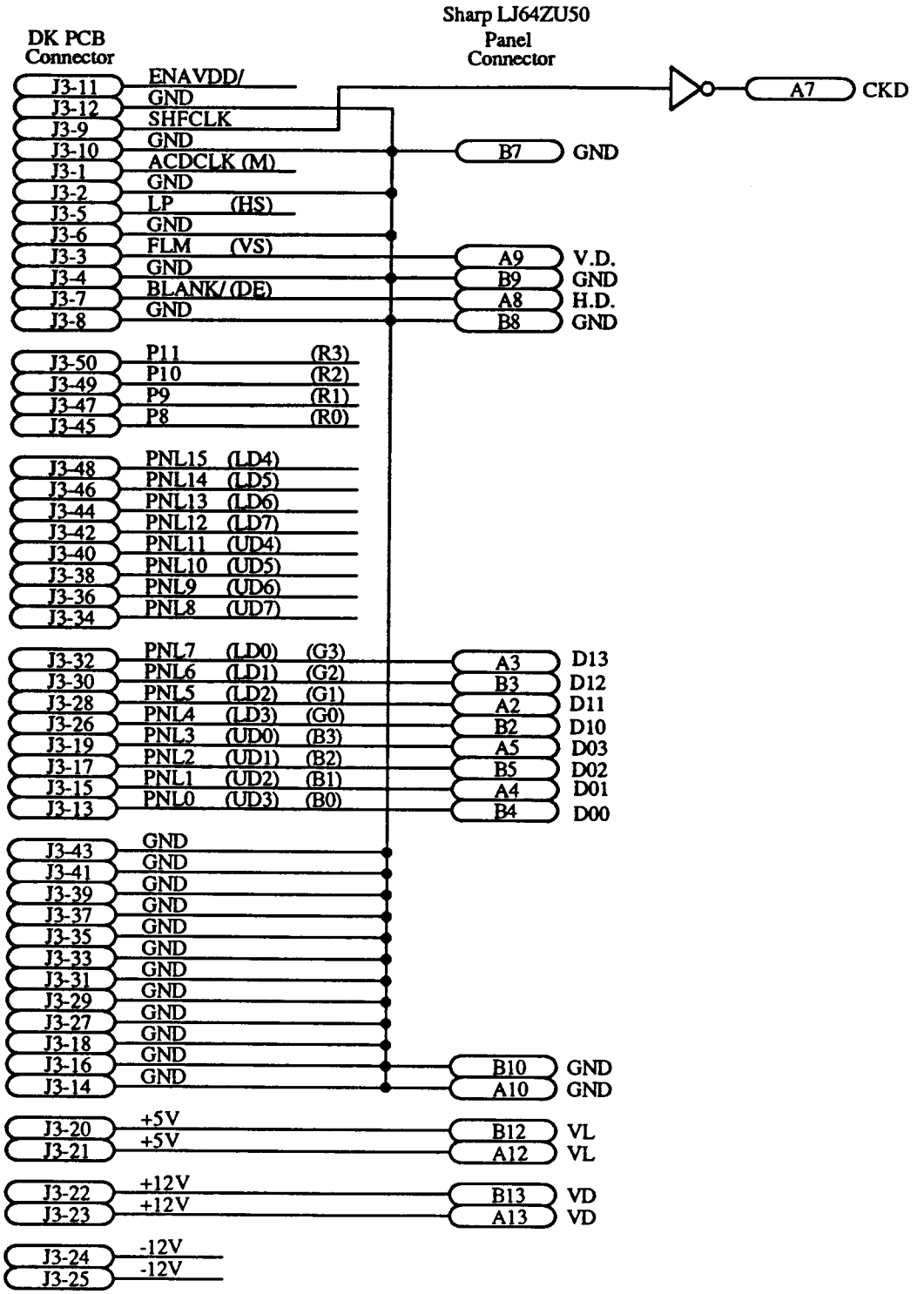
65520 / 530 Interface - Sanyo LCM-6494-24NAC (640x480 Monochrome LCD DD Panel)



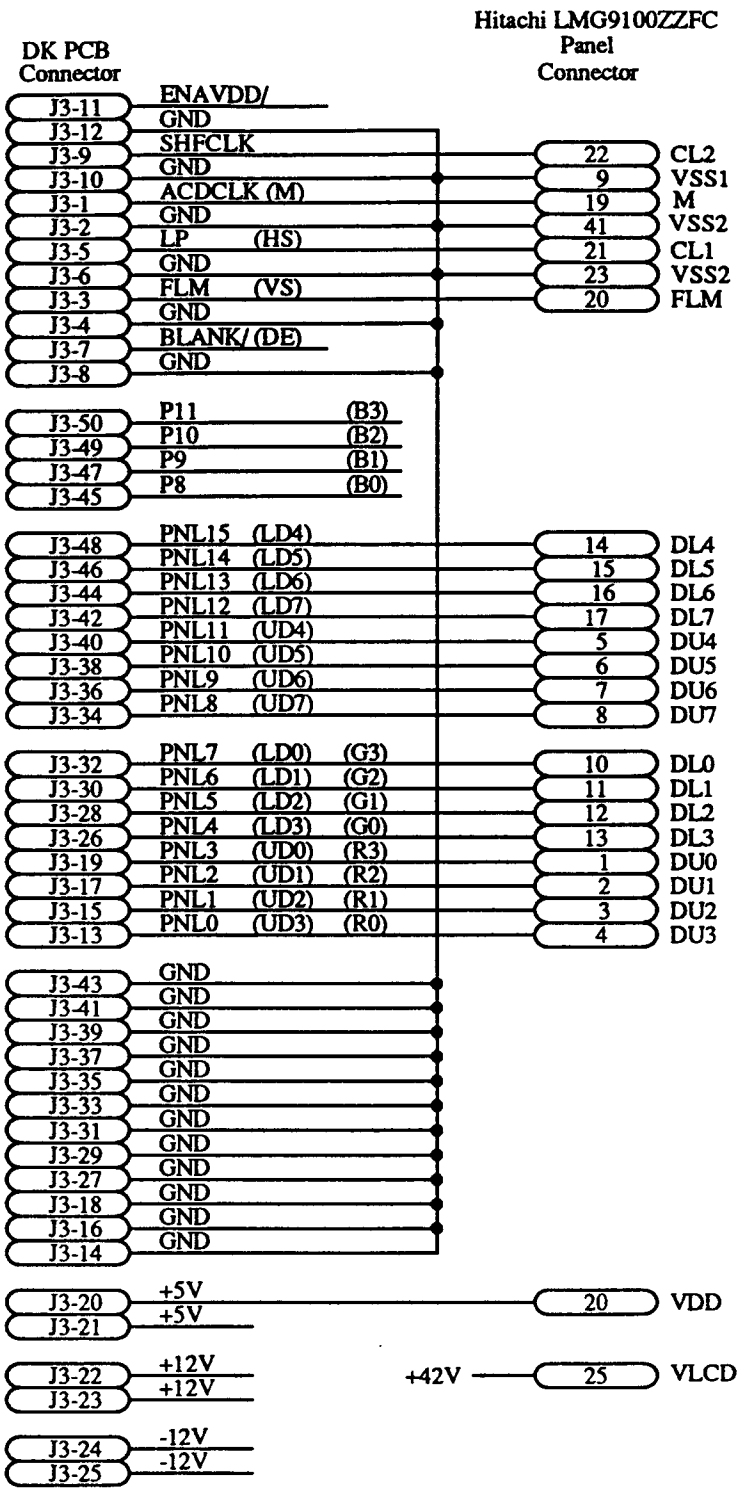
65520 / 530 Interface - Hitachi LMG5162XUFC (640x480 Monochrome LCD DD Panel)



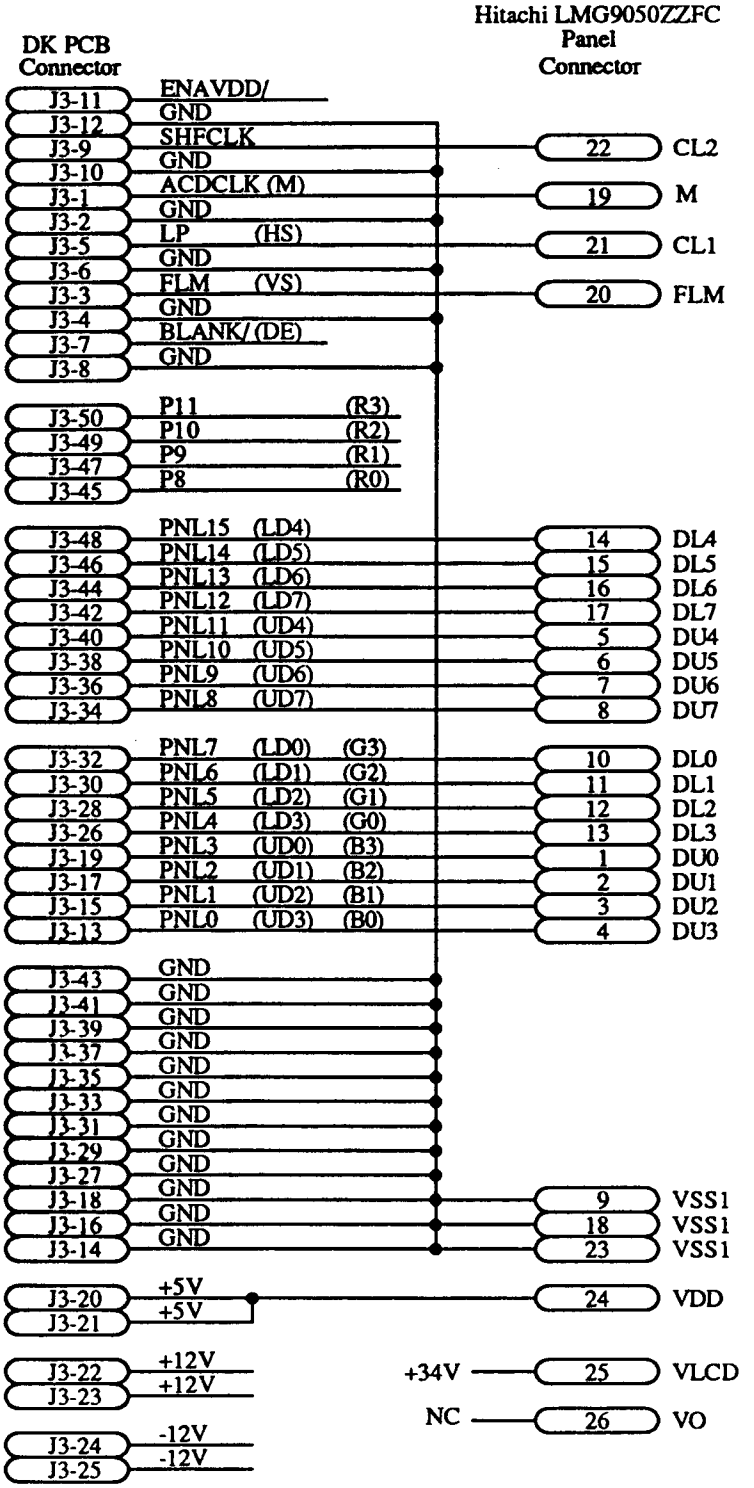
65520 / 530 Interface - Matsushita S804 (640x480 16-Gray Level Plasma Panel)



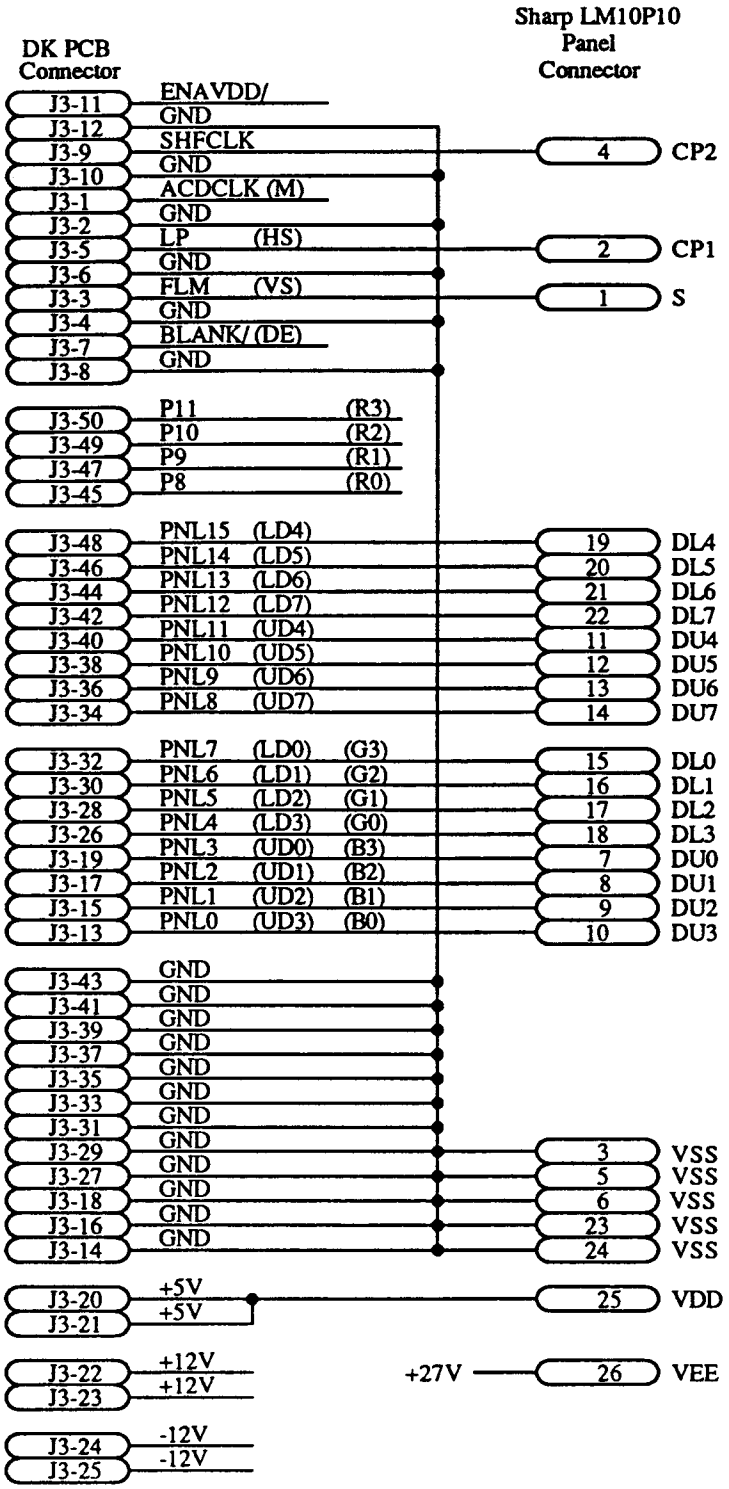
65520 / 530 Interface - Sharp LJ64ZU50 (640x480 16-Gray Level EL Panel)



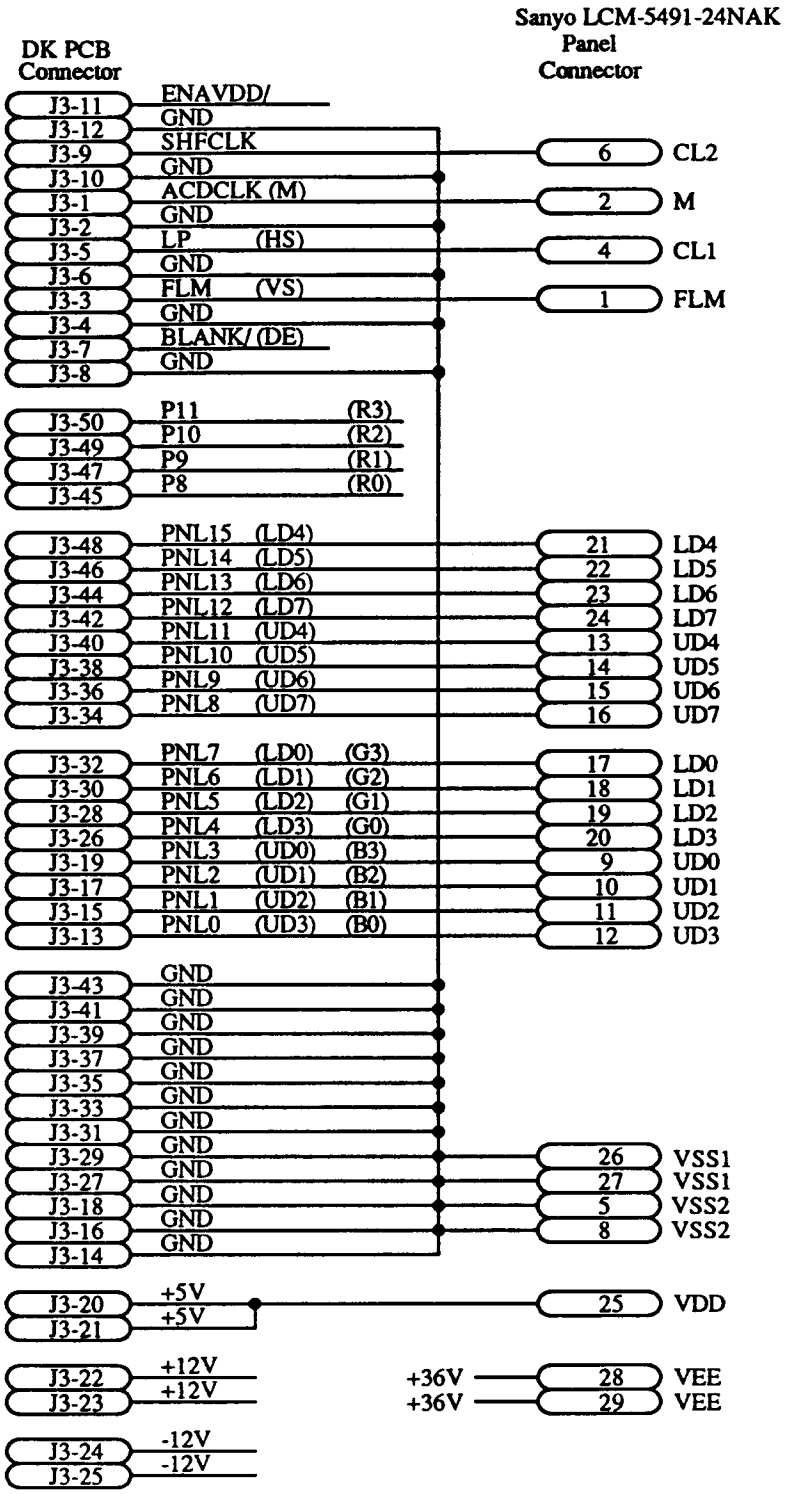
65520 / 530 Interface - Hitachi LMG9100ZZFC (1280x1024 Monochrome LCD DD Panel)



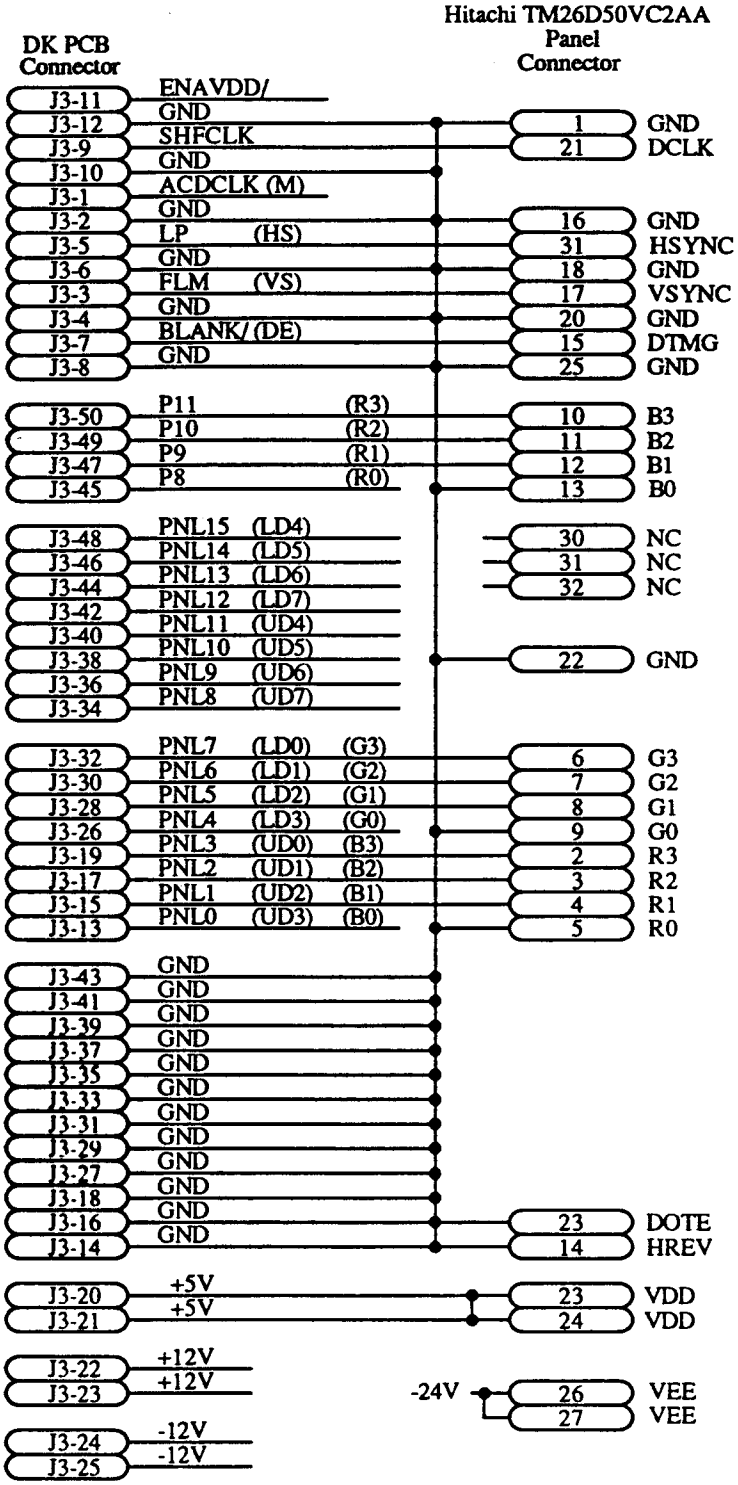
65520 / 530 Interface - Hitachi LMG9050ZZFC (1024x768 Monochrome LCD DD Panel)



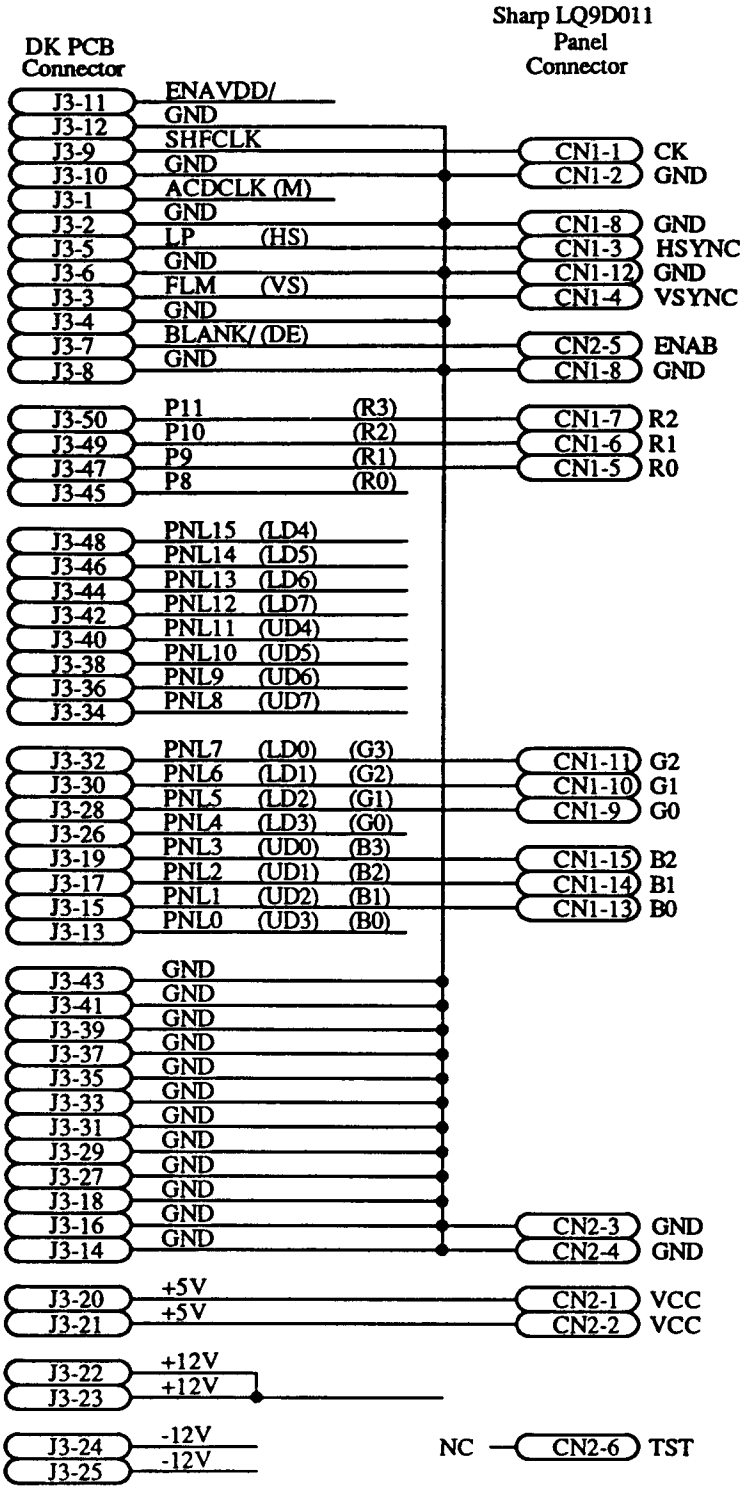
65520 / 530 Interface - Sharp LM10P10 (1024x768 Monochrome LCD DD Panel)



65520 / 530 Interface - Sanyo LCM-5491-24NAK (1024x768 Monochrome LCD DD Panel)



65520 / 530 Interface - Hitachi TM26D50VC2AA (640x480 512-Color TFT LCD Panel)



65520 / 530 Interface -Sharp LQ9D011 (640x480 512 Color LCD TFT Panel)

—This Page Intentionally Left Blank—

Flat Panel Timing

This section shows detailed timing diagrams for the 65520 / 530 outputting data and control sequences to a variety of panel types. The 65520 is a highly configurable controller which can interface to virtually all existing monochrome LCD, EL, Plasma and Color TFT LCD panels. The 65530 is pin compatible with the 65520 and contains a superset of the 65520 features and can interface to virtually all existing panels (monochrome and color). The panel types supported are:

Dual panel-Double drive (DD)
- 8 pixels/clock, 1 bit/pixel

Dual panel-Single drive (DS)
- 1 pixel/clock, 6 bits/pixel
- 2 pixels/clock, 4 bits/pixel
- 4 pixels/clock, 2 bits/pixels
- 8 pixels/clock, 1 bit/pixel

Single panel-Single drive (SS)
- 1 pixel/clock, 6 bits/pixel
- 2 pixels/clock, 4 bits/pixel
- 4 pixels/clock, 2 bits/pixels
- 8 pixels/clock, 1 bit/pixel

The panel type (PT) is determined by XR51 bits 1-0:

00 Single panel-Single drive (SS)
10 Dual panel-Single drive (DS)
11 Dual panel-Double drive (DD)

The 65520 and 65530 provide 4, 8 and 16 level Frame Rate Control (FRC) techniques to generate multiple gray levels on monochrome panels.

The FRC selected is determined by XR50 bits 1-0:

00 8-frame FRC
01 16-frame FRC
10 4-frame FRC

Additionally, if XR50 bits 1-0 are 11, XR50 bits 7-6 control VAM and FRC:

00 VAM
01 3 bits/pixel VAM
10 2-frame FRC
11 2-frame FRC + 3 bits/pixel VAM (530 only)

The 65520/530 can be programmed to output 1 pixel per shift clock, 2 pixels per shift clock, 4 pixels per shift clock or 8 pixels per shift clock. This is achieved by programming the frequency ratio between the dot clock and the shift clock.

The shift clock divide (CD) is set by XR50 bits 5-4:

00 shift clock = dot clock; 1 pixel/shift clock
01 shift clock = dot clock/2; 2 pixels/shift clock
10 shift clock = dot clock/4; 4 pixels/shift clock
11 shift clock = dot clock/8; 8 pixels/shift clock

The pixel output timings are shown for the following panel configurations:

1) Dual Panel-Double Drive 640x480
Monochrome LCD Panel
8 pixels/shift clock, 1bit/pixel

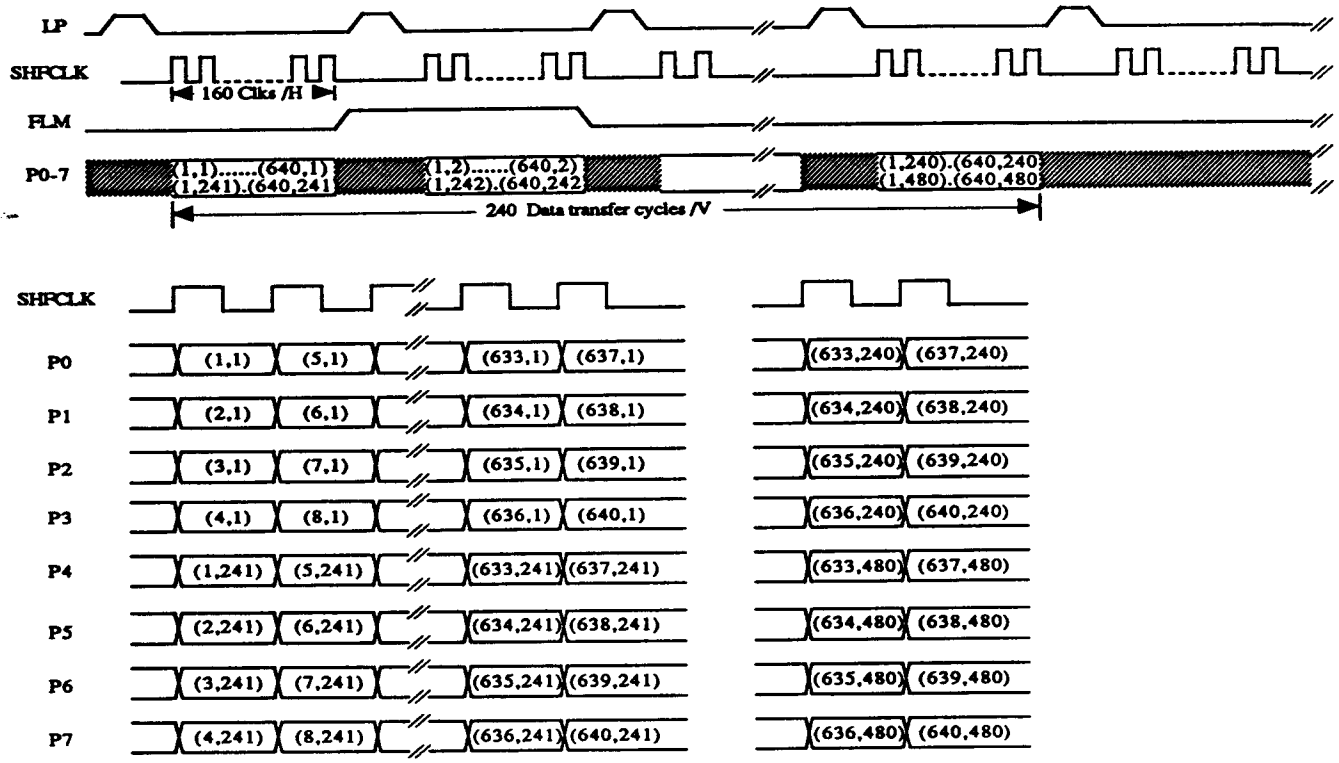
CD = 10 (with Frame Accelerator)
CD = 11 (without Frame Accelerator)
FRC = 00, 01, 10, 11
PT = 11

2) Dual Panel-Single Drive 640x480
Monochrome LCD Panel
4 pixels/shift clock, 2 bits/pixel

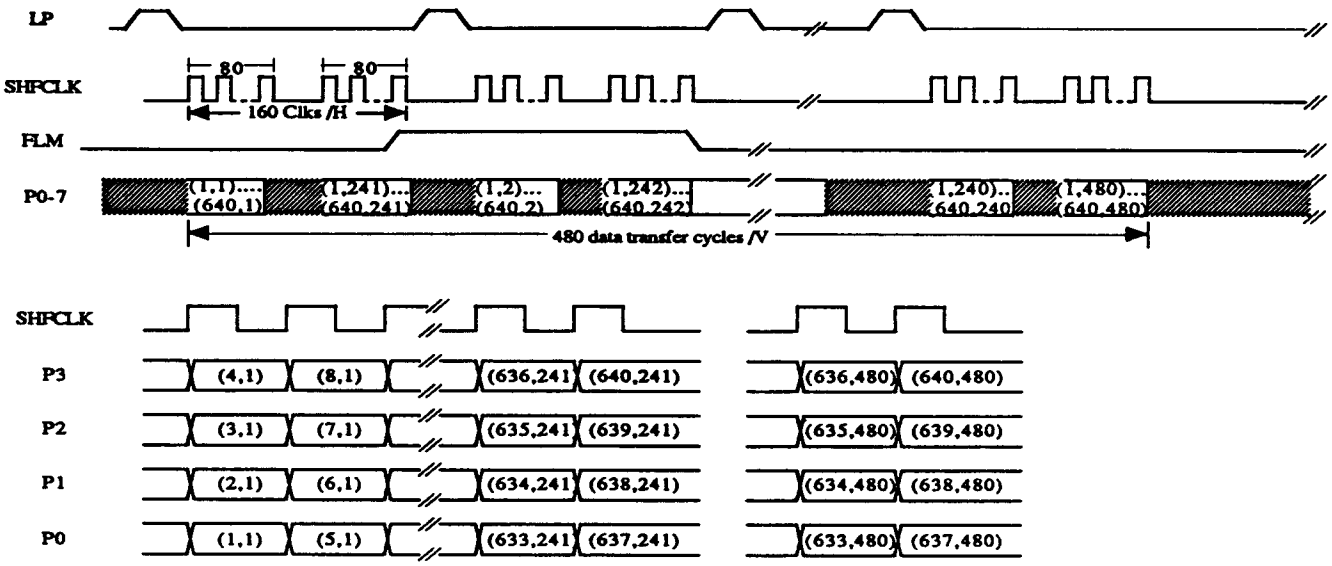
CD = 10
FRC = 00, 01, 10
PT = 10

3) Single Panel-Single Drive Plasma/EL Panel
2 Pixels/Shift Clock, 4 Bits/pixel Interface

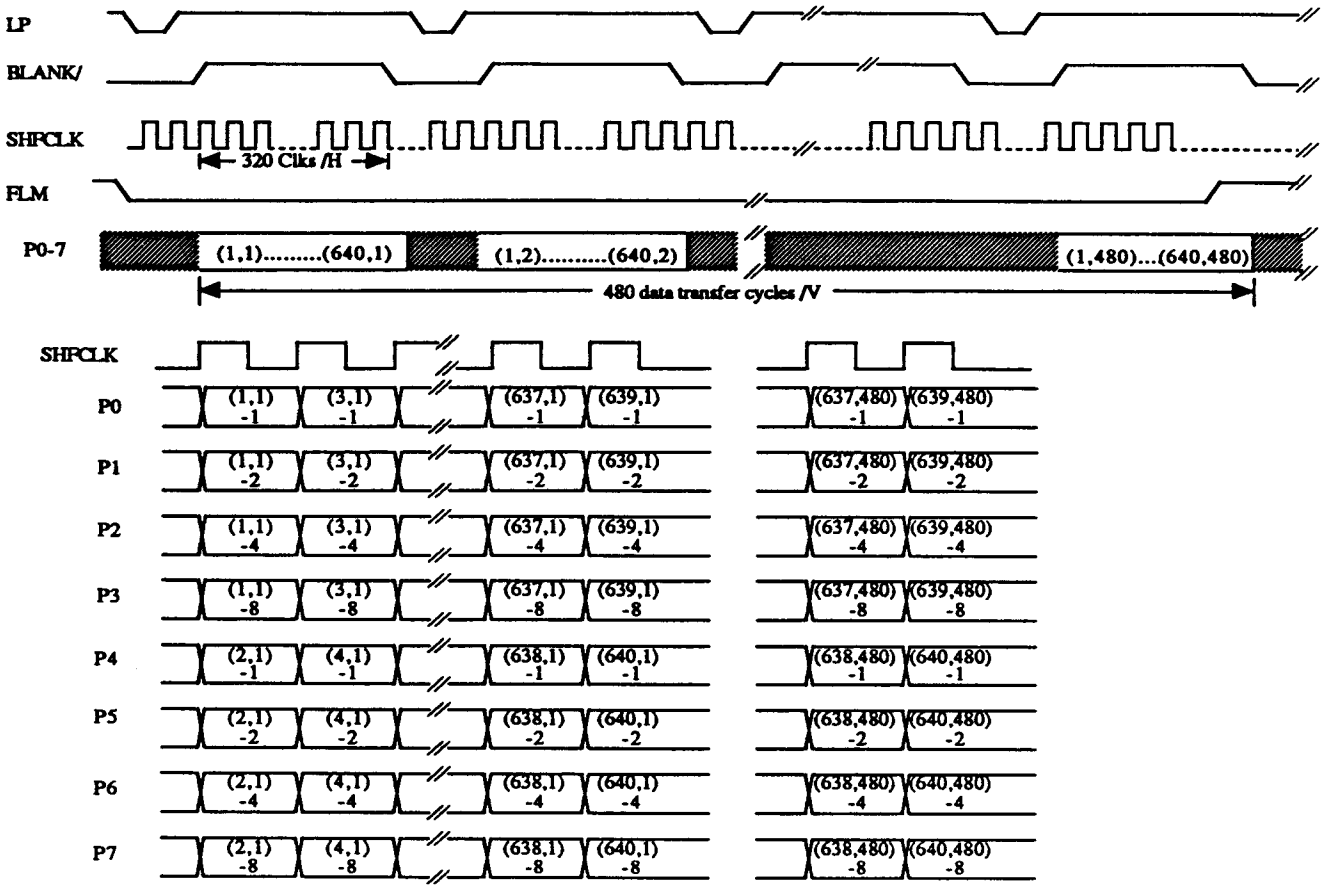
CD = 01
FRC = 11
PT = 00



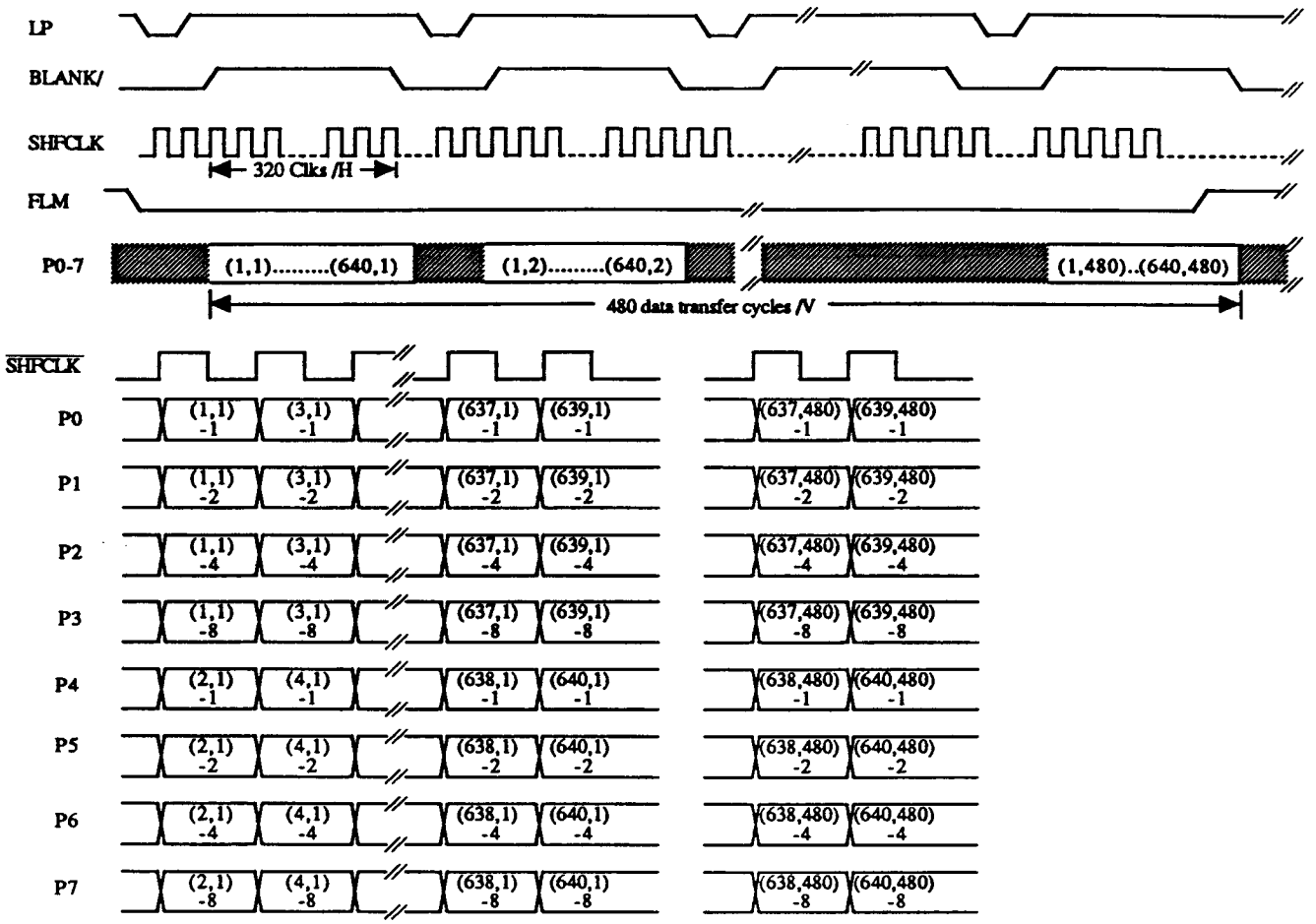
Panel Timing - LCD DD



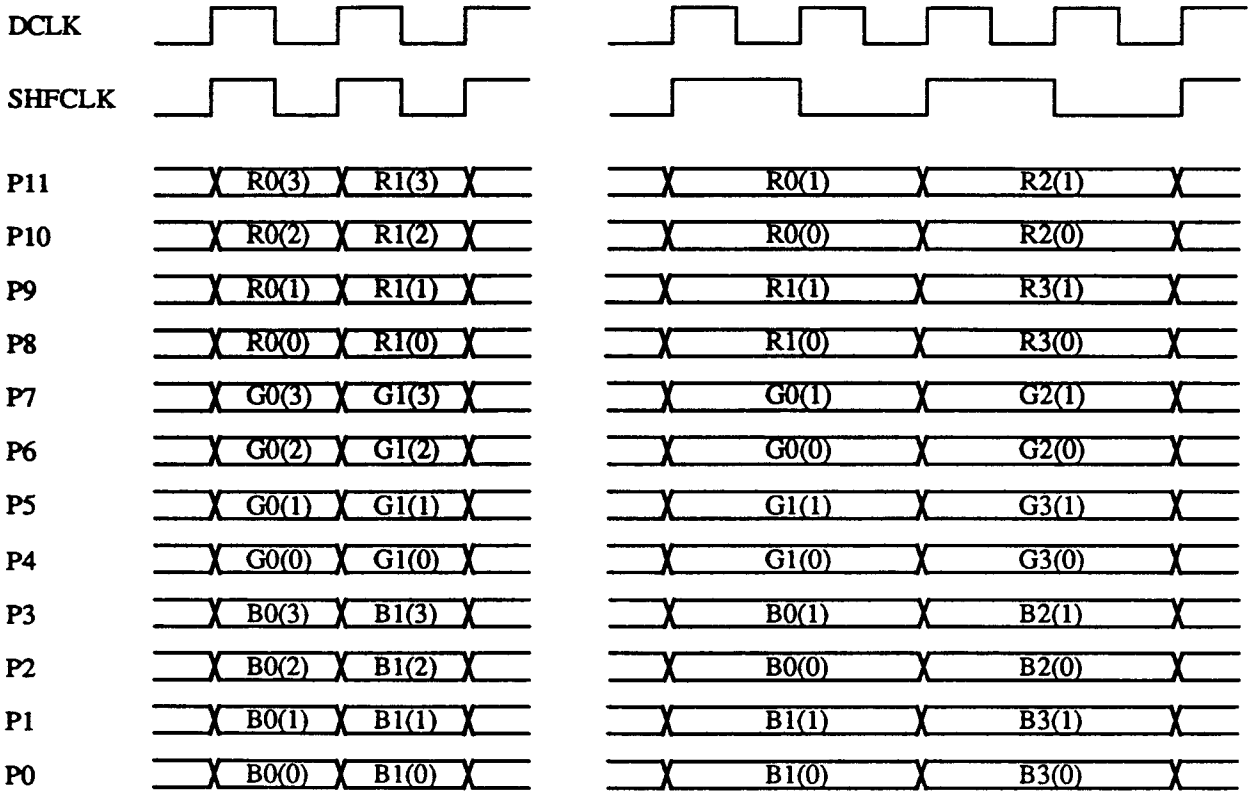
Panel Timing - LCD DS 4-Bit Pack



Panel Timing - Plasma Panel with 2 Pixels/Shift Clock

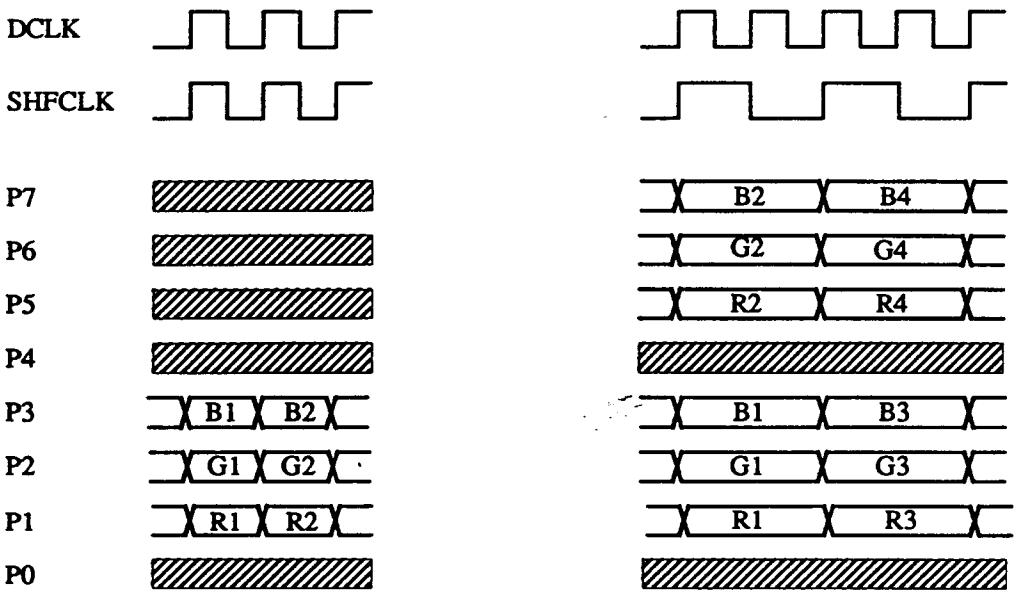


Panel Timing - EL Panel with 2 Pixels/Shift Clock



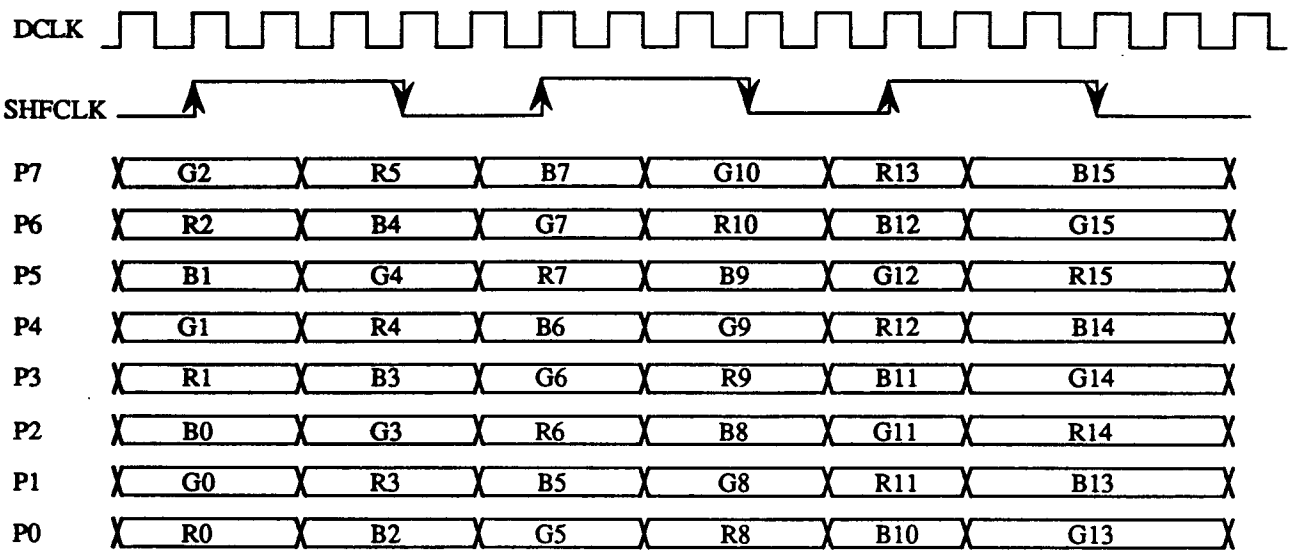
CD:	00 (1 pixel /clock)	01 (2 pixels /clock)
VAM:	4 Level 8 Level 16 Level	4 Level

Panel Timing - Color TFT LCD Panel with Voltage Amplitude Modulation (VAM)



	00 (1 pixel/clock)	01 (2 pixel/clock)
CD:		
FRC:	None 3 Level 4 Level 16 Level	None 3 Level 4 Level 16 Level

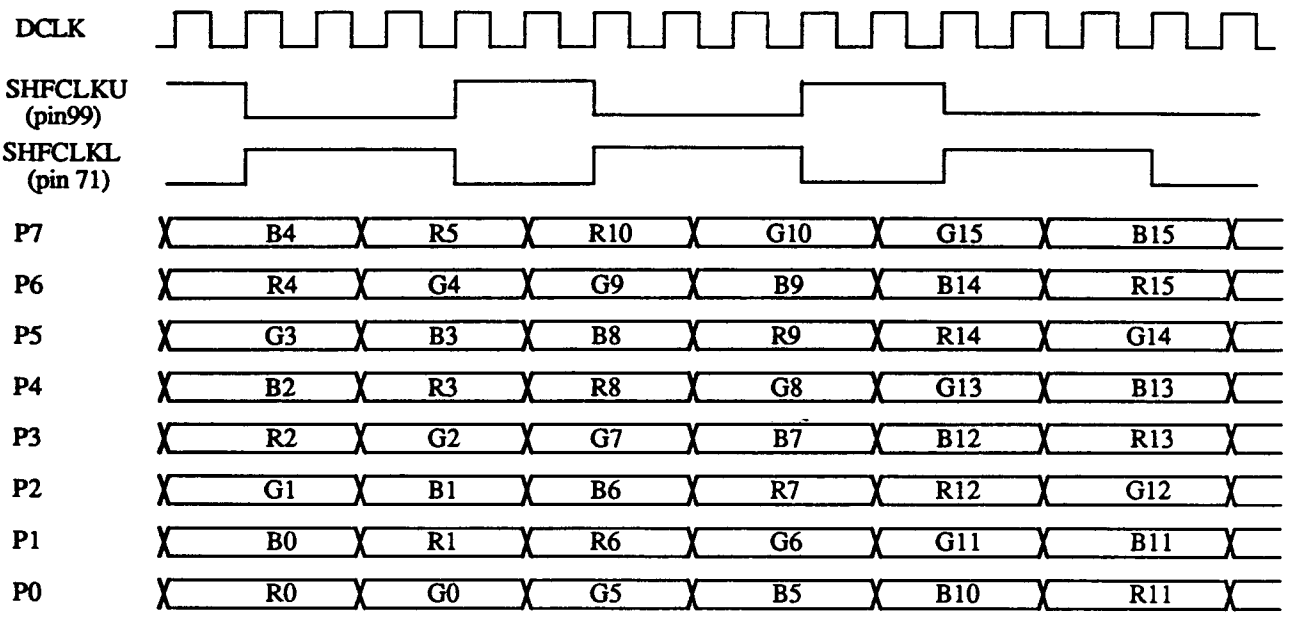
Panel Timing - Color STN LCD 3-Bit Interface (65530 only)



CD: 10 (5 & 1/3 pixels / clock)

FRC: None, 3 level, 4 level, 16 level

Panel Timing - Color STN LCD 4-Bit Pack Interface (65530 only)



CD: 10 (5 & 1/3 pixels / clock)

FRC: None, 3 level, 4 level, 16 level

Panel Timing - Color STN LCD Extended 4-Bit Pack Interface (65530 only)

This Page Intentionally Left Blank

Flat Panel Pixel Timing

The 65520 / 530 is the most flexible flat panel graphics controller available, enabling the widest possible range of panel interfaces. This section includes timing diagrams for the following configurations:

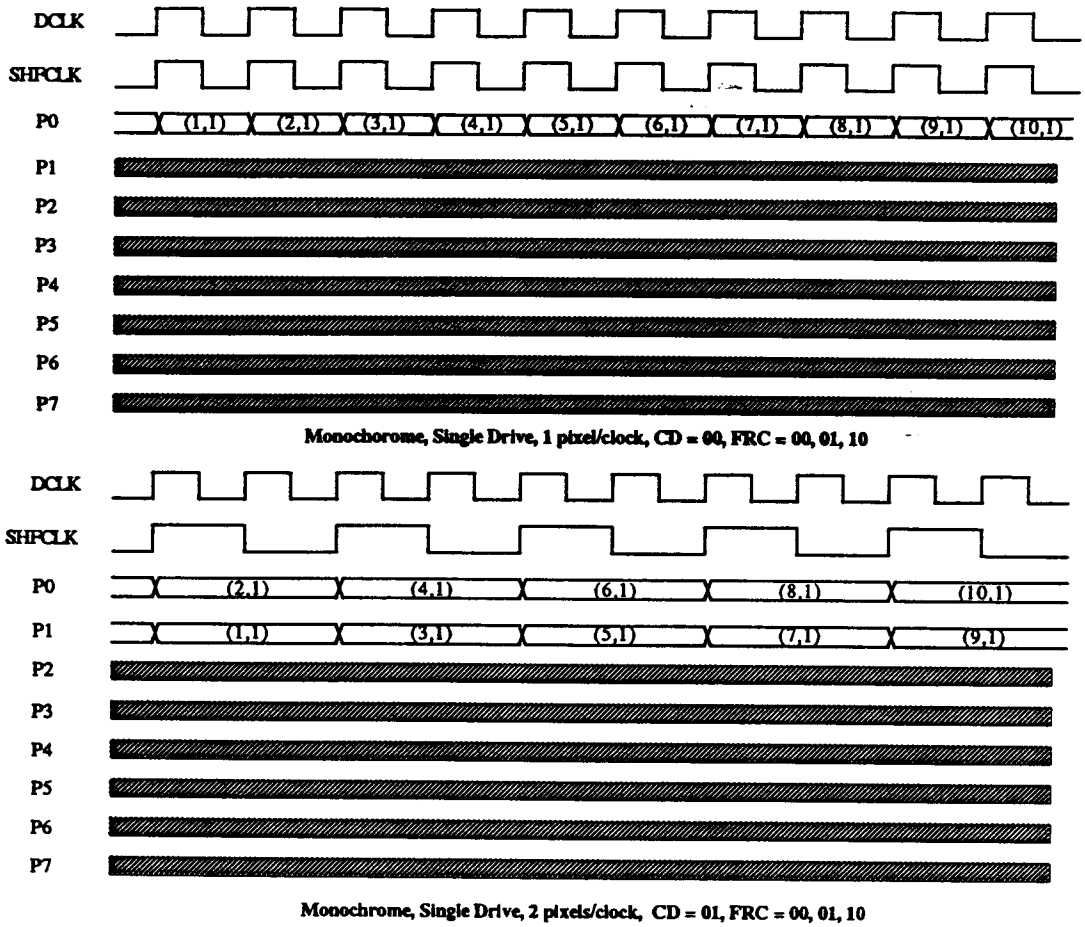
- Monochrome, Single Drive, 1 pixel/clock
- Monochrome, Single Drive, 2 pixels/clock
- Monochrome, Single Drive, 4 pixels/clock
- Monochrome, Single Drive, 8 pixels/clock
- Panel with 16 internal levels of gray, Single Drive, 1 pixel/clock, 4 bits/pixel
- Panel with 16 internal levels of gray, Single Drive, 2 pixels/clock, 4 bits/pixel
- Monochrome, Double Drive, 8 pixels/clock
- Monochrome, Double Drive, 8 pixels/clock with Frame Accelerator
- Monochrome, Double Drive, 1024 x 768 16 pixels/clock without Frame Accelerator
- Monochrome, Double Drive, 1024 x 768 16 pixels/clock with Frame Accelerator
- Monochrome, Double Drive, 1280 x 1024 16 pixels/clock without Frame Accelerator
- Monochrome, Double Drive, 1280 x 1024 16 pixels/clock with Frame Accelerator

Extension register 50 (XR50) bits 5-4 define the clock divide (CD):

00 - Shift clock frequency = dot clock frequency
01 - Shift clock frequency = dot clock frequency/2
10 - Shift clock frequency = dot clock frequency/4
11 - Shift clock frequency = dot clock frequency/8

Extension Register 50 (XR50) bits 1-0 determine the FRC level used:

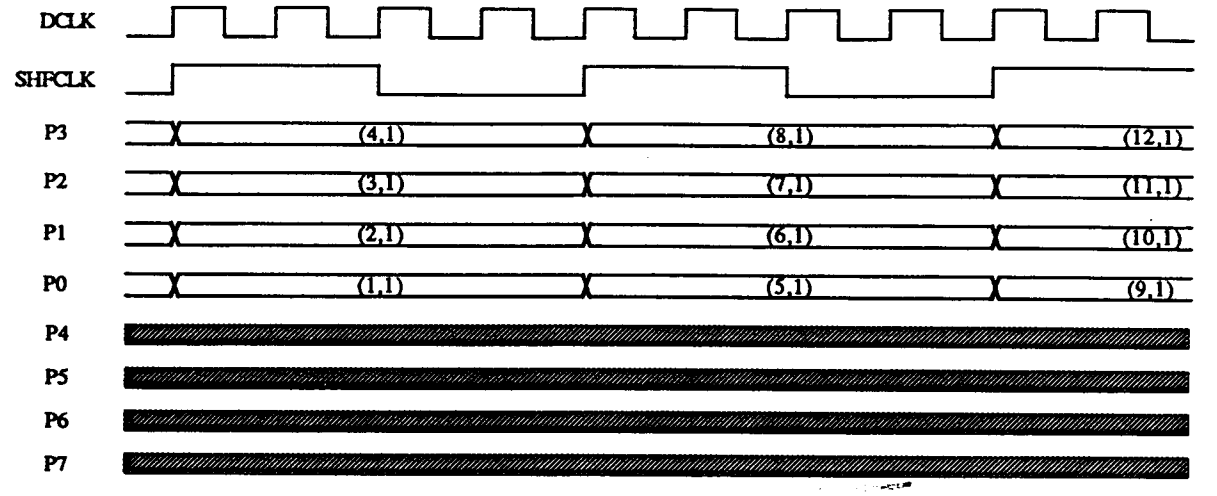
00 - 8-frame FRC
01 - 16-frame FRC
10 - 4-frame FRC



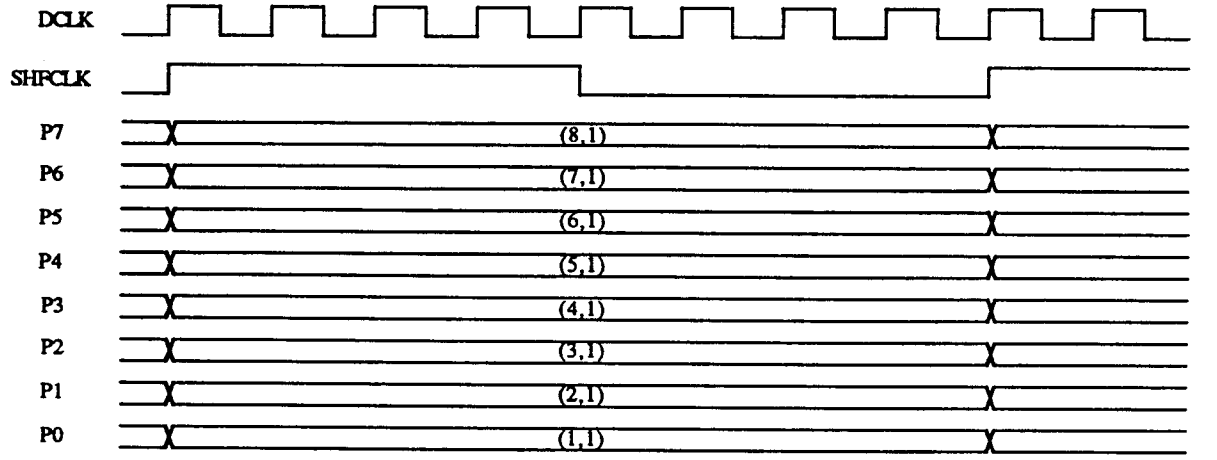
Panel Pixel Timing - Single Drive (Clock Divide 00 & 01)

These timing diagrams show the 65520 / 530 outputs to the flat panel for two scenarios:

1) One pixel per shift clock (where shift clock frequency = dot clock frequency) for monochrome panels with no internal gray-scale generation
2) Two pixels per shift clock (where shift clock frequency = dot clock frequency / 2) for monochrome panels with no internal gray-scale generation



Monochrome, Single Drive, 4 pixels/clock, CD = 10, FRC =00, 01, 10

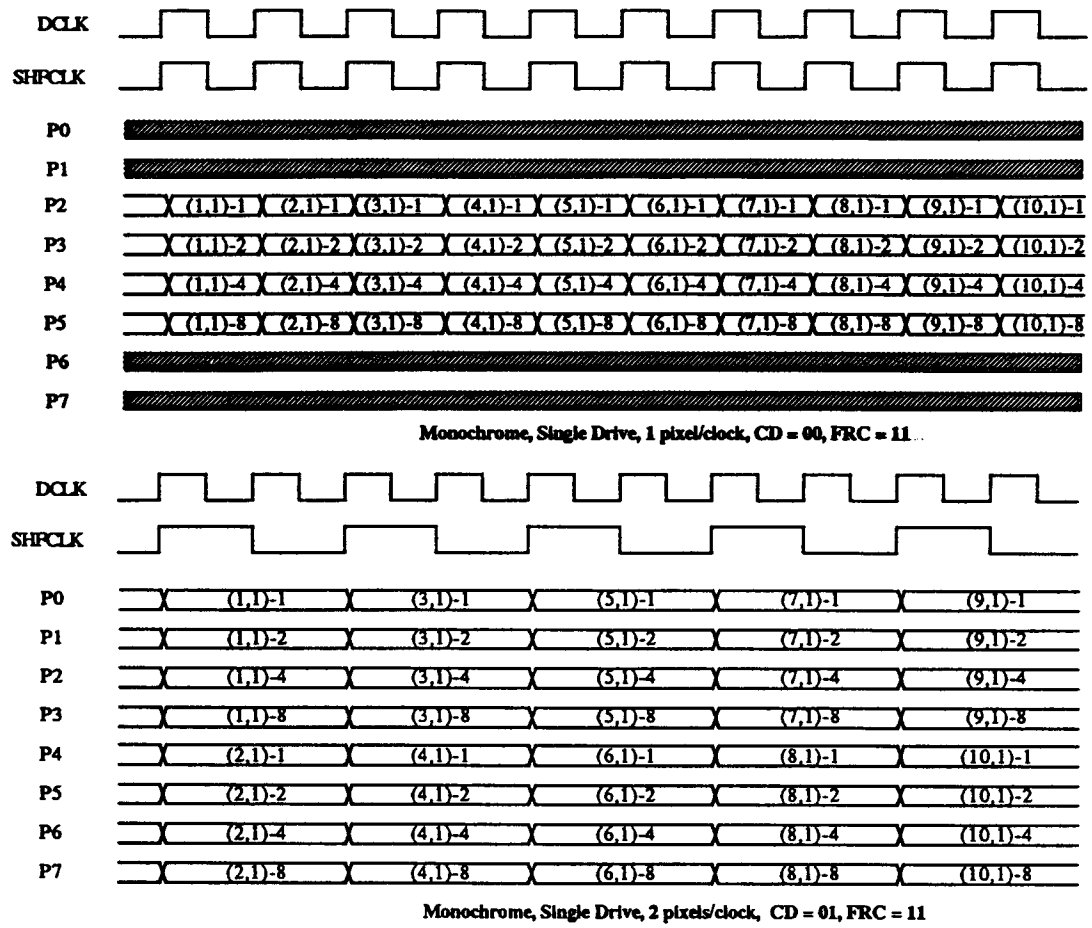


Monochrome, Single Drive, 8 pixels/clock, CD = 11, FRC = 00,01,10

Panel Pixel Timing - Single Drive (Clock Divide 10 & 11)

These timing diagrams show the 65520 / 530 outputs to the flat panel for two scenarios:

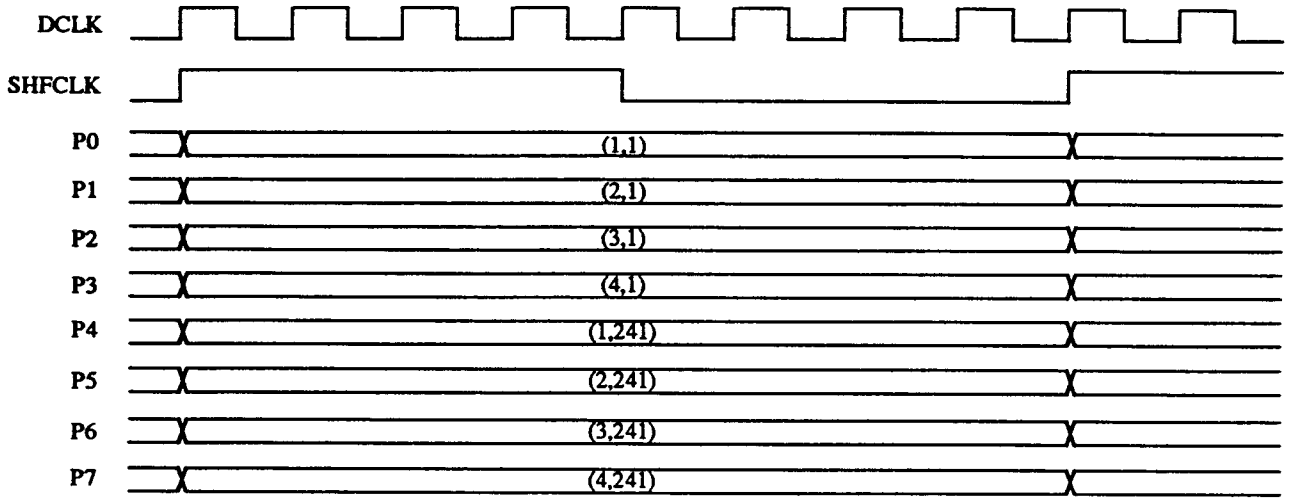
1) Four pixels per shift clock (where shift clock frequency = dot clock frequency / 4) for monochrome panels with no internal gray-scale generation
2) Eight pixels per shift clock (where shift clock frequency = dot clock frequency / 8) for monochrome panels with no internal gray-scale generation



Panel Pixel Timing - Single Drive (Clock Divide 00 & 01)

These timing diagrams show the 65520 / 530 outputs for a monochrome flat panel display with 16 levels of internal gray scale generation. Two scenarios are presented:

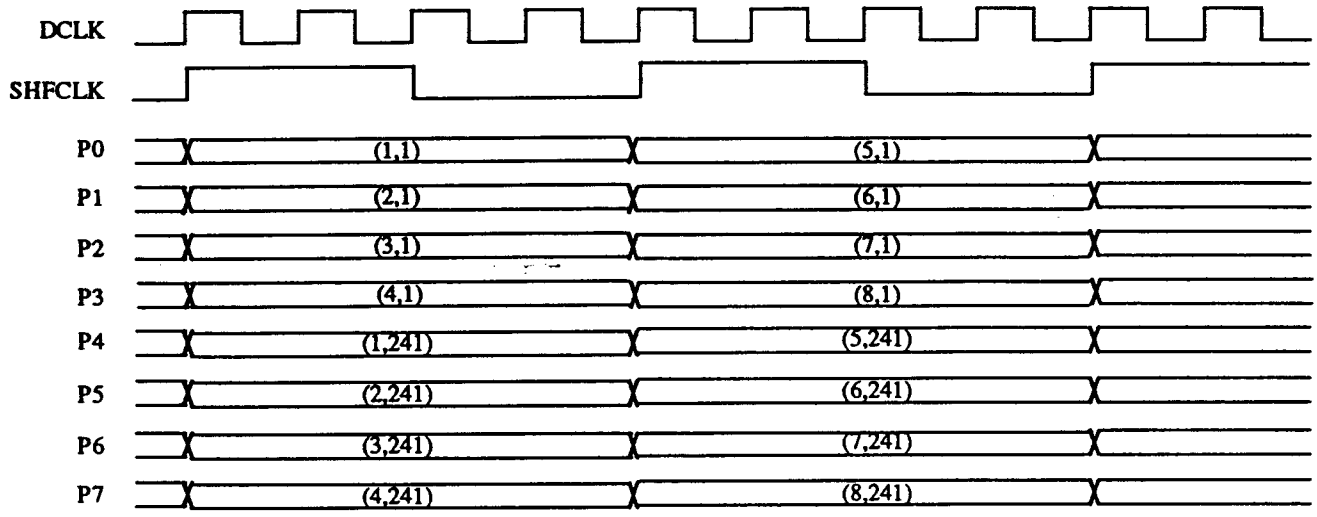
1) One pixel per shift clock (where shift clock frequency = dot clock frequency)
2) Two pixels per shift clock (where shift clock frequency = dot clock frequency / 2)



Monochrome, Double Drive, 8 pixels/clock, CD = 11, FRC = 00, 01, 10
Without Frame Accelerator

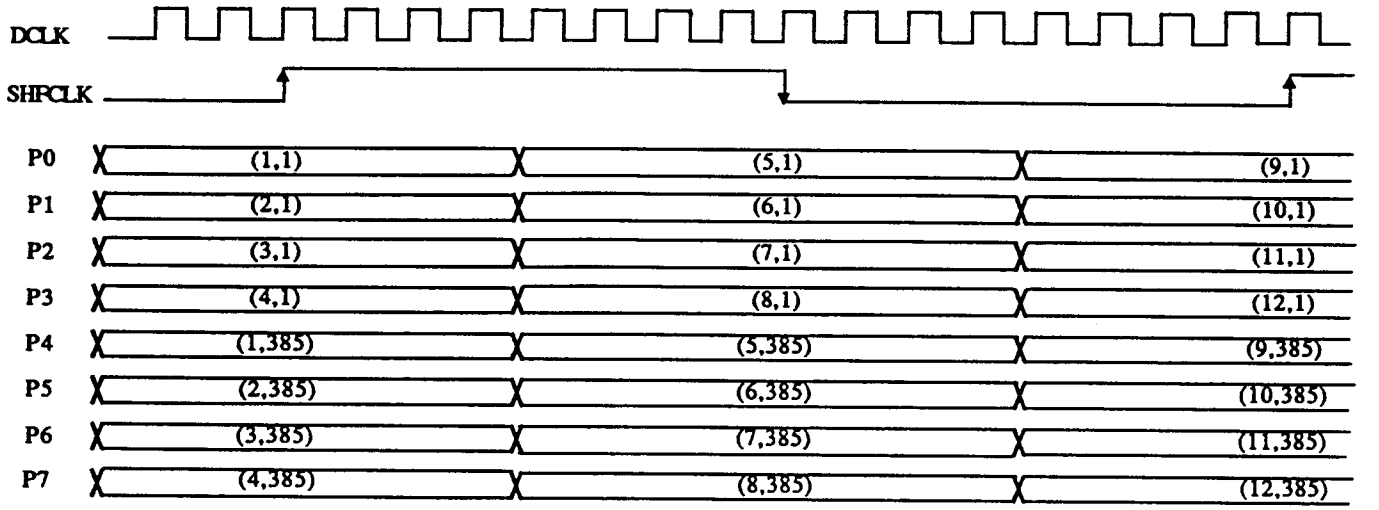
Panel Pixel Timing - Monochrome Double Drive (Clock Divide By 8)

This timing diagram shows the 65520 / 530 outputs for a double drive monochrome panel with an eight pixels per shift clock interface where the shift clock frequency equals the dot clock frequency divided by 8.



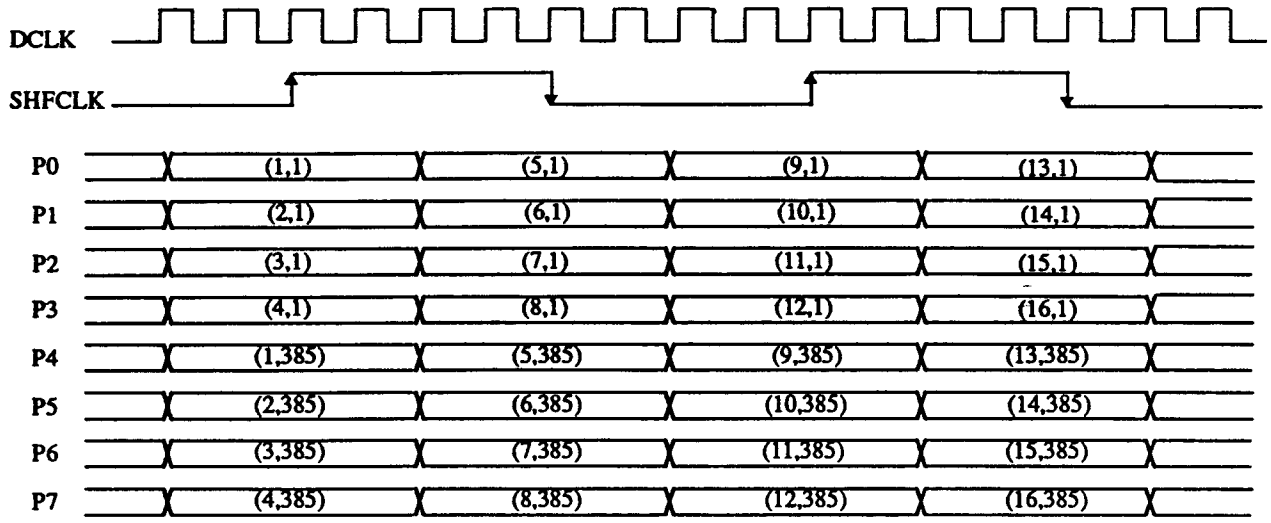
Monochrome, Double Drive, 8 pixels/clock, CD = 10 , FRC = 00, 01, 10
With Frame Acceleration

Panel Pixel Timing - 640x480 LCD-DD with Frame Buffer Acceleration (Clock Divide By 4)



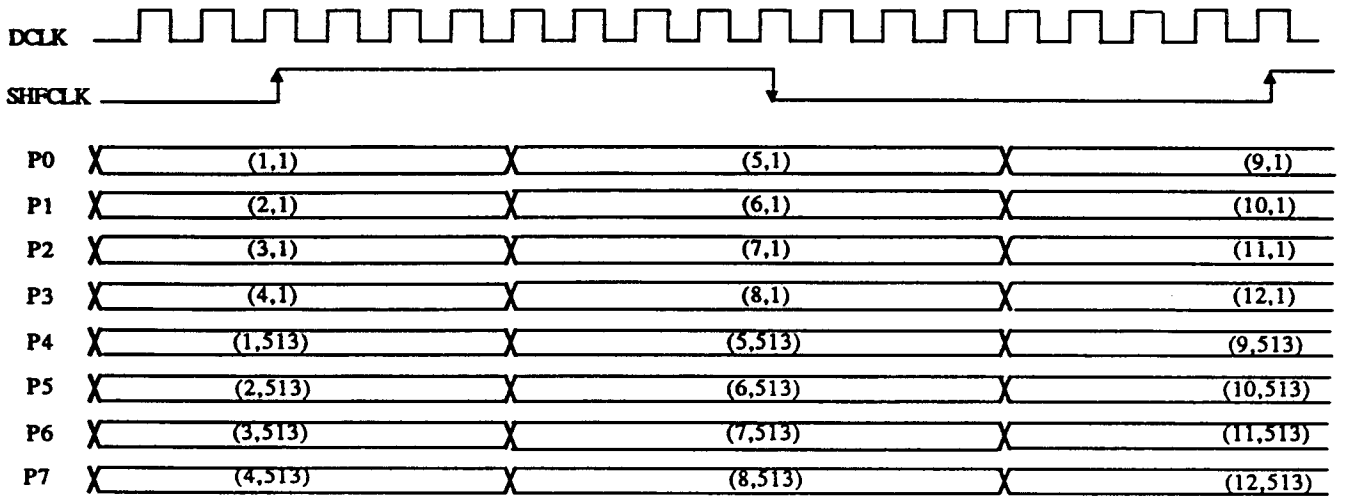
65520/530 Pixel Shift Order for a 1024x768 1 bit/pixel Monochrome LCD-DD Panel (CD=11)

Panel Pixel Timing - 1024 x 768 LCD-DD without Frame Buffer Acceleration



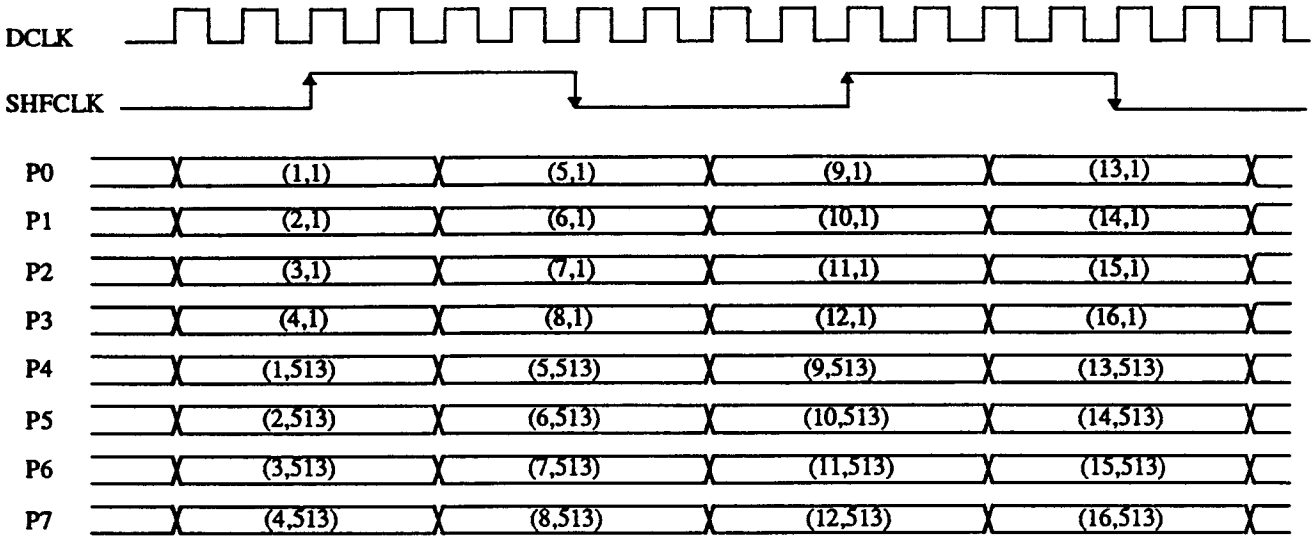
65520/530 Pixel Shift Order for a 1024x768 1 bit/pixel Monochrome LCD-DD Panel With Frame Acceleration (CD = 10)

Panel Pixel Timing - 1024 x 768 LCD-DD with Frame Buffer Acceleration



65520/530 Pixel Shift Order for a 1280x1024 1 bit/pixel Monochrome LCD-DD Panel Without Frame Acceleration (CD= 11)

Panel Pixel Timing - 1280 x 1024 LCD-DD without Frame Buffer Acceleration



65520/530 Pixel Shift Order for a 1280x1024 1 bit/pixel Monochrome LCD-DD Panel With Frame Acceleration (CD = 10)

Panel Pixel Timing - 1280 x 1024 LCD-DD with Frame Buffer Acceleration

Electrical Specifications

ABSOLUTE MAXIMUM CONDITIONS

Symbol	Parameter	Min	Typ	Max	Units
P_D	Power Dissipation	–	–	1	W
V_{CC}	Supply Voltage	–0.5	–	7.0	V
V_I	Input Voltage	–0.5	–	V_{CC}+0.5	V
V_O	Output Voltage	–0.5	–	V_{CC}+0.5	V
T_{OP}	Operating Temperature (Ambient)	–25	–	85	°C
T_{STG}	Storage Temperature	–40	–	125	°C

Note: Permanent device damage may occur if Absolute Maximum Ratings are exceeded.
Functional operation should be restricted to the conditions described under Normal Operating Conditions.

NORMAL OPERATING CONDITIONS

Symbol	Parameter	Min	Typ	Max	Units
V_{CC}	Supply Voltage (5V ±10%)	4.5	5	5.5	V
V_{CC}	Supply Voltage (3.3V ±10%)	3.0	3.3	3.6	V
T_A	Ambient Temperature	0	–	70	°C

DAC CHARACTERISTICS

(Under Normal Operating Conditions Unless Noted Otherwise)

Symbol	Parameter	Notes	Min	Typ	Max	Units
V_O	Output Voltage	Io ≤ 10 mA	1.5	–	–	V
Io	Output Current	Vo ≤ 1V @ 37.5Ω Load	21	–	–	mA
	Full Scale Error		–	–	±5	%
	DAC to DAC Correlation		–	1.27	–	%
	DAC Linearity		±2	–	–	LSB
	Full Scale Settling Time		–	–	28	nS
	Rise Time	10% to 90%	–	–	6	nS
	Glitch Energy		–	–	200	pVsec
	Comparator Sensitivity		–	50	–	vM

Note: Unless otherwise specified, specifications above apply to both 5V and 3.3V operation.

Electrical specifications contained herein are preliminary and subject to change without notice.

DC CHARACTERISTICS

(Under Normal Operating Conditions Unless Noted Otherwise)

Symbol	Parameter	Notes	Min	Typ	Max	Units
I_{CCDE}	Power Supply Current	0°C, 5.5V, 50 MHz Clk, DAC Enabled	–	150	170	mA
I_{CCDO}	Power Supply Current	0°C, 5.5V, 50 MHz Clk, DAC Disabled	–	125	150	mA
I_{CCDE}	Power Supply Current	0°C, 3.3V, 40 MHz Clk, DAC Enabled	–	TBD	TBD	mA
I_{CCDO}	Power Supply Current	0°C, 3.3V, 40 MHz Clk, DAC Disabled	–	TBD	TBD	mA
I_{CCS}	Power Supply Current	0°C, 5.5V, Standby	–	TBD	1	mA
I_{IL}	Input Leakage Current		–100	–	+100	uA
I_{OZ}	Output Leakage Current	High Impedance	–100	–	+100	uA
V_{IL}	Input Low Voltage	All input pins	–0.5	–	0.8	V
V_{IH}	Input High Voltage	All input pins except clocks	2.0	–	V_{CC}+0.5	V
		CLK0, CLK1, CLK2, CLK3	2.8	–	V_{CC}+0.5	V
V_{OL}	Output Low Voltage	Under max load per table below (5V)	–	–	0.45	V
V_{OL}	Output Low Voltage	Under max load per table below (3.3V)	–	–	0.5	V
V_{OH}	Output High Voltage	Under max load per table below (5V)	V_{CC}–0.5	–	–	V
V_{OH}	Output High Voltage	Under max load per table below (3.3V)	2.4	–	–	V

DC DRIVE CHARACTERISTICS

(Under Normal Operating Conditions Unless Noted Otherwise)

Symbol	Parameter	Output Pins	DC Test Conditions	Min	Units
I_{OL}	Output Low Drive	RDY, IRQ, 0WS/, IOCS16/	$V_{OUT}=V_{OL}$, V_{CC}=4.5V	7	mA
		HSYNC and VSYNC	$V_{OUT}=V_{OL}$, V_{CC}=4.5V	24	mA
		P0-7, PCLK, SHFCLK, D0-15	$V_{OUT}=V_{OL}$, V_{CC}=4.5V	3.5	mA
		RASA/, RASB/, CASA/, CASB/	$V_{OUT}=V_{OL}$, V_{CC}=4.5V	3.5	mA
		BLANK/, FLM, LP, FPEN/	$V_{OUT}=V_{OL}$, V_{CC}=4.5V	4	mA
		All other outputs	$V_{OUT}=V_{OL}$, V_{CC}=4.5V	2	mA
I_{OH}	Output High Drive	RDY, IRQ, 0WS/, IOCS16/	$V_{OUT}=V_{OH}$, V_{CC}=4.5V	8	mA
		HSYNC and VSYNC	$V_{OUT}=V_{OL}$, V_{CC}=4.5V	24	mA
		P0-7, PCLK, SHFCLK, D0-15	$V_{OUT}=V_{OH}$, V_{CC}=4.5V	4	mA
		RASA/, RASB/, CASA/, CASB/	$V_{OUT}=V_{OH}$, V_{CC}=4.5V	4	mA
		BLANK/, FLM, LP, FPEN/	$V_{OUT}=V_{OH}$, V_{CC}=4.5V	4	mA
		All other outputs	$V_{OUT}=V_{OH}$, V_{CC}=4.5V	2	mA

AC TEST CONDITIONS

(Under Normal Operating Conditions Unless Noted Otherwise)

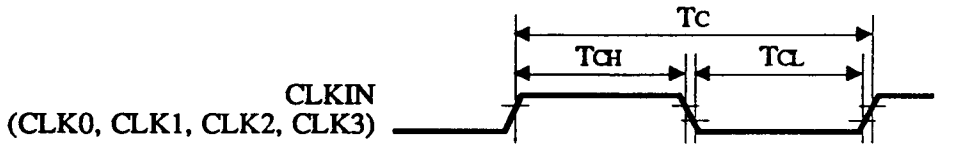
Output Pins	Output Low Voltage	Output High Voltage	Capacitive Load
D0-15, RDY, IRQ, 0WS/, IOCS16/	V_{OL}	3.0V	150pF
P0-7, PCLK, SHFCLK, FPEN/	V_{OL}	3.0V	150pF
HSYNC, VSYNC, BLANK/, FLM, LP	V_{OL}	3.0V	150pF
All Others	V_{OL}	3.0V	25pF

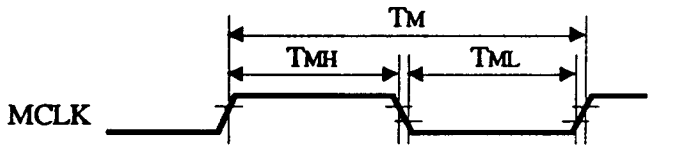
Note: Unless otherwise specified, specifications above apply to both 5V and 3.3V operation.

Electrical specifications contained herein are preliminary and subject to change without notice.

AC TIMING CHARACTERISTICS - CLOCK TIMING

Symbol	Parameter	Notes	Min	Typ	Max	Units
T_C	CLK Period	50.350 MHz, (5V)	20	–	–	nS
T_C	CLK Period	40 MHz, (3.3V)	25	–	–	nS
T_{CH}	CLK High Time		$0.45T_C$	–	$0.55T_C$	nS
T_{CL}	CLK Low Time		$0.45T_C$	–	$0.55T_C$	nS
T_M	MCLK Period	50.350 or 56.644 MHz	17.6	–	20	nS
T_{MH}	MCLK High Time		$0.45T_M$	–	$0.55T_M$	nS
T_{ML}	MCLK Low Time		$0.45T_M$	–	$0.55T_M$	nS
T_{RF}	Clock Rise / Fall		–	–	5	nS
–	MCLK Frequency for 100 ns DRAMs (5V)		–	50.350	–	MHz
–	MCLK Frequency for 80 ns DRAMs (5V)		–	56.644	–	MHz

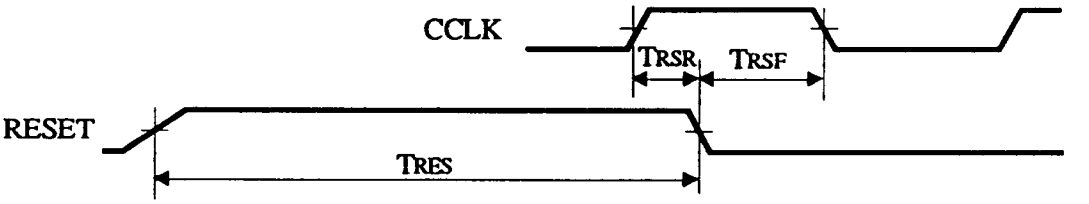




Clock Timing

AC TIMING CHARACTERISTICS - RESET TIMING

Symbol	Parameter	Notes	Min	Typ	Max	Units
TRES	RESET Pulse Width		64Tc	–	–	nS
TRSR	RESET Delay from CCLK rising edge	Local Bus only	4	–	–	nS
TRES	RESET Delay to CCLK falling edge	Local Bus only	13	–	–	nS



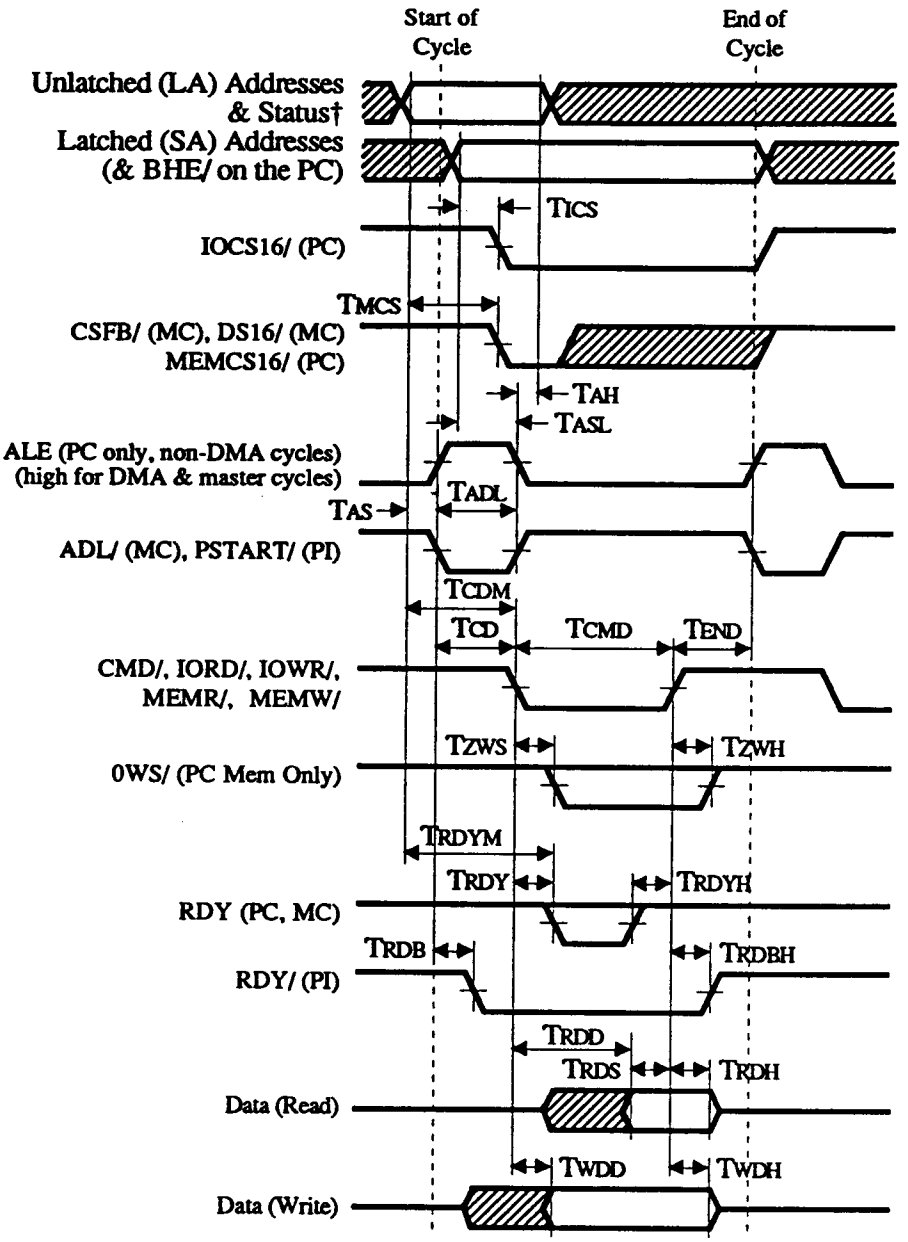
RESET Timing

Note: Unless otherwise specified, specifications above apply to both 5V and 3.3V operation.

FOR REFERENCE ONLY: BUS TIMING CHARACTERISTICS

Symbol	Parameter	8 MHz PC Bus	12.5 MHz MC Bus	20 MHz PI Bus	Units
TADL	Address Latch Pulse Width	50 min	40 min	50 min	nS
TCD	Delay from Start of Cycle to Command Strobe	50 min	40 min	50 min	nS
TCDM	Delay from Address Valid to Command Strobe	109 min	85 min	–	nS
TCMD	Command Strobe Pulse Width (Asynchronous Cycle)	176 min	90 min	70 min	nS
TCMD	Command Strobe Pulse Width (Synchronous Cycle)	176 min	90 min	40 min	nS
TEND	Delay from End of Command to Start of Next Cycle	50 min	40 min	0 min	nS
TAS	Address Setup to Start of Cycle	0 min	10 min	10 min	nS
TASL	Address Setup to Start of Command	29 min	–	–	nS
TAH	Address Hold from Start of Command	5 min	5 min	–5 min	nS
TRDD	Read Data Delay from Start of Command	187 max	60 max	–	nS
TRDS	Read Data Setup to End of Command	62 min	30 min	29 min	nS
TRDH	Read Data Hold from End of Command (Data Turnoff)	0 min	0 min	12 min	nS
		30 max	30 max	30 max	nS
TWDD	Write Data Delay from Start of Command	40 max	0 max	14 max	nS
TWDH	Write Data Hold from End of Command (Data Turnoff)	10 min	10 min	10 min	nS
		40 max	40 max	40 max	nS
TICS	Delay from Address to IOCS16/	90 max	–	–	nS
TMCS	Delay from Address to MEMCS16/, DS16/, CSFB/	66 max	55 max	–	nS
TZWS	Delay from Start of Command to Start of 0WS/ (16-bit)	40 max	–	–	nS
TZWS	Delay from Start of Command to Start of 0WS/ (8-bit)	1 min	–	–	SYSCLK
TZWH	Delay to End of 0WS/ from End of Command	30 max	–	–	nS
TRDY	Delay to Start of RDY from Start of Command	30 max	–	–	nS
TRDYM	Delay to Start of RDY from Address & Status Valid	–	30 max	–	nS
TRDYH	Delay from End of RDY to End of Command	1 SYSCLK	60 min	–	nS
TRDB	Delay from Start of Cycle to RDY/ Low (Sync)	–	–	28 max	nS
TRDB	Delay from Start of Cycle to RDY/ Low (Async)	–	–	92 min	nS
TRDBH	Delay from End of Command to RDY/ High	–	–	20 max	nS

Note: PC bus specifications correspond to an 8 MHz bus (SYSCLK period of 125nS) (12 MHz bus SYSCLK period would be 80nS)
MC bus specifications correspond to a 25MHz CPU (PS/2 Model 80)
PI bus specifications correspond to 20 MHz CPU; timing specifications scale with clock frequency for other CPU speeds
0WS/ is synchronous to SYSCLK in some systems and has other timing restrictions than shown above (esp. for 8-bit cycles)
Either 0WS/ or RDY may be asserted, but not both (PC Bus)
0WS/ is used for memory accesses only; it works for I/O writes in some systems but not for I/O reads
At the end of the cycle, RDY and 0WS/ should be driven high before being tri-stated
RDY in the MC bus should be generated based on address, status, and MIO/ only



† Status signals are: MIO/ (MC, PI), S0/ & S1/ (MC), AEN (PC-I/O), BHE/ (MC, PI), RD/ (PI), RFSH/ (PC-Mem)

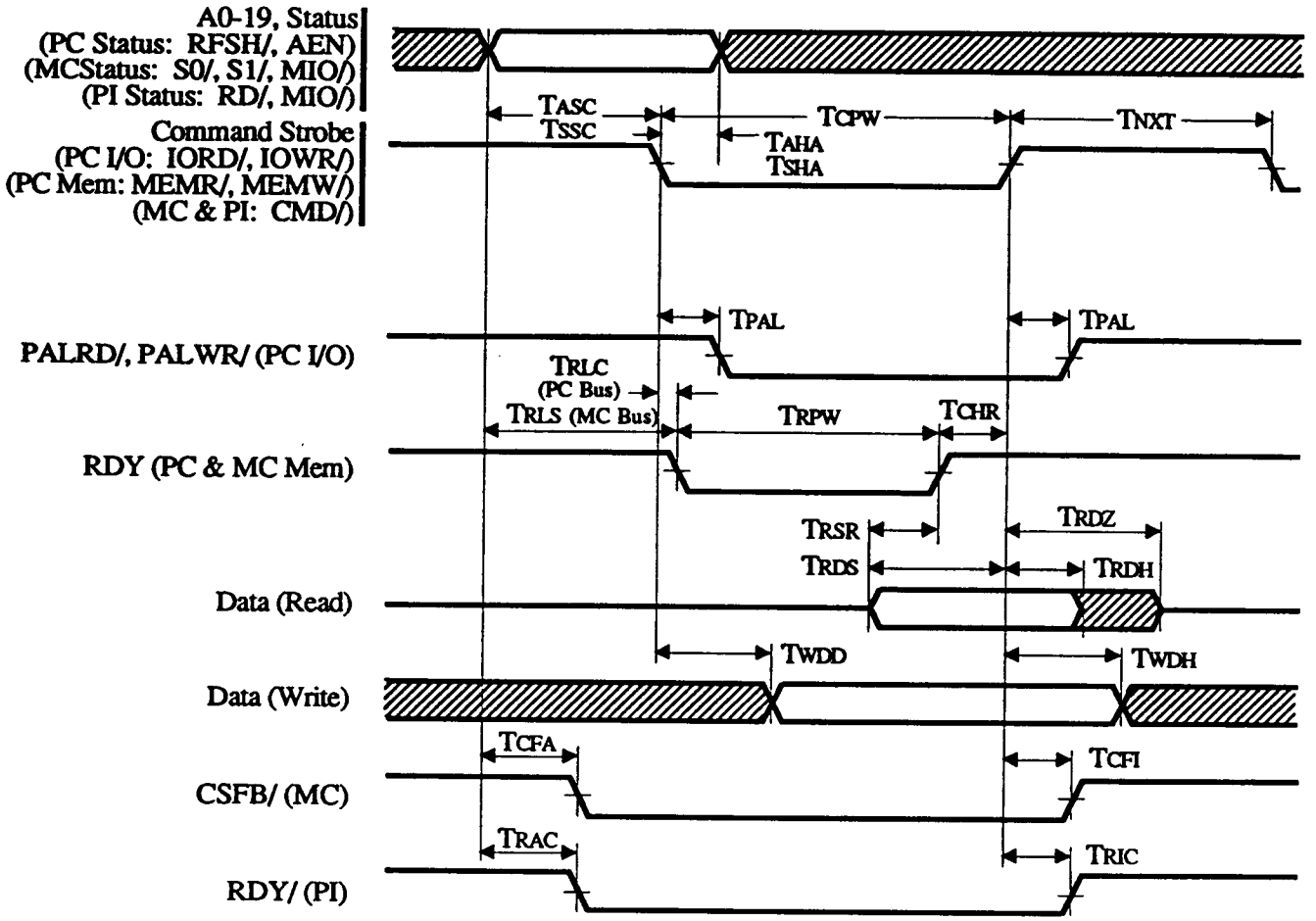
Note: Addresses must be latched on the leading edge of PSTART/ for the PI bus (addresses are not valid on the trailing edge)
Addresses should be latched on the trailing edge of ALE for the PC bus (addresses are not valid on the leading edge)
Addresses should be latched on the leading or trailing edge of ADL/ for the MC bus (addresses are valid on both edges)
Addresses may be latched on the leading edge of CMD/ instead on PC and MC bus (not PI!) if ALE or ADL/ are not used

PC / MC / PI Bus Timing Characteristics for Non-Bus-Master Peripheral Devices

AC TIMING CHARACTERISTICS - BUS TIMING

Symbol	Parameter	Notes	Min	Typ	Max	Units
T_{CPW}	Command Strobe Pulse Width	PC Bus	120	–	–	nS
T_{CPW}	Command Strobe Pulse Width	MC & PI Bus	90	–	–	nS
T_{CHR}	Command Strobe Hold from Ready	Mem Accesses Only	0	–	–	nS
T_{NXT}	Command Strobe Inactive to Next Strobe		80	–	–	nS
T_{ASC}	Address Setup to Command Strobe (5V)		30	–	–	nS
T_{ASC}	Address Setup to Command Strobe (3.3V)		50	–	–	nS
T_{SSC}	Status Setup to Command Strobe (5V)		30	–	–	nS
T_{SSC}	Status Setup to Command Strobe (3.3V)		50	–	–	nS
T_{AHA}	Address Hold from Address Enable		0	–	–	nS
T_{SHA}	Status Hold from Address Enable		20	–	–	nS
T_{RDS}	Read Data Setup to Read Strobe		30	–	–	nS
T_{RSR}	Read Data Setup to Ready	Mem Accesses Only	25	–	–	nS
T_{RDH}	Read Data Hold from Read Strobe		10	–	–	nS
T_{RDZ}	Read Data Tristated from Read Strobe (5V)		–	–	40	nS
T_{RDZ}	Read Data Tristated from Read Strobe (3.3V)		–	–	66	nS
T_{WDD}	Write Data Delay from Address Enable		–	–	20	nS
T_{WDH}	Write Data Hold from Write Strobe		10	–	–	nS
T_{RLC}	RDY Low Delay from Command Strobe (5V)	PC Bus Mem Only	–	–	40	nS
T_{RLC}	RDY Low Delay from Command Strobe (3.3V)	PC Bus Mem Only	–	–	66	nS
T_{RLS}	RDY Low Delay from Status (5V)	MC Bus Mem Only	–	–	40	nS
T_{RLS}	RDY Low Delay from Status (3.3V)	MC Bus Mem Only	–	–	66	nS
T_{RPW}	RDY Pulse Width	Mem Accesses Only	0	–	128Tm	nS
T_{CFA}	CSFB/ Active from Address/Status Valid (5V)	MC Bus Only	–	–	40	nS
T_{CFA}	CSFB/ Active from Address/Status Valid (3.3V)	MC Bus Only	–	–	66	nS
T_{CFI}	CSFB/ Inactive from End of Strobe (5V)	MC Bus Only	–	–	40	nS
T_{CFI}	CSFB/ Inactive from End of Strobe (3.3V)	MC Bus Only	–	–	66	nS
T_{RAC}	RDY/ Active from Command Strobe	PI Bus Only	2Tm	–	–	nS
T_{RIC}	RDY/ Inactive from Command Strobe (5V)	PI Bus Only	–	–	40	nS
T_{RIC}	RDY/ Inactive from Command Strobe (3.3V)	PI Bus Only	–	–	66	nS

Note: Unless otherwise specified, specifications above apply to both 5V and 3.3V operation.

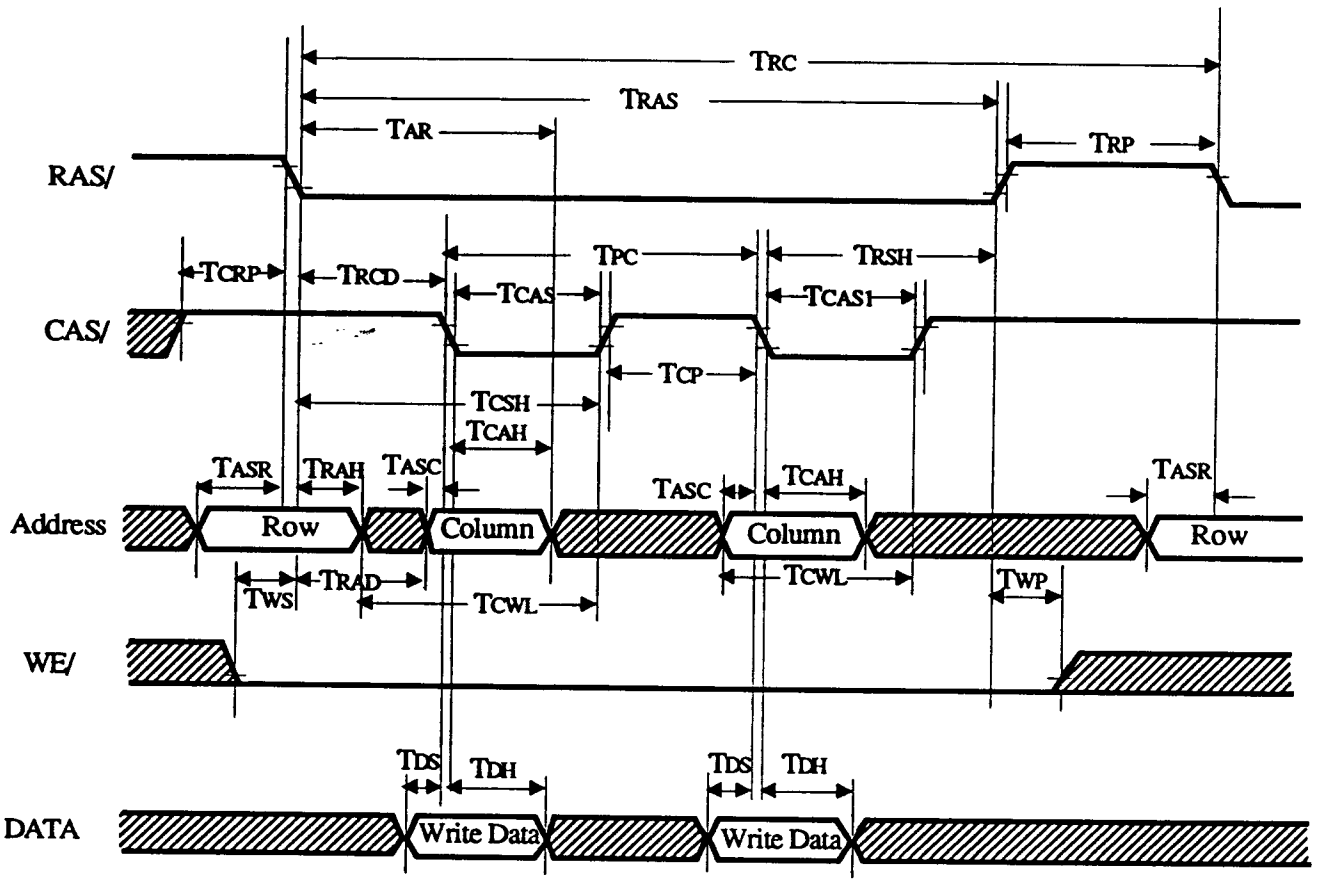


Bus Cycle Timing

AC TIMING CHARACTERISTICS - DRAM TIMING

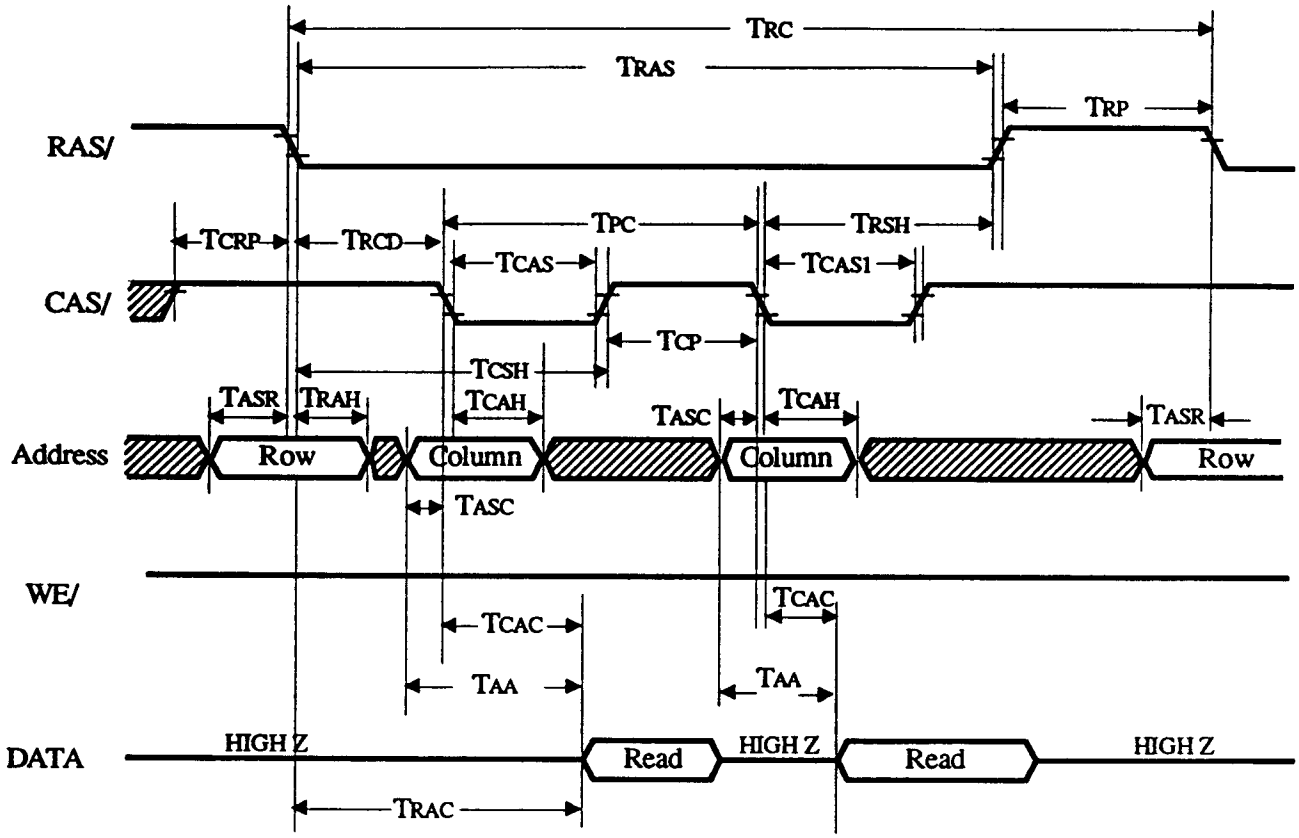
Symbol	Parameter	2 DRAM Min	2 DRAM Max	4 DRAM Min	4 DRAM Max	Units
T_{RC}	Read/Write Cycle Time	18Tm – 5	–	12Tm – 5	–	nS
T_{RAS}	RAS/ Pulse Width	14Tm – 5	–	8Tm – 5	–	nS
T_{RP}	RAS/ Precharge	4Tm	–	4Tm	–	nS
T_{CRP}	CAS/ to RAS/ precharge	4Tm – 5	–	4Tm – 5	–	nS
TCSH	CAS/ Hold from RAS/	5Tm	–	5Tm	–	nS
T_{RCD}	RAS/ to CAS/ delay	3Tm – 5	–	3Tm – 5	–	nS
T_{RSH}	RAS/ Hold from CAS/	2Tm – 5	–	2Tm – 5	–	nS
T_{CP}	CAS/ Precharge	Tm – 5	–	Tm – 5	–	nS
T_{CAS}	CAS/ Pulse Width	3Tm – 5	–	3Tm – 5	–	nS
T_{CAS1}	CAS/ Pulse Width (Fast Page Cycle)	2Tm – 5	–	2Tm – 5	–	nS
T_{ASR}	Row Address Setup to RAS/	2Tm – 10	–	2Tm – 10	–	nS
TASC	Column Address Setup to CAS/	Tm – 10	–	Tm – 10	–	nS
T_{RAH}	Row Address Hold from RAS/	Tm	–	Tm	–	nS
T_{CAH}	Column Address Hold from CAS/	Tm	–	Tm	–	nS
T_{CAC}	Data Access Time from CAS/	–	2Tm – 5	–	2Tm – 5	nS
T_{RAC}	Data Access time from RAS/	5Tm	–	5Tm	–	nS
T_{DS}	Write Data Setup to CAS/	Tm – 5	–	Tm – 5	–	nS
T_{DH}	Write Data Hold from CAS/	2Tm – 5	–	2Tm – 5	–	nS
TPC	CAS Cycle Time	3Tm	–	3Tm	–	nS
T_{WS}	WE/ Setup to RAS/	5	–	2Tm	–	nS
T_{WP}	WE/ Hold from RAS/	0	–	–	–	nS

Note: Unless otherwise specified, specifications above apply to both 5V and 3.3V operation.



DRAM Page Mode Write Cycle Timing

Note: The above diagram represents a typical page mode write cycle.
The number of actual CAS cycles may vary between 0 and 4.

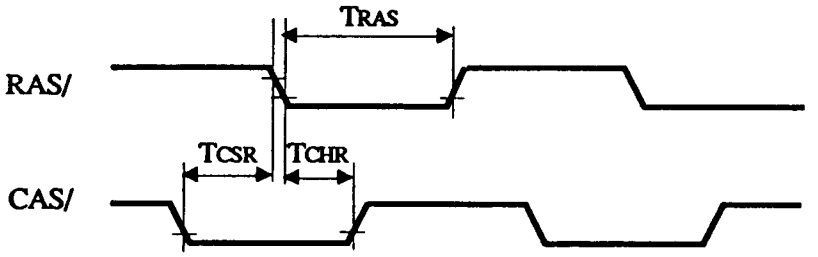


DRAM Page Mode Read Cycle Timing

Note: The above diagram represents a typical page mode read cycle. The number of actual CAS cycles may vary. The maximum number of CAS cycles allowed is 32 (when the FIFO is being filled).

AC TIMING CHARACTERISTICS - REFRESH TIMING

Symbol	Parameter	Notes	Min	Typ	Max	Units
T_{CHR}	RAS to CAS delay	Tm = 17.7 @ 56 MHz	5Tm – 5	–	5Tm + 5	nS
T_{CSR}	CAS to RAS delay	5Tm = 88.3 ns (56 MHz) or 100 ns (50MHz)	Tm – 5	–	Tm + 5	nS
TRAS	RAS pulse width		5Tm – 5	–	5Tm + 5	nS



CAS-Before-RAS (CBR) DRAM Refresh Cycle Timing

Note: Unless otherwise specified, specifications above apply to both 5V and 3.3V operation.

AC TIMING CHARACTERISTICS - VRAM TIMING

Symbol	Parameter	2 VRAM Min	2 VRAM Max	4 VRAM Min	4 VRAM Max	Units
T_{RC}	Read/Write Cycle Time	12Tm	–	9Tm	–	nS
T_{RAS}	RAS/ Pulse Width	8Tm	–	5Tm	–	nS
T_{AR}	Column Address Hold from RAS/	Tm	–	Tm	–	nS
T_{RP}	RAS/ Precharge	4Tm	–	4Tm	–	nS
T_{CRP}	CAS/ to RAS/ precharge	4Tm	–	4Tm	–	nS
T_{CSH}	CAS/ Hold from RAS/	5Tm	–	5Tm	–	nS
T_{RCD}	RAS/ to CAS/ delay	2Tm	–	2Tm	–	nS
T_{RSH}	RAS/ Hold from CAS/	2Tm	–	2Tm	–	nS
T_{CPN}	CAS/ Precharge	Tm	–	Tm	–	nS
T_{CAS}	CAS/ Pulse Width	3Tm	–	3Tm	–	nS
T_{CAS1}	CAS/ Pulse Width (Fast Page Cycle)	2Tm	–	2Tm	–	nS
T_{ASR}	Row Address Setup to RAS/	2Tm - 10	–	2Tm - 10	–	nS
T_{ASC}	Column Address Setup to CAS/	Tm -10	–	Tm -10	–	nS
T_{RAD}	Column Address from RAS/	Tm	–	Tm	–	nS
T_{RAH}	Row Address Hold from RAS/	Tm	–	Tm	–	nS
T_{CAH}	Column Address Hold from CAS/	Tm	–	Tm	–	nS
T_{CAC}	Data Access Time from CAS/	–	2Tm	–	2Tm	nS
T_{RAC}	Data Access Time from RAS/	–	5Tm	–	5Tm	nS
T_{OEA}	Data Access Time from OE/	–	4Tm	–	4Tm	nS
T_{WP}	WE/ Pulse Width	6Tm	–	6Tm	–	nS
T_{DS}	Write Data Setup to CAS/	Tm	–	Tm	–	nS
T_{DH}	Write Data Hold from CAS/	2Tm	–	2Tm	–	nS
T_{DHR}	Write Data Hold from RAS/	4Tm	–	4Tm	–	nS
T_{WS}	WE/ Setup to RAS/	5	–	2Tm	–	nS
T_{WP}	WE/ Hold from RAS/	0	–	–	–	nS

Note: Unless otherwise specified, specifications above apply to both 5V and 3.3V operation.

AC TIMING CHARACTERISTICS - DISPLAY MEMORY (VRAM)

VRAM TIMING - TIMING SPECIFICATIONS (continued)

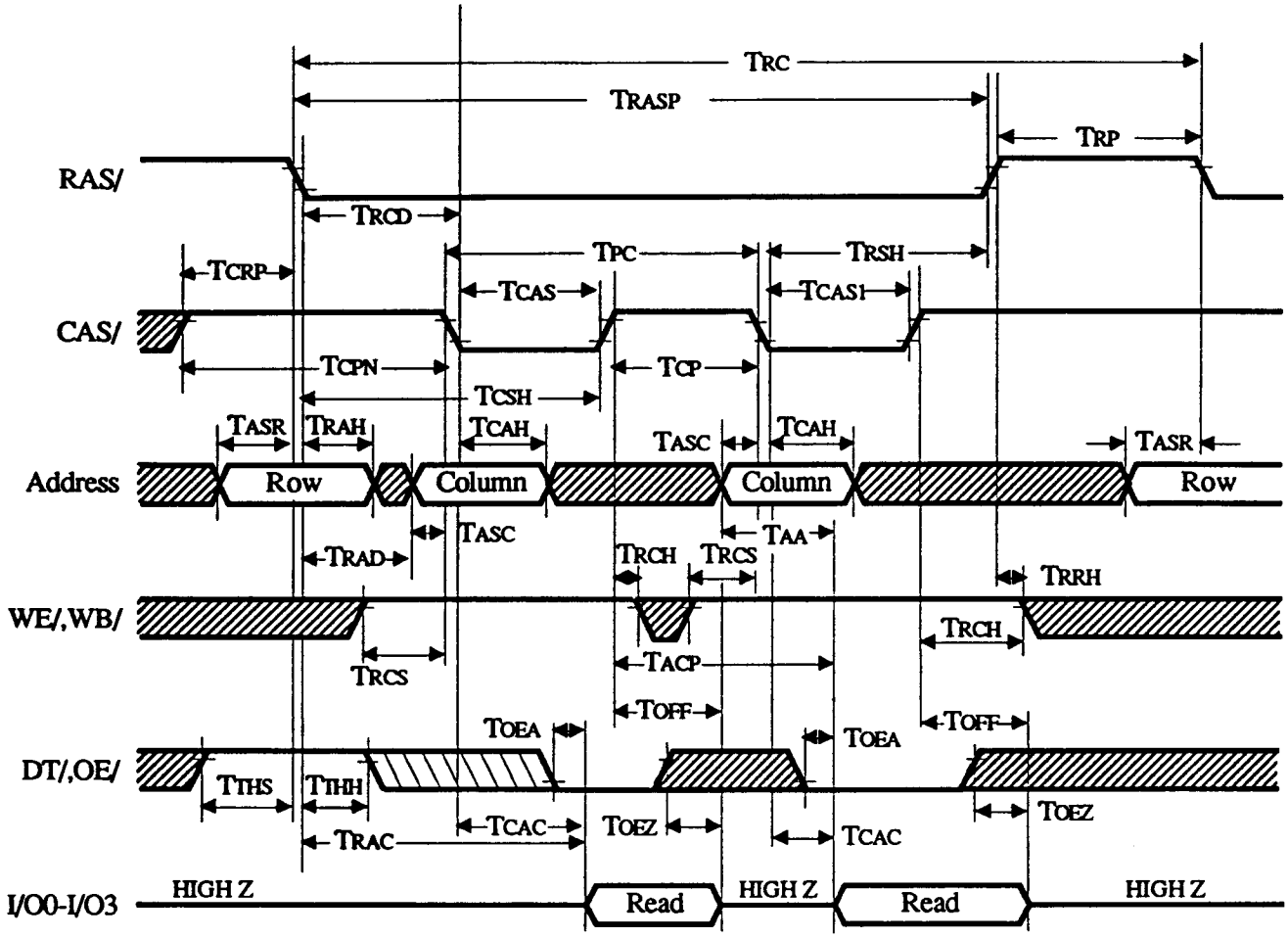
Symbol	Parameter	Min	Typ	Max	Units
T_{DLS}	DT/ Low Setup	$T_M - 5$	–	–	nS
T_{RDH}	DT/ Low Hold after RAS/ Low	$4T_M$	–	–	nS
T_{CDH}	DT/ Low Hold after CAS/ Low	$3T_M - 5$	–	–	nS
T_{THS}	DT/ High Setup	$T_M - 5$	–	–	nS
T_{THH}	DT/ High Hold	T_M	–	–	nS

VRAM TIMING - CLOCK USED FOR SERIAL PORT

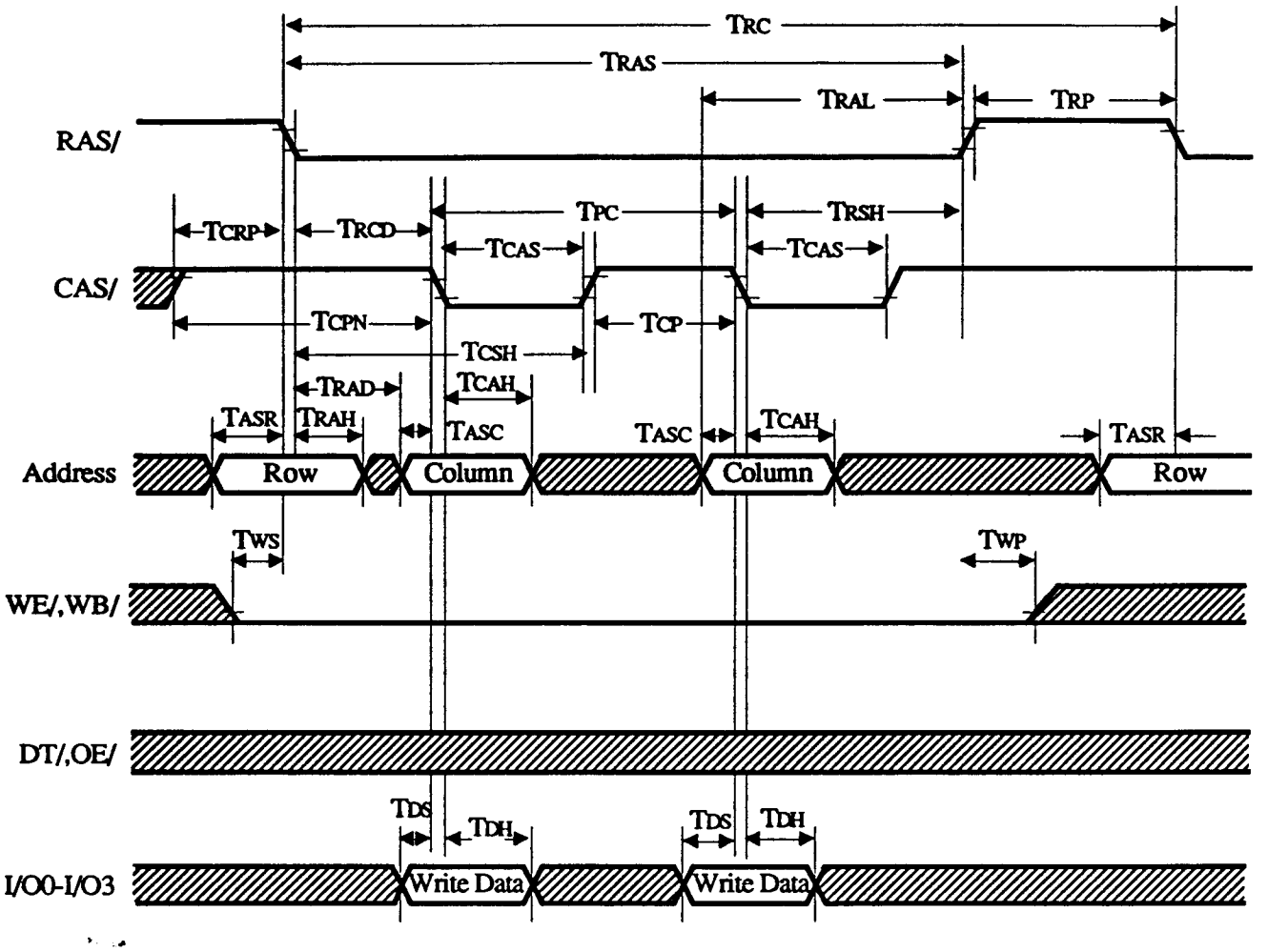
Symbol	Parameter	Min	Typ	Max	Units
T_{SCC}	Sequencer Clock	40	–	50	nS

VRAM TIMING - SERIAL PORT TIMING

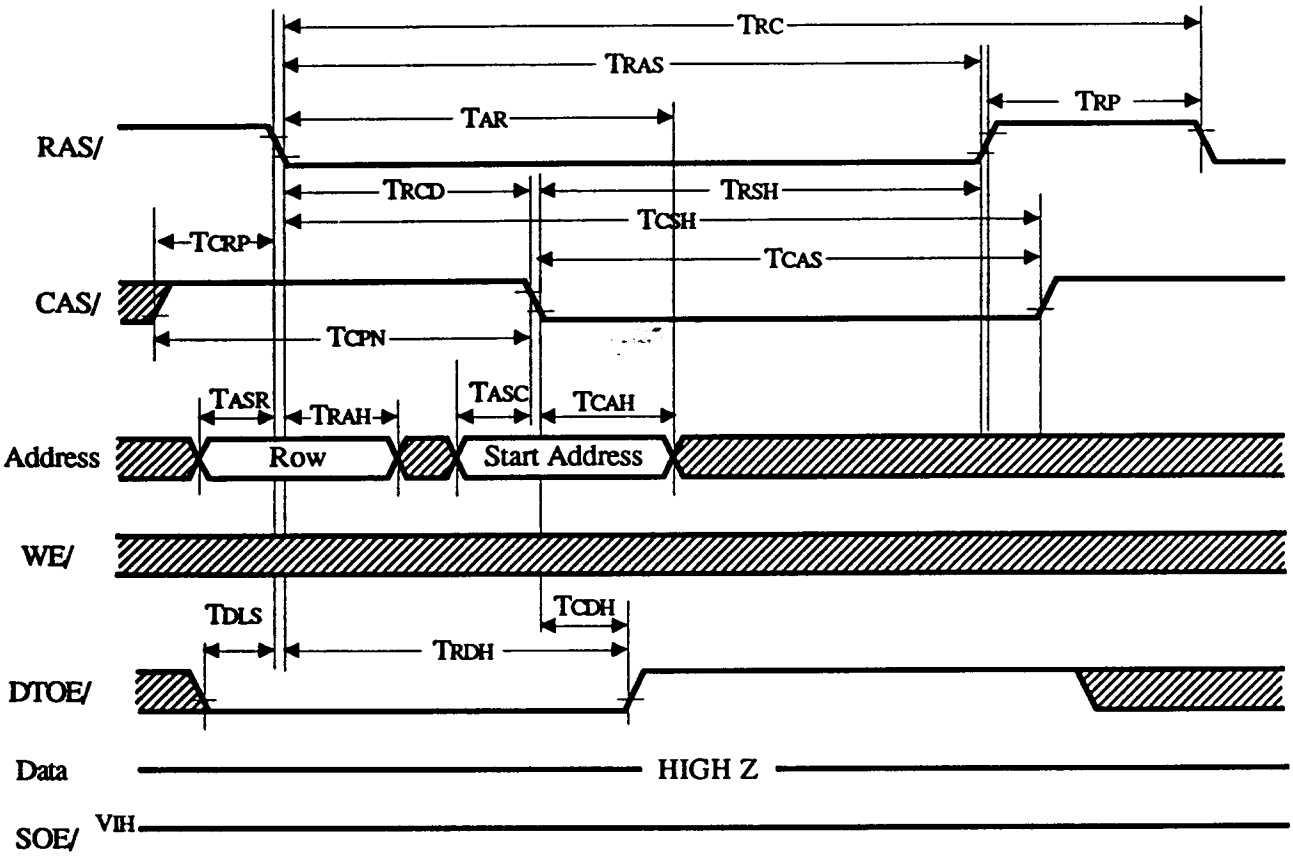
Symbol	Parameter	Min	Typ	Max	Units
T_{SC}	SC Cycle Time	–	0.45 T_{SCC}	–	nS
T_{SCP}	SC Precharge Time	–	0.45 T_{SCC}	–	nS
T_{SCA}	Access Time from SC	–	–	25	nS
T_{SOH}	Serial Output Hold Time	5	–	–	nS



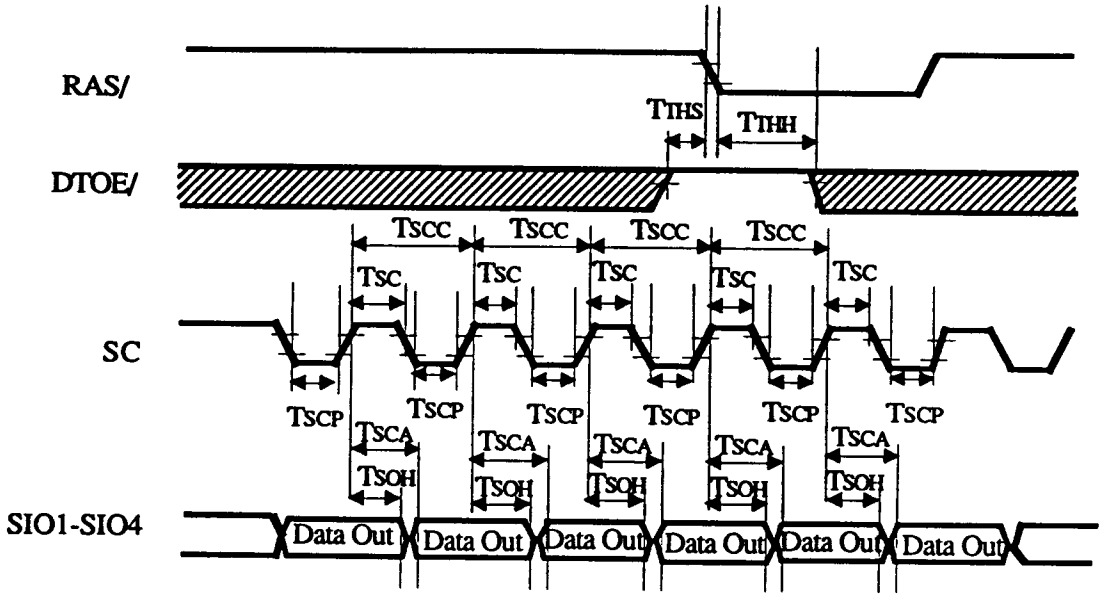
VRAM Page Mode Read Cycle Timing



VRAM Page Mode Write Cycle Timing



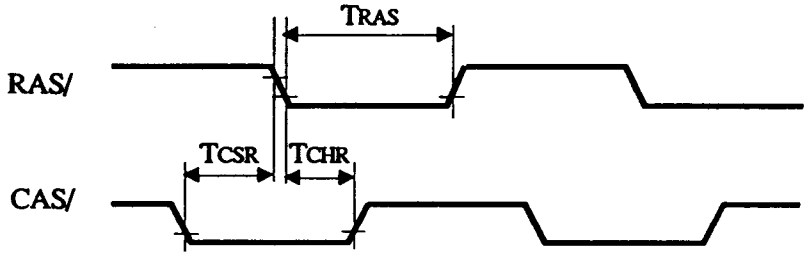
VRAM Transfer Cycle Timing



VRAM Serial Read Cycle Timing

AC TIMING CHARACTERISTICS - VRAM REFRESH TIMING

Symbol	Parameter	Notes	Min	Typ	Max	Units
T_{CHR}	RAS to CAS delay	Tm = 17.7 @ 56 MHz	5Tm – 5	–	5Tm + 5	nS
T_{CSR}	CAS to RAS delay	5Tm = 88.3 ns (56 MHz) or 100 ns (50MHz)	Tm – 5	–	Tm + 5	nS
T_{RAS}	RAS pulse width		5Tm – 5	–	5Tm + 5	nS

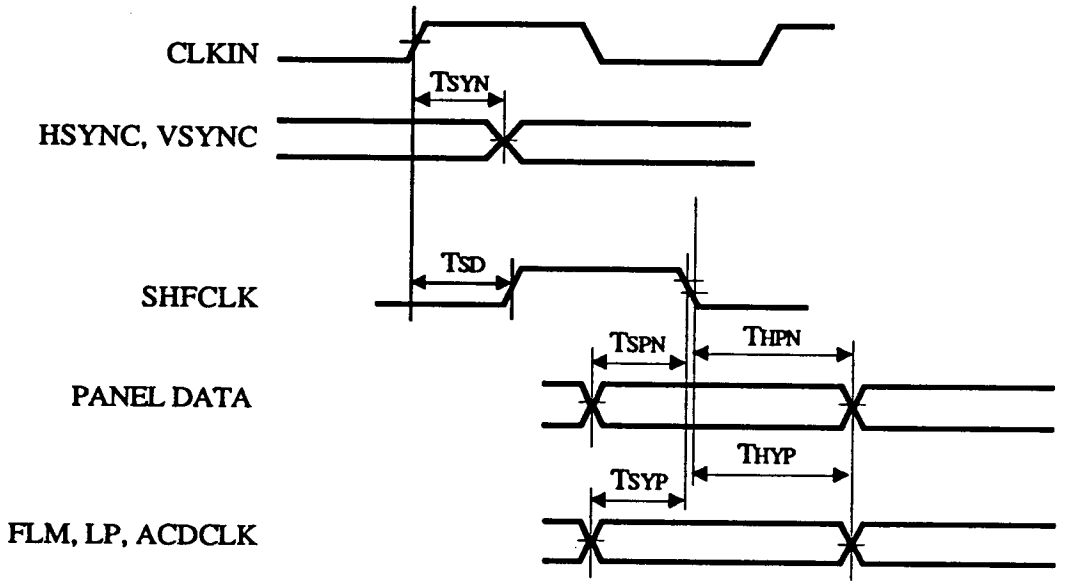


CAS-Before-RAS (CBR) VRAM Refresh Cycle Timing

Note: Unless otherwise specified, specifications above apply to both 5V and 3.3V operation.

AC TIMING CHARACTERISTICS - VIDEO TIMING

Symbol	Parameter		Min	Max	Units
T_{SYN}	HSYNC, VSYNC delay from CLKIN (5V)		–	50	nS
T_{SYN}	HSYNC, VSYNC delay from CLKIN (3.3V)		–	80	nS
T_{SD}	CLKIN to SHFCLK delay (5V)		–	30	nS
T_{SD}	CLKIN to SHFCLK delay (3.3V)		–	50	nS
T_{SPN}	Panel data setup to SHFCLK		5	–	nS
T_{HPN}	Panel data hold to SHFCLK		10	–	nS
T_{SYP}	FLM, LP, ACDCLK setup to SHFCLK (5V)		5	–	nS
T_{SYP}	FLM, LP, ACDCLK setup to SHFCLK (3.3V)		8	–	nS
T_{HYP}	FLM, LP, ACDCLK hold to SHFCLK (5V)		10	–	nS
T_{HYP}	FLM, LP, ACDCLK hold to SHFCLK (3.3V)		16	–	nS

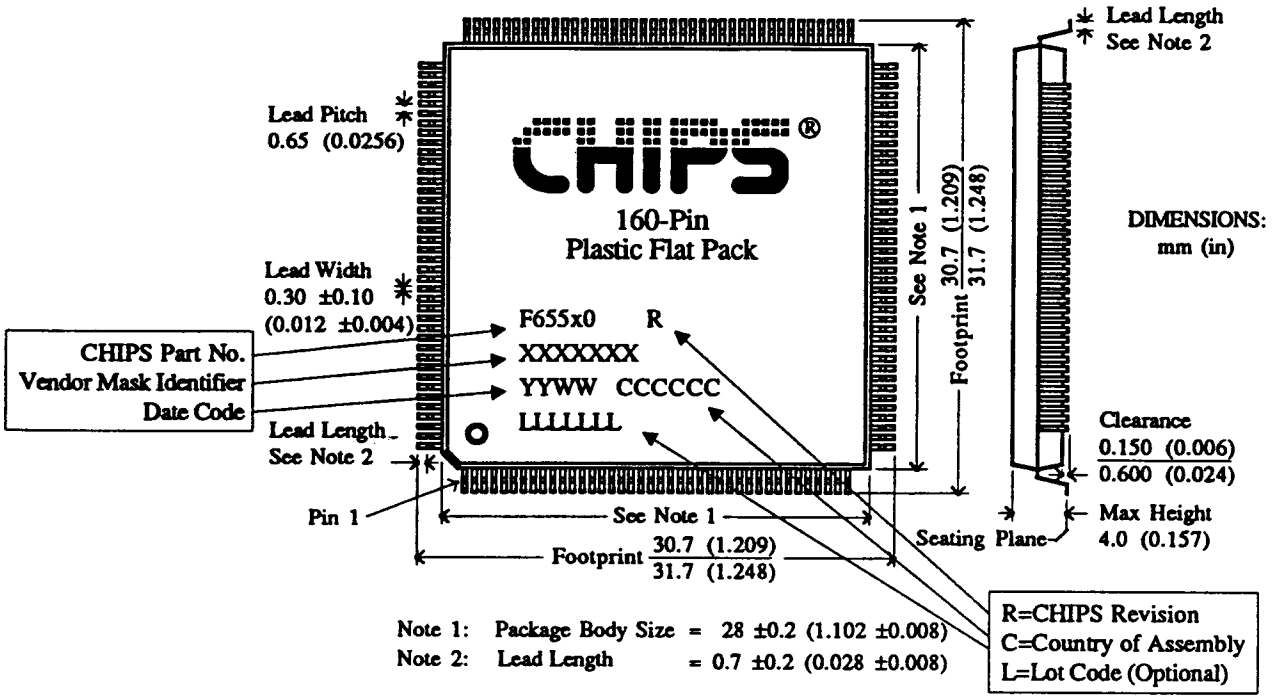


Flat Panel and CRT Video Data and Control Signal timing

Note: Unless otherwise specified, specifications above apply to both 5V and 3.3V operation.

This Page Intentionally Left Blank

Mechanical Specifications



Suggested PCB Pad Layout