Data Sheet
STC803/809/810-811/812/-823/824/825-6342/6343/6344/6345
µP Supervisor Circuits

Features

- Precision supply-voltage monitor
  - 4.63V (STC8xxL, STC634xL)
  - 4.38V (STC8xxM, STC634xM)
  - 3.08V (STC8xxT, STC634xT)
  - 2.93V (STC8xxS, STC634xS)
  - 2.63V (STC8xxR, STC634xR)
  - 2.32V (STC8xxZ, STC634xZ)
  - 2.20V (STC8xxY, STC634xY)
- 200ms reset pulse width
- Debounced CMOS-compatible manual-reset input (811, 812, 823, 825, 6342-6344)
- Reset Output Signal for Watchdog and Power Abnormal, Manual Reset
- Reset Push-Pull output (STC809,811,823, 824,825,6342,6345)
- Reset Open-Drain output (STC803/6343)
- Voltage monitor for power-fail or low battery warning
- Guaranteed $\overline{\text{RESET}}$/RESET valid at V_{CC} = 1.0V

Introduction

The STCxxx family microprocessor (µP) supervisory circuits are targeted to improve reliability and accuracy of power-supply circuitry in µP systems. These devices reduce the complexity and number of components required to monitor power-supply and battery functions.

The main functions are:

1. Asserting reset output during power-up, power-down and brownout conditions for µP system;
2. Detecting power failure or low-battery conditions with a 1.25V threshold detector;
3. Watchdog functions;
4. Manual reset.

Applications

- Power-supply circuitry in µP systems

Ordering Information

	Part No.	$\overline{\text{RESET}}$ output		RESET output (push-pull)	Manual Reset Input	Power Fail Detector (1.25V)	Watchdog Input	Package
		Push-Pull	Open-Drain					
1	STC803X	-	√	-	-	-	-	SOT23-3
2	STC809X	√	-	-	-	-	-	
3	STC810X	-	-	√	-	-	-	
4	STC811X	√	-	-	√	-	-	SOT23-5
5	STC812X	-	-	√	√	-	-	
6	STC823X	√	-	-	√	-	√	
7	STC824X	√	-	√	-	-	√	
8	STC825X	√	-	√	√	-	-	
9	STC6342X	√	-	-	√	√	-	SOT23-6
10	STC6343X	-	√	-	√	√	-	
11	STC6344X	-	-	√	√	√	-	
12	STC6345X	√	-	√	-	√	-	

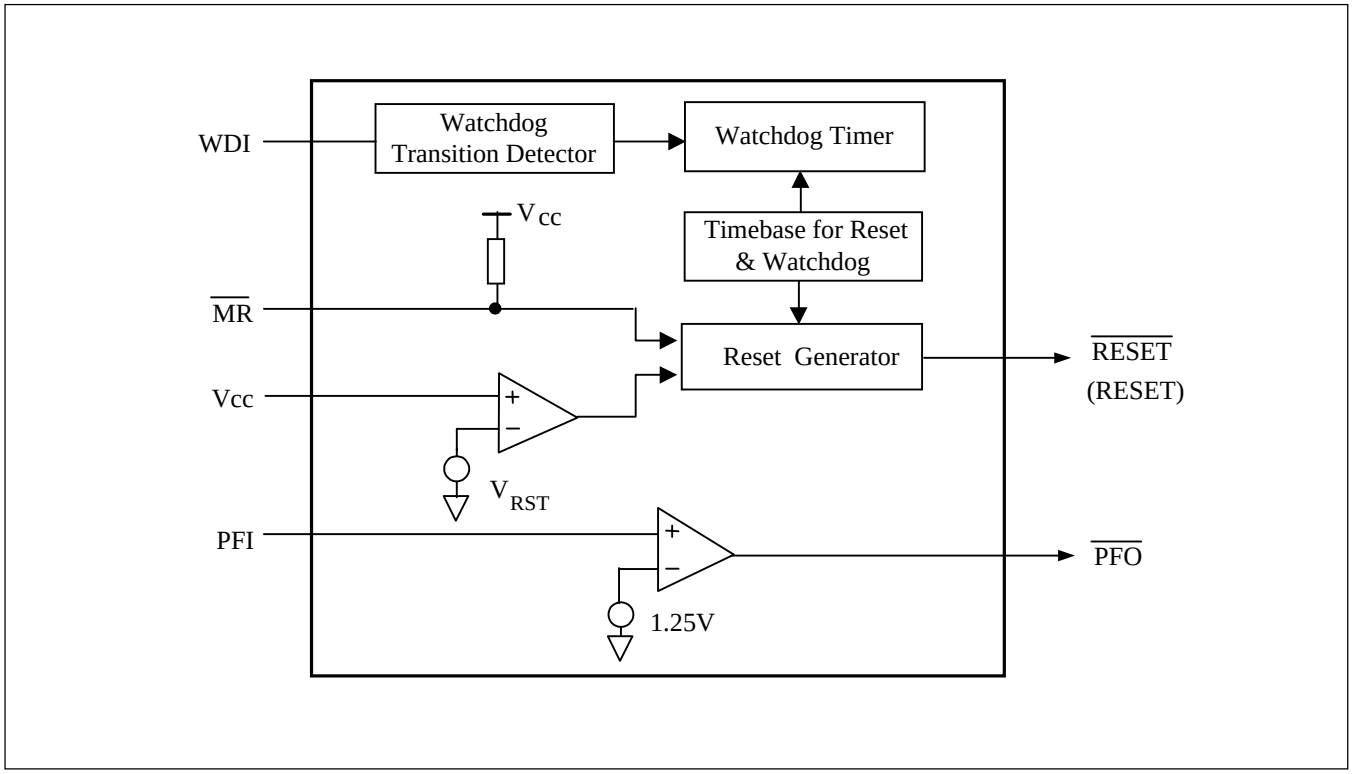
Suffix: X -- Monitored Voltage

Suffix X	L	M	T	S	R	Z	Y
Reset threshold (V)	4.63	4.38	3.08	2.93	2.63	2.32	2.20

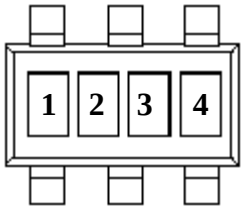
Contents

Block Diagram

Figure 1. Block Diagram



Marking Information



Code	Description
1 2	Part Number
3	Year
4	Work Week

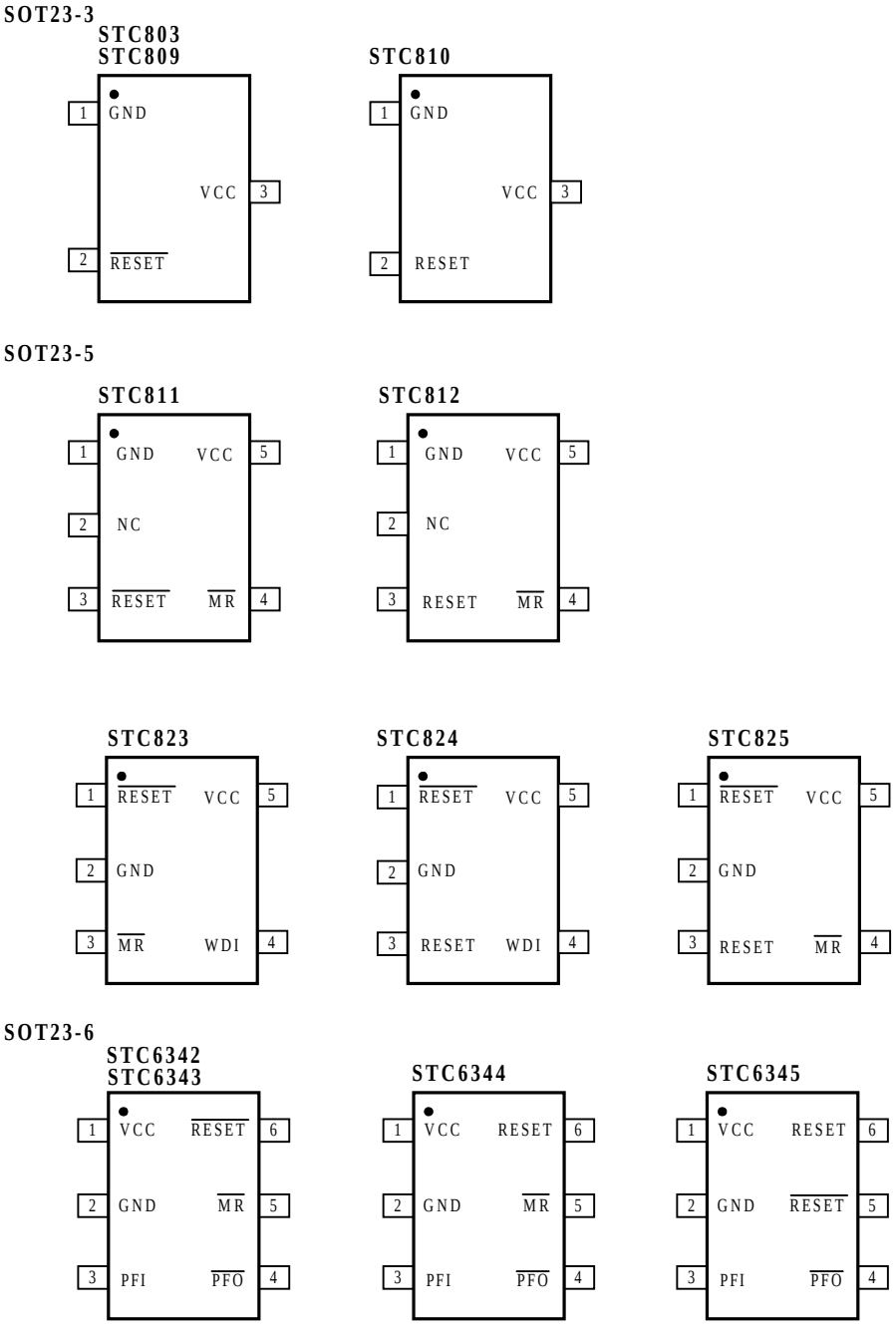
Part Number Code

Code 1 2	Part No.	Code 1 2	Part No.	Code 1 2	Part No.
AA	STC809L	BC	STC803L	CE	STC6342L
AB	STC809M	BD	STC803M	CF	STC6342M
AC	STC809T	BE	STC803T	CG	STC6342T
AD	STC809S	BF	STC803S	CH	STC6342S
AE	STC809R	BG	STC803R	CI	STC6342R
AF	STC809Z	BH	STC803Z	CJ	STC6342Z
AG	STC809Y	BI	STC803Y	CK	STC6342Y
AH	STC810L	BJ	STC823L	CL	STC6343L
AI	STC810M	BK	STC823M	CM	STC6343M
AJ	STC810T	BL	STC823T	CN	STC6343T
AK	STC810S	BM	STC823S	CO	STC6343S
AL	STC810R	BN	STC823R	CP	STC6343R
AM	STC810Z	BO	STC823Z	CQ	STC6343Z
AN	STC810Y	BP	STC823Y	CR	STC6343Y
AO	STC811L	BQ	STC824L	CS	STC6344L
AP	STC811M	BR	STC824M	CT	STC6344M
AQ	STC811T	BS	STC824T	CU	STC6344T
AR	STC811S	BT	STC824S	CV	STC6344S
AS	STC811R	BU	STC824R	CW	STC6344R
AT	STC811Z	BV	STC824Z	CX	STC6344Z
AU	STC811Y	BW	STC824Y	CY	STC6344Y
AV	STC812L	BX	STC825L	CZ	STC6345L
AW	STC812M	BY	STC825M	DA	STC6345M
AX	STC812T	BZ	STC825T	DB	STC6345T
AY	STC812S	CA	STC825S	DC	STC6345S
AZ	STC812R	CB	STC825R	DD	STC6345R
BA	STC812Z	CC	STC825Z	DE	STC6345Z
BB	STC812Y	CD	STC825Y	DF	STC6345Y

Pin Information

Pin Configuration

Figure 2. Pin Configuration



Pin Description

Table 2. Pin Description

Pin Name	Type	Description
$\overline{MR}$	I	**Manual-Reset: (CMOS).** Active low. Pull low to force a reset. Reset remains asserted for the duration of the Reset Timeout Period after $\overline{MR}$ transitions from low to high. Leave unconnected or connected to VCC if not used.
Vcc	Power	**Power Supply:** Reset is asserted when V_{CC} drops below the Reset Threshold Voltage (V_{RST}). Reset remains asserted until V_{CC} rises above V_{RST} and keep asserted for the duration of the Reset Timeout Period (t_{RS}) once V_{CC} rises above V_{RST}.
GND	Ground	**Ground Reference** for all signals
PFI	I	**Power-Fail Voltage Monitor Input.** When PFI <V_{PFT} , $\overline{PFO}$ goes low. Connect PFI to GND or Vcc when not used.
$\overline{PFO}$	O	**Power-Fail Output:** it gets low and sinks current when PFI is less than 1.25V; otherwise PFO stays high.
WDI	I	Watchdog Input (CMOS). If WDI remains high or low for the duration of the watchdog timeout period (t_{WD}), the internal watchdog timer trigger a reset output. Floating WDI or connecting WDI to a high-impedance three-state buffer disables the watchdog feature. The internal watchdog timer clears whenever reset is asserted or WDI occurs a rising or falling edge.
$\overline{RESET}$	O	**Active-Low Reset Output (Push-Pull or Open-Drain).** It goes low when Vcc is below the reset threshold. It remains low for about 200ms after one of the following occurs: Vcc rises above the reset threshold (V_{RST}), the watchdog triggers a reset, or $\overline{MR}$ goes from low to high.
RESET	O	**The inverse of $\overline{RESET}$**, active high. Whenever $\overline{RESET}$ is high, RESET is low.
NC	-	**No connection**

Functional Description

Reset Output

A microprocessor's (µP's) reset input starts the µP in a known state. Whenever the µP is in an unknown state, it should be held in reset. The supervisory circuits assert reset during power-up and prevent code execution errors during power-down or brownout conditions.

On power-up, once Vcc reaches about 1.0V, $\overline{\text{RESET}}$ is a guaranteed logic low of 0.4V or less. As Vcc rises, $\overline{\text{RESET}}$ stays low. When Vcc rises above the reset threshold, an internal timer releases $\overline{\text{RESET}}$ after about 200ms. $\overline{\text{RESET}}$ pulses low whenever Vcc drops below the reset threshold, i.e. brownout condition. If brownout occurs in the middle of a previously initiated reset pulse, the pulse continues for at least another 200ms. On power-down, once Vcc falls below the reset threshold, $\overline{\text{RESET}}$ stays low and is guaranteed to be 0.4V or less until Vcc drops below 1.0V. Fig 4 shows the timing relationship.

The active-high RESET output is simply the inverse of the $\overline{\text{RESET}}$ output, and is guaranteed to be valid with Vcc down to 1.0V.

Watchdog Timer

The STC**823/824** watchdog circuit monitors the µP's activity. If the µP does not toggle the watch-dog input (WDI) within 1.6s, reset asserts. As long as reset is asserted or the WDI input is toggled, the watchdog timer will stay clear and will not count. As soon as reset is released, the timer will start counting. WDI input pulses as short as 50ns can be detected.
Disable the watchdog function by leaving WDI unconnected or by three-stating driver connected to WDI.

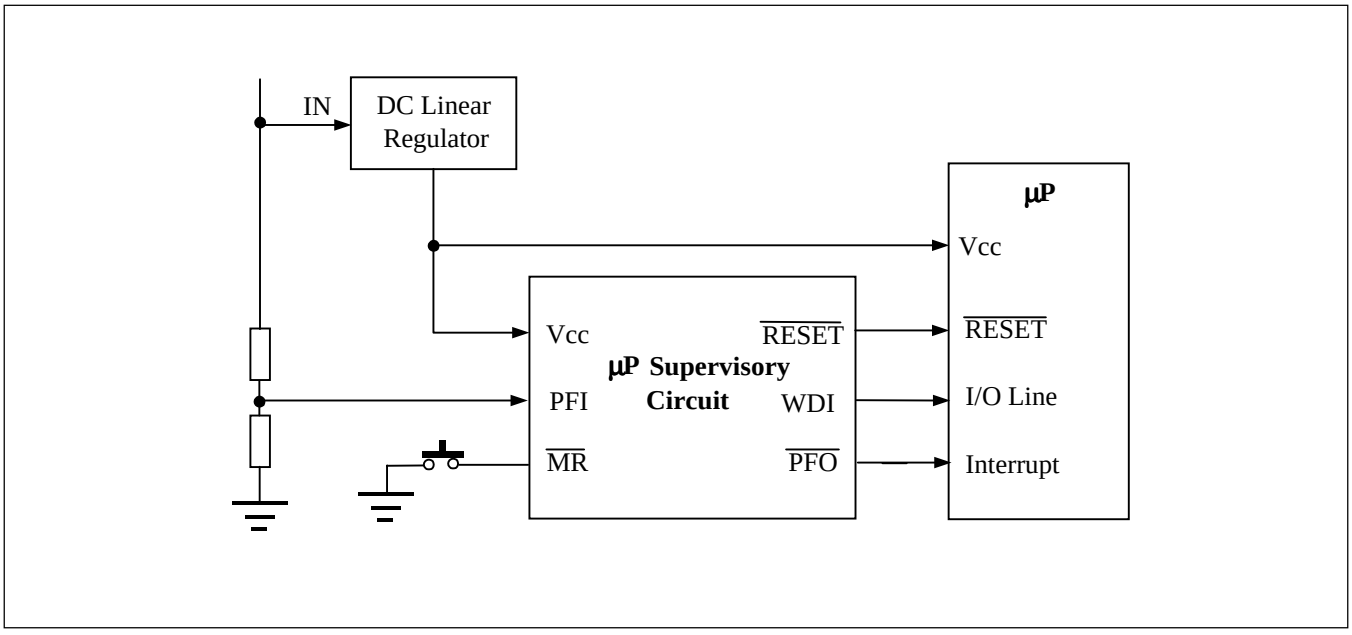
Manual Reset

The manual-reset input ($\overline{\text{MR}}$) allows reset to be triggered by a push button switch. $\overline{\text{MR}}$ has an internal pullup resistor, so it can be left open when not used.

Power-Fail Comparator

The power-fail comparator can be used for various purposes because its output and noninverting input are not internally connected. The inverting input is internally connected to a 1.25V reference.

Figure 3. Typical Application Circuit



Detailed Specifications

Absolute Maximum Ratings

Storage Temperature ..... -65°C to +150°C
Ambient Temperature with Power Applied ..... -40°C to +85°C
Supply Voltage to Ground Potential (Vcc to GND) ..... -0.3V to +7.0V
DC Input Voltage (All inputs except Vcc and GND) ..... -0.3V to V_{CC}+0.3V
DC Output Current (All outputs) 20mA
Power Dissipation 320mW
(Depend on package)

Note:
Stresses greater than those listed under MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

Recommended Operation Condition

Table 3. DC Electrical Characteristics

Sym	Description	Test Conditions	Min	Typ	Max	Unit
V_{CC}	Supply Voltage for xxxL, xxxM		4.5	5.0	5.5	V
	Supply Voltage for xxT, xxxS		3.0	3.3	5.5	V
	Supply Voltage for xxxR		2.7	3.0	5.5	V
	Supply Voltage for xxxZ, xxxY		2.4	2.5	5.5	V
V_{IH}	Input High Voltage		$0.7V_{CC}$			V
V_{IL}	Input Low Voltage				$0.3V_{CC}$	V
T_A	Operating Temperature		-40		85	°C

DC Electrical Characteristics

Table 4. DC Electrical Characteristics

(Vcc=V_{RN}+5% to 5.5V, T_A= -40~85℃, unless otherwise noted)

Symbol	Description	Test Conditions		Min	Typ	Max	Unit
V_{CC}	Operating Voltage Range			1.0		5.5	V
I_{CC}	Supply Current	Vcc = 5V, No load			20	50	µA
V_{IH}	Input High Voltage	Pin: $\overline{MR}$, WDI		0.7 Vcc			V
V_{IL}	Input Low Voltage	Pin: $\overline{MR}$, WDI				0.3 Vcc	V
V_{RST}	Reset Threshold Voltage (Note 1)	T_A= -40 ~ 85℃		V_{RN}-2.5%	V_{RN}	V_{RN}+2.5%	V
			STCxxxL	4.514	4.63	4.746	
			STCxxxM	4.271	4.38	4.490	
			STCxxxT	3.003	3.08	3.157	
			STCxxxS	2.857	2.93	3.003	
			STCxxxR	2.564	2.63	2.696	
			STCxxxZ	2.262	2.32	2.378	
			STCxxxY	2.145	2.20	2.255	
V_{RTH}	Reset Threshold Hysteresis(Note 1)	Vcc varies between V_{RN}±5%			70		mV
V_{OH}	Output High Voltage	Vcc ≥ 4.5V Isource=800µA		Vcc-1.5			V
		Vcc ≥ 2.7V Isource=500µA		0.8 Vcc			
		Vcc ≥ 1.8V Isource=150µA		0.8 Vcc			
V_{OL}	Output Low Voltage	Vcc ≥ 4.5V I_{sink}=3.2mA				0.4	V
		Vcc ≥ 2.7V I_{sink}=1.2mA				0.3	
		Vcc ≥ 1.2V I_{sink}=100µA				0.3	
I_{LKG}	Open-Drain Output Leakage Current	V_{CC} > $V_{TH(MAX)}$ for STC803 and STC6343				1	µA
V_{PFT}	PFI Input Threshold	V_{PFI} varies from 1.5V and 1.0V		1.20	1.25	1.30	V
I_{PFI}	PFI Input Leakage Current					±25	nA
I_{WDI}	Average WDI Input Current (Note 2)	WDI connected to V_{CC}: 5.5V			120	160	µA
		WDI connected to GND		-20	-15		
r	MR pull-up resistor (internal)	STC811/7812		10	20	30	kΩ
		STC823/824/825		35	52	75	
		STC6342/6343/6344		60			

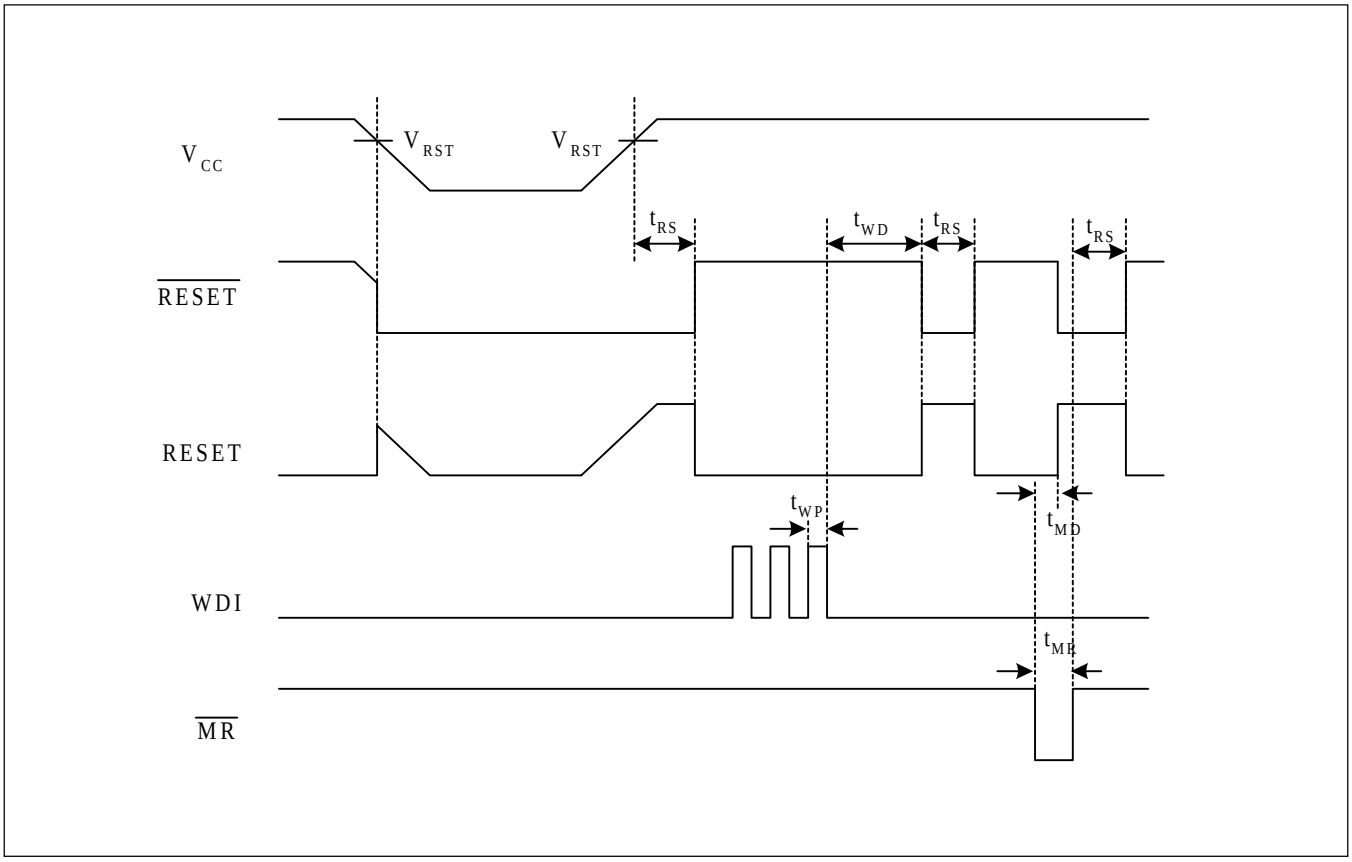
* Valid for both $\overline{RESET}$ and RESET. V_{RN} is nominal reset threshold voltage.
** WDI is internally serviced within the watchdog period if WDI is left unconnected.

AC Electrical Characteristics

Table 5. AC Electrical Characteristics

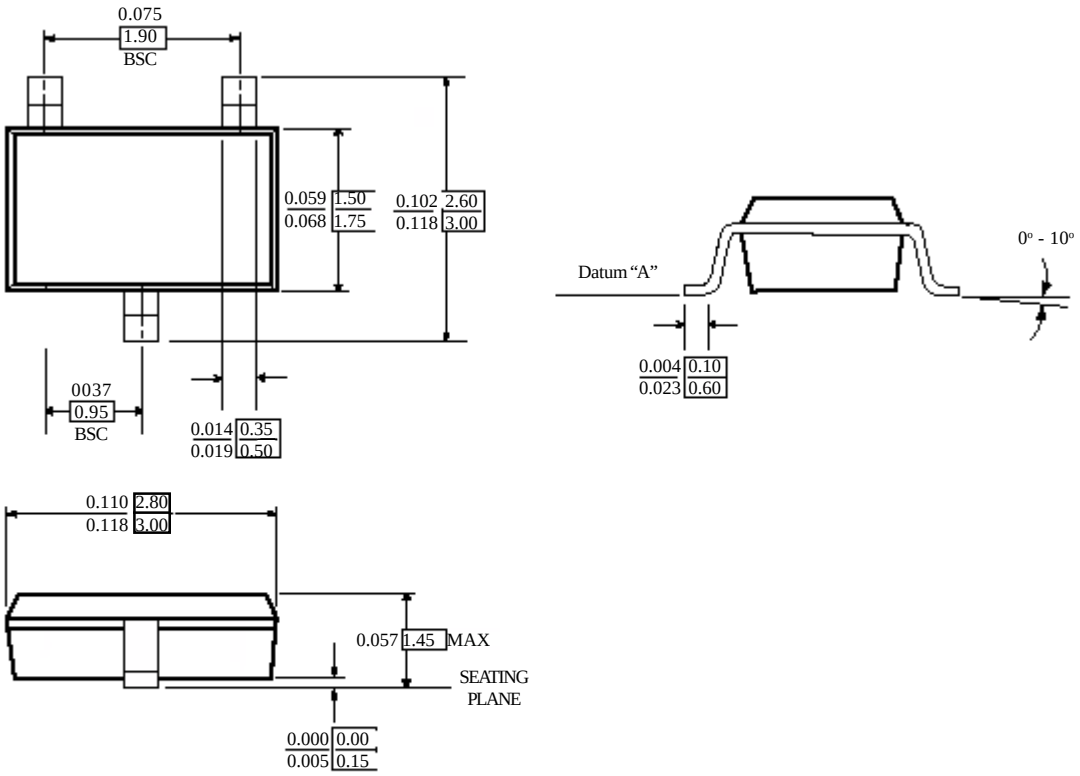
Sym	Description	Test Conditions	Min	Typ	Max	Units
t_{RS}	Reset Pulse Width	$\overline{MR}$ from low to High	140	200	280	ms
t_{WD}	Watchdog Timeout Period	WDI and $\overline{MR}$ tied to V_{CC}, $V_{CC} > V_{RN} + 5\%$	1.12	1.6	2.25	s
t_{MR}	$\overline{MR}$ Pulse Width		1			µs
t_{MD}	$\overline{MR}$ to RESET Delay	V_{CC} = 5.0V			250	ns
t_{WP}	WDI Pulse Width		50			ns

Figure 4. Watchdog Timing Diagram



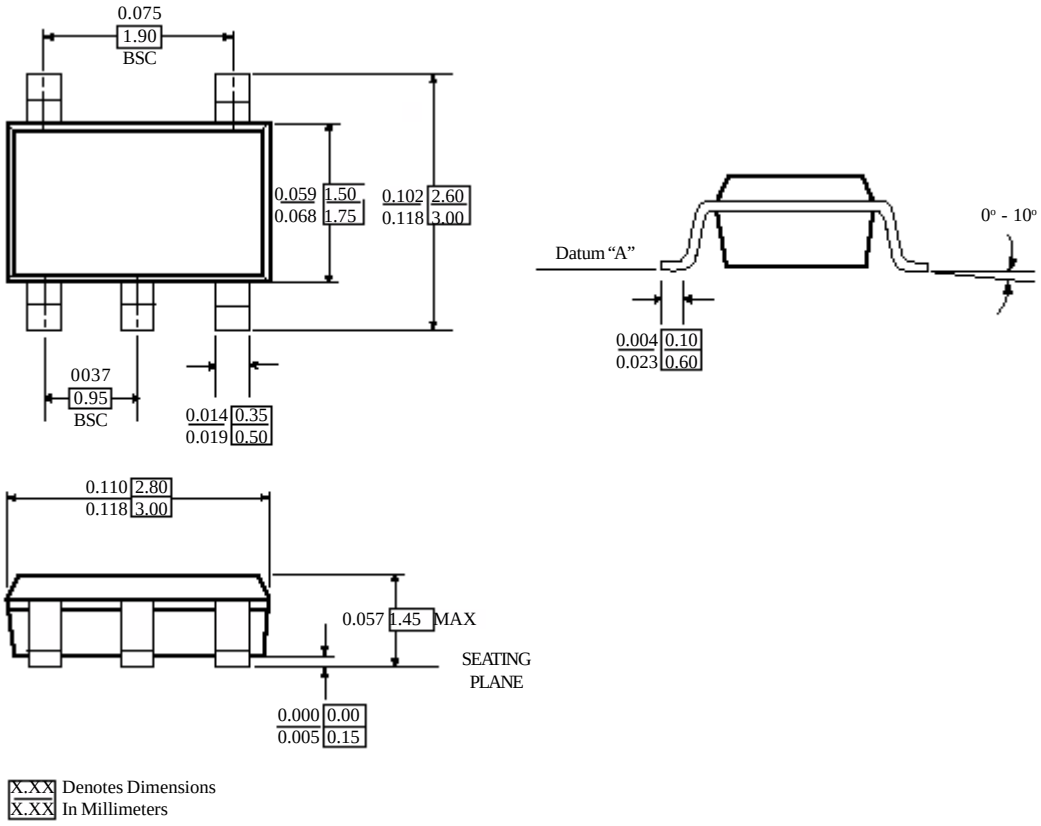
Mechanical Information

Figure 5. SOT23-3



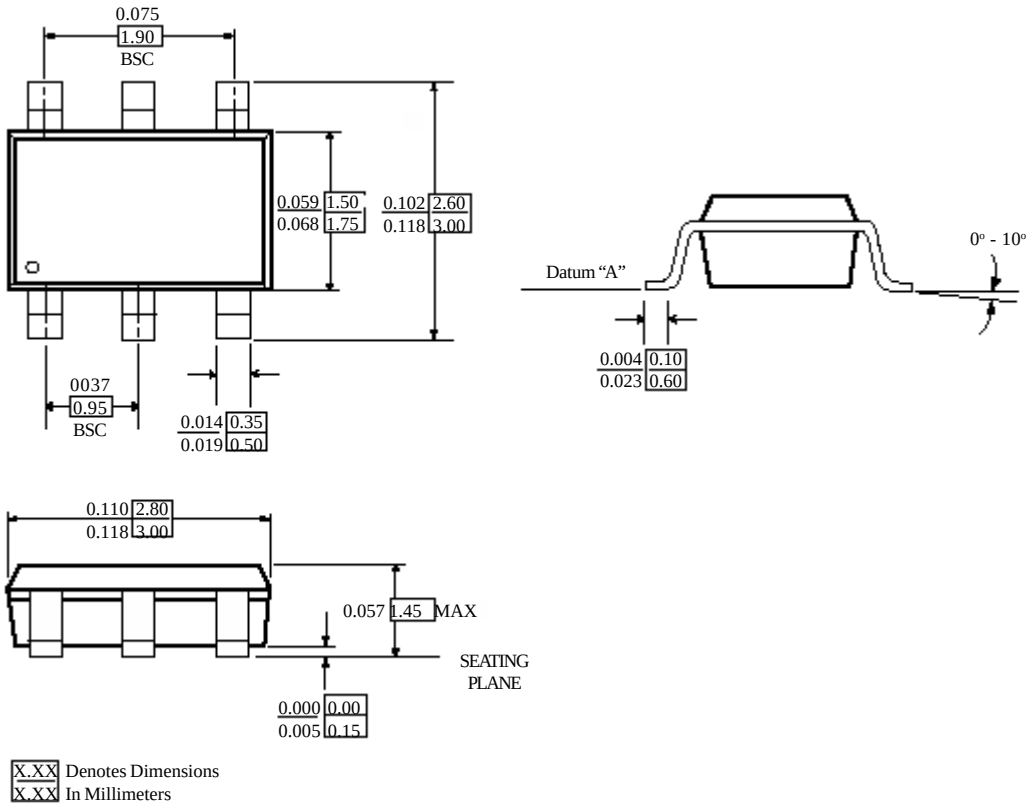
Notes:
1)Controlling dimensions in millimeters
2)Ref: EIAJ SC-74A
3)Foot length is measured at flat portion of foot, reference to Datum A

Figure 6. SOT23-5



Notes:
1)Controlling dimensions in millimeters
2)Ref: EIAJ SC-74A
3)Foot length is measured at flat portion of foot, reference to Datum A

Figure 7. SOT23-6



Notes:
1)Controlling dimensions in millimeters
2)Ref: EIAJ SC-74A
3)Foot length is measured at flat portion of foot, reference to Datum A