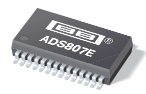
BURR - BROWN®



ADS807

SpeedPlus™ 12-Bit, 53MHz Sampling ANALOG-TO-DIGITAL CONVERTER

FEATURES

- SPURIOUS FREE DYNAMIC RANGE: 82dB at 10MHz f_{IN}
- HIGH SNR: 67.5dB (2Vp-p), 69dB (3Vp-p)
- LOW POWER: 335mW
- INTERNAL OR EXTERNAL REFERENCE
- LOW DNL: 0.5LSB
- FLEXIBLE INPUT RANGE: 2Vp-p to 3Vp-p
- 28-LEAD SSOP PACKAGE

APPLICATIONS

- COMMUNICATIONS IF PROCESSING
- COMMUNICATIONS BASESTATIONS
- TEST EQUIPMENT
- MEDICAL IMAGING
- VIDEO DIGITIZING
- CCD DIGITIZING

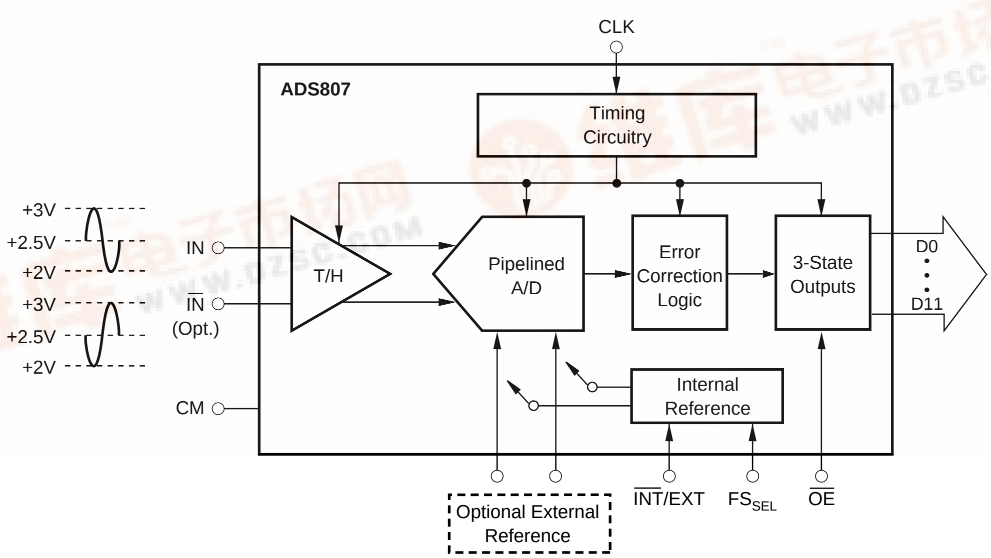
DESCRIPTION

The ADS807 is a high-speed, high dynamic range, 12-bit pipelined analog-to-digital converter. This converter includes a high-bandwidth track-and-hold that gives excellent spurious performance up to and beyond the Nyquist rate. The differential nature of this track-and-hold and A/D circuitry minimizes even-order harmonics and gives excellent common-mode noise immunity. The track-and-hold can also be operated single-ended.

The ADS807 provides for setting the full-scale range of the converter without any external reference circuitry. The internal reference can be disabled allowing low drive, internal references to be used for improved tracking in multichannel systems.

The ADS807 provides an overrange indicator flag to indicate an input signal that exceeds the full-scale input range of the converter. This flag can be used to reduce the gain of front end gain control circuitry. There is also an output enable pin to allow for multiplexing and testability on a PC board.

The ADS807 employs digital error correction techniques to provide excellent differential linearity for demanding imaging applications.



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...111 • Internet: http://www.burr-brown.com/ • Cable: BBRCORP • Telex: 066-6491 • FAX: (520) 889-1510 • Immediate Product Info: (800) 548-6132

SPECIFICATIONS

At T_A = full specified temperature range, V_S = +5V, differential input range = 2V to 3V for each input, sampling rate = 50MHz, unless otherwise noted.

		ADS807E			
PARAMETER	**CONDITIONS**	**MIN**	**TYP**	**MAX**	**UNITS**
RESOLUTION			12 Guaranteed		Bits
Specified Temperature Range	Ambient Air	–40		+85	°C
ANALOG INPUT					
2V Full-Scale Input Range (Differential)	2Vp-p, INT or EXT Ref	2		3	V
2V Full-Scale Input Range (Single-Ended)	2Vp-p, INT or EXT Ref	1.5		3.5	V
3V Full-Scale Input Range (Differential)	3Vp-p, INT or EXT Ref	1.75		3.25	V
3V Full-Scale Input Range (Single-Ended)	3Vp-p, INT or EXT Ref	1		4	V
Analog Input Bias Current			1		µA
Analog Input Bandwidth			270		MHz
Input Impedance			1.25 || 3		MΩ || pF
CONVERSION CHARACTERISTICS					
Sample Rate		10k		53M	Samples/s
Data Latency			6		Clock Cycles
DYNAMIC CHARACTERISTICS					
Differential Linearity Error (largest code error)					
f = 1MHz			±0.5	±1.0	LSB
f = 10MHz	f_S = 40MHz		±0.5	±1.0	LSB
No Missing Codes	f_S = 50MHz, T_A = +25°C		Guaranteed		
No MIssing Codes	f_S = 40MHz, Full Temp		Guaranteed		
Integral Nonlinearity Error, f = 1MHz			±2.0	±4.0	LSBs
Spurious Free Dynamic Range[1]					
f = 1MHz (–1dB input)			83		dBFS[2]
f = 10MHz (–1dB input)		67	82		dBFS
f = 20MHz (–1dB input)			76		dBFS
f = 40MHz (undersampling)			76		dBFS
f = 1MHz to 10MHz, f_S = 40MHz	2Vp-p, Single-Ended Input	62	69		dBFS
Two-Tone Intermodulation Distortion[3]					
f = 12MHz and 13MHz (–7dB each tone)			71		dBc
Signal-to-Noise Ratio (SNR)					
f = 1MHz (–1dB input)		63	68		dB
f = 10MHz (–1dB input)		63	68		dB
f = 20MHz (–dB input)			66		dB
f = 40MHz (undersampling)			67		dB
f = 1MHz to 10MHz, f_S = 40MHz		63	67.5		dB
f = 1MHz to 10MHz, f_S = 40MHz	2Vp-p, Single-Ended Input	60	67		dB
f = 1MHz (–1dB input)	3Vp-p		69		dB
f = 10MHz (–1dB input)	3Vp-p		69		dB
Signal-to-(Noise + Distortion) (SINAD)[4]					
f = 1MHz (–1dBFS input)		61	67		dB
f = 10MHz (–1dBFS input)		61	67		dB
f = 20MHz (–1dBFS input)			67		dB
f = 1MHz to 10MHz, f_S = 40MHz		63	67		dB
f = 1MHz to 10MHz, f_S = 40MHz	2Vp-p, Single-Ended Input	60	64		dB
f = 1MHz (–1dBFS input)	3Vp-p		69		dB
f = 10MHz (–dBFS Input)	3Vp-p		69		dB
Output Noise	Input Grounded		0.2		LSBs rms
Aperture Delay Time			2		ns
Aperture Jitter			1.2		ps rms
Overvoltage Recovery Time			2		ns
DIGITAL INPUTS					
Logic Family			CMOS		
Convert Command	Start Conversion		Rising Edge of Convert Clock		
High Level Input Current[5] (V_{IN} = 5V)				+50	µA
Low Level Input Current (V_{IN} = 0V)				+10	µA
High Level Input Voltage		+2.4			V
Low Level Input Voltage				+1.0	V
Input Capacitance			5		pF

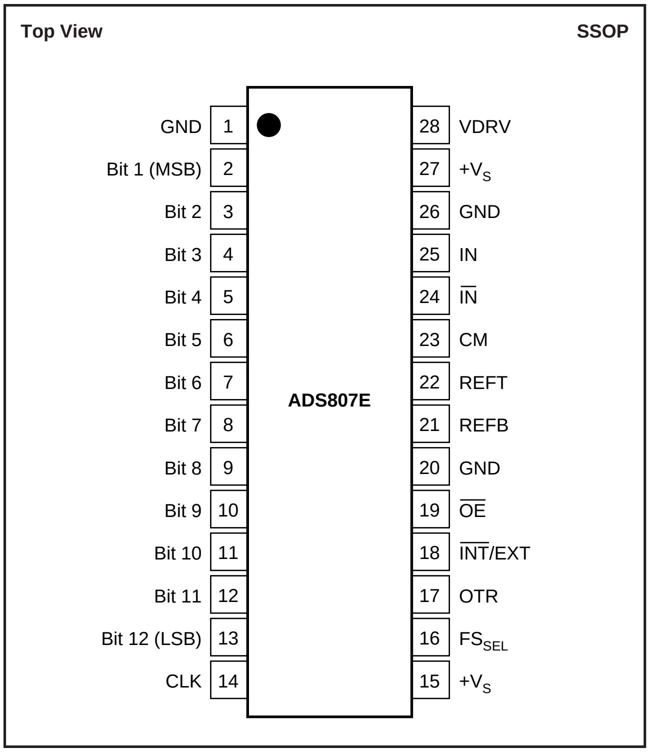
SPECIFICATIONS

At T_A = full specified temperature range, V_S = +5V, differential input range = 2V to 3V for each input, sampling rate = 50MHz, unless otherwise noted.

PARAMETER	CONDITIONS	ADS807E			UNITS
		MIN	TYP	MAX	
DIGITAL OUTPUTS					
Logic Family			CMOS		
Logic Coding			Straight Offset Binary		
Low Output Voltage (I_{OL} = 50µA)	VDRV = 5V			+0.1	V
Low Output Voltage, (I_{OL} = 1.6mA)	VDRV = 5V			+0.2	V
High Output Voltage, (I_{OH} = 50µA)	VDRV = 5V	+4.9			V
High Output Voltage, (I_{OH} = 0.5mA)	VDRV = 5V	+4.8			V
Low Output Voltage, (I_{OL} = 50µA)	VDRV = 3V			+0.1	V
High Output Voltage, (I_{OH} = 50µA)	VDRV = 3V	+2.8			V
3-State Enable Time	$\overline{OE}$ = L(5)		20	40	ns
3-State Disable Time	$\overline{OE}$ = H(5)		2	10	ns
Output Capacitance			5		pF
ACCURACY (Internal Reference, 2Vp-p, Unless Otherwise Noted)					
Zero Error (Referred to –FS)	at 25°C		±1.0	±2.0	%FS
Zero Error Drift (Referred to –FS)			16		ppm/°C
Gain Error(6)	at 25°C		±1.5	±2.5	%FS
Gain Error Drift(6)			66		ppm/°C
Gain Error(7)	at 25°C		±1.0	±1.5	%FS
Gain Error Drift(7)			23		ppm/°C
Power Supply Rejection of Gain	ΔV_S = ±5%	50	70		dB
REFT Tolerance					
2V Full Scale	Deviation From Ideal 3.0V		±10	±65	mV
3V Full Scale	Deviation From Ideal 3.25V		±20	±100	mV
REFB Tolerance					
2V Full Scale	Deviation From Ideal 2.0V		±10	±65	mV
3V Full Scale	Deviation From Ideal 1.75V		±20	±100	mV
External REFT Voltage Range		REFB + 0.4	3	V_S – 1.70	V
External REFB Voltage Range		1.70	2	REFT – 0.4	V
Reference Input Resistance			1		kΩ
POWER SUPPLY REQUIREMENTS					
Supply Voltage: $+V_S$	Operating	+4.75	+5.0	+5.25	V
Supply Current: $+I_S$	Operating		60		mA
Power Dissipation: VDRV = 5V	External Reference		305	360	mW
VDRV = 3V	External Reference		290	350	mW
VDRV = 5V	Internal Reference		350	390	mW
VDRV = 3V	Internal Reference		335	380	mW
Thermal Resistance, θ_{JA}					
28-Lead SSOP			50		°C/W

NOTES: (1) Spurious Free Dynamic Range refers to the magnitude of the largest harmonic. (2) dBFS means dB relative to Full Scale. (3) Two-tone intermodulation distortion is referred to the largest fundamental tone. This number will be 6dB higher if it is referred to the magnitude of the two-tone fundamental envelope. (4) Effective number of bits (ENOB) is defined by as (SINAD – 1.76)/6.02. (5) A 50kΩ pull-down resistor is inserted internally on $\overline{OE}$ pin. (6) Includes internal reference. (7) Excludes internal reference.

PIN CONFIGURATION



PIN DESCRIPTIONS

PIN	DESIGNATOR	DESCRIPTION
1	GND	Ground
2	Bit 1	Data Bit 1 (MSB)
3	Bit 2	Data Bit 2
4	Bit 3	Data Bit 3
5	Bit 4	Data Bit 4
6	Bit 5	Data Bit 5
7	Bit 6	Data Bit 6
8	Bit 7	Data Bit 7
9	Bit 8	Data Bit 8
10	Bit 9	Data Bit 9
11	Bit 10	Data Bit 10
12	Bit 11	Data Bit 11
13	Bit 12	Data Bit 12 (LSB)
14	CLK	Convert Clock
15	$+V_S$	+5V Supply
16	FS_{SEL}	HI = 3V, LO = 2V
17	OTR	Out of Range Indicator
18	$\overline{INT}$/EXT	Reference Select: HIGH or Floating = External LOW = Internal 50kΩ pull up
19	$\overline{OE}$	Output Enable
20	GND	Ground
21	REFB	Bottom Reference/Bypass
22	REFT	Top Reference/Bypass
23	CM	Common-Mode Voltage Output
24	$\overline{IN}$	Complementary Analog Input
25	IN	Analog Input
26	GND	Ground
27	$+V_S$	+5V Supply
28	VDRV	Logic Driver Supply Voltage

ABSOLUTE MAXIMUM RATINGS

$+V_S$	+6V
Analog Input	(–0.3V) to ($+V_S$ + 0.3V)
Logic Input	(–0.3V) to ($+V_S$ + 0.3V)
Case Temperature	+100°C
Junction Temperature	+150°C
Storage Temperature	+150°C

ELECTROSTATIC DISCHARGE SENSITIVITY

This integrated circuit can be damaged by ESD. Burr-Brown recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

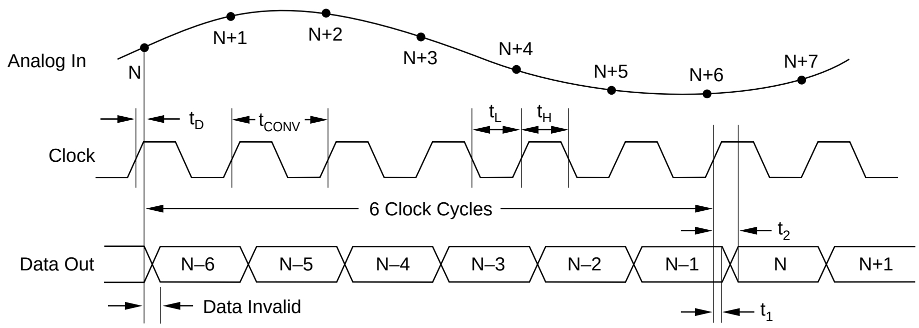
ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

PACKAGE/ORDERING INFORMATION

PRODUCT	PACKAGE	PACKAGE DRAWING NUMBER(1)	SPECIFIED TEMPERATURE RANGE	PACKAGE MARKING	ORDERING NUMBER(2)	TRANSPORT MEDIA
ADS807E	28-Lead SSOP	324	–40°C to +85°C	ADS807E	ADS807E	Tube
"	"	"	"	"	ADS807E/1K	Tape and Reel

NOTES: (1) For detailed drawing and dimension table, please see end of data sheet, or Appendix C of Burr-Brown IC Data Book or download from www.burr-brown.com. (2) Models with a slash (/) are available only in Tape and Reel in the quantities indicated (e.g., /1K indicates 1000 devices per reel). Ordering 1000 pieces of "ADS807E/1K" will get a single 1000-piece Tape and Reel. For detailed Tape and Reel mechanical information, refer to Appendix B of Burr-Brown IC Data Book.

TIMING DIAGRAM



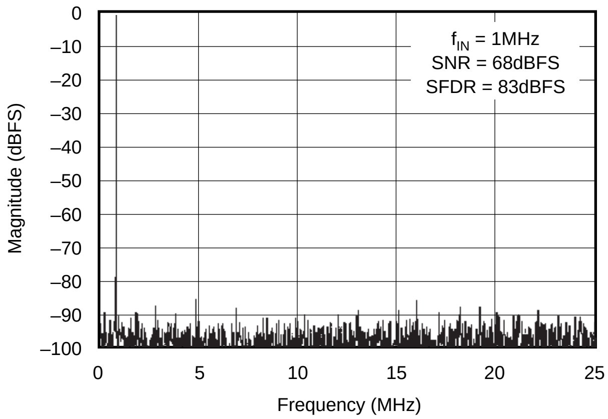
SYMBOL	DESCRIPTION	MIN	TYP	MAX	UNITS
t_{CONV}	Convert Clock Period	18.87		100µs	ns
t_L	Clock Pulse Low	9.4	$t_{CONV}/2$		ns
t_H	Clock Pulse High	9.4	$t_{CONV}/2$		ns
t_D	Aperture Delay		2		ns
t_1 (1)	Data Hold Time, C_L = 0pF	2.7			ns
t_2 (1)	New Data Delay Time, C_L = 15pF max			12	ns

NOTE: (1) t_1 and t_2 times are valid for VDRV voltages of +2.7V to +5V.

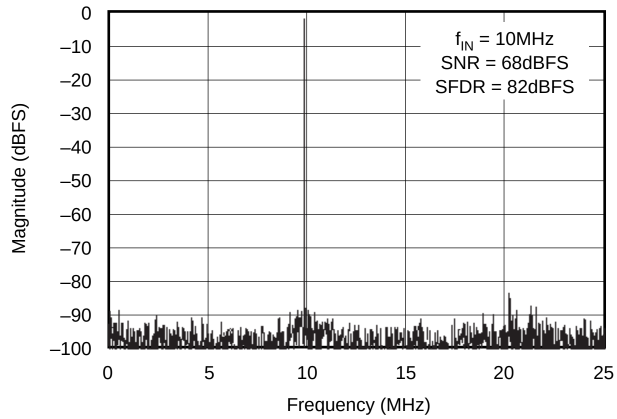
TYPICAL PERFORMANCE CURVES

At T_A = full specified temperature range, differential input range = 2V to 3V, sampling rate = 50MHz, and internal reference, unless otherwise noted.

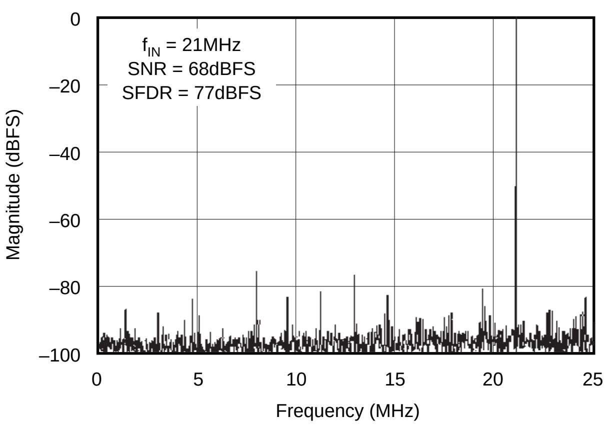
SPECTRAL PERFORMANCE



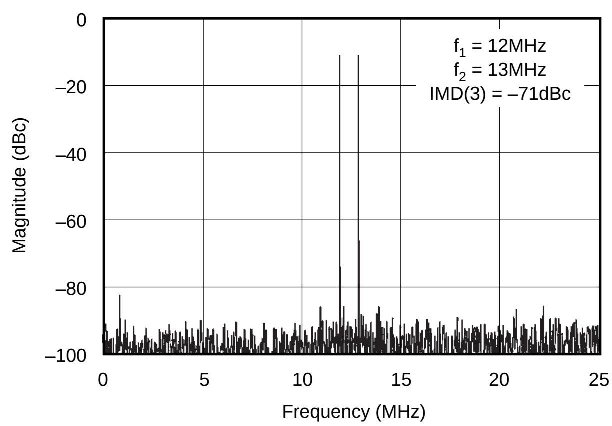
SPECTRAL PERFORMANCE



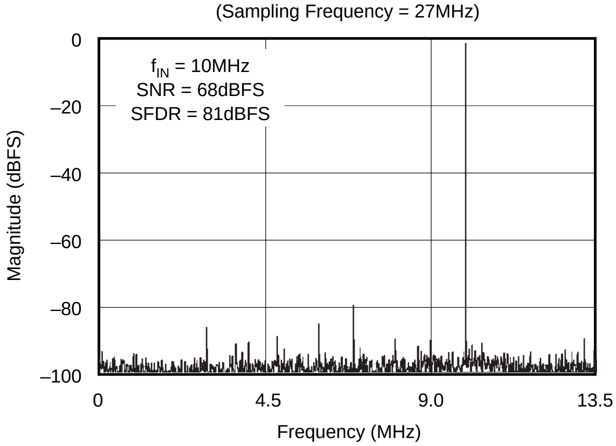
SPECTRAL PERFORMANCE



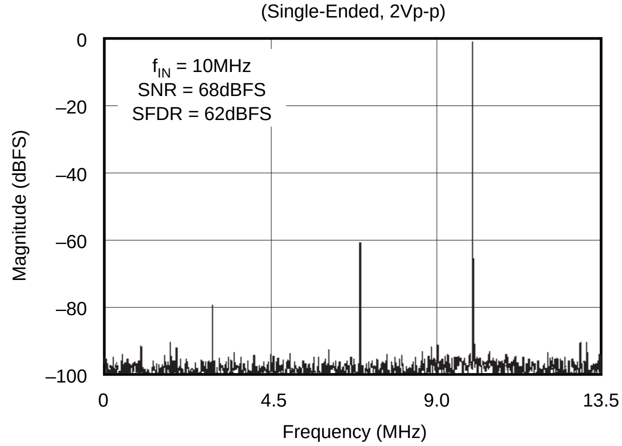
TWO-TONE INTERMODULATION DISTORTION



SPECTRAL PERFORMANCE
(Sampling Frequency = 27MHz)

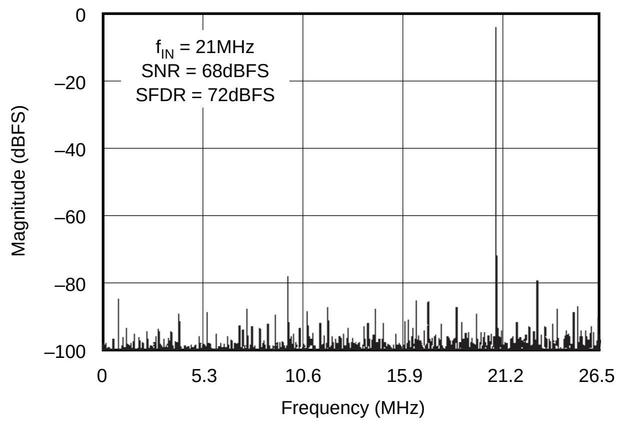


SPECTRAL PERFORMANCE
(Single-Ended, 2Vp-p)

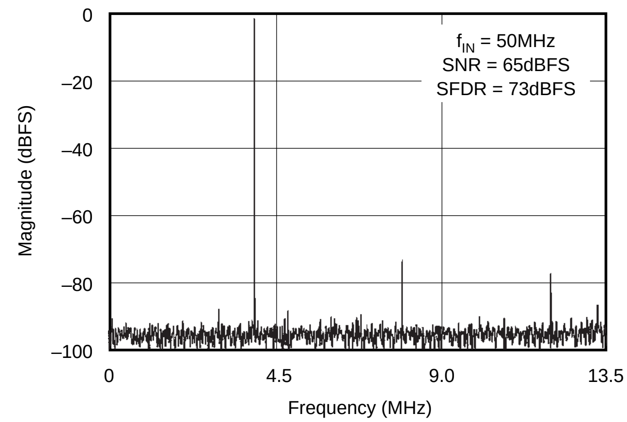


TYPICAL PERFORMANCE CURVES (CONT)

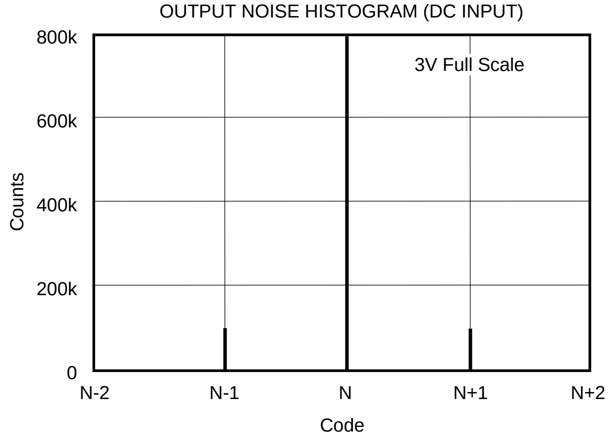
At T_A = full specified temperature range, differential input range = 2V to 3V, sampling rate = 50MHz, and internal reference, unless otherwise noted.



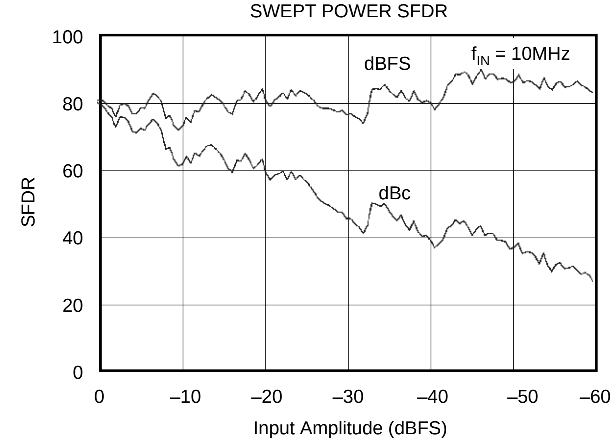
SPECTRAL PERFORMANCE
(Sampling Frequency = 53MHz)



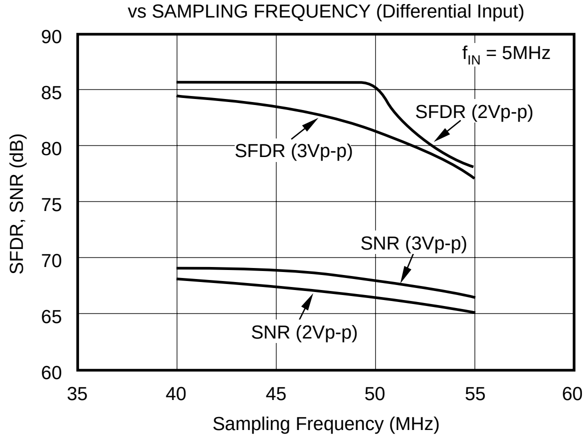
UNDERSAMPLING
(Sampling Frequency = 27MHz)



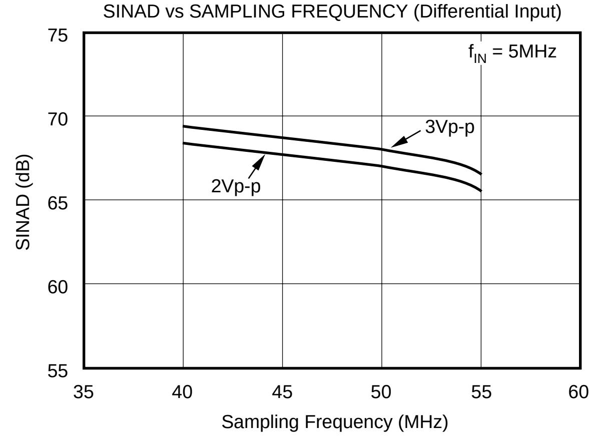
OUTPUT NOISE HISTOGRAM (DC INPUT)



SWEPT POWER SFDR



DYNAMIC PERFORMANCE
vs SAMPLING FREQUENCY (Differential Input)

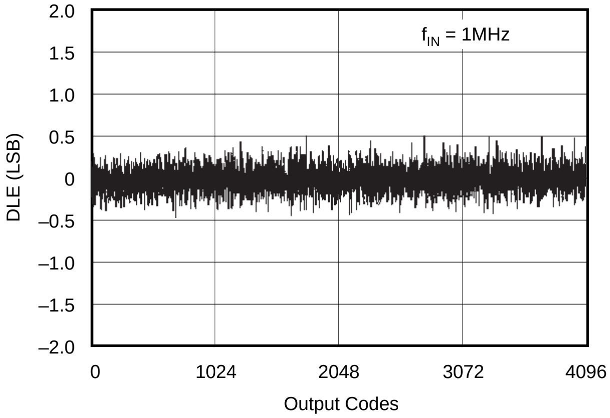


SINAD vs SAMPLING FREQUENCY (Differential Input)

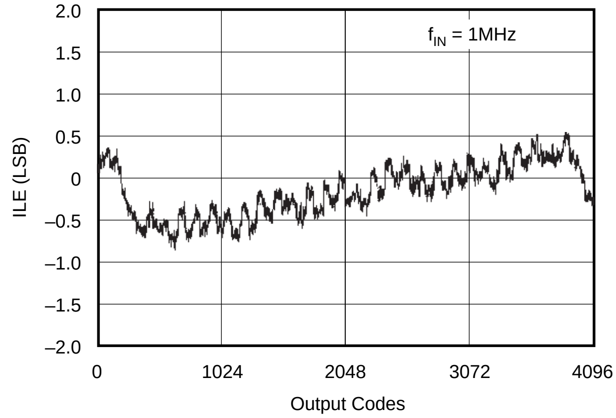
TYPICAL PERFORMANCE CURVES (CONT)

At T_A = full specified temperature range, differential input range = 2V to 3V, sampling rate = 50MHz, and internal reference, unless otherwise noted.

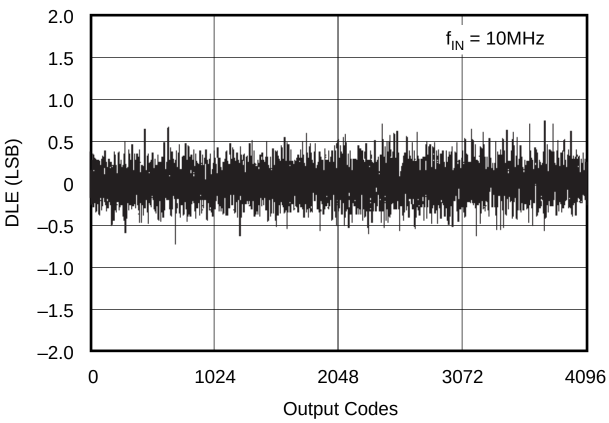
DIFFERENTIAL LINEARITY ERROR



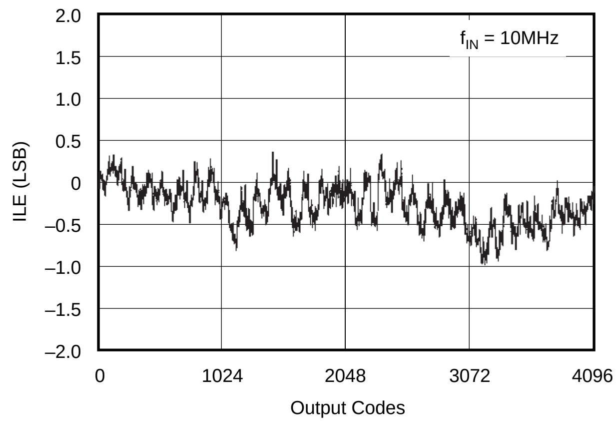
INTEGRAL LINEARITY ERROR



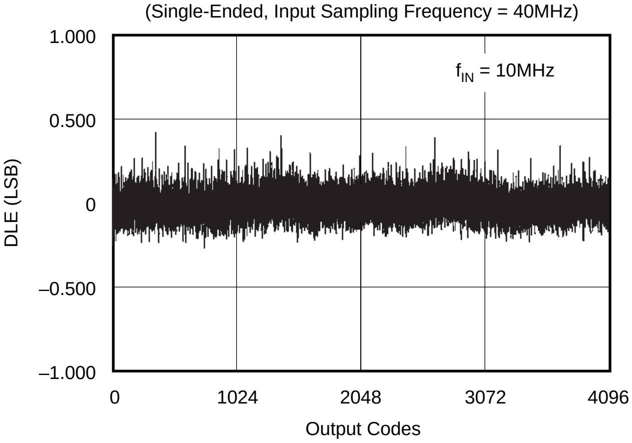
DIFFERENTIAL LINEARITY ERROR



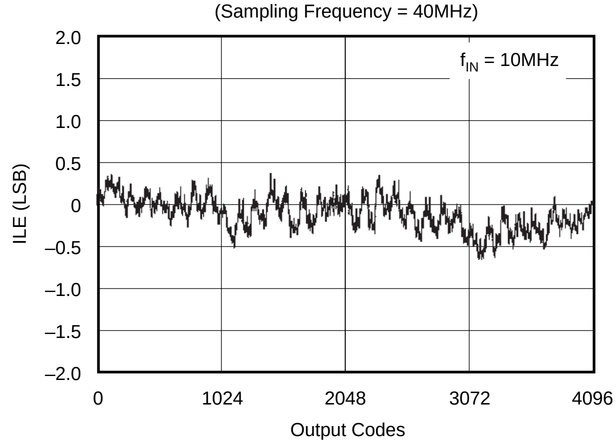
INTEGRAL LINEARITY ERROR



DIFFERENTIAL LINEARITY ERROR
(Single-Ended, Input Sampling Frequency = 40MHz)



INTEGRAL LINEARITY ERROR
(Sampling Frequency = 40MHz)



APPLICATION INFORMATION

THEORY OF OPERATION

The ADS807 is a high-speed CMOS A/D converter which employs a pipelined converter architecture consisting of 12 internal stages. Each stage feeds its data into the digital error correction logic ensuring excellent differential linearity and no missing codes at the 12-bit level. The output data becomes valid after the rising clock edge (see Timing Diagram). The pipeline architecture results in a data latency of 6 clock cycles.

The analog input of the ADS807 consists of a differential track-and-hold circuit. The differential topology along with tightly matched poly-poly capacitors produce a high level of AC performance at high sampling rates and in undersampling applications.

Both inputs (IN, $\overline{IN}$) require external biasing using a common-mode voltage that is typically at the mid-supply level ($+V_S/2$).

DRIVING THE ANALOG INPUTS

The analog inputs of the ADS807 are a very high impedance. They should be driven through an R-C network designed to pass the highest frequency of interest. This prevents high frequency noise in the input from affecting SFDR and SNR. The ADS807 can be used in a wide variety of applications and deciding on the best performing analog interface circuit depends on the type of application. The circuit definition should include considerations of input frequency spectrum and amplitude, single-ended or differential drive and available power supplies. For example, communication (frequency domain) applications process frequency bands not including DC. In imaging (time domain) applications, the input DC component must be maintained into the A/D converter. Features of the ADS807, including full-scale select (FS_{SEL}), external reference, and CM output provide flexibility to accommodate a wide range of applications. The ADS807 should be configured to meet application objectives while observing the headroom requirements of the driving amplifiers to yield the best overall performance.

The ADS807 input structure allows it to be driven either single-ended or differentially. Differential operation of the ADS807 requires an in-phase input signal and a 180° out-of-phase part simultaneously applied to the inputs (IN, $\overline{IN}$). The differential operation offers a number of advantages which, in most applications, will be instrumental in achieving the best dynamic performance of the ADS807:

- the signal swing is half of that required for the single-ended operation and therefore, is less demanding to achieve while maintaining good linearity performance from the signal source
- the reduced signal swing allows for more headroom in the interface circuitry and therefore, a wider selection of the best suitable driver op amp
- even-order harmonics are minimized
- improves the noise immunity based on the converter's common-mode input rejection

Using the single-ended mode, the signal is applied to one of the inputs, while the other input is biased with a DC voltage to the required common-mode level. Both inputs are equal in terms of their impedance and performance, except that applying the signal to the complementary input ($\overline{IN}$) instead of the IN input will invert the input signal relative to the output code. For example, in case the input driver operates in inverting mode, using $\overline{IN}$ as the signal input will restore the phase of the signal to its original orientation. Time-domain applications may benefit from a single-ended interface configuration and its reduced circuit complexity. While maintaining good signal-to-noise ratio (SNR), driving the ADS807 with a single-ended signal will result in a reduction of the distortion performance. Employing dual supply amplifiers and AC-coupling will usually yield the best results, while DC-coupling and/or single-supply amplifiers impose additional design constraints due to their headroom requirements, especially when selecting the 3Vp-p input range. However, single-supply amplifiers have the advantage of inherently limiting their output swing to within the supply rails. Alternatively, a voltage limiting amplifier, like the OPA688, may be considered to set fixed-signal limits and avoid any severe overrange condition for the A/D converter.

The full-scale input range of the ADS807 is defined by the reference voltages. For example, setting the range select pin to FS_{SEL} = LOW, and using the internal references (REFT = +3.0V and REFTB = +2.0V), the full-scale range is defined to: FSR = 2 • (REFT – REFB) = 2Vp-p.

The trade-off of the differential input configuration versus the single-ended is its higher complexity. In either case, the selection of the driver amplifier should be such that the amplifier's performance will not degrade the A/D's performance. The ADS807 operates on a single power supply, which requires a level shift to a ground-based bipolar input signals to comply with its input voltage range requirements.

The input of the ADS807 is of a capacitive nature and the driving source needs to provide the current to charge or discharge the input sampling capacitor while the track-and-hold is in track mode. This effectively results in a dynamic input impedance which depends on the sampling frequency. It most applications, it is recommended to add a series resistor, typically 20Ω to 50Ω, between the drive source and the converter inputs. This will isolate the capacitive input from the source, which can be crucial to avoid gain peaking when using wideband operational amplifiers. Secondly, it will create a first-order, low-pass filter in conjunction with the specified input capacitance of the ADS807. Its cut-off frequency can be adjusted even further by adding an external shunt capacitor from each signal input to ground. The optimum values of this R-C network depend on a variety of factors which include the ADS807 sampling rate, the selected op amp, the interface configuration and the particular application (time domain versus frequency domain). Generally, increasing the size of the series resistor and/or capacitor will improve the SNR performance, but depending on the signal source, large resistor values may be detrimental to achieving good harmonic distortion. In any case, optimizing the R-C values for the specific application is encouraged.

Transformer Coupled, Single-Ended to Differential Configuration

If the application requires a signal conversion from a single-ended source to drive the ADS807 differentially, an RF transformer might be a good solution. The selected transformer must have a center tap in order to apply the common-mode DC voltage necessary to bias the converter inputs. AC grounding the center tap will generate the differential signal swing across the secondary winding. Consider a step-up transformer to take advantage of a signal amplification without the introduction of another noise source. Furthermore, the reduced signal swing from the source may lead to improved distortion performance.

The differential input configuration provides a noticeable advantage of achieving good SFDR over a wide range of input frequencies. In this mode, both inputs of the ADS807 see matched impedances. Figure 1 shows the schematic for the suggested transformer coupled interface circuit. The component values of the R-C low-pass may be optimized depending on the desired roll-off frequency. The resistor across the secondary side (R_T) should be calculated using the equation $R_T = n^2 \times R_G$ to match the source impedance (R_G) for good power transfer and VSWR.

The circuit example of Figure 1 shows the voltage feedback amplifier OPA680 driving the RF transformer, which converts the single-ended signal into a differential. The OPA680 can be employed for either single or dual supply operation. For details on how to optimize its frequency response, refer to the OPA680 data sheet. With the 49.9Ω series output resistor, the amplifier emulates a 50Ω source (R_G). Any DC content of the signal can be easily blocked by a capacitor (0.1µF) and to also to avoid DC loading of the op amp's output stage.

AC-Coupled, Single-Ended to Differential Interface with Dual-Supply Op Amps

Communications applications, in particular, demand a very high dynamic range and low levels of intermodulation distortion but, usually allow the input signal to be AC-coupled into the A/D converter. Appropriate driver amplifiers need to be selected to maintain the excellent distortion performance of the ADS807. Often, these op amps deliver the lowest distortion with a small, ground centered signal swing that requires dual power supplies. Because of the AC-coupling, this requirement can be easily accomplished and the needed level shifting of the input signal can be implemented without affecting the driver circuit.

Figure 2 shows an example of such an interface circuit specifically designed to maximize the dynamic performance. The voltage feedback amplifier, OPA642, maintains an excellent distortion performance for input frequencies of up to 15MHz. The two amplifiers (A1, A2) are configured as an inverting and noninverting gain stage to convert the input signal from single-ended to differential. The nominal gain for this stage is set to +2V/V. The outputs of the OPA642s are AC-coupled to the converter's differential inputs. This will keep the distortion performance at its best since the signal range stays within the linear region of the op amp and sufficient headroom to the supply rails can be maintained. Four resistors located between the top (REFT) and bottom (REFB) reference shift the input signal to a common-mode voltage of approximately +2.5V.

The interface circuit of Figure 2 can be modified to extend the bandwidth to approximately 25MHz by replacing the OPA642 with its decompensated version, the OPA643. The OPA643 provides the necessary slew rate for a low distortion front end to the ADS807. With a minimum gain stability of +3, the gain resistors have to be modified, as well as optimizing the series resistor and shunt capacitance at each of the converter inputs.

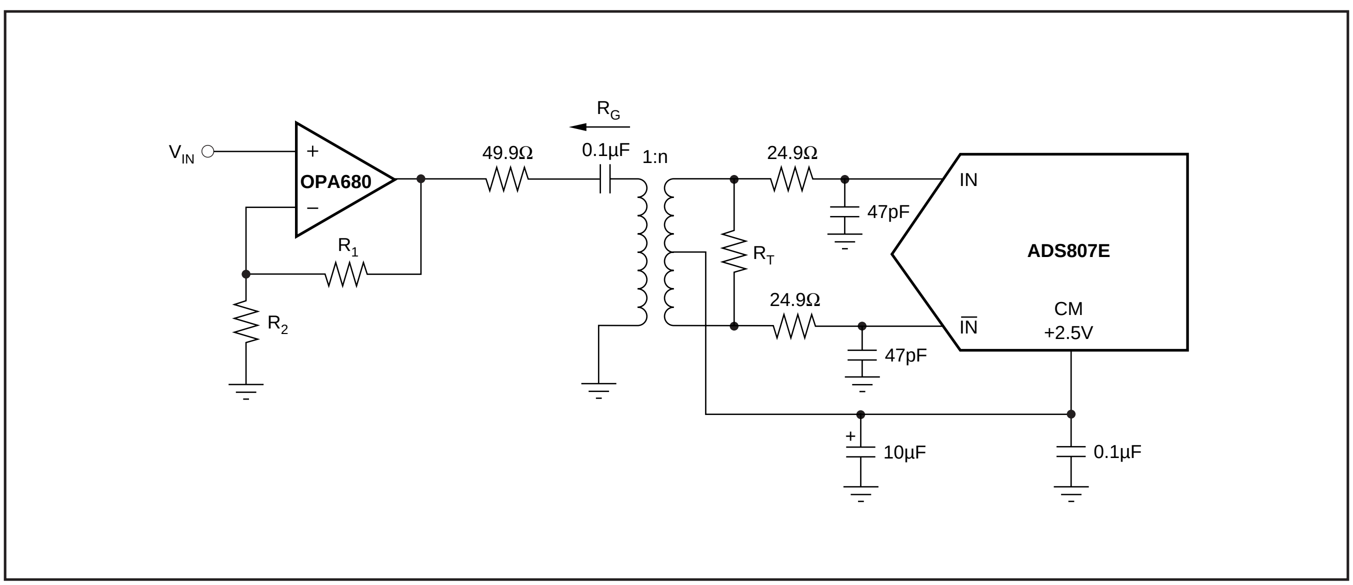


FIGURE 1. Converting a Single-Ended Input Signal into a Differential Signal Using a RF-Transformer.

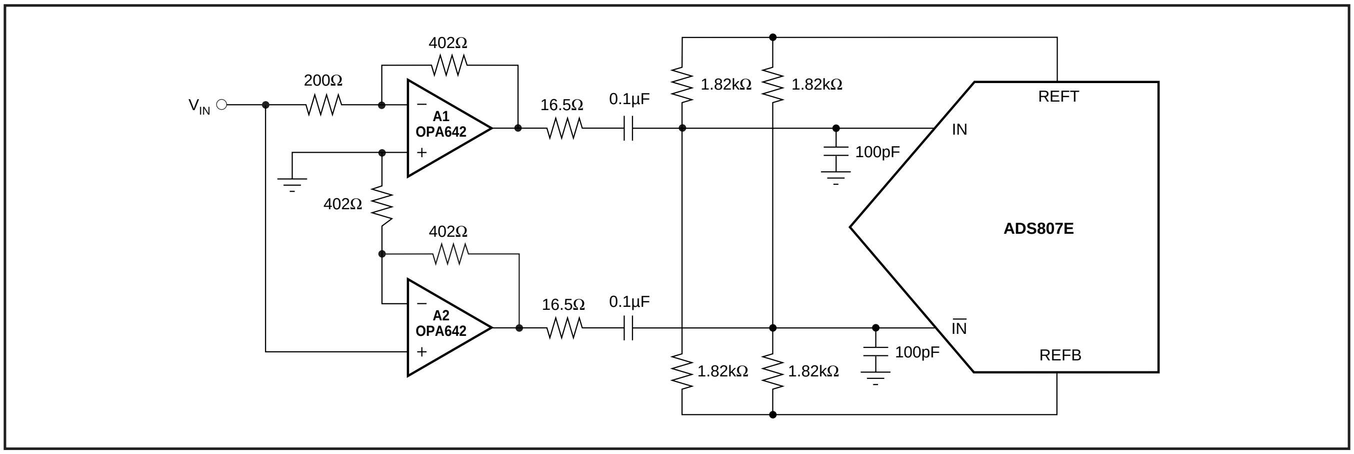


FIGURE 2. AC-Coupled Differential Driver Interface with OPA642.

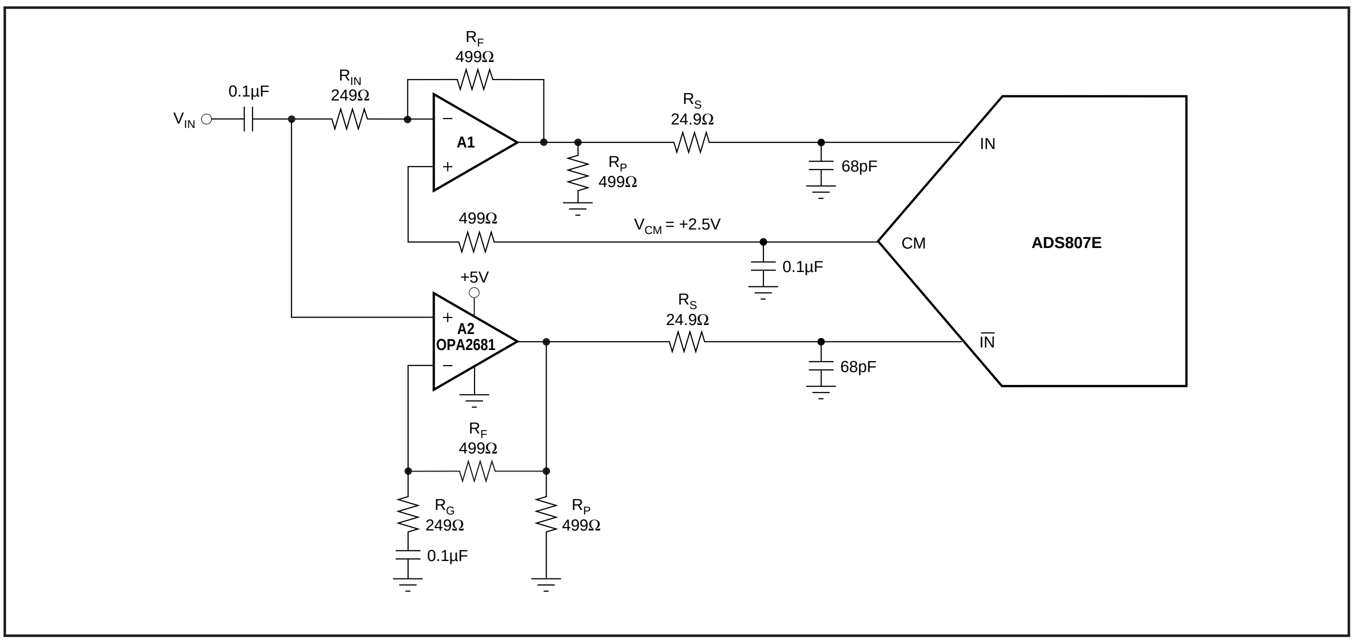


FIGURE 3. AC-Coupled, Differential Interface for Single-Supply Operation.

AC-Coupled, Single-Ended-to-Differential Interface for Single-Supply Operation

The previously discussed interface circuit can be modified if the system only allows for a single supply operation, e.g., V_S = +5V. Single-supply operation requires the driver amplifier to be biased as well in order to process a bipolar input signal. Typically, single-supply amplifiers do not achieve distortion performance as well as dual-supply op amps. The driver amplifier's output swing must exceed the full-scale input range of the converter. In addition, dual op amps, such as the current-feedback OPA2681, should be considered since they provide the closest open-loop gain and phase matching between the two channels. Shown in Figure 3 is a single-supply interface circuit for an AC-coupled input signal. With the ADS807 set to the 2Vp-p input range, the top and bottom references (REFT, REFB) provide an output voltage of +3.0V and +2.0V, respectively. The CM output of the ADS807 is used to bias the inputs of the driving amplifiers. Using the OPA2681 on a single +5V supply, its ideal [illegible] is +2.5V, which coincides with the recommended common-mode input level for the ADS807, thus obviating the need for coupling capacitors between the amplifiers and the converter.

The addition of a small series resistor (R_S) between the output of the op amps and the input of the ADS807 will be beneficial in almost all interface configurations. It will decouple the op amp's output from the capacitive load and avoid gain peaking, which can result in increased noise. For best spurious and distortion performance, the resistor value should be kept below 100Ω. Furthermore, the series resistor in combination with the shunt capacitor, establishes a passive low-pass filter limiting the bandwidth for the wideband noise thus improving the SNR. The spurious free dynamic range of this single-supply front end is limited by the 2nd harmonic distortion. An improvement of several dB may be realized by adding a pull-down resistor (R_P) at the output of each amplifier. This pulls a DC bias current out of the output stage of the amplifier. It is set to approximately 5mA in the shown example, but will vary depending on the amplifier used.

Single-Ended, AC-Coupled, Dual Supply Interface

The circuit provided in Figure 4 shows typical connections for using the ADS807 in a single-ended input configuration. The bias requirements for AC-coupling are provided by a single resistor to the CM output lead. The single-ended mode of operation should be considered for ease of interface complexity and applications where the dynamic performance can be compromised. The series resistor R_S, along with the shunt capacitance, provide the means to adjust the bandwidth and optimize the performance towards good signal-to-noise ratio. In addition, the amplifier configuration can be easily modified for an anti-aliasing filter based on a second-order Sallen-Key or Multiple-Feedback topology.

The interface example shown in Figure 4 operates with the full-scale range of the ADS807 set to 2Vp-p, leaving sufficient headroom for the output of the OPA642 to drive the converter and maintain low signal distortion.

DC-Coupled, Differential Driver with Level Shift

Several applications will require that the bandwidth of the signal path include DC, in which case, the signal has to be DC-coupled to the A/D converter. An op amp based interface circuit can be configured to scale and level shift the input signal to be compatible with the selected input range of the A/D converter. The circuit shown in Figure 5 employs a dual op amp, OPA2681, to drive the input of the ADS807 differentially. The single-supply, general purpose op amp OPA234 is added to buffer the common-mode voltage of +2.5V, available at the CM pin, and apply it to the input of the driver amplifier. This sets the correct DC voltage to bias the inputs of the ADS807. It should be noted that any DC voltage differences between the IN and $\overline{\text{IN}}$ inputs of the ADS807 will result in an offset error.

Using the OPA2681, this circuit can be operated either with a single or a dual ±5V supply.

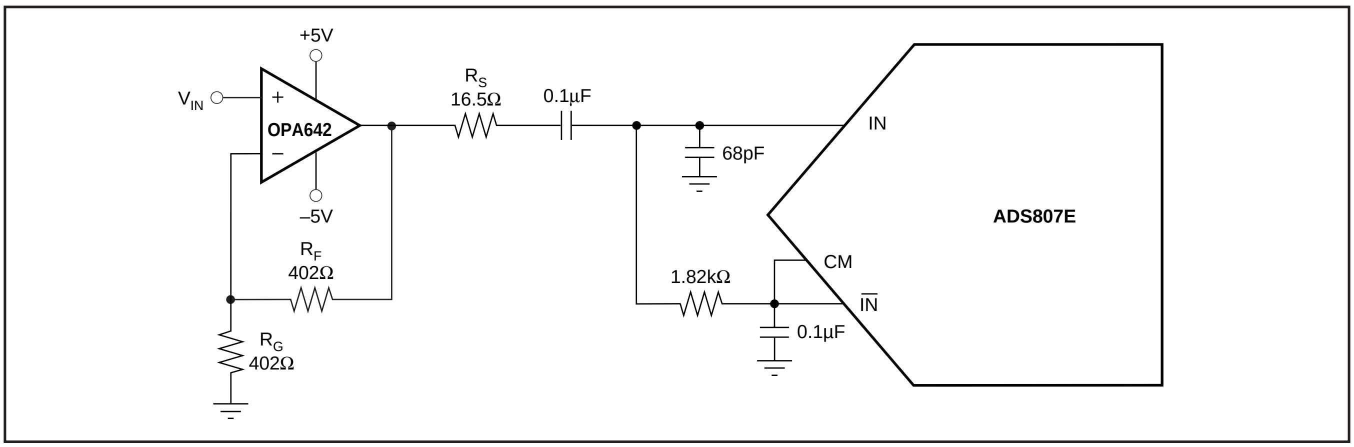
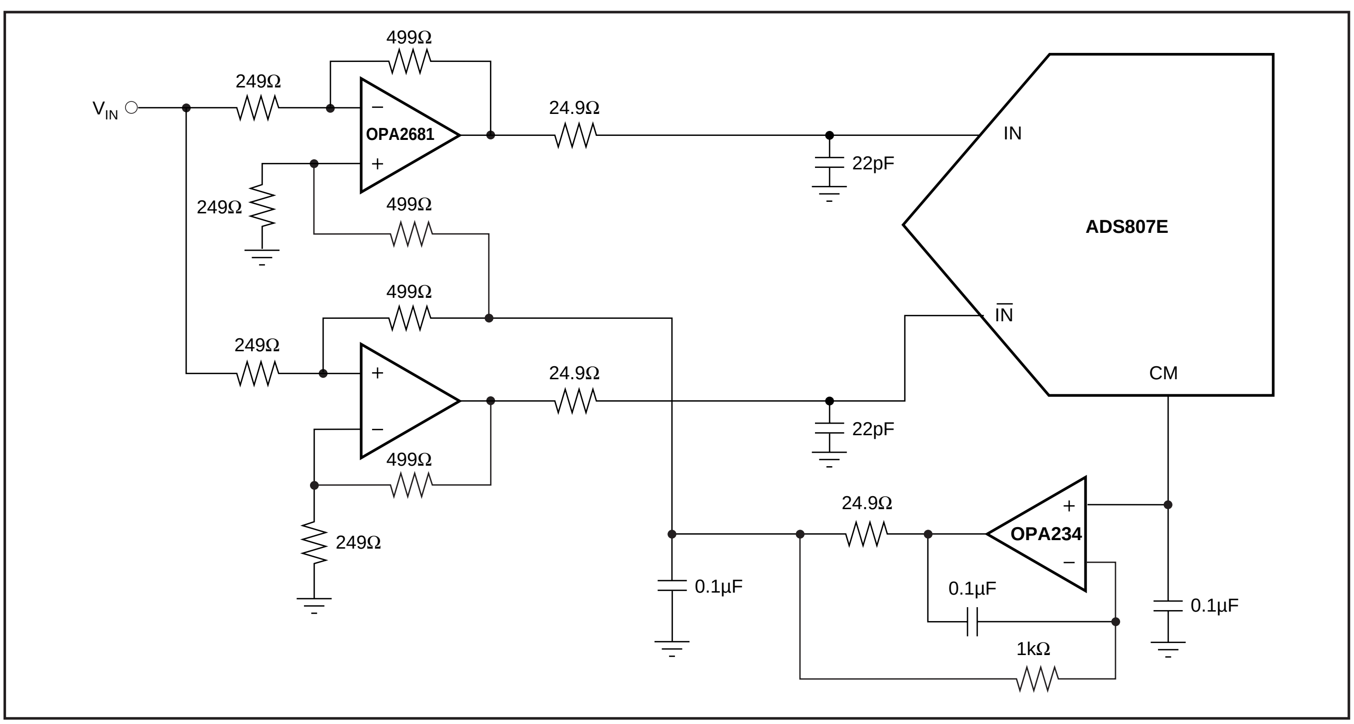


FIGURE 4. AC-Coupling the Dual Supply Amplifier OPA642 to the ADS807 for a 2Vp-p Full-Scale Input Range.



FI t Driver with Level Shifting.

REFERENCE OPERATION

The internal reference consists of a bandgap voltage reference, the drivers for the top and bottom reference, and the resistive reference ladder. The bandgap reference circuit includes logic functions that allow setting the analog input swing of the ADS807 to a differential full-scale range of either 2Vp-p or 3Vp-p by simply tying the FS_{SEL} pin to a LOW or HIGH potential, respectively. While operating the ADS807 in the external reference mode, the buffer amplifiers for the REFT and REFB are disabled. The ADS807 has an internal 50kΩ pull-down resistor at the range select pin (RSEL). Therefore, this pin can be either hardwired to ground or left unconnected, which will default the converter to a 2Vp-p full-scale input range (FSR). While set for the 2Vp-p range, the top and bottom reference voltages will be REFT = +3.0V and REFB = +2.0V. Switching to the 3Vp-p range changes those voltages to REFT = +3.25V and REFB = +1.75V. The reference buffers can be utilized to supply up to 1mA (sink and source) to external circuitry. To ensure proper operation with any reference configuration, it is necessary to provide solid bypassing at all reference pins in order to keep the clock feedthrough to a minimum, see Figure 6. Good performance requires using 0.1µF low inductance capacitors. All bypassing capacitors should be located as close to their respective pins as possible.

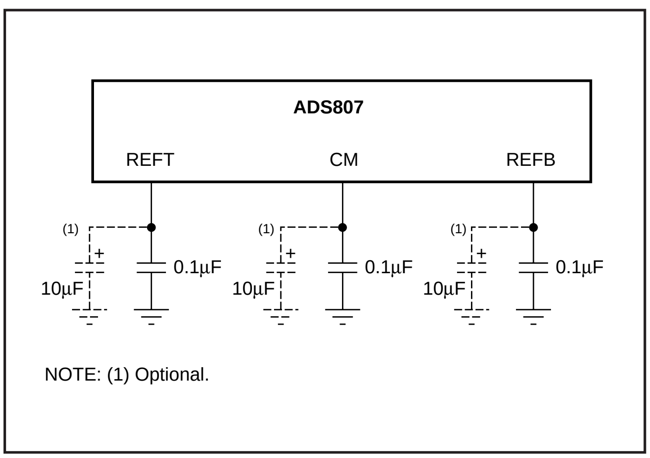


FIGURE 6. Recommended Bypassing for the Reference Pins.

USING EXTERNAL REFERENCES

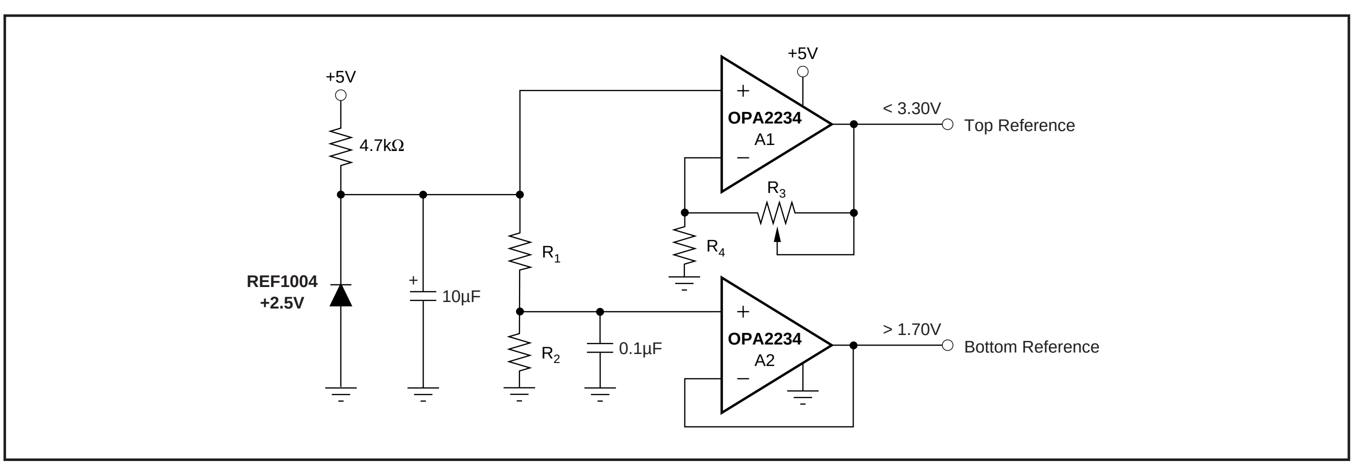
For even more design flexibility, the internal reference can be disabled and an external reference voltage used. The utilization of an external reference may be considered for applications requiring higher accuracy, improved temperature performance, or a wide adjustment range of the converter's full-scale range. In multichannel applications, the use of a common external reference has the benefit of obtaining better matching and drift of the full-scale range between converters. Figure 7 gives an example of an external reference circuit using a single-supply, low power, dual op amp (OPA2234).

The external references can vary as long as the value of the external top reference (REFT EXT) stays within the range of V_S – 1.70V and REFB + 0.4V, and the external bottom reference (REFB EXT) stays within 1.70V and REFT – 0.4V. Note that the function of the range selector pin (FS_{SEL}) is disabled while the converter operates in external reference mode. Setting the ADS807 for external reference mode requires the $\overline{INT}$/EXT pin (pin 18) to be HIGH.

The logic level applied to the $\overline{INT}$/EXT pin of the ADS807 determines if the converter operates with either the built-in reference or external reference voltages. Because this function pin has an internal 50kΩ pull-up resistor, the default configuration is external reference mode. Grounding this pin will activate the internal reference option.

The input track and hold amplifier is differential. A positive 1Vp-p on the $\overline{IN}$ and its compliment, a negative 1Vp-p, on the IN (as shown in Figure 3) results in 2Vp-p on the output of the T/H. Likewise, 2Vp-p on the IN and 0Vp-p on the $\overline{IN}$ (as shown in Figure 4) results in 2Vp-p on the output of the T/H. Therefore, the reference voltages, REFT and REFB, are the same for both differential and single-ended inputs. See Table I.

The external references may be changed for different tasks. The ADS807 will follow the external references with a latency of 8 to 10 clock cycles. If it is desired to use $\overline{INT}$/EXT and FS_{SEL} to change the configuration of a circuit for different tasks, a large amount of time must be allowed. This time could be hundreds of microseconds. Refer to the Diagram on the front page. Note that there is no disconnect for external references. If it is desired to switch between internal and external references, disconnect switches must be added between the external references and the ADS807.



for an External Reference Driver Using the Dual, Single-Supply Op Amp, OPA2234.

INPUT	REFERENCE	IN (Pin-25)	$\overline{IN}$ (Pin-24)	REFT	REFB
2Vp-p Differential 1Vp-p Times 2 Inputs	Internal or External	2V to 3V	3V to 2V	+3V	+2V
2Vp-p Single-Ended 2Vp-p Times 1 Input	Internal or External	1.5V to 3.5V	$2.5V_{DC}$	+3V	+2V
3Vp-p Differential 1.5Vp-p Times 2 Inputs	Internal or External	1.75V to 3.35V	3.25V to 1.75V	+3.25V	+1.75V
3Vp-p Single-Ended 3Vp-p Times 1 Input	Internal or External	1V to 4V	$2.5V_{DC}$	+3.25V	+1.75V

TABLE I. Reference Voltages for Input Signal Ranges.

DIGITAL INPUTS AND OUTPUTS

Clock Input Requirements

Clock jitter is critical to the SNR performance of high speed, high resolution A/D converters. Clock jitter leads to aperture jitter (t_A), which adds noise to the signal being converted. The ADS807 samples the input signal on the rising edge of the CLK input. Therefore, this edge should have the lowest possible jitter. The jitter noise contribution to total SNR is given by the following equation. If this value is near your system requirements, input clock jitter must be reduced.

$$Jitter\ SNR = 20 \log \frac{1}{2\pi f_{IN}\ t_A}\ rms\ signal\ to\ rms\ noise$$

where: f_{IN} is input signal frequency
t_A is rms clock jitter

Particularly in undersampling applications, special consideration should be given to clock jitter. The clock input should be treated as an analog input in order to achieve the highest level of performance. Any overshoot or undershoot of the clock signal may cause degradation of the performance. When digitizing at high sampling rates, the clock should have 50% duty cycle ($t_H = t_L$), along with fast rise and fall times of 2ns or less.

Over Range Indicator (OTR)

If the analog input voltage exceeds the set full-scale range, an over range condition exists. The 'OTR' pin of the ADS807 can be used to monitor any such out-of-range condition. This 'OTR' output is updated along with the data output corresponding to the particular sampled analog input voltage. Therefore, the OTR data is subject to the same pipeline delay as the digital data. The OTR output is LOW when the input voltage is within the defined input range. It will go to HIGH if the applied signal exceeds the full-scale range.

Data Outputs

The output data format of the ADS807 is in positive Straight Offset Binary code, see Table II and Table II. This format can easily be converted into the Two's Binary Complement code by inverting the MSB.

It is recommended that the capacitive loading on the data lines be as low as possible (< 15pF). Higher capacitive loading will cause larger dynamic currents as the digital outputs are changing. Those high current surges can feed back to the analog portion of the ADS807 and affect the performance. If necessary, external buffers or latches close to the converter's output pins may be used to minimize the capacitive loading. They also provide the added benefit of isolating the ADS807 from high frequency digital noise on the bus coupling back into the converter.

SINGLE-ENDED INPUT ($\overline{IN}$ = CM, Pin-23)	STRAIGHT OFFSET BINARY (SOB)
+FS–1LSB (IN = CMV + FSR/2)	1111 1111 1111
+1/2 FS	1100 0000 0000
Bipolar Zero (IN = V_{CM})	1000 0000 0000
–1/2 FS	0100 0000 0000
–FS (IN = CMV – FSR/2)	0000 0000 0000

TABLE II. Coding Table for Single-Ended Input Configuration with $\overline{IN}$ Tied to the Common-Mode Voltage.

DIFFERENTIAL INPUT	STRAIGHT OFFSET BINARY (SOB)
+FS-1LSB (IN = +3V, $\overline{IN}$ = +2V)	1111 1111 1111
+1/2 FS	1100 0000 0000
Bipolar Zero (IN = $\overline{IN}$ = V_{CM})	1000 0000 0000
–1/2 FS	0100 0000 0000
–FS (IN = +2V, $\overline{IN}$ = +3V)	0000 0000 0000

TABLE III. Coding Table for Single-Ended Input Configuration with $\overline{IN}$ Tied to the Common-Mode Voltage.

Digital Output Driver Supply (VDRV)

The ADS807 features a dedicated supply pin for the output logic drivers, VDRV, which is not internally connected to the other supply pins. Setting the voltage at VDRV to +5V or +3V, the ADS807 produces corresponding logic levels and can directly interface to the selected logic family. The output stages are designed to supply sufficient current to drive a variety of logic families. However, it is recommended to use the ADS807 with +3V logic supply. This will lower the power dissipation in the output stages due to the lower output swing and reduce current glitches on the supply line which may affect the AC performance of the converter. In some applications, it might be advantageous to decouple the VDRV pin with additional capacitors or a pi-filter.

GROUNDING AND DECOUPLING

Proper grounding, bypassing, short trace lengths, and the use of power and ground planes are particularly important for high frequency designs. Multilayer PC boards are recommended for best performance since they offer distinct advantages such as minimizing ground impedance, separation of signal layers by ground layers, etc. The ADS807 should be treated as an analog component. Whenever possible, the supply pins should be powered by the analog supply. This will ensure the most consistent results, since digital supply lines often carry high levels of noise which otherwise would be coupled into the converter and degrade the achievable performance. All ground connections on the ADS807 are internally joined together obviating the design of split ground planes. The ground pins (1, 20, 26) should directly connect to an analog ground plane which covers the PC board area under the converter. While designing the layout it is important to keep the analog signal traces separated from any digital lines to prevent noise coupling onto the analog signal path. Because of the its high sampling rate, the ADS807 generates high frequency current transients and noise (clock feedthrough) that are fed back into the supply and reference lines. This requires that all supply and reference pins are sufficiently bypassed. Figure 8 shows the recommended decoupling scheme for the ADS807. In most cases, 0.1µF ceramic chip capacitors at each pin are adequate to keep the impedance low over a wide frequency range. Their effectiveness largely depends on the proximity to the individual supply pin. Therefore, they should be located as close to the supply pins as possible. If system supplies are not a low enough impedance, adding a small tantalum capacitor will yield the best results.

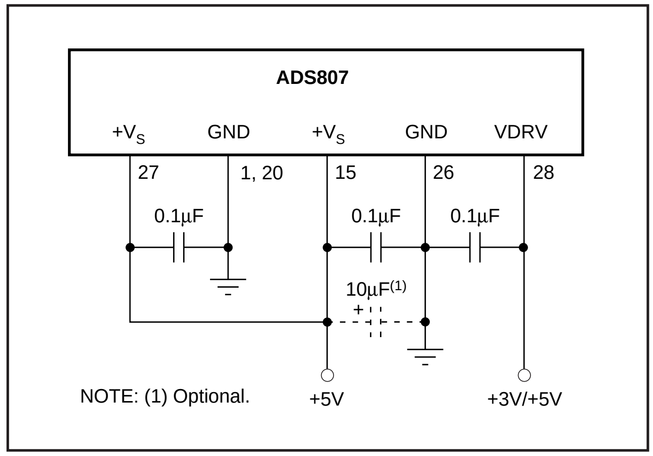


FIGURE 8. Recommended Bypassing for the Supply Pins.

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